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Reconfigurable FPGA Realization of Fractional-Order Chaotic Systems

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ABSTRACT This paper proposes FPGA realization of an IP core for generic fractional-order derivative based on Grünwald-Letnikov approximation. This generic design is applied to achieve reconfigurable realization of fractional-order chaotic systems. The fractional-order real-time configuration boosts the suitability of this particular realization for different applications, including dynamic switching, synchronization, and encryption. The proposed design targets optimized utilization of the FPGA internal resources and efficient employment of the external peripherals: switches and I/O ports in the FPGA board. The digital design of the fractional-order dependent terms: binomial coefficients and power function is proposed. Three approximations of the power function using curve fitting are compared, settling on the quadratic approximation that balances accuracy and efficiency. Three fractional-order chaotic systems: Liu, Li and Chen four-wing, are verified for both commensurate and incommensurate orders cases, using one approach for the commensurate order case and two approaches for the incommensurate order case. The reconfigurable design is realized on the Artix-7 FPGA board, yielding throughputs of 1.1266, 1.1266, and 1.434 Gbit/s for both commensurate and incommensurate orders cases of the three systems, respectively. Compared to recent related works, the proposed implementation demonstrates its efficient hardware utilization and suitability for potential applications.

INDEX TERMS FPGA, fractional calculus, Grünwald-Letnikov, fractional-order chaotic systems.

I. INTRODUCTION

Chaos is reported in systems that are very sensitive to initial conditions such that a slight variation leads to a significant difference in behaviour [1], [2]. Continuous-time chaotic differential equations have higher dimension and time series complexity than discrete-time maps. They must be discretized and solved numerically to be effectively used in digital communication and security applications. Fractional calculus, which enables differentiation and integration of arbitrary real order, can describe the actual dynamics of natural phenomena more accurately than the special case of integer order [3]. It also enhances the controllability through the extra degrees of freedom offered by the fractional orders.

Fractional calculus and chaos-based applications have gained increasing attention in many fields such as controller design [4]–[6], communications systems [7], synchronization [8], traffic flow control [9], encryption [10]–[14], pseudo-random number generators [15]–[17], oscillator design [18], [19], filters [20], [21], deep learning and convolutional neural networks [22] and bioimpedance modeling [23], [24].

The fractional-order derivative/integral has many definitions including the Riemann-Liouville (RL), Caputo and Grünwald-Letnikov (GL) [25]. The RL definition is given by [25]:

$$ {}_{a}^{RL}D_{t}^{q}f(t) = \frac{1}{\Gamma(n-q)}\frac{d^n}{dt^n}\int_a^t \frac{f(\tau)}{(t-\tau)^{q-n+1}}d\tau. \quad (1) $$

The Caputo definition is given by [25]:

$$ {}_{a}^{C}D_{t}^{q}f(t) = \frac{1}{\Gamma(n-q)}\int_a^t \frac{f^{(n)}(\tau)}{(t-\tau)^{q-n+1}}d\tau, \quad (2) $$

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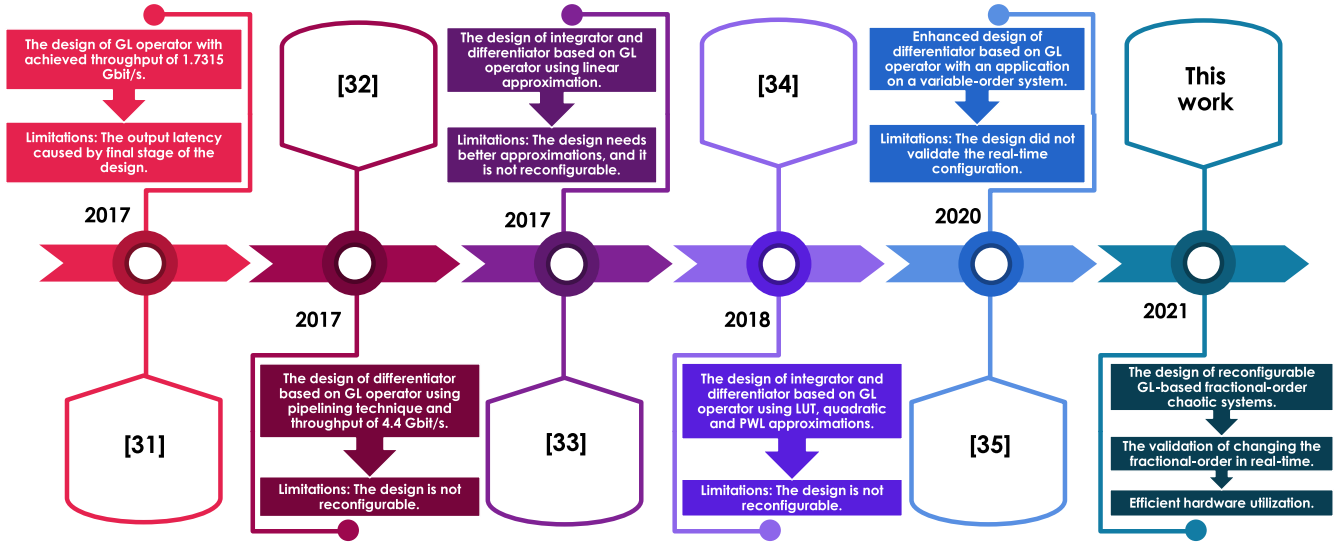


FIGURE 1. The time line of GL digital realization and the proposed improvement.

where q is the fractional-order and $n-1 < q < n$. The summation form of the GL definition is given by [25]:

$$ {}_{a}^{GL}D_{t}^{q}x(t) = \frac{1}{h^q}\sum_{j=0}^{\lfloor (t-a)/h \rfloor} w_j^{(q)} x(t-jh), \tag{3} $$

where $w_j^{(q)}$ are the binomial coefficients calculated recursively as:

$$ w_0^{(q)} = 1, \quad w_j^{(q)} = \left(1 - \frac{q+1}{j}\right) w_{j-1}^{(q)}, \quad j = 1, 2, .. \tag{4} $$

Although fractional-order chaotic systems provide several advantages in various applications, their hardware implementation faces some challenges due to memory dependence [26]–[28]. With the rise of digital signal processors and Field-Programmable Gate Arrays (FPGAs), realizations in digital hardware have become more practical for industrial use [29]. Fixed-point operations are widely used for hardware realizations to save costs and enhance speed. However, a high order of approximation is required to reach a good computational throughput.

Various methods have been proposed to realize the fractional-order integration and differentiation operators [29]–[35]. In some of these methods, e.g. [29], [30], high-level software such as MATLAB was used to generate the Hardware Description Language (HDL) code of these operators based on Finite Impulse Response (FIR) filter. Other researches [36] presented implementations based on LabVIEW. Nevertheless, they neither improved the performance nor optimized the hardware resources. Digital design and FPGA implementation of GL and Caputo derivatives were presented in [31]. The advantage of GL over Caputo in digital realization include smaller area, better performance, avoiding the complexity of implementing Sinc or Gaussian functions, unlike Caputo implementation [31]. Major advantages for the GL over RL and Caputo definitions in digital applications are the GL discretized form and the short memory principle [31]. For FPGA implementation of GL, a fixed window size approximation of length L is given by:

$$ {}_{t-L}^{GL}D_{t}^{q}x(t) = \frac{1}{h^q}\sum_{j=0}^{L} w_j^{(q)} x(t-jh), \tag{5} $$

where h is the step size, L is the window size. Based on the short memory principle, the error due to this approximation is bounded by [31]:

$$ \Delta(t) = \left| {}_{a}^{GL}D_{t}^{\alpha}f(t) - {}_{t-L}^{GL}D_{t}^{\alpha}f(t) \right| \leq \frac{ML^{-\alpha}}{|\Gamma(1-\alpha)|}, \tag{6} $$

where $a + L < t < b$ and $|f(t)| < M$ when $a < t < b$. So, it can be inferred that the error is reduced by increasing the window size.

Figure 1 presents the time line of GL digital realization, which has been gradually enhanced since [31], in which FPGA implementation of the GL operator was proposed using the window approach. The achieved throughput of GL in [31] was 1.7315 Gbit/s. The limitation of [31] is the GL output latency caused by the final stage of the design. So, in [32], a different architecture of fractional-order differentiator based on GL operator was proposed using the window approach and the pipelining technique that resulted in higher frequency and, hence, higher throughput. The achieved throughput of GL in [32] was 4.4 Gbit/s. However, the proposed design in [32] was not reconfigurable, and the fractional-order was provided at the design time and cannot be changed in real-time. Afterwards, in [33], a new algorithm was proposed to implement the fractional-order integrator and differentiator based on GL using the window and linear approximation approaches. To achieve better accuracy, two enhanced versions of the GL fractional

order integrator and differentiator: the window and quadratic approximation approach and the piece-wise linear (PWL) approximation approach, were proposed in [34]. The PWL approach improved the maximum absolute error than the linear, and quadratic approximation approaches as reported in [34]. Still, no reconfigurability was introduced in these approaches. In [35], an enhanced design of the GL was proposed. However, [35] did not validate the fractional-order real-time configuration and proposed a variable-order system switching between only two fractional-order values stored in the design.

More recent researches presented applications of GL digital realization, such as: [37], which presented an automated digital design tool of a fractional-order controllable multi-scroll attractor. Moreover, fractional-order chaotic systems based on the GL realization were employed in encryption applications [12]. However, all these works lack reconfigurability where they provided fractional orders at the design time. Any change in the fractional-order value requires a change in the hardware realization and, consequently, a new HDL code.

The FPGA realization of IP core for generic fractional-order derivative, which allows the reconfigurability of fractional orders in the processing time, is required for different potential applications. This generic FPGA system can realize many fractional-order applications on hardware, e.g., edge detection [38], [39], control [40], [41], synchronization [42] and encryption [43]. Additionally, it can replace the current realizations of mixed-signal and digitally implemented fractional-order applications with the reconfigurable one, e.g., analog/mixed-signal systems [44], [45], control [46] and encryption [12], [47]–[49]. Furthermore, it can be used in variable-order chaotic systems [50], [51], dynamic switching and synchronization [52], and encryption applications with dynamic encryption key [53]. This paper proposes a reconfigurable GL-based design of fractional-order chaotic systems, which enables introducing the fractional-order directly in real-time from the FPGA board. The usage of FPGA board switches and I/O ports validates changing the fractional order in real-time. It achieves a generic design which solves the lack of reconfigurability problem in [31]–[35]. Digital design and hardware architecture of the computational blocks for fractional-order dependent terms are proposed. The reconfigurable design is applied to three different fractional-order chaotic systems: Liu, Li and Chen four-wing with optimized hardware and the possibility of changing the fractional-order through a wide range in real-time, unlike the system in [35]. The proposed design and implementation targets an efficient utilization of FPGA internal resources and the external peripherals: switches and I/O ports in the FPGA board.

The rest of this paper is organized as follows: Section II reviews the GL-based solution of fractional-order chaotic systems and the chaotic properties of three systems used for validation. Section III describes the digital design of the fractional-order dependent terms in the proposed reconfigurable generic GL and their hardware architecture. Section IV extends the proposed design to implement three reconfigurable fractional-order systems, where one approach for the commensurate order case and two approaches for the incommensurate orders case are presented. Section V provides the FPGA simulation and experimental results for both commensurate and incommensurate cases. The hardware resources utilization and efficiency are compared, discussing their suitability for potential applications. A comparison is also made between Liu system implementation based on reconfigurable GL and based on the traditional one in [32] and other recent related works. Finally, Section VI concludes the work.

II. GL-BASED SOLUTION OF THREE FRACTIONAL-ORDER CHAOTIC SYSTEMS

The general form of a fractional order system with three differential equations is given by:

$$D^{q_1}x = f_1(x, y, z), \tag{7a}$$
$$D^{q_2}y = f_2(x, y, z), \tag{7b}$$
$$D^{q_3}z = f_3(x, y, z), \tag{7c}$$

The GL definition of this system is as follows [3]:

$$x(t_{k-1}) = f_1(x(t_{k-1}), y(t_{k-1}), z(t_{k-1}))h^{q_1} - \sum_{j=1}^{n} w_j^{(q_1)} x(t_{k-j}), \tag{8a}$$

$$y(t_{k-1}) = f_2(x(t_{k-1}), y(t_{k-1}), z(t_{k-1}))h^{q_2} - \sum_{j=1}^{n} w_j^{(q_2)} y(t_{k-j}), \tag{8b}$$

$$z(t_{k-1}) = f_3(x(t_{k-1}), y(t_{k-1}), z(t_{k-1}))h^{q_3} - \sum_{j=1}^{n} w_j^{(q_3)} z(t_{k-j}), \tag{8c}$$

where q_1, q_2, q_3 are the fractional orders, $n = L$ for a window size L and approximated GL operator and $n = k$ when the whole state memory is used in calculations.

A. LIU SYSTEM

The fractional-order Liu system [3], [54] is given by:

$$D^{q_1}x = -ax - ey^2, \tag{9a}$$
$$D^{q_2}y = by - dxz, \tag{9b}$$
$$D^{q_3}z = -cz + mxy, \tag{9c}$$

and can be solved based on (8) as:

$$x(t_{k-1}) = (-ax(t_{k-1}) - ey^2(t_{k-1}))h^{q_1} - \sum_{j=1}^{L} w_j^{(q_1)} x(t_{k-j}), \tag{10a}$$

$$y(t_{k-1}) = (by(t_{k-1}) - dx(t_{k-1})z(t_{k-1}))h^{q_2} - \sum_{j=1}^{L} w_j^{(q_2)} y(t_{k-j}), \tag{10b}$$

$$z(t_{k-1}) = (-cz(t_{k-1}) + mx(t_{k-1})y(t_{k-1}))h^{q_3}$$

$$-\sum_{j=1}^{L} w_j^{(q_3)} z(t_{k-j}), \tag{10c}$$

where $h = 0.01$, $a = e = 1$, $b = 2.5$, $d = m = 4$, $c = 5$ and $L = 16$. The equilibrium points and the corresponding eigenvalues for Liu system are given in Table 1. From the eigenvalues of the linearized Jacobian matrix, $E_{2,3}$ are saddle points of index two as they have two unstable eigenvalues and, hence, a two-scroll attractor exists.

TABLE 1. Liu system equilibrium points, the corresponding eigenvalues and equilibrium point type.

Equilibrium point	Eigenvalues	Type
E_1=(0,0,0)	-1,-5,2.5	Saddle point
E_2=(-0.88388, -0.940150,0.664786)	-4.388,0.44388±3.346j	Saddle point
E_3=(-0.88388,0.940150,-0.664786)	-4.388,0.44388±3.346j	Saddle point

B. LI SYSTEM

The fractional-order Li system [55] is given by:

$$D^{q_1} x = a(y - x), \tag{11a}$$
$$D^{q_2} y = (c - a)x + cy - dxz, \tag{11b}$$
$$D^{q_3} z = -bz + ey^2, \tag{11c}$$

and can be solved based on (8) as:

$$x(t_{k-1}) = (a(y(t_{k-1}) - x(t_{k-1})))h^{q_1} - \sum_{j=1}^{L} w_j^{(q_1)} x(t_{k-j}), \tag{12a}$$

$$y(t_{k-1}) = ((c - a)x(t_{k-1}) + cy(t_{k-1}) - dx(t_{k-1})z(t_{k-1}))h^{q_2} - \sum_{j=1}^{L} w_j^{(q_2)} y(t_{k-j}), \tag{12b}$$

$$z(t_{k-1}) = (-bz(t_{k-j}) + ey^2(t_{k-j}))h^{q_3} - \sum_{j=1}^{L} w_j^{(q_3)} z(t_{k-j}), \tag{12c}$$

where $h = 2^{-8}$, $a = 8$, $b = 1$, $c = 8$, $d = 1$, $e = 1$ and $L = 19$. Similarly, the stability of Li system is studied in Table 2 indicating the existence of two-scroll attractor.

C. CHEN FOUR-WING SYSTEM

The fractional-order Chen four-wing system [56] is given by:

$$D^{q_1} x = ax - yz, \tag{13a}$$
$$D^{q_2} y = -by + xz + d\,|x|\,, \tag{13b}$$
$$D^{q_3} z = -cz + xy, \tag{13c}$$

and can be solved based on (8) as:

$$x(t_{k-1}) = (ax(t_{k-1}) - y(t_{k-1})z(t_{k-1}))h^{q_1} - \sum_{j=1}^{L} w_j^{(q_1)} x(t_{k-j}), \tag{14a}$$

$$y(t_{k-1}) = (-by(t_{k-1}) + x(t_{k-1})z(t_{k-1}) + d\,|x(t_{k-1})|)h^{q_2} - \sum_{j=1}^{L} w_j^{(q_2)} y(t_{k-j}), \tag{14b}$$

$$z(t_{k-1}) = (-cz(t_{k-j}) + x(t_{k-j})y(t_{k-j}))h^{q_3} - \sum_{j=1}^{L} w_j^{(q_3)} z(t_{k-j}), \tag{14c}$$

where $h = 2^{-8}$, $a = \frac{20}{7}$, $d = 0.5$, $b = 10$, $c = 4$ and $L = 20$ for the commensurate orders case $q_1 = q_2 = q_3$ and $L = 25$ for the incommensurate orders case $q_1 \neq q_2 \neq q_3$. The system has only one equilibrium point at the origin with eigenvalues $\lambda = -10, -2, \frac{20}{7}$ indicating instability and chaotic behavior.

TABLE 2. Li system equilibrium points, the corresponding eigenvalues and equilibrium point type.

Equilibrium point	Eigenvalues	Type
E_1=(0,0,0)	-8,-1,8	Saddle point
E_2=(-2.8284,-2.8284,8)	-4.2709,1.6355±5.2245j	Saddle point
E_3=(2.8284,2.8284,8)	-4.2709,1.6355±5.2245j	Saddle point

Table 3 shows samples of the behavior of the three systems at different values of the fractional orders for the commensurate order case. In addition, Fig. 2 shows their continuous bifurcation diagram versus $0.7 < q_1 < 1$, where $q_2 = q_3 = q_1$. It shows that the three systems have a relatively wide range of fractional orders corresponding to chaotic behavior. Hence, a reconfigurable digital design that directly introduces the fractional-order to the FPGA board and allows its real-time change is beneficial.

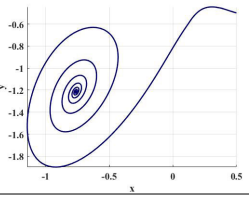
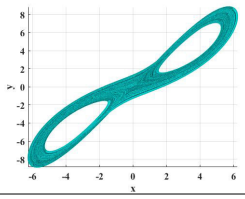
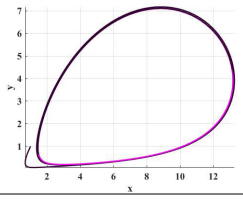
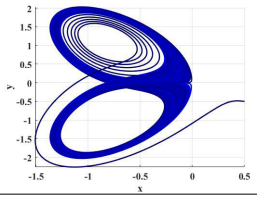
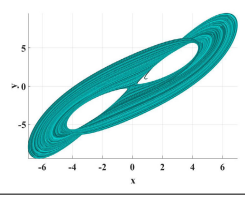
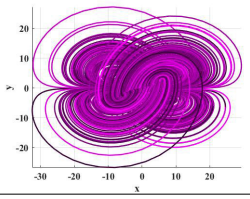
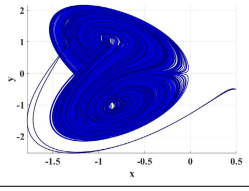
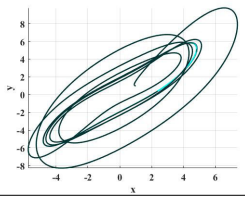
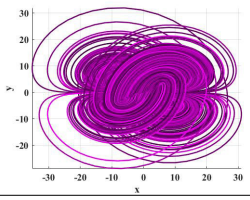
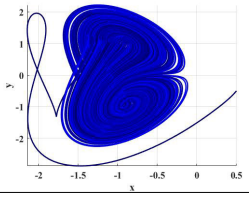
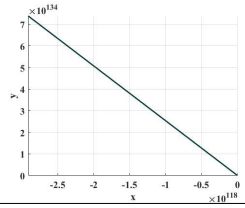
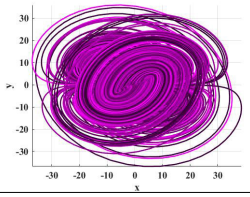
III. RECONFIGURABLE GL DIGITAL DESIGN

This section illustrates the proposed reconfigurable generic GL digital design and its hardware architecture.

A. BINOMIAL COEFFICIENTS AND GENERIC GL BLOCK

The GL implementation of [32] subdivides its operations into two parts. The first part is the binomial coefficients given by (4), which were stored in a LUT. The second part is the summation of (5), which was implemented by row and column vector dot product as shown in Fig. 3. Each upcoming input is multiplied by all the binomial coefficients based on the fixed window approach. The output is the summation of $(x_j w_i)$ product at different times, where $j = \{0, 1, \ldots, n\}$ and $i = \{0, 1, \ldots, n\}$. Two LUTs are required in the hardware, the first one stores the binomial coefficients w_0 to w_n, and the second one stores the output of the addition from $(x_i w_1 + d_1)$ to $(x_i w_n + d_n)$ with zero padding in the most significant part while $(x_0 w_0 + d_0)$ is directly taken as the first output. The input is multiplied by all the binomial coefficients stored in the first LUT (Coefficients LUT), then the output is added to the data previously stored in the second LUT (Data LUT). Multipliers and adders are required to accumulate the output of the GL design [32]. The main problem in the GL implementation of [32] is that it uses fixed binomial coefficients stored in a LUT. Any change in the fractional-order value requires a new set of coefficients to be stored in the LUT.

TABLE 3. Simulation results for Liu, Li and Chen four-wing systems.

	Liu System $L=16, h=0.01, a=e=1, b=2.5, d=m=4, c=5$	Li System $L=19, h=2^{-8}, a=8, b=1, c=8, d=1, e=1$	Chen Four-Wing System $L=20, h=2^{-8}, a=\frac{20}{7}, d=0.5, b=10, c=4$
$q=0.8$			
$q=0.9$			
$q=0.95$			
$q=1$			

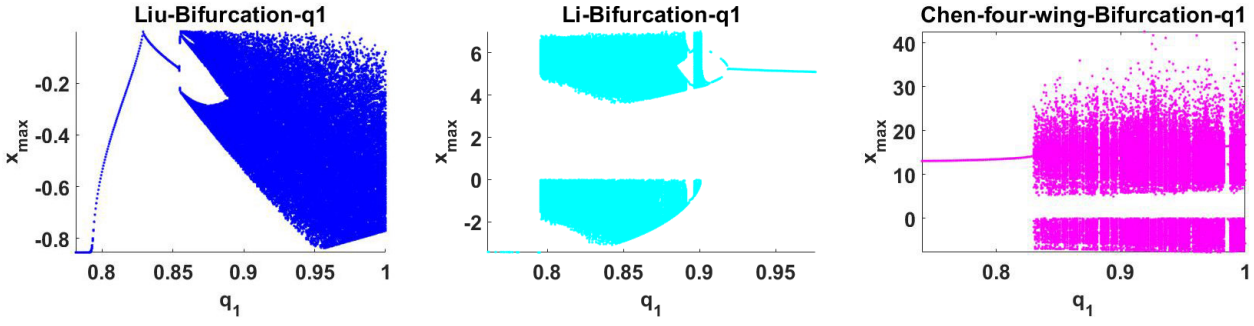


FIGURE 2. Bifurcation diagrams of the commensurate fractional-order systems a) Liu b) Li c) Chen four-wing.

The proposed design in this paper solves the design limitation in [32] by generating the binomial coefficients for any change in the fractional-order.

Figure 4 shows the digital realization for the proposed steps of generating the binomial coefficients calculated from (4) towards computing generic GL using the fractional-order q as an external input. The proposed reconfigurable GL output presents the summation term in the differential equations of a fractional-order chaotic system (8). The proposed design requires three adders, three multipliers, divider, inverter, counter, demux, two LUTs and four registers to store the fractional-order, the coefficient value, the input and the output, respectively. The proposed reconfigurable generic GL works as follows:

- The fractional-order, e.g., q is stored in a register of width 14-bit.
- The fractional-order q is added to one, and the counter value j is multiplied by one; then the addition's output is divided by the multiplication's output. This multiplication is to reserve the integer value of j into a fixed-point representation to be used in the division operation without affecting the counter value. This operation avoids the complexity in implementing $1/j$ generation block using LUT or quadratic approximation in [35].

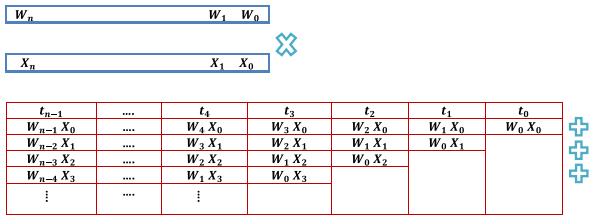


FIGURE 3. Summation term of (5).

- The divider's output is subtracted from one and the output is multiplied by the value w_0 stored in a register to produce w_1 which is reserved in the same register to be used in the following cycles.
- Consequently, q is used to generate all binomial coefficients $(w_0, w_1, \ldots, w_n)$ for the chosen window size L then the coefficients are stored in the Coefficients LUT.
- The input signal, e.g., x is initialized and stored in a register and then updated every clock cycle.
- Every clock cycle, the input x is multiplied by all the coefficients stored in the Coefficients LUT, and the multiplication output is added to the data previously stored in the Data LUT, where $(d_0, d_1, \ldots, d_n)$ are initialized to zero.
- The GL output in the first cycle will be $(x_0w_0 + d_0)$ and the results $(x_0w_1 + d_1), \ldots, (x_0w_n + d_n)$ will be stored in the Data LUT.

The fractional-order input q is a 14-bit fixed-point, 2b for the integer part and 12b for the fractional part. The input x is defined as a 28-bit fixed-point, 8b integer part and 20b fractional part. The values stored in the Coefficients LUT are 22-bit fixed-point, 2b for the integer part, and 20b for the fractional part. They are calculated according to (4). The values stored in the Data LUT are 50-bit fixed-point, 10b for the integer part, and 40b for the fractional part. The output is truncated to get 28b to be an input to the next cycle. An adder's input carry is one to perform the two's complement with the inverter for the subtraction operation.

B. POWER FUNCTION BLOCK USING CURVE FITTING METHODOLOGY

The proposed h^q generation block is realized based on curve fitting methodology. The main problem in implementing chaotic systems using reconfigurable GL design is realizing the power operation h^q for a fractional-order input q. Curve fitting is the process of constructing a curve, or mathematical function, that has the best fit to a series of data points [57], [58]. The MATLAB curve fitting toolbox uses the method of least squares when fitting data [58]. The goal of least squares method is to minimize the sum of squares due to error (SSE). SSE measures the total deviation of the response values from the fit, which is also called the summed square of residuals [57], [58]. SSE calculation is given by:

$$\text{SSE} = \sum_{i=1}^{n_t} (y_{exp}(t_i) - y_{mod}(t_i))^2, \tag{15}$$

where $y_{exp}(t_i)$ is the observed data value, $y_{mod}(t_i)$ is the model predicted value, n_t is the number of data points. In our application, the data points are exact, and the purpose is to find a less complicated function approximation for h^q. The curves can be fit using polynomial and rational functions. Choosing the optimal hardware polynomial fit with the best accuracy is a real challenge. Based on section II, h^q is generated for the range $0.7 < q < 1$. Three different approximations of h^q are assessed using MATLAB curve fitting toolbox [58].

1) LINEAR APPROXIMATION

Using linear approximation, h^q is approximated to be a first degree polynomial as follows:

$$h^q_{Linear} = c_1 q + c_2, \tag{16}$$

where $c_1 = -0.09664$ and $c_2 = 0.01038$ for $h = 0.01$ and $0.7 < q < 1$. Figure 5(a) shows the hardware implementation of h^q based on linear approximation, where the fractional-order input q in 14-bit fixed-point can be inserted into the hardware block of the linear function with the constant coefficients c_1, c_2 and generates h^q in 22-bit fixed-point. The proposed design requires one adder and one multiplier.

2) QUADRATIC APPROXIMATION

Using quadratic approximation, h^q is approximated to be a second degree polynomial as follows:

$$h^q_{Quadratic} = c_1 q^2 + c_2 q + c_3, \tag{17}$$

where $c_1 = 0.2193$, $c_2 = -0.4695$ and $c_3 = 0.2606$ for $h = 0.01$ and $0.7 < q < 1$ for Liu system. Figure 5(b) shows the hardware implementation of h^q based on quadratic approximation. The proposed design requires two adders and three multipliers. For Li and Chen four-wing systems, $c_1 = 0.1454$, $c_2 = -0.3007$ and $c_3 = 0.1595$ for $h = 2^{-8}$ and the same range of q.

3) RATIONAL APPROXIMATION

Using rational approximation, h^q is approximated to be linear/linear rational function as follows:

$$h^q_{Rational} = \frac{c_1 q + c_2}{q + c_3}, \tag{18}$$

where $c_1 = -0.02169$, $c_2 = 0.0277$ and $c_3 = -0.3872$ for $h = 0.01$ and $0.7 < q < 1$. Figure 5(c) shows the hardware implementation of h^q based on rational approximation. The proposed design requires two adders, one multiplier and one divider.

Figure 6 shows the three approximations versus the theoretical one for $h = 0.01$, where the accuracy is better for both quadratic and rational approximations than the linear one as further indicated by the shown error graph. Goodness-of-fit statistics such as SSE and Root mean squared error (RMSE) are used to evaluate the accuracy. RMSE is known as the fit standard error, which estimates the random component's standard deviation in the data [57], [58].

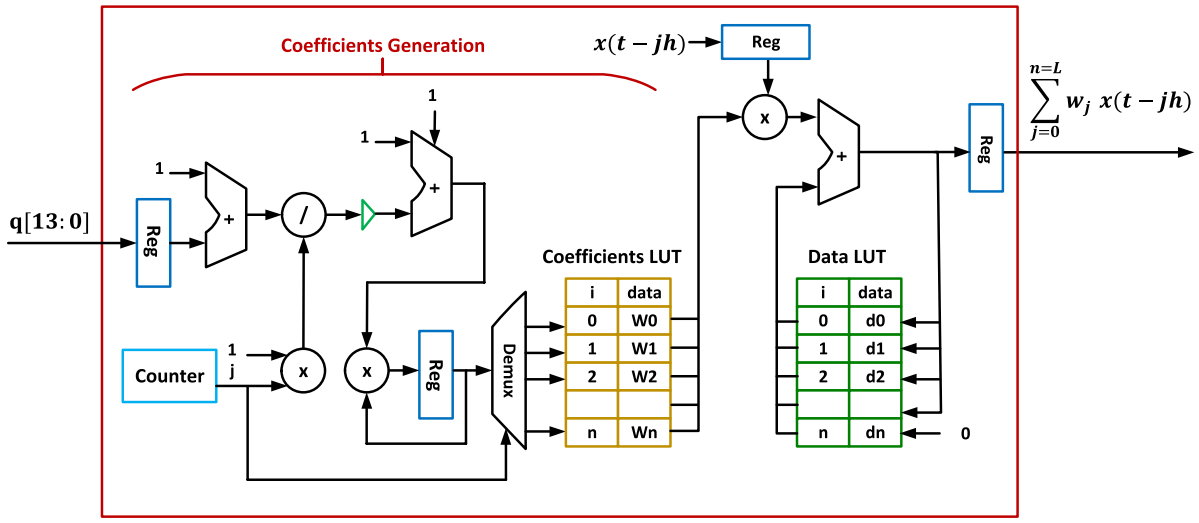


FIGURE 4. The hardware architecture of the reconfigurable generic GL design.

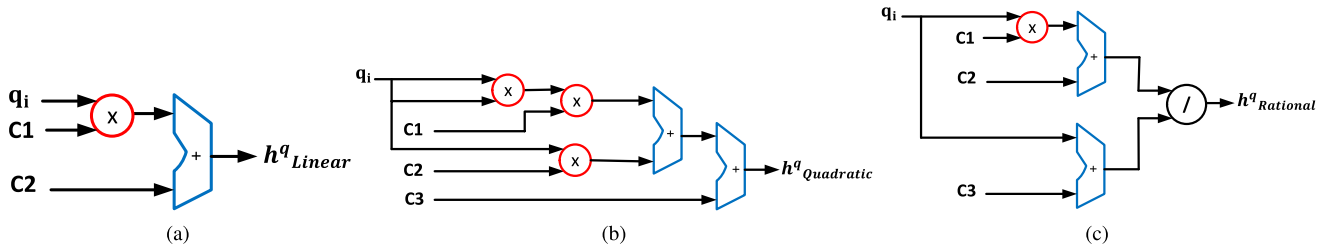


FIGURE 5. h^q Hardware implementation using curve fitting (a) linear, (b) quadratic and (c) rational approximations.

TABLE 4. Goodness of fit statistics of different approximations for 0.01^q.

Approximation Type	SSE	RMSE
Linear	7.722e-5	0.001632
Quadratic	1.089e-6	0.0001972
Rational	8.545e-9	9.62e-5

The error calculations are given by:

$$\text{MSE} = \frac{\text{SSE}}{n_t - n_p}, \tag{19a}$$

$$\text{RMSE} = \sqrt{\text{MSE}}, \tag{19b}$$

where n_p is the number of estimated model parameters. Table 4 gives the values of the goodness-of-fit measures for linear, quadratic and rational approximations for $h = 0.01$, where the best accuracy is reported for the rational approximation design.

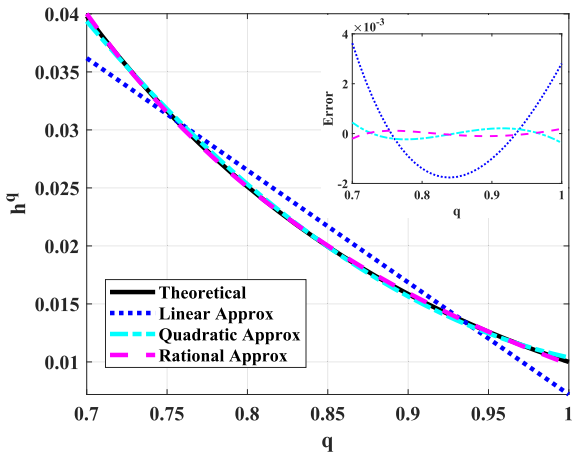


FIGURE 6. h^q Curve fit for $h = 0.01$.

IV. RECONFIGURABLE FPGA IMPLEMENTATION OF CHAOTIC SYSTEMS

The basic building blocks of the IP core for generic fractional-order derivative based on GL: binomial coefficients generation and h^q generation blocks are applied to achieve the reconfigurability of the fractional-order chaotic systems using the steps illustrated in the flowchart in Fig.7 and Algorithm 1. First, the inputs clk, rst and q are read from the FPGA board. Then, the value of h^q is calculated and used to compute the first term of (8) (denoted in Fig.7 by x_1, y_1 and z_1). Afterwards, the coefficients w_j are generated and used to calculate the second term of (8) (denoted in Fig.7 by x_2, y_2 and z_2). Finally, the outputs,which represent the state variables x, y and z, are produced using the subtraction of the two mentioned terms of (8) in each clk cycle.

Figure 8 presents the general design for any fractional-order chaotic generator with three differential equations. Three registers are used to store the state variables x, y and

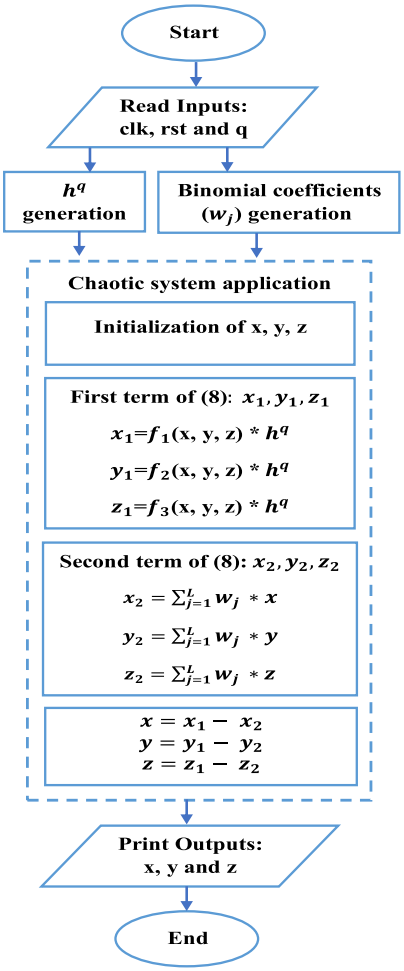


FIGURE 7. Flowchart of the IP core for generic fractional-order derivative based on GL with a chaotic system application.

z. The numerical solution for each variable is implemented using a combinational circuit. Three fractional orders are introduced as inputs to the h^q generation blocks and the generic GL blocks. The fractional-orders are used to calculate h^q based on curve fitting approximation of Section III-B and to evaluate the dot product in the system of differential equations based on generic GL in Section III-A.

For the commensurate order case $q_1 = q_2 = q_3 = q$, the fractional-order is introduced to the FPGA board through 14 switches as shown in Fig. 9. For the incommensurate order case $q_1 \neq q_2 \neq q_3$, two approaches are introduced for FPGA board connections. The first approach (A) is shown in Fig. 10, where the fractional orders are introduced to the FPGA board through 14 switches and 28 entries through JA, JB, JC, JD ports. The second approach (B) shown in Fig. 11 targets a more efficient utilization of the peripherals, where all the three fractional orders are inserted to the FPGA board through the 15 switches only. Each fractional-order refer to 5 switches (bits) covering up to 2^5 levels or 32 values. For example, to cover the range of orders from 0.7 to 1 with step 0.01, it can be distributed on 31 levels as shown in Fig. 11. In approach (A), the fractional-orders can vary through wide range without constraints given the corresponding h^q approximation. However, in approach (B), the fractional-orders can take one of the 32 values only and hence the corresponding h^q values are stored without the need for an approximation. Consequently, approach (B) needs less computational circuits than approach (A); yet, it consumes more storage for the values of the fractional-orders and the corresponding h^q.

Algorithm 1 Pseudo Code of the IP Core for Generic Fractional-Order Derivative Based on GL With a Chaotic System Application

1- Inputs: clk, rst, q, Outputs: x, y, z
2- Binomial coefficients generation
Definition of w_0
for $j = 1, \ldots, L$ do
$w_j = (1 - ((1 + q)/(1 * j))) * w_{j-1}$
end for
3 -h^q generation for quadratic approximation
$h^q = c_1 * q * q + c_2 * q + c_3$
4- Chaotic system application
- Initialization of x, y, z
- First term of (8) computation
$x_1 = f_1(x, y, z) * h^q$
- Second term of (8) computation
$x_2 = d_0 + (w_0 * x)$
for $j = 1, \ldots, L$ do
$d_{j-1} = d_j + (w_j * x)$
end for
- $x = x_1 - x_2$
Similarly repeat for y and z calculation

Following Fig. 8, the hardware implementation of the fractional-order Liu system (10) is illustrated in Fig. 12(a). Each of the three registers x, y and z is represented by a 28-bit fixed point, 8b for the integer part and 20b for the fractional part. The proposed design requires six adders, eleven multipliers, squarer, seven inverters, three h^q generation blocks and three generic GL blocks. The squarer is used to compute y^2. The binomial coefficients are 22-bit fixed-point, 2b the integer part and 20b for the fractional part, while the constants are 28-bit fixed-point, 8b the integer part, and 20b for the fractional part. The output of each multiplier and generic GL blocks are truncated to get 28b for x, y and z. Similarly, the hardware implementation of the fractional-order Li system (12) is illustrated in Fig. 12(b). It requires seven adders, nine multipliers, squarer, six inverters, in addition to the three h^q and generic GL blocks. The hardware implementation of the fractional-order Chen four-wing system (14) is illustrated in Fig. 12(c). It requires seven adders, ten multipliers, an absolute block used as a comparator, six inverters and the same common blocks.

V. RESULTS AND DISCUSSION

First, we compare the proposed different curve fitting for h^q discussed in Section III-B experimentally. FPGA resources summary for different approximations of 0.01^q is presented

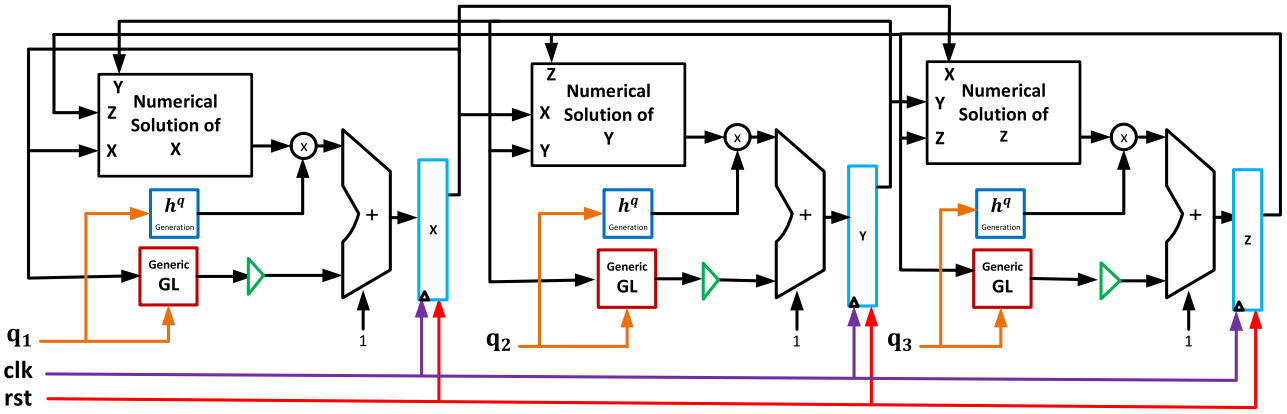


FIGURE 8. Reconfigurable hardware architecture of fractional-order chaotic systems.

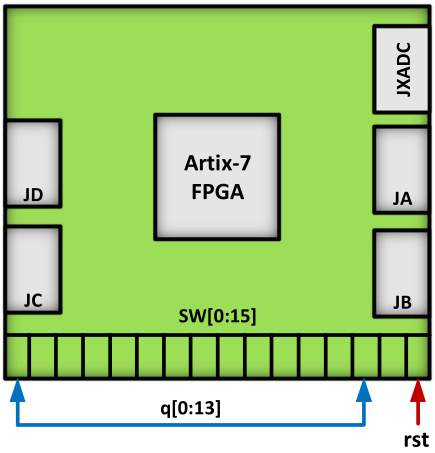


FIGURE 9. FPGA board connections for commensurate orders.

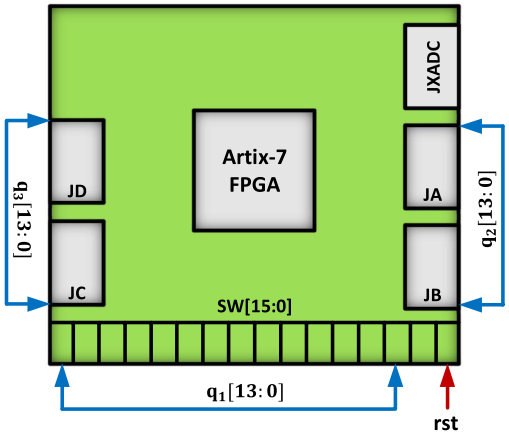
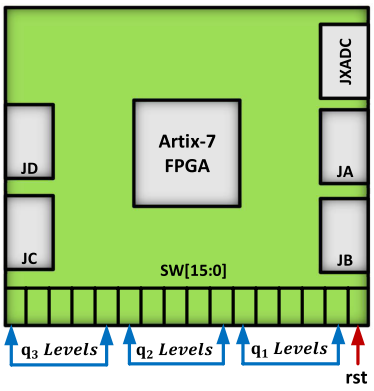


FIGURE 10. FPGA board connections for incommensurate orders using approach (A).

in Table 5. The quadratic implementation consumes fewer slices and slice registers than those in linear and rational implementations. On the other hand, it consumes more DSPs. The achieved throughput for linear, quadratic, and rational approximations is 4.83, 2.76, and 0.253 Gbit/s, respectively.

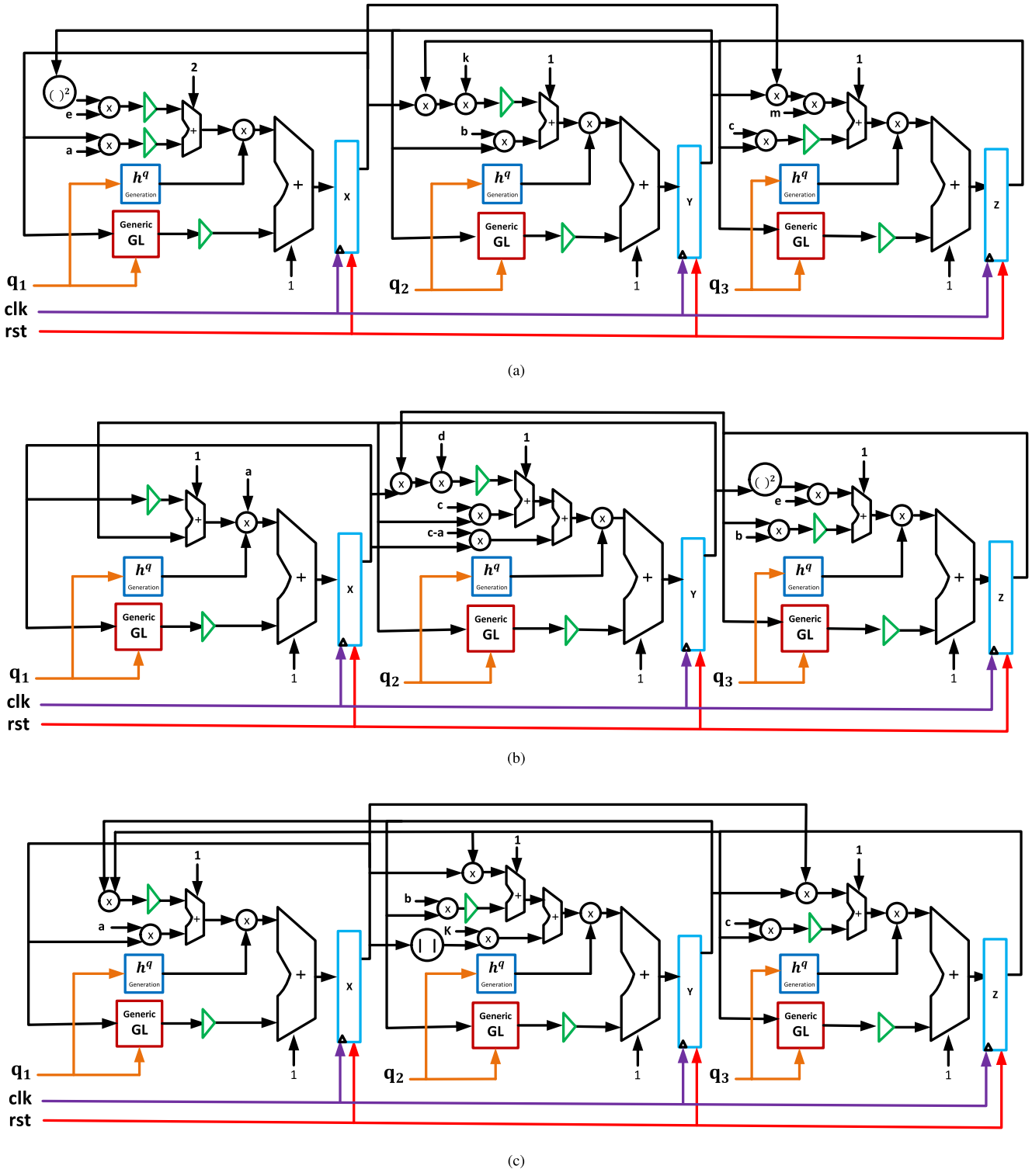


Level	q_i Value
1	0.70
2	0.71
3	0.72
4	0.73
5	0.74
. . .	. . .
28	0.97
29	0.98
30	0.99
31	1

FIGURE 11. FPGA board connections for incommensurate orders using approach (B).

The proposed design for the reconfigurable fractional-order systems is written in Verilog HDL with the simulation of Xilinx ISE 14.7 and implemented on Xilinx FPGA Artix-7 XC7A100TCSG324 by using Chip scope. The logic in the FPGA resources tables is automatically chosen by the compiler. Several compilations provide the same dynamics. The maximum frequency refers to the global clock frequency used to update the synchronous logic. The source of the clock is the external crystal oscillator associated with the Artix-7 board. Summary of FPGA implementation results for Liu system using different approximations for h^q is presented in Table 6. The achieved throughput is 1.1266 Gbit/s for the three implementations. When compromising the utilization and the approximation accuracy for the three implementations, the quadratic approximation is the most appropriate. Hence, computing h^q using quadratic approximation is chosen for implementing Li and Chen four-wing systems to compromise between accuracy, utilization, and speed.

Table 7 presents FPGA resources of Liu, Li and Chen four-wing systems for the commensurate order case. The achieved throughputs, in this case, are 1.1266, 1.1266 and 1.434 Gbit/s for the three systems, respectively.



(a)

(b)

(c)

FIGURE 12. Reconfigurable hardware architectures of (a) Liu, (b) Li and (c) Chen four-wing systems.

Table 8 gives FPGA resources of the three systems for the incommensurate order case for the two proposed approaches. Approach (A) consumes fewer slices than approach (B) since the fractional orders can be inserted directly into the design in real-time. While in approach (B), the fractional orders are selected in real-time among a specific set of values (31 values) stored in the design based on switch signals. Approach (B) has less arithmetic complexity as there is no need for h^q generation blocks. So, it generally consumes fewer, or sometimes equal, slice registers and DSPs as approach (A).

TABLE 5. FPGA resources summary comparison using different approximations for 0.01^q.

Logic Utilization	Total No of slices	Total No of slices Registers	Max Freq (MHz)	DSP Multipliers	Throughput (Gbit/s)
Linear	10	40	219.587	2	4.83
Quadratic	9	28	125.468	4	2.76
Rational	686	85	11.486	1	0.253

TABLE 6. Liu System FPGA resources summary comparison using different approximations for h^q.

Logic Utilization	Total No of slices	Total No of slices Registers	Max Freq (MHz)	DSP Multipliers	Throughput (Gbit/s)
Liu (Linear)	981	2251	40.237	161	1.1266
Liu (Quadratic)	970	2229	40.237	163	1.1266
Liu (Rational)	1601	2230	40.237	160	1.1266

TABLE 7. FPGA resources summary comparison for the commensurate Liu, Li and Chen four-wing systems using quadratic approximation for h^q.

Logic Utilization	Total No of slices	Total No of slices Registers	Max Freq (MHz)	DSP Multipliers	Throughput (Gbit/s)
Liu ($q = 0.95$)	970	2229	40.237	163	1.1266
Li ($q = 0.9$)	1103	2717	40.237	176	1.1266
Chen Four-Wing ($q = 0.9$)	5694	3540	51.214	216	1.434

TABLE 8. FPGA resources summary comparison for the incommensurate Liu, Li and Chen four-wing systems using approaches (A) and (B) and quadratic approximation for h^q.

Logic Utilization	Total No of slices	Total No of slices Registers	Max Freq (MHz)	DSP Multipliers	Throughput (Gbit/s)
Liu (A) ($q_1 = 0.95, q_2 = 0.9, q_3 = 1$)	1354	2246	40.237	201	1.1266
Liu (B) ($q_1 = 0.95, q_2 = 0.9, q_3 = 1$)	2261	2246	40.237	189	1.1266
Li (A) ($q_1 = 0.9, q_2 = 0.95, q_3 = 1$)	1631	2743	40.237	216	1.1266
Li (B) ($q_1 = 0.9, q_2 = 0.95, q_3 = 1$)	2661	2717	40.237	208	1.1266
Chen Four-Wing (A) ($q_1 = 0.9, q_2 = 0.9, q_3 = 1$)	14317	5130	51.214	216	1.434
Chen Four-Wing (B) ($q_1 = 0.9, q_2 = 0.9, q_3 = 1$)	14747	5062	51.214	216	1.434

TABLE 9. Comparison between the proposed implementation of Liu and Liu implementation in [32].

Logic Utilization	Total No of slices	Total No of slices Registers	Max Freq (MHz)	DSP Multipliers	Throughput (Gbit/s)
Proposed Liu implementation	970	2229	40.237	163	1.1266
Liu implementation in [32]	5688	4962	38.874	99	1.554

The systems are implemented at the same values of the parameters given in Section II. Throughputs of 1.1266, 1.1266 and 1.434 Gbit/s are achieved for the incommensurate order case of the three systems, respectively. Figs. 13 show the experimental oscilloscope results using the Artix-7 FPGA board. Figs. 13 (a)-(c) show the commensurate cases of Liu, Li and Chen four-wing systems, and Fig. 13(d) shows the incommensurate case of Liu system (Approach A).

Table 9 presents a comparison between the proposed implementation of Liu system with 28-bit fixed-point and Liu system implementation in [32] with 32-bit fixed-point. The proposed implementation achieves fewer slices by 82.95%, less number of slice registers by 55%, higher frequency by 3.39% because it uses more optimal window size L and 28-bit fixed-point for x, y and z instead of 32-bit fixed-point. The proposed implementation consumes higher DSPs than [32] due to the increase of the arithmetic operations needed for achieving the reconfigurability. The lower throughput is owed to its calculation method by multiplying the number of output bits by the produced frequency, and the proposed Liu design assigns fewer bits for x, y and z compared to the increase in the produced frequency.

The reconfigurability of the GL design in [35] was not verified, where the proposed system was limited to switch between two fractional orders stored in the design using a select signal, while this work achieved the real-time reconfigurability of the GL design. Additionally, h^q calculation in [35] was restricted to h values that equal power of 2, while this work provided a generic design for any h value, which added a greater tolerance in changing the step size than [35].

The proposed design and implementation represents an IP core for reconfigurable fractional-order derivative based on GL, which paves the way towards several applications that require dynamic fractional-orders, including variable-order chaotic systems, dynamic switching and synchronization and encryption applications with dynamic encryption key.

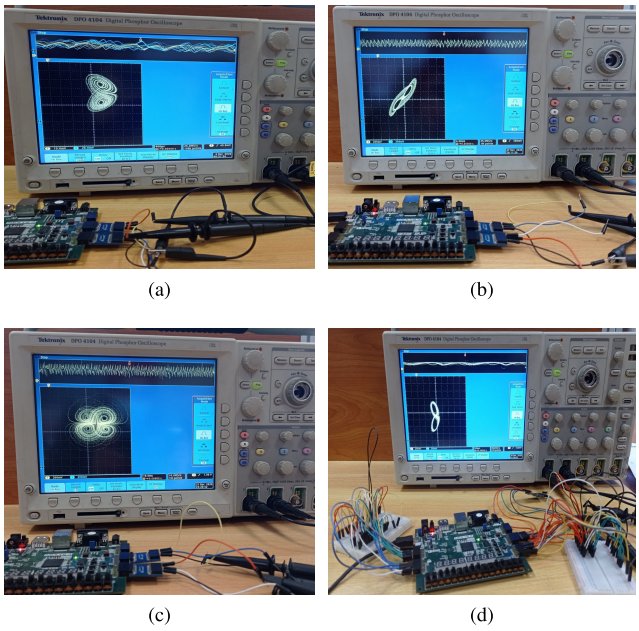


FIGURE 13. FPGA experimental results for the commensurate (a) Liu, (b) Li, (c) Chen four-wing systems and (d) the incommensurate Liu system (Approach A).

The proposed implementation can be further extended to include real-time reconfigurability of all system parameters with wide ranges corresponding to chaotic behavior. Further optimization and time constraints can be explored to enhance both hardware resources utilization and maximum frequency and, hence, efficiency and throughput.

VI. CONCLUSION

A reconfigurable FPGA implementation of fractional-order chaotic systems based on GL approximation was proposed. The fractional-order real-time configuration was validated unlike previous introduced works, which set its value at design time. The proposed hardware architecture achieved optimized utilization of the FPGA internal resources and efficient employment of the external peripherals: switches and I/O ports in the FPGA board. The digital design of the fractional-order dependent terms: binomial coefficients and power function was proposed. First, binomial coefficients were computed from the fractional order's variable value rather than stored in LUT for fixed orders. Second, the power function h^q was computed using curve fitting, where the quadratic approximation balanced accuracy and efficiency. Three fractional-order chaotic systems that exhibit chaotic behavior for a wide range of the fractional-order were selected for verification. The three systems were implemented with reduced window size and the number of bits assigned to the state variables for better utilization and efficiency. Throughputs of 1.1266, 1.1266 and 1.434 Gbit/s were achieved for both commensurate and incommensurate order cases of the three systems, respectively.

The FPGA simulation and experimental oscilloscope results for both commensurate and incommensurate cases were demonstrated using the Aritex-7 FPGA board. Regarding the incommensurate order case, approach (A) utilized 14 switches or 14 entries for each fractional-order and computed h^q, while approach (B) restricted each fractional-order to 5 switches corresponding to 32 values and stores h^q. Consequently, approach (B) consumed more slices to store the values of the fractional-order and h^q than those in approach (A). However, approach (B) had fewer computational circuits, which consumed fewer, or sometimes equal, slice registers and DSPs than those in approach (A). The proposed Liu achieved less number of slices than [32] by 82.95%, less number of slice registers by 55%, higher frequency by 3.39%; yet, larger DSPs to achieve reconfigurability. Potential applications of the proposed reconfigurable implementation include variable-order chaotic systems, dynamic switching and synchronization, and encryption applications with a dynamic encryption key.

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