IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 22, 2021, accepted June 9, 2021, date of publication June 14, 2021, date of current version June 21, 2021.

*Digital Object Identifier 10.1109/ACCESS.2021.3088939*

# Comparative Analysis of Hybrid NPP and NPC Seven-Level Inverter With Switched-Capacitor

**YUANMAO YE, (Member, IEEE), GUOXIN ZHANG, JINLIANG HUANG, SHIKAI CHEN, AND XIAOLIN WANG**

School of Automation, Guangdong University of Technology, Guangzhou 510006, China

Corresponding author: Xiaolin Wang (xiaolinwang@gdut.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 51907033, and in part by the Natural Science Foundation of Guangdong Province under Grant 2020A1515110977.

**ABSTRACT** In this work, the general structure of a hybrid NPP/NPC seven-level inverter is derived from a dual-T-type inverter. Compared with the original structure, the general structure is more flexible as there are four specific circuit configurations to meet different applications. In addition to self-balanced capacitor voltages and boost capability, various commercial NPP and NPC modules can be used to speed up the design process. Circuit description, operation principle, modulation and simulation results are analyzed comparatively. Theoretical analysis and simulation comparison indicate that the four configurations of the hybrid NPP/NPC inverter have their own merits and demerits. Especially, except for a bidirectional switch, all switching components of the NPP + NPC configuration have the same voltage stress as the dc input voltage making it is better in the aspect of component selection, and it is more suitable for high voltage applications. The performance of the NPP + NPC inverter is experimentally demonstrated by an 1kW prototype and its efficiency is closed to 96%.

**INDEX TERMS** Multilevel inverter, neutral-point-piloted, neutral-point-clamped, switched-capacitor.

## I. INTRODUCTION

With the rapid development of new energy and electric vehicles, the demand for high-performance inverters is growing rapidly [1], [2]. As multilevel inverters (MLIs) have the advantages of near-sinusoidal output voltage waveforms, reduced voltage stress (*dv/dt*), operation with lower switching frequency and so on, they have been widely applied in motor drivers, renewable energy sources and high-voltage dc transmission [3]. The conventional types of MLIs, such as neutral-point-clamped (NPC) and flying capacitor (FC) inverters, are very attractive due to their advantages of high efficiency and high power density [4], [5]. However, when these topologies are expanded to more output levels, their applications are restricted by complex clamping circuits and the imbalance of capacitor voltage [6]. Another conventional type of MLI, cascaded H-bridge (CHB) inverter, attracts attention because of its superiority like modularity and simple structure [7]. However, a large number of isolated dc sources are required for each H-bridge unit [8]. Additionally, neutral-point-piloted (NPP) inverter, also known as T-type inverter, is successfully applied for high-speed motor drives [9]. In theory, the NPP has the same operation and control as the NPC [10]. However, two high-voltage-rated switches are employed in NPP and this structure is usually limited to the three-level configuration [11], [12].

To get more output levels, various hybrid MLIs have been developed by combining NPC, FC, CHB and NPP in [13]–[18]. Specifically, the nested NPP (NNPP) inverter presented in [13] is capable of generating five output levels. To reduce the number of switches, another 5-level NNPP inverter is developed in [14] by removing one bidirectional switch, but at the cost of a complex strategy for capacitors' voltage balancing. In the work [15], [16], two hybrid seven-level inverters are developed by cascading the end-side flying-capacitor-fed H-bridge with the front-side three-level inverter. With the combination of some features of 3-level FC and 3-level NPC, the active NPC (ANPC) 7-level inverter is introduced in [17]. In the work [18], the 9-level ANPC inverter is formed by a two-level converter and a five-level ANPC unit. However, a common problem for the MLIs of [15]–[18] is that the voltage balance of capacitors depends on the proper selection of redundant switching states, which requires complex voltage sensors and

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

control algorithms. Moreover, none of the MLIs of [13]–[18] have voltage-boosting capability.

To improve the voltage-boosting capability and solve the problem of capacitor voltage balancing, a new type of MLIs based on switched-capacitor (SC) technique has been developed in recent years [19]–[21]. In SC-MLIs, SCs are taken as dc voltage sources and they are charged by the dc source through switching components. From the aspect of minimizing power transmission loss, it is desirable to use fewer switches in the charging path of SCs [22]. Taking the 7-level SC-MLIs presented in [23]–[30] as examples, there are four transistors found in SCs' charging path of [24]–[30], while two transistors found in SC's charging path of [23]. In addition, the 7-level inverter of [23] is developed by cascading two NPP units. Various commercial three-level NPP modules can therefore be used to reduce the design difficulty and speed up commercialization. However, the two NPP units are with different voltage stresses. This is not beneficial to the selection of components.

In theory, a three-level NPC circuit has the same function as a T-type unit, and then the dual-T-type 7-level inverter can be extended to four different structures, i.e., NPP + NPP [23], NPP + NPC, NPC + NPC and NPC + NPP. Considering the three-level NPC and NPP circuits have different configurations and they have their own merit and demerit, the four structures of 7-level inverters must have different performances. Hence, the purpose of this paper is to analyze the four structures and compare their performance, and then find the best solution for 7-level inverters.

The rest of the paper is organized as follows. In Section II, the general structure of the hybrid NPP/NPC 7-level inverter is derived from the dual-T-type 7-level inverter of [23]. Then, the operation is analyzed and the characteristics of the four structures are compared comprehensively. In Section III, the hybrid NPP/NPC 7-level inverter is further analyzed when it operates with the PD-PWM strategy. After that, various existing 7-level inverters are taken into comparison with the four structures of the hybrid NPP/NPC 7-level inverter in Section IV. The simulation and experimental verification are given in Section V and the paper is finally concluded in Section VI.

## II. HYBRID NPP/NPC SEVEN-LEVEL TOPOLOGIES

### A. CIRCUIT DESCRIPTION

As shown in Fig. 1(a), the dual-T-type 7-level inverter of [23] involves two dc-link capacitors $C_{dc1}$ and $C_{dc2}$, two SCs $C_{S1}$ and $C_{S2}$, two T-type switching units as well as two charging transistors $T_1$ and $T_2$ for SCs. Considering the three-level NPC switching circuit has the same function as a T-type unit and the two charging transistors $T_1$ and $T_2$ can be replaced with two diodes $D_{S1}$ and $D_{S2}$, the general structure of the hybrid NPP/NPC 7-level inverter is derived as illustrated in Fig. 1(b) and its three-phased configuration is shown in Fig. 1(c). As the NPC and NPP units have the same function and both of them can be equivalent to a kind of circuit that is implemented by three switches, as depicted in Fig. 1(d).

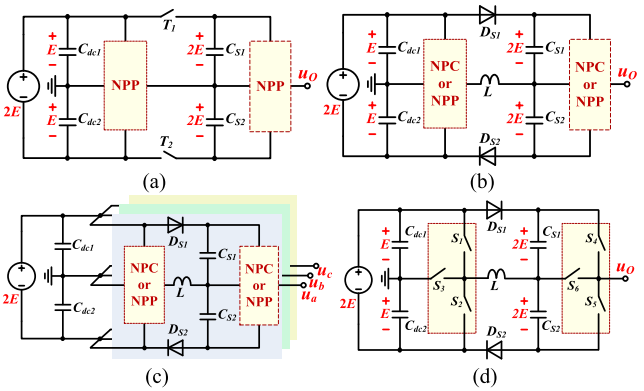



**FIGURE 1.** Hybrid NPP/NPC 7-level inverter. (a) Dual-T-type structure [23]. (b) General structure. (c) Three-phase configuration. (d) Equivalent circuit.

When the dc input voltage is $2E$, the capacitor $C_{S1}$ and $C_{S2}$ are charged by the dc source through $S_2 - D_{S1}$ and $S_1 - D_{S2}$, respectively. Hence, the transistors $S_1 - S_2$, diodes $D_{S1} - D_{S2}$ and capacitors $C_{S1} - C_{S2}$ are rated at $2E$ while the switch $S_3$ is rated at $E$. As the switches $S_4$ and $S_5$ are in parallel with the series-connection of $C_{S1}$ and $C_{S2}$ and the switch $S_6$ is connected at the midpoint of $C_{S1}$ and $C_{S2}$, the voltage stresses for $S_4$ and $S_5$ are $4E$ while that for $S_6$ is $2E$.

In addition, to reduce charging current variation *di/dt* of SCs at switching instants, a small inductor $L$ is inserted between the left-side unit and the midpoint of $C_{S1}$ and $C_{S2}$. Its value is very small so that the effect will be neglected in the following analysis.

### B. OPERATION PRINCIPLE

To facilitate analysis, it is assumed that all switching devices are ideal and all the capacitors are so large that their voltages are constant.

At any time, only one of the switches $S_1 \sim S_3$ is turned ON while the other two are OFF and the switches $S_4 \sim S_6$ have the same operation principle, there are therefore a total of 9 switching states correspond to 7 levels of the output voltage, as illustrated in Table 1. Note that 1 and 0 represent ON and OFF states of the related switch, respectively. Capacitors' states of 'C', 'D' and 'N' are indicative of charging, discharging and idle states, respectively.

**TABLE 1.** Switching states of the equivalent circuit of fig. 1(d).

| Switching states | Switches | | Capacitors | | Output |
|---|---|---|---|---|---|
| | $S_{1,2,3}$ | $S_{4,5,6}$ | $C_{S1}$ | $C_{S2}$ | $u_o$ |
| 1 | 100 | 100 | D | C | $+3E$ |
| 2 | 001 | 100 | D | N | $+2E$ |
| 3 | 010 | 100 | C | N | $+E$ |
| 4 | 100 | 001 | N | C | $+E$ |
| 5 | 001 | 001 | N | N | 0 |
| 6 | 010 | 001 | C | N | $-E$ |
| 7 | 100 | 010 | N | C | $-E$ |
| 8 | 001 | 010 | N | D | $-2E$ |
| 9 | 010 | 010 | C | D | $-3E$ |

To optimize the capacitor voltage ripples, the states '4' and '6' will not be adopted in actual operation so that the remaining 7 state circuits are shown in Fig. 2. It indicates that the capacitors $C_{S1}$ and $C_{S2}$ are recharged by the dc source directly for the levels of $\pm E$ and $\pm 3E$. And the load current can flow in both directions.

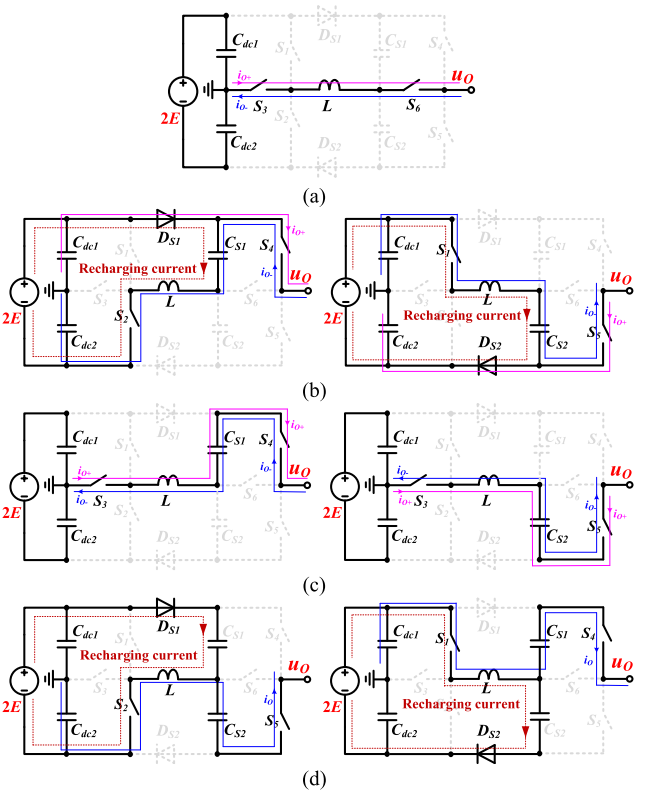



**FIGURE 2.** State circuits of the hybrid NPP/NPC 7-level inverter. (a) $u_O = 0$. (b) $u_O = \pm$E. (c) $u_O = \pm$2E. (d) $u_O = \pm$3E.

### C. SELF-BALANCED CAPACITOR VOLTAGES

As illustrated in Fig. 1 and Table 1, both of structure and operation of the hybrid NPP/NPC 7-level inverter are symmetrical. The capacitors $C_{S1}$ and $C_{S2}$ are responsible for the positive- and negative-half cycles of the output voltage, respectively. For both resistive and inductive loads, the functions of the two capacitors are the same and they handle the same amount of power. Hence, the two capacitor voltages are balanced naturally. Moreover, $C_{S1}$ and $C_{S2}$ are connected in parallel with the dc input source for the levels of $+E$ and $-E$, respectively. Their voltages can therefore be balanced to the same as the input voltage $2E$ automatically.

### D. PRE-CHARGING CIRCUIT AND SOFT-START

Although all the capacitors of the hybrid NPP/NPC inverter can be self-charged to their rated voltages after start-up, the inrush charging current will occur as two diodes $D_{S1}$ and $D_{S2}$ are connected in series with the dc source and the initial capacitor voltages are zero. This will challenge the safety of components. To overcome this issue, a soft-start circuit is developed as shown in Fig. 3(a). It is formed by a current limiting resistor $R_S$ and its by-pass switch $T$.

During the soft-start stage, the by-pass switch $T$ is turned OFF and all charging current flows through the current limiting resistor $R_S$. The two transistors $S_1$ and $S_2$ are controlled by a pair of complementary high-frequency square wave signals, so that $C_{S1}$ and $C_{S2}$ are alternately charged by the dc source through $S_2 - D_{S1}$ and $S_1 - D_{S2}$. After all the capacitors are charged to their rated voltages, the by-pass switch $T$ is turned ON.

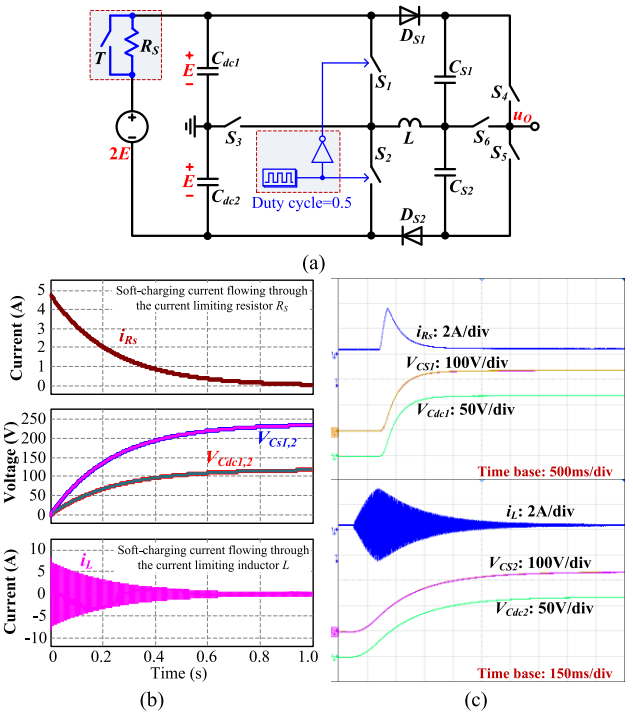



**FIGURE 3.** Soft-start of the hybrid NPP/NPC 7-level inverter. (a) Circuit configuration. (b) Simulation waveforms. (c) Experimental results.

When the dc input voltage is 240V, $R_S = 50\Omega$, $C_{dc1} = C_{dc2} = 1500\mu$F, $C_{S1} = C_{S2} = 2000\mu$F, $L = 1\mu$H and the switching frequency for $S_1$ and $S_2$ is set to 5kHz, the simulation and experimental waveforms including the capacitors' voltages $V_{CS1,2}$, $V_{Cdc1,2}$, the start-up current $i_{Rs}$ and the capacitors' current $i_L$ are shown in Figs. 3(b) and 3(c). The results indicate that the start charging current of capacitors is effectively limited by the soft-start circuit. Finally, the voltages $V_{CS1,2}$ and $V_{Cdc1,2}$ stabilize at 240V and 120V, respectively.

### E. COMPARISON OF DIFFERENT CONFIGURATIONS

As mentioned before, there are four specific configurations for the hybrid NPP/NPC 7-level inverter. Table 2 shows the comparison of the four configurations regarding the number of transistors ($N_T$), the number of diodes ($N_D$), the number of capacitors ($N_C$), the number of gate drivers ($N_G$), the maximum blocking voltage (MBV) of switching components,

**TABLE 2.** Comparison of the four circuit configurations.

| Circuit configurations | $N_T$ | $N_D$ | $N_C$ | $N_G$ | MBV ($\times E$) | $TSV_{sw}$ ($\times E$) | $TSV_{dio}$ ($\times E$) |
|---|---|---|---|---|---|---|---|
| NPC+NPC | 8 | 6 | 4 | 8 | 2 | 12 | 10 |
| NPC+NPP | 8 | 4 | 4 | 7 | 4 | 16 | 6 |
| NPP+NPP | 8 | 2 | 4 | 6 | 4 | 18 | 4 |
| NPP+NPC | 8 | 4 | 4 | 7 | 2 | 14 | 8 |

**TABLE 3.** Switching states of the NPP + NPC 7-level inverter.

| Switching states | Switches | | Capacitors | | Output |
|---|---|---|---|---|---|
| | $S_{1,2,3}$ | $S_{4,5,6,7}$ | $C_{S1}$ | $C_{S2}$ | $u_o$ |
| 1 | 100 | 1100 | D | C | $+3E$ |
| 2 | 001 | 1100 | D | N | $+2E$ |
| 3 | 010 | 1100 | C | N | $+E$ |
| 4 | 001 | 0110 | N | N | 0 |
| 5 | 100 | 0011 | N | C | $-E$ |
| 6 | 001 | 0011 | N | D | $-2E$ |
| 7 | 010 | 0011 | C | D | $-3E$ |

as well as the total standing voltage (TSV) of switches and diodes.

The comparison result indicates that the four circuit configurations have the same number of transistors and capacitors. The configuration NPC + NPC has minimum MBV and TSV of switches, but it requires the maximum number of diodes and gate drivers and its TSV of diodes is up to 10. The configurations NPC + NPP and NPP + NPP have fewer diodes and gate drivers as well as lower TSV of diodes, but their MBV is twice of NPC + NPC. The configuration NPP + NPC has two more diodes than the NPP + NPP and higher TSV than the NPC + NPC, but it has the lowest MBV and TSV of switches as well as less number of diodes and gate drivers. Overall, each configuration has its own merits and demerits. Just from the aspect of the selection of switches, NPP + NPC is better as all switching components are rated at the dc input voltage $2E$ except the bidirectional switch $S_3$. Hence, the following sections take it as an example to analyze the features of the hybrid NPP/NPC 7-level inverter.

## III. PERFORMANCE ANALYSIS WITH PD-PWM STRATEGY

### A. MODULATION

As well known, multi-carrier PWM (MCPWM) is the most popular modulation strategy for MLIs. For single-phase MLIs, there is almost the same performance for the three types of MCPWM methods, i.e., phase-disposition PWM (PD-PWM), phase-opposition-disposition PWM (POD-PWM) and alternate-phase-opposition-disposition PWM (APOD-PWM). For the three-phase configuration of MLIs, however, the PD-PWM is much better than POD-PWM and APOD-PWM in the aspects of waveform shape and THD of the output line voltages [31]. Hence, this work adopts the PD-PWM to modulate the NPP + NPC 7-level inverter and then analyzes its performance.

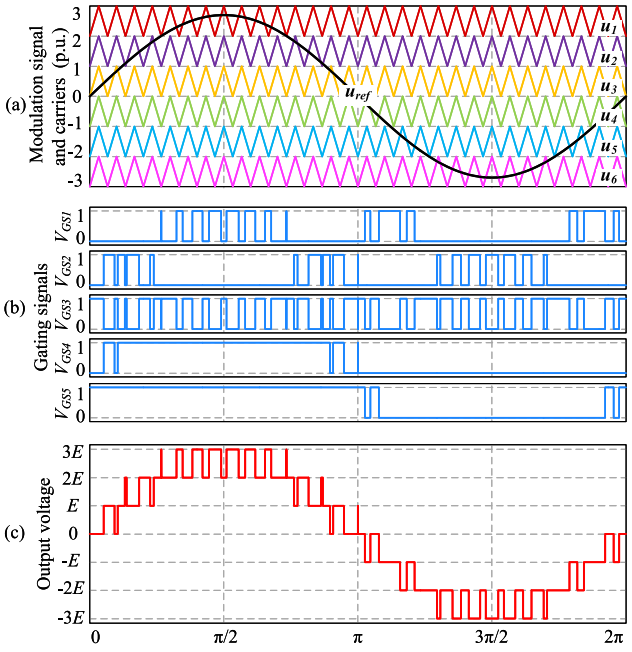



**FIGURE 4.** PD-PWM strategy for the NPP + NPC 7-level inverter. (a) Modulation signal and carriers. (b) Gating signals. (c) Output voltage.

When the PD-PWM is applied, there are six carriers $u_1 \sim u_6$ used to compare with the reference signal $u_{ref}$ to generate the gating signals of the NPP + NPC 7-level inverter as shown in Fig. 4(a). As illustrated in Table 3, the transistor $S_4$ is turned ON for the levels of $+E$ to $+3E$. Its gating signal $V_{GS4}$ is therefore generated by comparing $u_{ref}$ with $u_3$, i.e., $V_{GS4} = 1$ when $u_{ref} > u_3$. Similarly, the gating signal $V_{GS5}$ is generated by comparing $u_{ref}$ with $u_4$, i.e., $V_{GS5} = 1$ when $u_{ref} > u_4$. The transistors $S_6$ and $S_7$ are controlled in complementary with $S_4$ and $S_5$, respectively. For the transistor $S_1$, it is turned ON for the levels of $-E$ and $+3E$. Its gating signal generation logic is that $V_{GS1} = 1$ when $u_{ref} > u_1$ or $u_5 < u_{ref} < u_4$. Similarly, the gating signal generation logic for the transistor $S_2$ is that $V_{GS2} = 1$ when $u_{ref} < u_6$ or $u_3 < u_{ref} < u_2$. The transistor $S_3$ is turned ON only when both $S_1$ and $S_2$ are OFF. With these gating signals' generation logic, the modulation logic circuit of the NPP + NPC 7-level inverter is summarized as shown in Fig. 5. As a result, the ideal waveforms for the gating signals and output voltage of the NPP + NPC 7-level inverter with PD-PWM are shown in Figs. 4(b) and 4(c).

### B. DESIGN OF SWITCHED CAPACITORS

The same as other SC-based MLIs, the value of capacitors should be determined by their voltage ripples.

With the PD-PWM, the capacitor $C_{S1}$ continuously discharges to the load during the interval of $\theta \sim \pi - \theta$, while $C_{S2}$ continuously discharges to the load during the interval of $\pi + \theta \sim 2\pi - \theta$, as illustrated in Fig. 6. The amount of charge flowing out of $C_{S1}$ during the interval of $\theta \sim \pi - \theta$ is equivalent to that flowing out of $C_{S2}$ during the interval

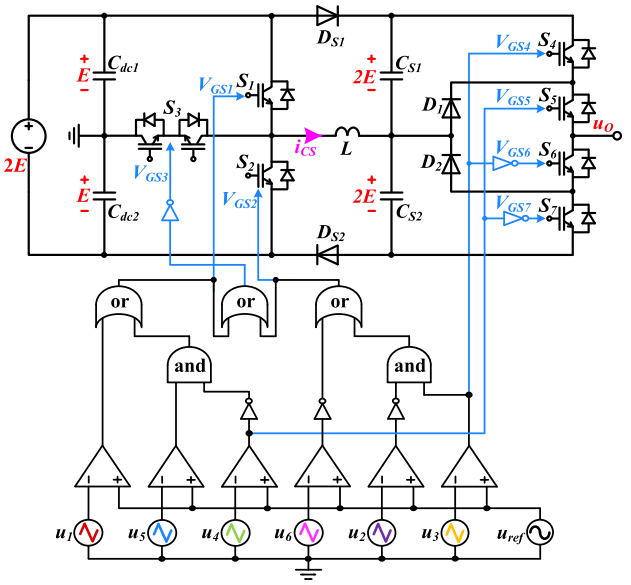



**FIGURE 5.** Modulation logic of the NPP + NPC 7-level inverter with PD-PWM strategy.

of $\pi + \theta \sim 2\pi - \theta$, i.e.,

$$Q_{CS1} = Q_{CS2} = \int_{\theta/\omega}^{(\pi-\theta)/\omega} I_O sin(\omega t - \varphi) dt \tag{1}$$

where $\omega$ is the angular frequency, $I_O$ is the amplitude of the load current, $\varphi$ is the phase difference between the output voltage and the load current, $\theta$ is an angle when the reference signal $u_{ref}$ reaches 2, i.e.,

$$\theta = \arcsin \frac{2}{A_{ref}} \tag{2}$$

where $A_{ref}$ is the amplitude of the reference signal $u_{ref}$. Assuming the two capacitors have the same capacitance $C_{S1,2}$, their voltage ripples are given by

$$\Delta V_{CS1,2} = \frac{Q_{Cs1,2}}{C_{s1,2}} \tag{3}$$

The maximum voltage ripple is obtained when the phase difference $\varphi = 0$, i.e. the load is pure resistive. In this case, the amplitude of the load current is $V_O/R$ and the amplitude of the output voltage is estimated by $V_O = E \times A_{ref}$. The voltage ripples can be further expressed by

$$\Delta V_{CS1,2} \leq \frac{2E}{\omega R C_{s1,2}} \sqrt{A_{ref}^2 - 4} \tag{4}$$

Considering that the voltage ripple ratio of SCs is $\delta = \Delta V_{CS1,2}/2E$ and $2E = 240$V, the output power and modulation ratio are $P_O = V_O \times I_O/2$ and $M_a = A_{ref}/3$, respectively, the capacitance $C_{S1,2}$ can be determined by

$$C_{S1,2} \geq \frac{P_O \sqrt{9M_a^2 - 4}}{64800\omega\delta M_a^2} \tag{5}$$

Intuitively, Fig. 7 shows the curves of the capacitance versus the modulation ratio and the output power,

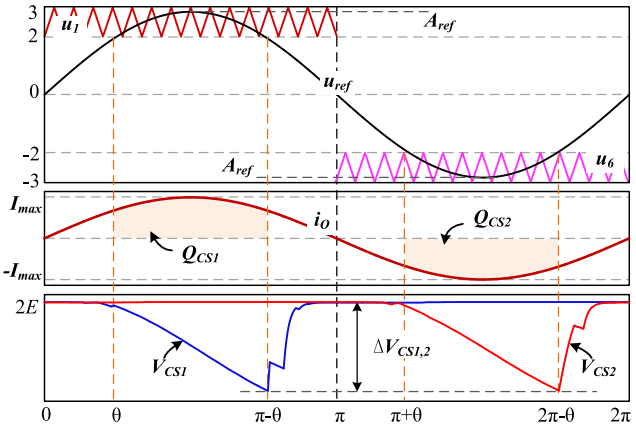



**FIGURE 6.** SCs' voltage ripples of the hybrid NPP/NPC 7-level inverter with PD-PWM strategy.

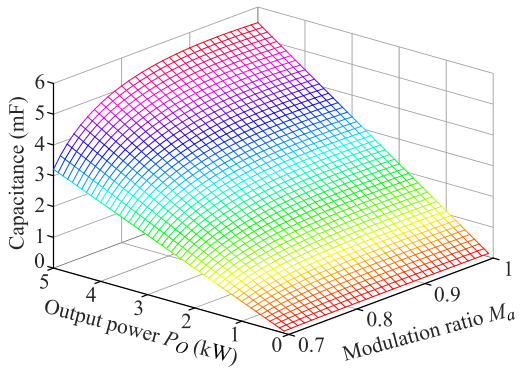



**FIGURE 7.** Capacitance versus the modulation ratio and the output power when $\delta = 10\%$.

when $\delta = 10\%$ and $\omega = 100\pi$. It indicates that $C_{S1,2}$ increases along with the modulation ratio $M_a$ and the output power $P_O$.

### C. CHARGING CURRENT STRESS REDUCTION

In the hybrid NPP/NPC 7-level inverter, $C_{S1}$ and $C_{S2}$ are charged by the dc source through $S_2 - D_{S1}$ and $S_1 - D_{S2}$, respectively. If there is no current limit, huge current pulses will appear at switching instants.

Taking $C_{S1}$ as an example, after continuously discharging for the interval of $\theta \sim \pi - \theta$, as illustrated in Fig. 6, it operates alternately in charging and discharging modes when the output level is switched between $+E$ and $+2E$. With the small inductor $L$, the equivalent discharging and charging circuits are shown in Figs. 8(a) and 8(b), and the ideal waveforms are depicted in Fig. 8(c), wherein $V_{F1}$ is the forward voltage drop of $D_{S1}$, $r_1$ is the total resistance of the charging loop.

The waveform of Fig. 8(c) indicates that the capacitor current can be switched from the load current $i_O$ to the pulse charging current immediately when $L = 0$. The charging current peak can be limited by the loop resistance $r_1$ but with high current stress $di/dt$.

When $L > 0$, the current will first drop from $-i_O$ to zero and then rise gradually. The greater the inductance $L$,

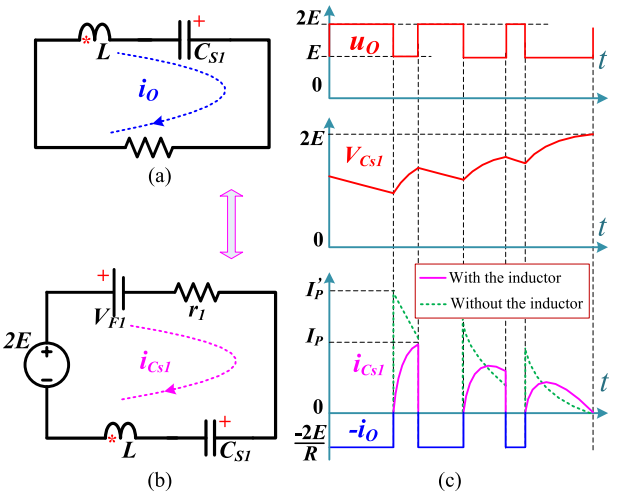



**FIGURE 8.** Operation of $C_{S1}$ when $u_O$ is switched between $+E$ and $+2E$. (a) Equivalent discharging circuit. (b) Equivalent charging circuit. (b) Capacitor voltage and current variation.

the slower the capacitor current variation and the slower the charging speed. Considering there is a small dead-time for $S_1$ and $S_2$ in practice, the inductor $L$ should therefore be so small that its current can drop to zero during the dead-time. In this case, the energy stored in the small inductor $L$ will be dissipated through sneak circuits as analyzed in [32].

Overall, the amplitude of the pulse charging current can be effectively limited by the components' parasitic resistance of the charging loop, and the current variation $di/dt$ can be limited by the inductor $L$.

### D. POWER LOSS ANALYSIS

As the NPP + NPC 7-level inverter operates alternately in the charging and discharging processes of capacitors, the power loss can be summarized into three categories which are charging loss of capacitors, switching loss of transistors and conduction loss caused by the load current.

#### 1) CHARGING LOSS OF SWITCHED CAPACITORS

For the NPP + NPC 7-level inverter, $C_{S1}$ is charged through $S_2 - D_{S1}$ for the level of $+E$ while $C_{S2}$ is charged through $S_1 - D_{S2}$ for the level of $-E$. The energy loss is the difference between the energy flowing out of the dc source and that flowing into the capacitor, and it is determined by the capacitors' voltage ripple $\Delta V_{CS1,2}$. Hence, the charging loss of $C_{S1}$ and $C_{S2}$ is given by

$$P_{Loss\_cr} = \frac{1}{2} C_{s1,2} \Delta V_{CS1,2}^2 f_{ref} \times 2 = C_{S1,2} \Delta V_{CS1,2}^2 f_{ref} \quad (6)$$

where again $C_{S1,2}$ is the capacitance, $\Delta V_{CS1,2}$ is the voltage ripple as shown in Fig. 6, $f_{ref}$ is the frequency of the reference signal $u_{ref}$. This part of power loss is actually absorbed by the parasitic resistance of components in the charging loop.

#### 2) SWITCHING LOSS OF TRANSISTORS

Generally, there are two methods for estimating the switching loss of a transistor, one of which is based on the overlap of the transistor's current and voltage at switching instants, and the other is based on the transistor's switching frequency $f_S$ and its parasitic capacitance $C_{OSS}$ as well as its voltage stress $V_{DS}$ [33], i.e.

$$P_{Loss\_sw} = f_S C_{oss} V_{DS}^2 \quad (7)$$

For the NPP unit, the switching frequency $S_3$ is equal to the carriers' frequency $f_C$ while that of $S_1$ and $S_2$ are half of the carriers' frequency $f_C$. The voltage stresses of $S_1$ and $S_2$ are $2E$ while that of $S_3$ is $E$, the switching loss of the NPP unit is therefore given by

$$P_{Loss\_sw1} = 4 f_C C_{oss1,2} E^2 + f_C C_{oss3} E^2 \quad (8)$$

where $C_{oss1,2}$ is the parasitic capacitance for $S_1$ and $S_2$, $C_{oss3}$ is that for $S_3$.

In addition, the diodes $D_{S1}$ and $D_{S2}$ have the same switching frequency as $S_1$ and $S_2$, their switching loss is therefore given by

$$P_{Loss\_sw2} = 4 f_C C_{osds1,2} E^2 \quad (9)$$

where $C_{osds1,2}$ is the parasitic capacitance for $D_{S1}$ and $D_{S2}$.

For the NPC unit, $S_4$ and $S_6$ operate at carriers' frequency when the output level is switched between 0 and $+E$, $S_5$ and $S_7$ operate at carriers' frequency when the output level is switched between 0 and $-E$, as shown in Fig. 3. As the diodes $D_1$ and $D_2$ provide current paths for the level of 0, their switching frequency is the same as $S_4 \sim S_7$. In one cycle of the output voltage, the number of state switching for each of $S_4 \sim S_7$ and $D_1 - D_2$ is therefore given by

$$n_S = 2 \times f_C \times \frac{\arcsin \frac{1}{A_{ref}}}{2\pi f_{ref}} = \frac{f_C}{\pi f_{ref}} \arcsin \frac{1}{A_{ref}} \quad (10)$$

where $A_{ref}$ is the amplitude of the reference signal $u_{ref}$.

As the voltage stresses for all components of the NPC are $2E$, their total switching loss is given by

$$\begin{aligned} P_{Loss_{sw3}} &= \left(4C_{oss4\sim7} + 2C_{osd1,2}\right) \times \left(n_S \times f_{ref}\right) \times (2E)^2 \\ &= \frac{\left(16C_{oss4\sim7} + 8C_{osd1,2}\right) E^2 f_C}{\pi} \arcsin \frac{1}{A_{ref}} \end{aligned} \quad (11)$$

where $C_{oss4\sim7}$ is the parasitic capacitance for $S_4 \sim S_7$, $C_{osd1,2}$ is that for $D_1$ and $D_2$.

The total switching loss of the NPP + NPC 7-level inverter is the sum of (8), (9) and (11).

#### 3) CONDUCTION LOSS CAUSED BY LOAD CURRENT

For the NPP unit, one of $S_1$, $S_2$ and $S_3$ are turned ON to provide paths for the load current at any time.

For the NPC unit, two of $S_4 \sim S_7$ are turned ON to provide paths for the load current at any time. The diodes $D_1$ and $D_2$ provide paths for the level of 0, therefore, there is no current flowing through them for a pure resistive load.

**TABLE 4. Comparison results of different 7-level inverters.**

| Topologies | $N_T$ | $N_D$ | $N_C$ | $N_G$ | $N_{S\_C}$ | TCT | VG (×$E$) | MBV (×$E$) | $TSV_{sw}$ (×$E$) | $TSV_{dio}$ (×$E$) | SB | CM | CF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [15] | 8 | 0 | 3 | 7 | - | 23 | 0.75 | 2 | 8 | 0 | No | Yes | 7 |
| [16] | 8 | 0 | 3 | 8 | - | 25.5 | 0.75 | 2 | 7 | 0 | No | No | 7.36 |
| [17] | 8 | 2 | 4 | 8 | - | 24 | 1 | 2 | 5 | 1 | No | No | 7.43 |
| [23] | 10 | 0 | 4 | 8 | 2 | 22 | 1.5 | 4 | 22 | 0 | Yes | Yes | 9.43 |
| [24] | 10 | 0 | 4 | 8 | 4 | 30 | 1.5 | 2 | 18 | 0 | Yes | Yes | 10 |
| [25] | 10 | 0 | 3 | 9 | 4 | 33 | 1.5 | 2 | 16 | 0 | Yes | No | 10.14 |
| [26] | 9 | 0 | 3 | 8 | 4 | 31.5 | 1.5 | 2 | 16 | 0 | Yes | No | 9.64 |
| [27] | 10 | 0 | 3 | 8 | 4 | 26 | 1.5 | 2 | 16 | 0 | Yes | No | 9 |
| [28] | 8 | 2 | 2 | 8 | 4 | 24 | 1.5 | 2 | 14 | 2 | Yes | No | 8.29 |
| [29] | 9 | 8 | 4 | 9 | 4 | 32 | 1.5 | 2 | 17 | 8 | Yes | No | 12.43 |
| [30] | 12 | 0 | 3 | 8 | 4 | 23 | 1.5 | 4 | 28 | 0 | Yes | No | 10.57 |
| NPC+NPP | 8 | 4 | 4 | 7 | 2 | 22 | 1.5 | 4 | 16 | 6 | Yes | Yes | 9.57 |
| NPC+NPC | 8 | 6 | 4 | 8 | 2 | 28 | 1.5 | 2 | 12 | 10 | Yes | Yes | 10.86 |
| NPP+NPP | 8 | 2 | 4 | 6 | 2 | 18 | 1.5 | 4 | 18 | 4 | Yes | Yes | 8.57 |
| NPP+NPC | 8 | 4 | 4 | 7 | 2 | 24 | 1.5 | 2 | 14 | 8 | Yes | Yes | 9.86 |

Considering the voltage stress for $S_{1,2,4\sim7}$ is double that for $S_3$ but $S_3$ is implemented by two anti-series transistors, it is assumed that all switches have the same on-resistance and the same forward voltage drop.

Except for the level of 0, the load current always flows through one dc-link capacitor. And it flows through one of $C_{S1}$ and $C_{S2}$ during the levels $\pm 2E$ and $\pm 3E$. To simplify the analysis, it is assumed that the load current always flows through one dc-link capacitor and one SCs, and the equivalent series resistance is $ESR_{eq} = ESRdc + ESR_{SC}$.

Summing up the above analysis, the conduction loss caused by the NPP and NPC units as well as the capacitors are therefore given by

$$P_{Loss\_Con1} = \left(3r_{S1} + ESR_{eq}\right) I_{rms}^2 + 3V_{FT} I_{av} \tag{12}$$

where $r_{S1}$ and $V_{FT}$ are the on-resistance and forward voltage drop for each of the transistors, $I_{rms}$ and $I_{av}$ are the rms and average values of the load current.

For the diodes $D_{S1}$ and $D_{S2}$, they provide load current paths for the levels of $\pm E$. And all currents charged into $C_{S1}$ and $C_{S2}$ have to flow through $D_{S1}$ and $D_{S2}$, respectively, and these currents are provided to load for the levels of $\pm 2E$ and $\pm 3E$. Hence, all load currents have to flow through $D_{S1}$ and $D_{S2}$. The power loss of the two diodes caused by the load current is therefore given by

$$P_{Loss\_Con2} = V_{FD} \times I_{av} = \frac{2\sqrt{2}}{\pi} I_{rms} V_{FD} \tag{13}$$

where $V_{FD}$ is the forward voltage drop of $D_{S1}$ and $D_{S2}$, $I_{av}$ is the average value of the load current for positive- or negative-half cycle.

The total conduction loss of the NPP + NPC 7-level inverter is the sum of (12) and (13).

## IV. COMPARISON WITH OTHER 7-LEVEL INVERTERS

For a fair study, various 7-level inverters presented in the recent three years are taken to compare with the hybrid NPP/NPC 7-level inverter in terms of the numbers of transistors ($N_T$), diodes ($N_D$), capacitors ($N_C$), gate drivers ($N_G$), the number of switching components ($N_{S\_C}$) in the charging path of SCs, the total conducting transistors (TCT) of all output levels, the MBV and TSV of switches and diodes, the voltage gain (VG), the cost function (CF), the self-balance (SB) capability for capacitor voltages, and the applicability of various 3-level NPC or NPP commercial modules (CM), as illustrated in Table 4. Here the VG is the ratio of the maximum output voltage to the dc input voltage, and the CF is defined by

$$CF = \frac{N_T + N_D + N_C + N_G + TCT + TSV_{sw} + TSV_{dio}}{7} \tag{14}$$

The comparison results indicate that two hybrid cascaded inverters of [15], [16] and the ANPC inverter of [17] have the minimum number of transistors and lower MBV and CF, but they don't have the boost capability and the voltage balance of the flying capacitors depends on the switching sequence selection. Hence, it is inevitable to sense the flying capacitors' voltage and control it through a complex algorithm. As mentioned before, the two NPP units in [23] are with different voltage stresses and its MBV is up to 4. In the works [24]–[29], the MBV is reduced to 2, and the TSV of switches and diodes of [24]–[28] is lower than the hybrid NPP/NPC topologies. However, the TCT of [24]–[26], [29] all exceeded 30 while the structure of [27], [28] cannot be extended for three-phase applications. For the inverter of [30], too many transistors are used. Additionally, the $N_{S\_C}$ of [24]–[30] is 4 which increases power transmission loss. In contrast, the four hybrid NPP/NPC topologies employ the fewest transistors and gate drivers. They have lower TCT, and the $N_{S\_C}$ is 2. The self-balanced capacitor voltages and boost capability are also competitive compared to the topologies of [15]–[17]. Moreover, various commercial 3-level NPC or NPP modules can be applied in the hybrid NPP/NPC topologies for simplifying the design process and speeding up commercialization.

Moreover, just from the aspect of the number of components, the PUC and MPUC 7-level inverters of [34], [35] use fewer components than the proposed inverter. However, the maximum voltage level of the PUC inverter is equal to the dc input voltage while that for the MPUC inverter is the

sum of the two dc sources. They therefore do not have boost capability. In contrast, the proposed uses a single dc source and it has boost capability. Of course, the boosting feature is at the cost of using two large capacitors $C_{S1}$ and $C_{S2}$. Moreover, easy three-phase expansion is another advantage of the proposed inverter compared with the PUC and MPUC inverters.

## V. SIMULATION AND EXPERIMENTAL RESULTS

To make a comparative analysis and verify the feasibility of the hybrid NPP/NPC 7-level inverter, both simulation and experimental results for single-phase configuration are provided in this section.

### A. SIMULATION RESULTS

Four simulation models were built in the PLECS software by referring to the structure of Fig. 1(b), wherein all parameters and components are given in Table 5.

**TABLE 5. Specification and components of the simulation models.**

| | |
|---|---|
| Input voltage | 480VDC |
| Output voltage's frequency | 50Hz |
| Carriers' frequency | 5kHz |
| modulation ratio $M_a$ | 0.9 |
| Capacitors $C_{dc1}$, $C_{dc2}$ | 1500μF(35mΩ) |
| Capacitors $C_{S1}$, $C_{S2}$ | 2000μF (70mΩ) |
| Current limitation inductor $L$ | 1μH |
| left-side unit of NPC | F3L50R06W1E3_B11 |
| right-side unit of NPC | F3L75R07W2E3_B11 |
| left-side unit of NPP | F3L225R07W2H3P_B63 |
| right-side unit of NPP | F3L75R12W1H3_B11 |
| Diodes $D_{S1}$, $D_{S2}$ | C3D20060D |

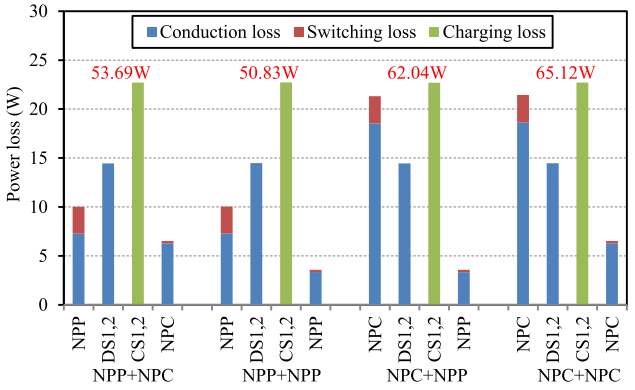



**FIGURE 9. Power loss breakdown of the hybrid NPP/NPC topologies for a resistive load 100Ω.**

Fig. 9 shows the power loss breakdown of the hybrid NPP/NPC topologies for a resistive load 100Ω. Specifically, the measured power loss caused by capacitors $C_{S1}$, $C_{S2}$ and diodes $D_{S1}$, $D_{S2}$ for four topologies are almost the same. As $C_{S1}$ and $C_{S2}$ are charged by the dc source through the left-side unit of Fig. 1(b), the power loss of the left-side unit is higher than that of the right-side unit. Based on the power loss analysis of Section III-D and the simulation parameters given in Table 5, three categories of power loss of the NPP + NPC configuration can be calculated, i.e., the charging loss of capacitors is 19.2W, the switching loss of transistors is 3.8W and the conduction loss caused by the load current is 28.54W. As a result, the total power loss of the NPP + NPC topology is 51.54W, which is slightly lower than the simulation result of 53.69W.

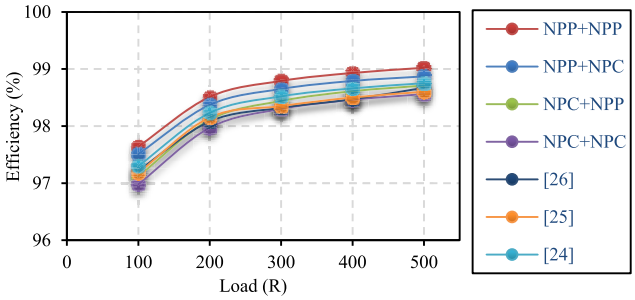



**FIGURE 10. Efficiency comparison.**

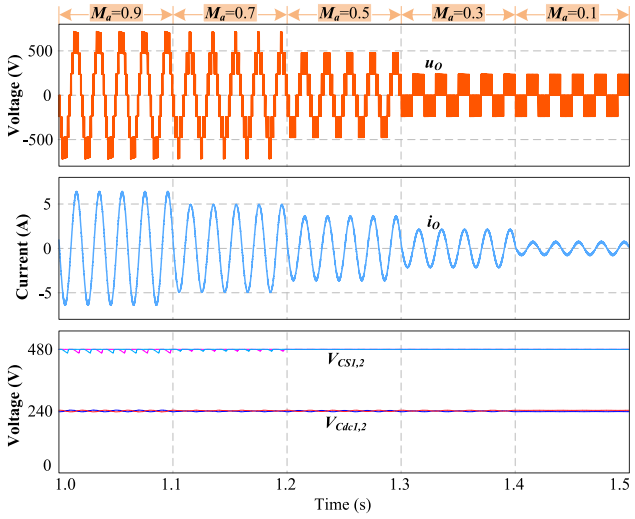



**FIGURE 11. Simulation results of $M_a$ changing of the NPP + NPC configuration for an inductive load 100Ω-50mH.**

Fig. 10 shows the efficiency comparison of the hybrid NPP/NPC topologies and the other three inverters of [24]–[26], wherein all simulation models were built in the PLECS software under the same conditions. It indicates that the two hybrid topologies of NPP + NPP and NPP + NPC have higher efficiency when the load changes from 100Ω to 500Ω. Moreover, although the NPP + NPP configuration has higher efficiency, it is difficult to be used for high voltage applications as it uses two high-voltage transistors. In contrast, the NPP + NPC configuration is more suitable for high voltage applications as it also has high efficiency and the unified blocking voltage of components.

When the modulation ratio $M_a$ changes from 0.9 to 0.1, the simulation results of the NPP + NPC inverter with an inductive load 100Ω-50mH are shown in Fig. 11. It indicates that the number of output levels changes from 7 to 5 and

further to 3 as the decrease of $M_a$. However, the four capacitors' voltages are very stable and self-balanced.

### B. EXPERIMENTAL RESULTS

An 1kW experimental prototype of the NPP + NPC 7-level inverter was built as shown in Fig. 12. The specification and components are listed in Table 6. The PD-PWM strategy is implemented in an FPGA controller and the modulation ratio $M_a$ is set to 0.9.

**TABLE 6. Specification and Components of the NPP + NPC 7-Level Prototype.**

| | |
|---|---|
| Input voltage | 240VDC |
| Rated power | 1kW |
| Output voltage's frequency | 50Hz |
| Carriers' frequency | 5kHz |
| Capacitors $C_{dc1}$, $C_{dc2}$ | 1500μF/35mΩ |
| Capacitors $C_{S1}$, $C_{S2}$ | 2000μF/40mΩ |
| Current limitation inductor $L$ | 1μH |
| Switches $S_1$, $S_2$, $S_4$, $S_5$, $S_6$ and $S_7$ | N-MOSFET, IRFP4868PBF |
| Bidirectional switch $S_3$ | 2×IRFP4568PBF |
| Diodes $D_1$, $D_2$, $D_{S1}$, $D_{S2}$ | DPG60C300HB |
| Controller | FPGA, EP4CE6F17C8N |

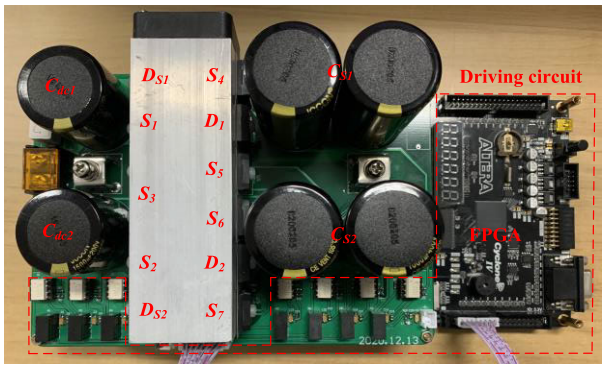
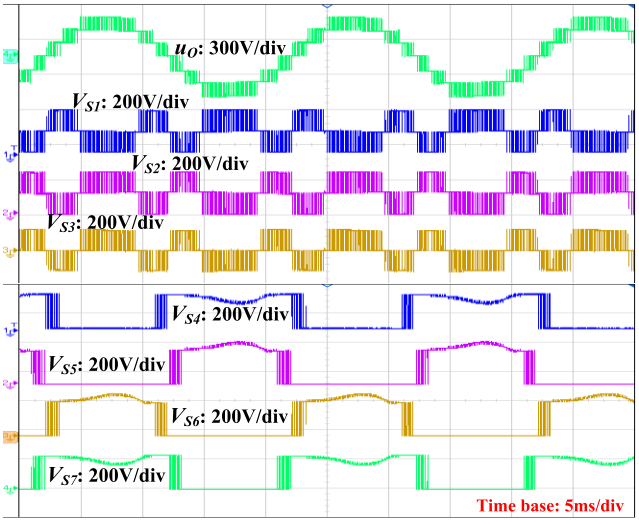


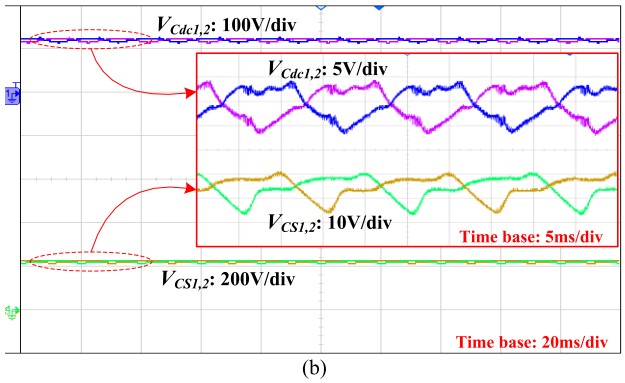

**FIGURE 12.** Experimental prototype of the NPP + NPC 7-level inverter.

Fig. 13 shows the experimental waveforms for a resistive load 50Ω. It can be observed from Fig. 13(a) that the output voltage $u_O$ is a 7-level PWM waveform and its maximum value is nearly 360V which is 1.5 times the dc input voltage. The measured rms value of $u_O$ is 224.58V. As the input current is 4.39A, the power conversion efficiency is therefore about 95.74%. Except for the switch $S_3$ is rated at 120V, all other switches are rated at 240V, which demonstrates that the voltage stresses for all switches do not exceed the dc input voltage. As shown in Fig. 13(b), the voltages of $C_{dc1}$ and $C_{dc2}$ are maintained at 120V while that of $C_{S1}$ and $C_{S2}$ are maintained at 120V. The measured voltage ripples for $C_{S1}$ and $C_{S2}$ are about 15.28V. It is higher than the theoretical value of 13.86V estimated by equation (4), which is mainly caused by the error of capacitance and the line impedance.

Fig. 14 shows the charging current waveform of the switched capacitors $C_{S1}$ and $C_{S2}$ with and without inductor $L$. The maximum charging current spike is found when the voltages of $C_{S1}$ and $C_{S2}$ reach their minimum values. With




(a)




(b)

**FIGURE 13.** Experimental results for a resistive load 50Ω. (a) Output voltage and Switches' voltages. (b) Capacitor voltages.

the small inductor $L$, the charging current changes smoothly at switching instants and its variation $di/dt$ is suppressed effectively.

Fig. 15 shows the experimental waveforms for an inductive load 50Ω-50mH. It can be observed from Fig. 15(a) that the output voltage $u_O$ is still a staircase PWM waveform and the output current $i_O$ is a nearly sinusoidal wave. The measured rms values of $u_O$ and $i_O$ are 224.36V and 4.25A, respectively. The capacitor voltages still can be self-balanced and have some ripples. As shown in Fig. 15(b), the harmonics of $u_O$ are mainly distributed around the carrier frequency 5kHz and its integer multiple and there are a few harmonics of $i_O$. The low harmonic components of $u_O$ are suppressed by the PD-PWM strategy.

The dynamic responses of the prototype are shown in Fig. 16. It indicates that the output current and capacitor voltages can quickly be in another steady state while the output voltage is very stable for the step-change of either resistive load or inductive load. Additionally, the power conversion efficiency increases to 96.85% when the load changes to 100Ω.

Finally, when the load R = 50Ω, the power loss distribution of the NPP + NPC 7-level prototype is estimated according

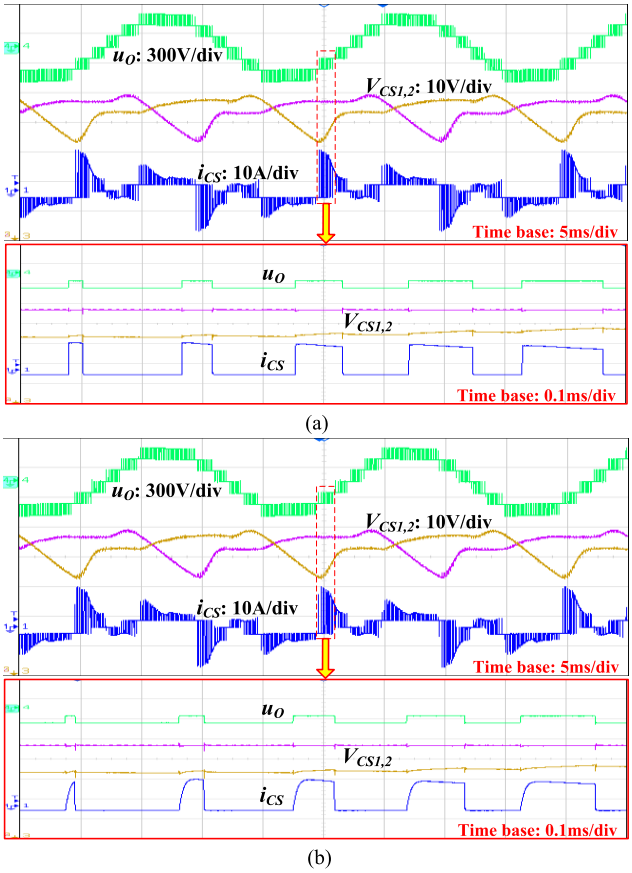



**FIGURE 14.** Charging current waveform of the switched capacitors $C_{S1}$ and $C_{S2}$. (a) Without inductor $L$. (b) With inductor $L$.

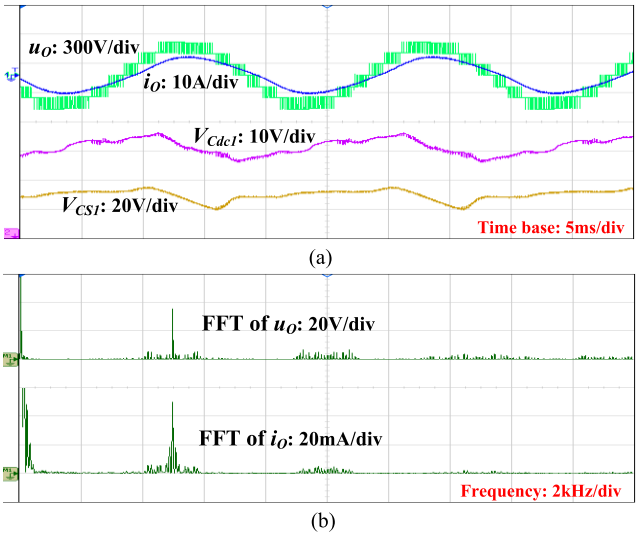



**FIGURE 15.** Experimental results for an inductive load 50Ω-50mH. (a) Output voltage, current and capacitor voltages. (b) Frequency spectrum of the output voltage and current.

to the analysis of Section III-D, as shown in Fig. 17. The results indicate that the majority of power loss is caused by the charging loss of the capacitors. This part of the loss will be consumed by the parasitic resistance in the charging loop including on-resistance of transistors and diodes and ESR

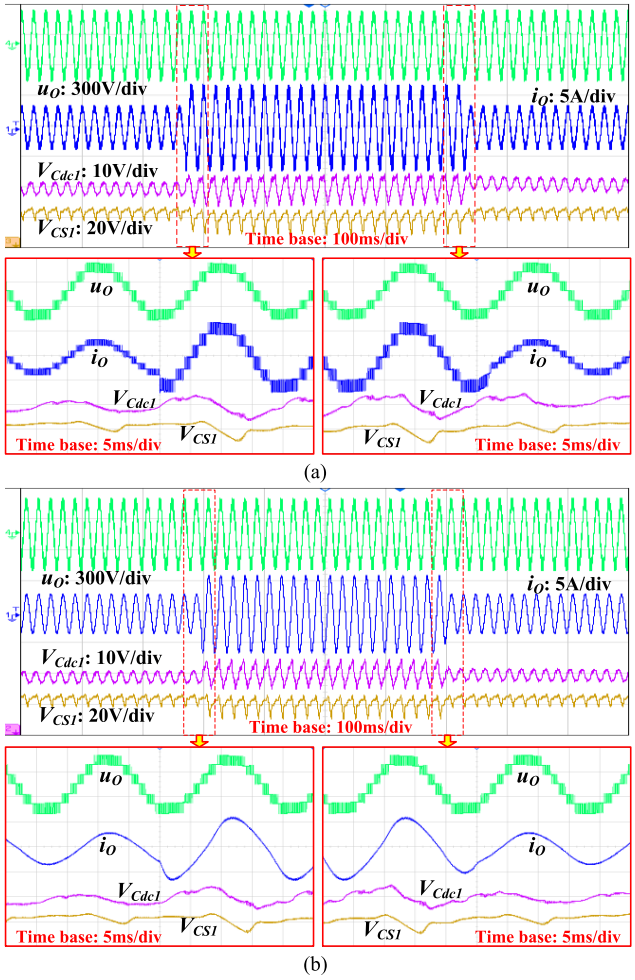



**FIGURE 16.** Waveforms of dynamic responses. (a) Step-change of load between 50Ω and 100Ω. (b) Step-change of load between 50Ω-50mH and 100Ω-50mH.

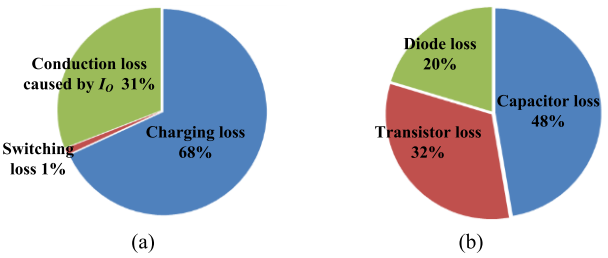



**FIGURE 17.** Power loss distribution of the prototype when R = 50Ω. (a) Three types of power losses. (b) Power loss breakdown of components.

of capacitors. As a result, capacitor loss accounts for the majority of total power loss, followed by transistor loss, while diode loss is relatively small.

## VI. CONCLUSION

This paper analyzed comparatively a hybrid NPP/NPC 7-level inverter structure with four specific circuit configurations. The general structure is derived from the recent work [23] and it has a boosting factor of 1.5 and self-balanced capacitor voltages. According to the theoretical analysis and

simulation results, it is found that the four configurations of the NPP/NPC inverter have their own merits and demerits. Especially, the dual-NPP inverter has the advantages of fewer components and higher efficiency, while the NPP + NPC configuration has lower voltage stress of components making it more suitable for high-voltage applications. Experimental results indicate that the NPP + NPC inverter has good performance for both steady-state and dynamic change of loads. In addition, various commercialized NPC and NPP modules can be used to simplify the design of the hybrid NPP/NPC inverters.

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**YUANMAO YE** (Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Jinan, Jinan, China, in 2007, the M.Sc. degree in control theory and control engineering from the South China University of Technology, Guangzhou, China, in 2010, and the Ph.D. degree from The Hong Kong Polytechnic University, Hong Kong, in 2016. From September 2010 to January 2014, he was with the Department of Electrical Engineering, The Hong Kong Polytechnic University, as a Research Assistant. He is currently a Professor with the School of Automation, Guangdong University of Technology. His research interests include multilevel inverters, battery management systems, and switched-capacitor technique and its industrial applications.

**GUOXIN ZHANG** was born in Shantou, China, in 1996. He received the B.Sc. degree from Guangdong Polytechnic Normal University, Guangzhou, China, in 2019. He is currently pursuing the M.Sc. degree with the School of Automation, Guangdong University of Technology, Guangzhou.

His research interests include multilevel inverters and switched-capacitor technique and its industrial applications.

**JINLIANG HUANG** was born in Shantou, China, in 1997. He received the B.Sc. degree in electrical engineering and automation from the Dongguan University of Technology, Dongguan, China, in 2020. He is currently pursuing the M.Sc. degree with the School of Automation, Guangdong University of Technology, Guangzhou, China.

His research interests include modular multilevel inverters and switched-capacitor power conversion technique.

**SHIKAI CHEN** was born in Shanwei, China, in 1996. He received the B.Sc. degree from Guangdong Polytechnic Normal University, Guangzhou, China, in 2018. He is currently pursuing the M.Sc. degree with the School of Automation, Guangdong University of Technology, Guangzhou.

His research interests include modular multilevel inverters and motor control.

**XIAOLIN WANG** received the B.Sc. degree in electrical engineering and automation from Three Gorges University, Yichang, China, in 2012, and the M.Sc. and Ph.D. degrees from The Hong Kong Polytechnic University, Hong Kong, in 2013 and 2018, respectively. She is currently an Assistant Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China.

Her research interests include battery management systems, energy balancing systems, distribution system planning, and vehicle to grid (V2G).