Highly Efficient HBT Power Amplifier Using High-Q Single- and Two-Winding Transformer With IMD3 Cancellation

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ABSTRACT This paper presents a highly efficient InGaP/GaAs HBT power amplifier (PA) implemented using a proposed high-Q single- and two-winding transformer. A single- and two-winding transformer is designed with a printed circuit board (PCB) to combine the output power with a reduced passive loss. Compared to a typical 1:2 two-winding transformer, an additional unit amplifier is connected at the mid-point of the secondary winding to construct a single-winding transformer without additional windings. An IMD3 cancellation technique using a single- and two-winding transformer is also proposed to obtain a high linear output power with high power-added efficiency (PAE) without additional design circuitry. The IMD3 components of the two input currents in the single- and two-winding transformer are 180° out-of-phase cancelling each other at output. The proposed PA is integrated with an InGaP/GaAs HBT process using a PCB transformer. The experimental results demonstrate that the PA achieves a saturated output power of 33.3 dBm, with a PAE of 61.3% at 0.91 GHz. The proposed PA is also tested with an orthogonal frequency-division multiplexing (OFDM) 64-quadrature amplitude modulation (QAM) signal having a bandwidth of 10 MHz and peak-to-average power ratio (PAPR) of 7.8 dB at 0.91 GHz to evaluate the improvement in linearity. The PA achieves an adjacent channel leakage ratio (ACLR) of −42 dBc up to an output power of 26.0 dBm with a PAE of 26.8% and current consumption of 297 mA.

INDEX TERMS InGaP/GaAs HBT power amplifier, IMD3 cancellation, single-winding transformer, PCB, femtocell.

I. INTRODUCTION

There is an increasing demand for high data rates in modern high-speed wireless communications. However, this requires an orthogonal frequency-division multiplexing (OFDM) signal with a high peak-to-average power ratio (PAPR). Therefore, a linear power amplifier (PA) is required with this signal to operate in the back-off region from its saturated output power to satisfy the linearity requirements. The linear output power is reduced with a large back-off from the saturated output power, and the power-added efficiency (PAE) also decreases significantly. To increase the linear output power of PAs, the saturated output power needs to be increased;

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for instance, the saturated output power of typical femtocell base-station PAs is more than 2 W [1]–[4].

Power-combining techniques have been actively studied to increase the output power of PAs. The transformer-based power-combining technique is a practical method as it can provide a matching function and a balun function with a relatively small form factor. Series power-combining transformers (SCTs) [5]–[12] and parallel power-combining transformers (PCTs) [13]–[15] are the most popular itransformers for combining power from several unit amplifiers. Both SCTs and PCTs are based on two-winding transformers. In addition, single- and two-winding based transformers have recently been introduced to take advantage of a single-winding based transformer, which can be implemented with a low loss and a compact size [16]–[19]. The saturated

output power and linear output power can be increased using power-combing transformers.

To achieve an output power more than 2 W by using a typical single-ended topology, the load resistance of the transistor should be significantly low. For instance, to deliver 2.5 W (34 dBm) output power (P_{OUT}) using a collector voltage swing of ± 5 V with a supply voltage (V_{CC}) of 5 V and a knee voltage (V_{KNEE}) of 0.5 V, the required load resistance (R_{IN}) can be calculated as

$$R_{IN} = \frac{(V_{CC} - V_{KNEE})^2}{2P_{OUT}} = \frac{(5V - 0.5V)^2}{2 \times 2.5W} = 4.05\Omega \quad (1)$$

For a 50-Ω load impedance, a large impedance transformation ratio is required. Slight variations in the passive output circuits may cause significant performance degradation. The higher the impedance transformation ratio of the passive circuits, the higher the loss [20]. However, when an additional amplifier is combined with power-combining passive circuits, the required impedance transformation is reduced by half, resulting in an improved passive loss. In addition, the design sensitivity for the performance variation in the passive output circuits can be reduced. However, considering practical implementations, the combining loss from an additional structure can degrade the passive efficiency of the passive output circuits. To effectively combine multiple unit amplifiers, a high-Q single- and two-winding transformer is proposed in our paper. A low quality factor in an output transformer can limit the overall performance, such as the output power and PAE of the implemented PAs. Hence in this work, a single- and two-winding transformer is implemented with a printed circuit board (PCB), providing a thick *Cu* metal layer.

For femtocell base-station applications, a higher linearity performance for the adjacent channel leakage ratio (ACLR) is typically required. The large back-off in typical PA designs that helps meet the required ACLR levels, leads to a considerable decrease in efficiency. Therefore, various linearization methods for HBT PA designs have been proposed to improve the linear output power. To compensate for nonlinear distortion, active bias circuits are widely used for typical HBT PA designs [2], [18], [21]–[24]. A dynamic feedback Darlington circuit has been proposed in [25]. A pre-distortion method between the first- and second-stage amplifiers has been proposed in [21]. In addition, an IMD3 cancellation method using two parallel-combined transistors has been introduced [2]. In this work, to enhance the linearity performance of the HBT PA, IMD3 cancellation using a single- and two-winding transformer is proposed. Moreover, an analysis of the proposed IMD3 cancellation method is presented.

The remainder of this paper is organized as follows. In Section II, the proposed high-Q single- and two-winding transformer is analyzed and compared with a typical 1:2 two-winding transformer and two-way power combining transformer to validate its effectiveness. Section III describes the operation of the proposed IMD3 cancellation mechanism with a single- and two-winding transformer. In Section IV,
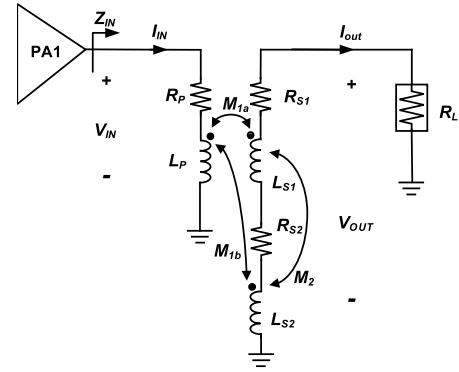

FIGURE 1. Equivalent circuit of a typical 1:2 two-winding transformer.

the measurement results of the implemented PA are presented. Finally, the conclusions of this work are highlighted in Section V.

II. HIGH-Q SINGLE- AND TWO-WINDING TRANSFORMER

Fig. 1 shows the equivalent non-ideal circuit of a typical 1:2 two-winding transformer. Each inductor and resistor in Fig. 1 represent the equivalent circuit parameters for each turn in the primary and secondary windings. A 1:2 turn ratio is typically used for an output power more than 2 W; thus, one turn for the primary side and two turns for the secondary side are chosen for this analysis. R_P and L_P are used for the primary winding, whereas two inductors (L_{S1} and L_{S2}) and resistors (R_{S1} and R_{S2}) are used for the two-turn secondary winding. Considering the voltages induced at the primary and secondary windings, the relationship between voltages and currents can be represented as

$$\begin{bmatrix} V_{IN} \\ V_{OUT} \end{bmatrix}$$
$$= \begin{bmatrix} R_P + j\omega L_P & -j\omega(M_{1a} + M_{1b}) \\ j\omega(M_{1a} + M_{1b}) & -(R_{S1} + R_{S2}) - j\omega(L_{S1} + L_{S2} + 2M_2) \end{bmatrix}$$
$$\times \begin{bmatrix} I_{IN} \\ I_{OUT} \end{bmatrix} \quad (2)$$

If $R_P = R_{S1} = R_{S2} = R$, $L_P = L_{S1} = L_{S2} = L$, and $M_{1a} = M_{1b} = M_1 \neq M_2$, V_{IN} and V_{OUT} can be defined as

$$V_{IN} = (R + j\omega L) I_{IN} - j2\omega M_1 I_{OUT} \quad (3)$$
$$V_{OUT} = j2\omega M_1 I_{IN} - 2[(R + j\omega(L + M_2)] I_{OUT}$$
$$= R_L I_{OUT} \quad (4)$$

where R_L is the output resistance, which is typically 50 Ω. The input impedance Z_{IN} of the transformer is expressed as follows:

$$Z_{IN} \equiv \frac{V_{IN}}{I_{IN}} \equiv R_{IN} + jX_{IN}$$
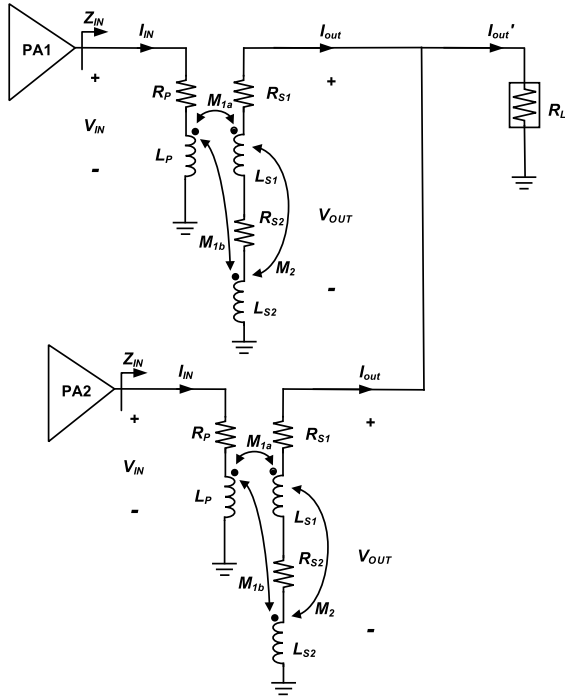$$= R + j\omega L + \frac{(2\omega M_1)^2}{(2R + R_L) + j2\omega(L + M_2)} \quad (5)$$

FIGURE 2. Equivalent circuit of a typical two-way power combining transformer.

where R_{IN} is the real part and X_{IN} is the imaginary part of Z_{IN}. R_{IN} is expressed as

$$R_{IN} = R + \frac{(2\omega M_1)^2(2R + R_L)}{(2R + R_L)^2 + [2\omega(L + M_2)]^2} \tag{6}$$

The transformer efficiency can be expressed as follows:

$$\eta_{Two-windng} \equiv \frac{P_L}{P_{IN}} \equiv \frac{R_L \, |I_{OUT}|^2}{R_{IN} \, |I_{IN}|^2} \tag{7}$$

where

$$I_{OUT} = \frac{j2\omega M_1}{(2R + R_L) + j2\omega(L + M_2)} I_{IN}$$

The equivalent non-ideal circuit of a two-way parallel power combining transformer is shown in Fig. 2. The two 1:2 two-winding transformers are connected in parallel. The relationship between voltage and current is represented by (8).

$$\begin{bmatrix} V_{IN} \\ V_{OUT} \end{bmatrix}$$
$$= \begin{bmatrix} R_P + j\omega L_P & -j\omega(M_{1a} + M_{1b}) \\ j\omega(M_{1a} + M_{1b}) & -(R_{S1} + R_{S2}) - j\omega(L_{S1} + L_{S2} + 2M_2) \end{bmatrix}$$
$$\times \begin{bmatrix} I_{IN} \\ I_{OUT} \end{bmatrix} \tag{8}$$

If $R_P = R_{S1} = R_{S2} = R$, $L_P = L_{S1} = L_{S2} = L$, and $M_{1a} = M_{1a} = M_{1b} = M_1 \neq M_2$, V_{IN} and V_{OUT} can be defined as

$$V_{IN} = (R + j\omega L) I_{IN} - j2\omega M_1 I_{OUT} \tag{9}$$
$$V_{OUT} = j2\omega M_1 I_{IN} - 2\left[(R + j\omega(L + M_2)\right] I_{OUT}$$
$$= R_L I'_{OUT} = R_L 2 I_{OUT} \tag{10}$$

The input impedance Z_{IN} of the transformer is expressed as follows:

$$Z_{IN} \equiv \frac{V_{IN}}{I_{IN}} = R + j\omega L + \frac{(2\omega M_1)^2}{(2R + 2R_L) + j2\omega(L + M_2)} \tag{11}$$

In addition, R_{IN} is calculated as follows:

$$R_{IN} = R + \frac{(2\omega M_1)^2(2R + 2R_L)}{(2R + 2R_L)^2 + [2\omega(L + M_2)]^2} \tag{12}$$

The transformer efficiency can be expressed as follows:

$$\eta_{Two-way} \equiv \frac{P_L}{P_{IN}} \equiv \frac{R_L \, |2I_{OUT}|^2}{2R_{IN} \, |I_{IN}|^2} \tag{13}$$

where

$$I_{OUT} = \frac{j2\omega M_1}{(2R + 2R_L) + j2\omega(L + M_2)} I_{IN}$$

Fig. 3 shows the equivalent non-ideal circuit of a single- and two-winding transformer. Compared with the circuit shown in Fig. 1, only one additional amplifier is connected to the middle of the secondary winding without increasing circuit complexity. Thus, the geometry of a single- and two-winding transformer shown in Fig. 3 is the same as a 1:2 two-winding transformer in Fig. 1. The voltage and current relationship is represented in (14), as shown at the bottom of the next page. If $R_P = R_{S1} = R_{S2} = R$, $L_P = L_{S1} = L_{S2} = L$, and $M_{1a} = M_{1b} = M_1 \neq M_2$, then V_{IN} and V_{OUT} can be defined as

$$V_{IN1} = (R + j\omega L) I_{IN1} + j\omega M_1 I_{IN2} - j2\omega M_1 I_{OUT} \tag{15}$$
$$V_{IN2} = j\omega M_1 I_{IN1} + (R + j\omega L) I_{IN2}$$
$$- (R + j\omega L + j\omega M_2) I_{OUT} \tag{16}$$
$$V_{OUT} = 2j\omega M_1 I_{IN1} + (R + j\omega L + j\omega M_2) I_{IN2}$$
$$- 2(R + j\omega L + j\omega M_2) I_{OUT} = R_L I_{OUT} \tag{17}$$

FIGURE 3. Equivalent circuit of a single- and two-winding transformer.
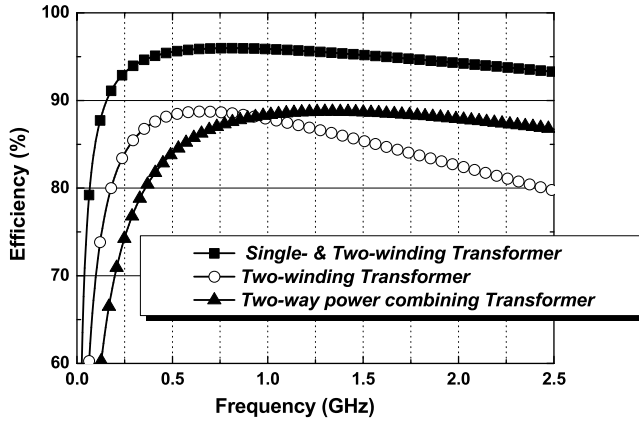
FIGURE 4. Calculated transformer efficiencies for a typical 1:2 two-winding transformer, two-way power combining transformer, and single- and two-winding transformer.

FIGURE 5. Calculated transformer efficiencies of a single- and two-winding transformer for different ratios between I_{IN1} and I_{IN2}.

The input impedances (Z_{IN1} and Z_{IN2}) of transformer are given by

$$
\begin{aligned}
Z_{IN1} &= \frac{V_{IN1}}{I_{IN1}} = R + j\omega L + j\omega M_1 \frac{I_{IN2}}{I_{IN1}} \\
&- 2j\omega M_1 \frac{2j\omega M_1 + (R + j\omega L + j\omega M_2)\frac{I_{IN2}}{I_{IN1}}}{2R + R_L + 2j\omega L + 2j\omega M_2}
\end{aligned} \tag{18}
$$

$$
\begin{aligned}
Z_{IN2} &= \frac{V_{IN2}}{I_{IN2}} = R + j\omega L + j\omega M_1 \frac{I_{IN1}}{I_{IN2}} \\
&- (R + j\omega L + j\omega M_2) \frac{R + j\omega L + j\omega M_2 + 2j\omega M_1 \frac{I_{IN1}}{I_{IN2}}}{2R + R_L + 2j\omega L + 2j\omega M_2}
\end{aligned} \tag{19}
$$

In addition, R_{IN1} and R_{IN2} are calculated as follows:

$$
R_{IN1} = R + \frac{4\omega^2 M_1^2 (2R + R_L) + 2\omega^2 R_L (M_1 L + M_1 M_2)\frac{I_{IN2}}{I_{IN1}}}{(2R + R_L)^2 + (2\omega L + 2\omega M_2)^2} \tag{20}
$$

The efficiency of the single- and two-winding transformer can be represented as

$$
\eta_{Single-\&Two-windng} \equiv \frac{|I_{out}|^2 \cdot R_L}{|I_{IN1}|^2 R_{IN1} + |I_{IN2}|^2 R_{IN2}} \tag{22}
$$

where

$$
I_{OUT} = \frac{2j\omega M_1 I_{IN1} + (R + j\omega L + j\omega M_2) I_{IN2}}{(2R + R_L) + j2\omega(L + M)}
$$

Fig. 4 illustrates the graph of the calculated transformer efficiencies for a typical 1:2 two-winding transformer, two-way power combining transformer, and single- and
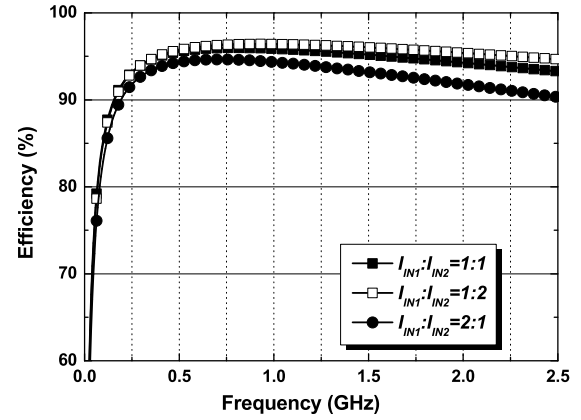
two- winding transformer. Here, R_L is 50 Ω, and the inductance (L) and resistance (R) are chosen as $L = 3.7$ nH and $R = \omega L / Q$ (quality factor $Q = 40$), respectively, considering the practical implementation of transformers on a PCB. The mutual inductance (M) is given by $M_1 = k_1 \sqrt{L \cdot L}$ ($k_1 = 0.57$) and $M_2 = k_2 \sqrt{L \cdot L}$ ($k_2 = 0.41$). All parameters are selected based on the values extracted from the results of electromagnetic (EM) simulation. As shown in Fig. 4, the calculated transformer efficiency of the single- and two-winding transformer is higher than efficiencies of the typical 1:2 two-winding transformer and two-way power combining transformer. As shown in Fig. 5, efficiency performances of a single- and two-winding transformer for different ratios between I_{IN1} and I_{IN2} are plotted. Efficiency of the single- and two-winding transformer decreases with an increase the ratio of I_{IN1} to I_{IN2}. However, the efficiency of the single- and two-winding transformer is still higher than the efficiency of the two other transformers. Fig. 6 shows the calculated transformer efficiencies of the single- and two-winding transformer for different values of Q; it can be seen that a higher transformer efficiency can be achieved by increasing Q. Therefore, a low passive loss can be realized using a high-Q transformer design with a PCB.

Fig. 7 offers a 3-D view of the proposed high-Q single- and two-winding transformer with a four-layer FR-4 PCB. The primary and secondary windings are implemented using 18-μm-thick M2 and M1 layers, respectively. The metal width of each winding is 100 μm. The spacing between the turns in the secondary winding is 100 μm, considering the minimum spacing rule for PCB implementation. The size of the proposed transformer is 2000 μm × 2400 μm. The EM simulations were performed using the Keysight ADS momentum.

$$
\begin{bmatrix} V_{IN1} \\ V_{IN2} \\ V_{OUT} \end{bmatrix} = \begin{bmatrix} R_p + j\omega L_p & j\omega M_{1b} & -j\omega(M_{1a} + M_{1b}) \\ j\omega M_{1b} & R_{S2} + j\omega L_{S2} & -(R_{S2} + j\omega L_{S2} + j\omega M_2) \\ j\omega(M_{1a} + M_{1b}) & (R_{S2} + j\omega L_{S2} + j\omega M_2) & -[R_{S1} + R_{S2} + j\omega(L_{S1} + L_{S2}) + j2\omega M_2] \end{bmatrix} \cdot \begin{bmatrix} I_{IN1} \\ I_{IN2} \\ I_{OUT} \end{bmatrix} \tag{14}
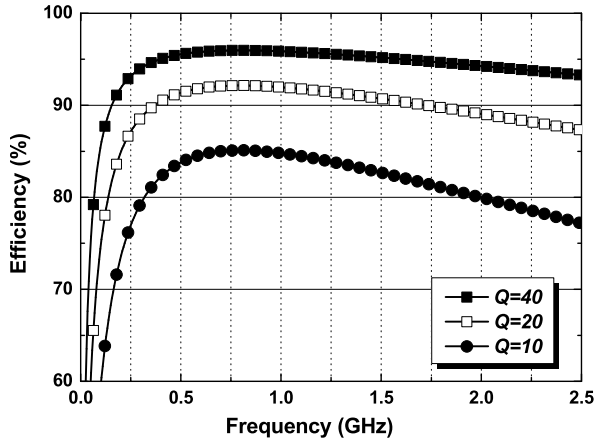$$

FIGURE 6. Calculated transformer efficiencies of a single- and two-winding transformer for different Q values.
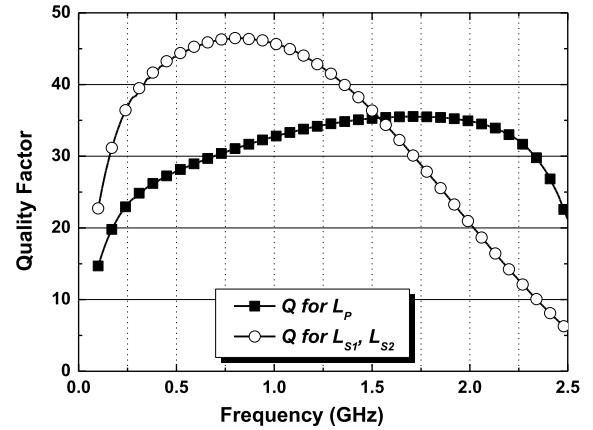

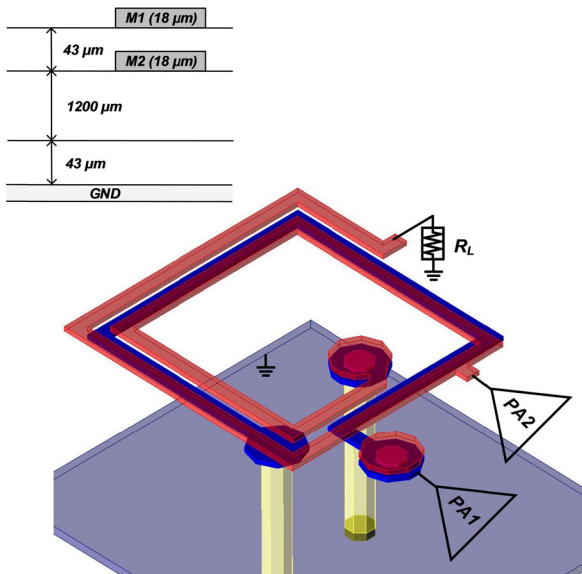**FIGURE 8.** EM simulated Q of the single- and two-winding transformer.

FIGURE 7. Layout of the single- and two-winding transformer using PCB.

FIGURE 9. EM simulated transformer efficiencies for a typical 1:2 two-winding transformer and single- and two-winding transformer.

Fig. 8 presents the Q values for each winding in the single- and two-winding transformer. The Q values for the primary winding (L_P) and secondary winding (L_{S1}, L_{S2}) are 32 and 46, respectively, at 0.91 GHz. Fig. 9 shows the passive efficiencies obtained via EM-simulation for the typical 1:2 two-winding transformer and the single- and two-winding transformer. Insertion loss is defined as the inverse of the maximum available gain, which is typically used to characterize the transformer efficiency [8], [9], [13]–[15], [17]–[19].
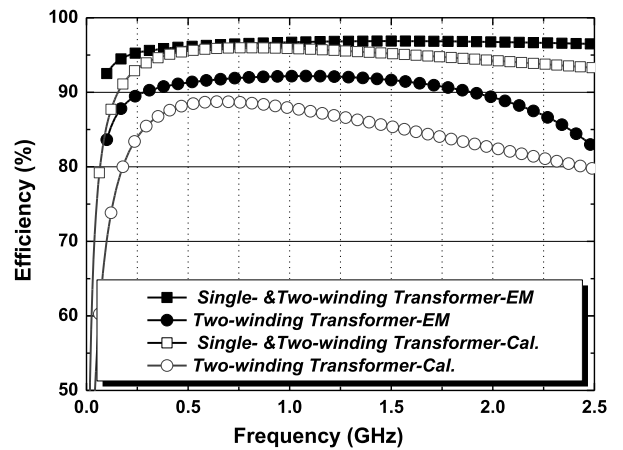
The EM simulated insertion losses are converted to efficiency performances to compare with the calculated results. As indicated in Fig. 9, a high-efficiency performance can be achieved using a single- and two-winding transformer. There is a minor difference between the calculated and EM simulated results. However, the trends from the EM simulated results agree with the trends from the calculated results. Through EM simulation, the transformer efficiency of the 1:2 two-winding transformer is found to be 92.1% at 0.91 GHz. A transformer efficiency of 96.7% is achieved using the single- and two-winding transformer at 0.91 GHz. Therefore, a PA capable of achieving high output power and high efficiency

$$R_{IN2} = R + \frac{\omega^2 (L + M_2)^2 (2R + R_L) - 2\omega^2 R (L + M_2)^2 + 2\omega^2 M_1 (L + M_2)^2 (2R + R_L) \frac{I_{IN1}}{I_{IN2}}}{(2R + R_L)^2 + (2\omega L + 2\omega M_2)^2}$$
$$- \frac{R^2 (2R + R_L) + 2\omega^2 R (L + M_2)^2 + 4\omega^2 R M_1 (L + M_2) \frac{I_{IN1}}{I_{IN2}}}{(2R + R_L)^2 + (2\omega L + 2\omega M_2)^2} \tag{21}$$
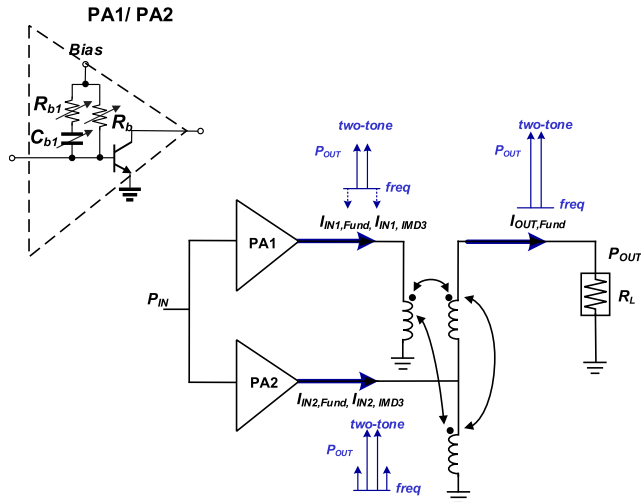
FIGURE 10. IMD3 cancellation using a single- and two-winding transformer.
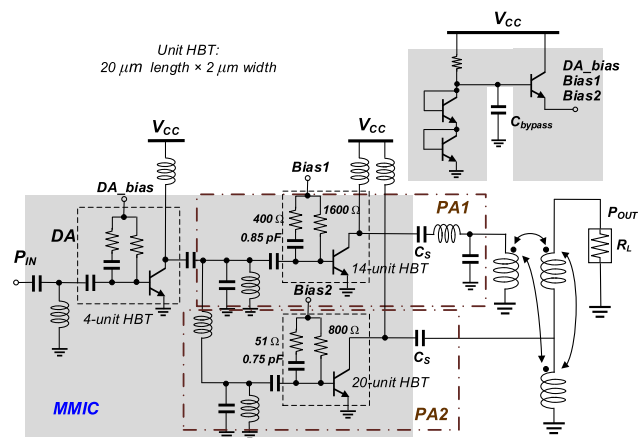

FIGURE 11. Total schematic of the proposed HBT PA with a single- and two-winding transformer.

can be implemented using the proposed high-Q single- and two-winding transformer.

III. IMD3 CANCELLATION WITH SINGLE- AND TWO-WINDING TRANSFORMER

To achieve high linearity without increasing the design complexity, an IMD3 cancellation mechanism using a single- and two-winding transformer is proposed, as shown in Fig. 10. Each unit transistor in PA1 and PA2 includes a ballast resistor R_b to prevent thermal runaway. A bypass circuit with R_{b1} and C_{b1} is added to the unit transistor to compensate for the decrease in the base bias voltage [23]. Change in R_b, R_{b1}, and C_{b1} causes a significant change in the phases of the IMD3 current components but do not cause a significant change in the phases of the fundamental current components [2]. The two PAs (PA1 and PA2) are connected through the single- and two-winding transformer, and different values for R_b, R_{b1}, and C_{b1} are selected to cancel the IMD3 current components from PA1 and PA2. Based on the voltage and
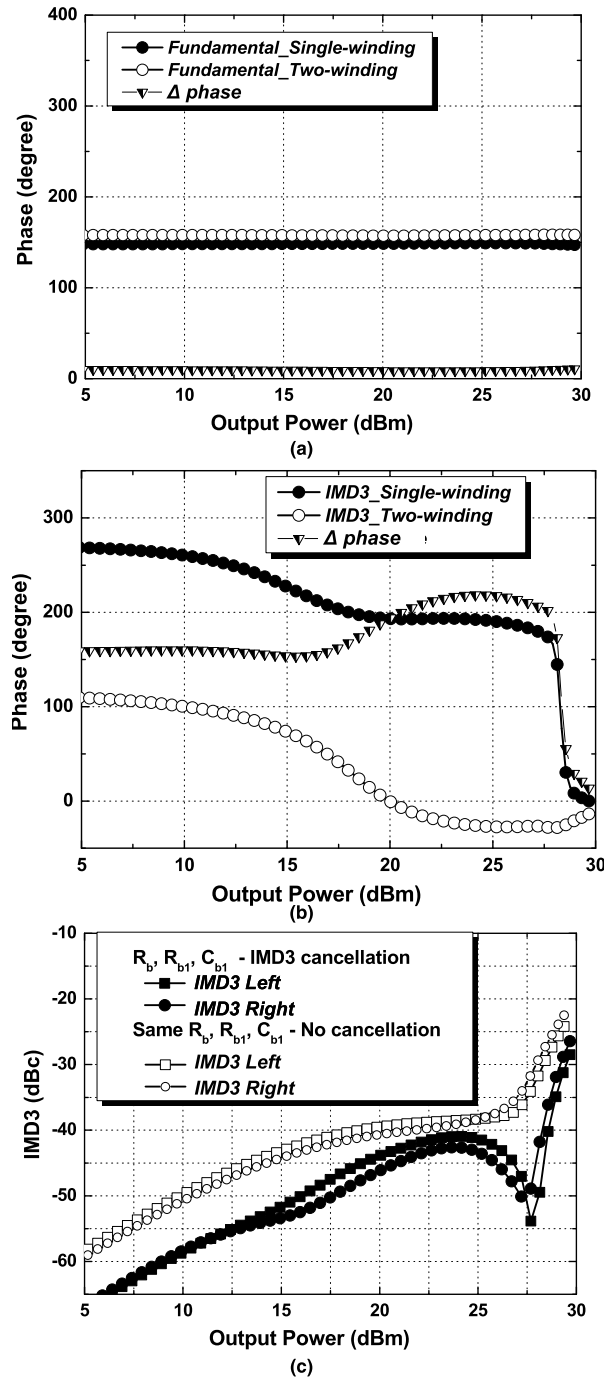

FIGURE 12. Simulated results of the proposed PA. (a) Phases of fundamental currents, (b) phases of IMD3 currents, and (c) total IMD3 of the proposed PA.

current relationship for the proposed transformer expressed in (14), the output current I_{OUT} is given by

$$I_{OUT} = \frac{2j\omega M_1 I_{IN1} + (R + j\omega L + j\omega M_2) I_{IN2}}{(2R + R_L) + j2\omega(L + M)} \quad (23)$$

The currents I_{IN1} and I_{IN2} from PA1 and PA2 are summed at the output. Therefore, if the phases of the fundamental currents from PA1 and PA2 are the same, the output
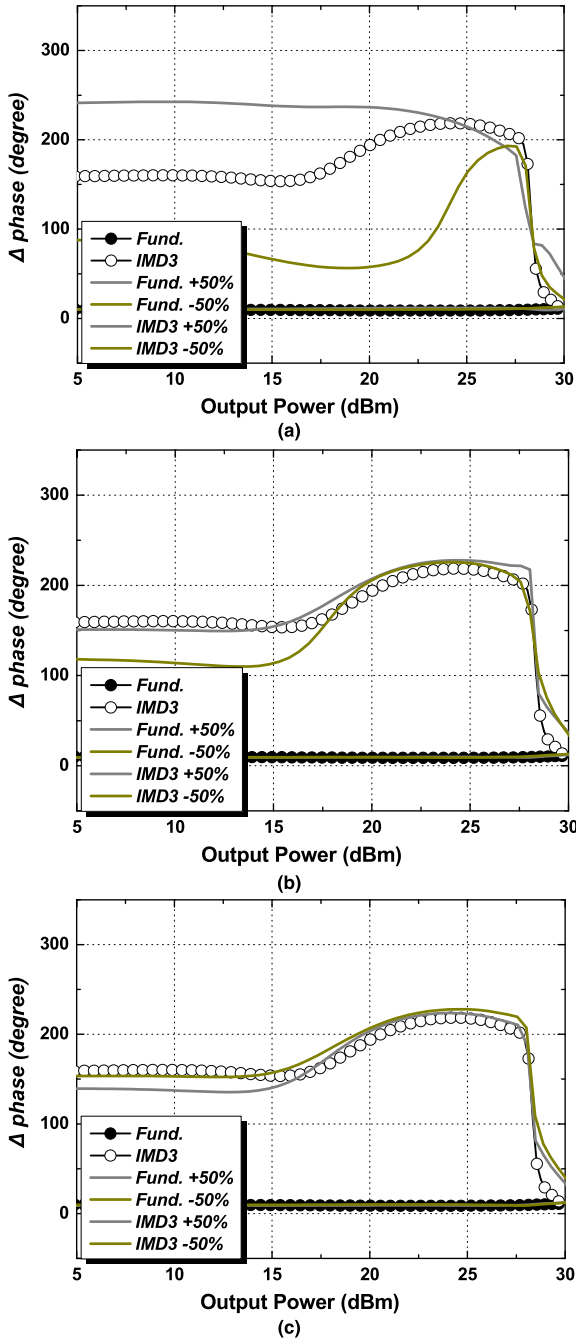
FIGURE 13. Simulated Δ phase results for variations of R_b, R_{b1}, and C_{b1}. (a) R_b of PA1, (b) R_{b1} of PA1, and (c) C_{b1} of PA1.
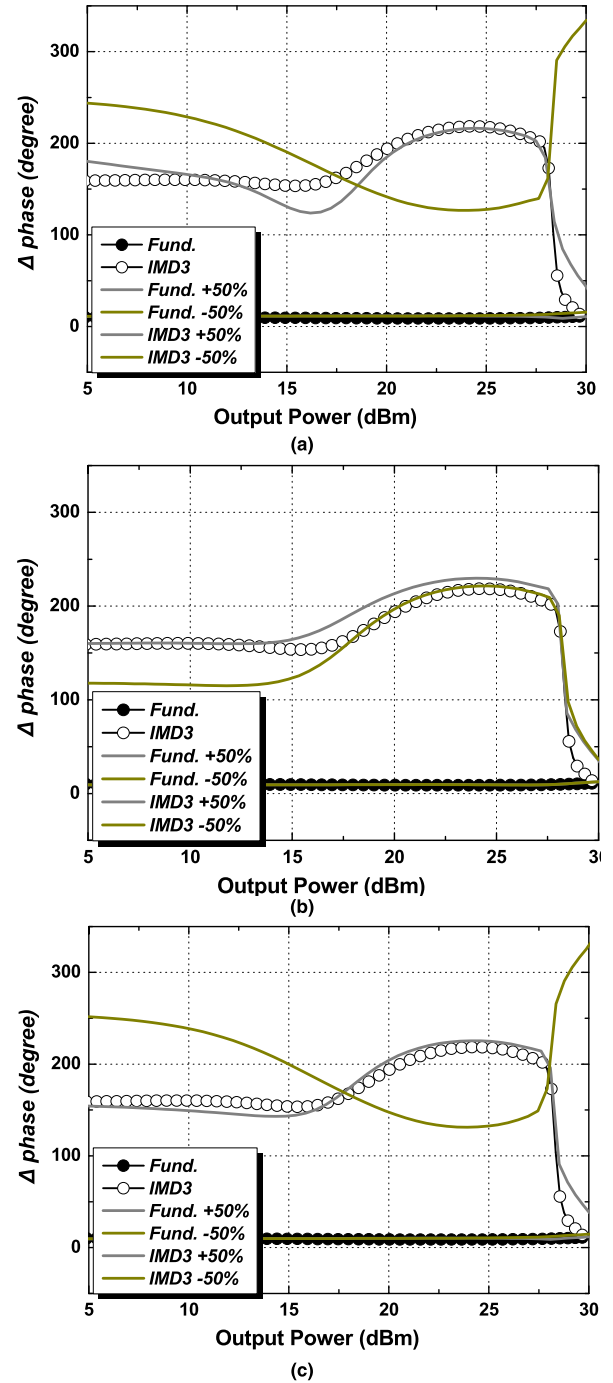

FIGURE 14. Simulated Δ phase results for variations of R_b, R_{b1}, and C_{b1}. (a) R_b of PA2, (b) R_{b1} of PA2, and (c) C_{b1} of PA2.

fundamental current increases. In contrast, if the IMD3 currents from PA1 and PA2 are 180° out-of-phase, they are cancelled each other at the output resulting in reduced IMD3 distortion. For the InGaP/GaAs HBT PA design, a two-stage configuration including a drive amplifier (DA) is used to provide sufficient gain of more than 30 dB. Fig. 11 shows the total schematic of the proposed PA with the single- and two-winding transformer for application in a femtocell base station. Multiple unit transistors are combined in the DA

and PA, and an active bias circuit including a linearization capacitor C_{bypass}, is adopted for nonlinear distortion [2], [22], [23]. The unit HBT comprises of an emitter of length 20 μm and width 2 μm. The 14-unit HBT and 20-unit HBT are used for PA1 and PA2, respectively. On-chip inductors and capacitors are used for the input and inter-stage matchings. For the configuration of the proposed single- and two-winding transformer, PA1 is connected to the primary winding of the
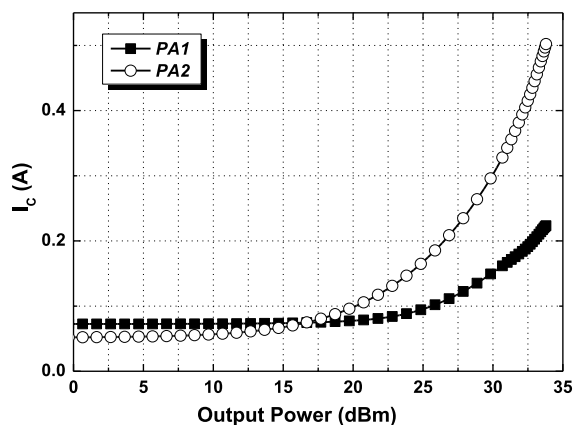
FIGURE 15. Simulated bias currents of PA1 and PA2 as a function of output power.
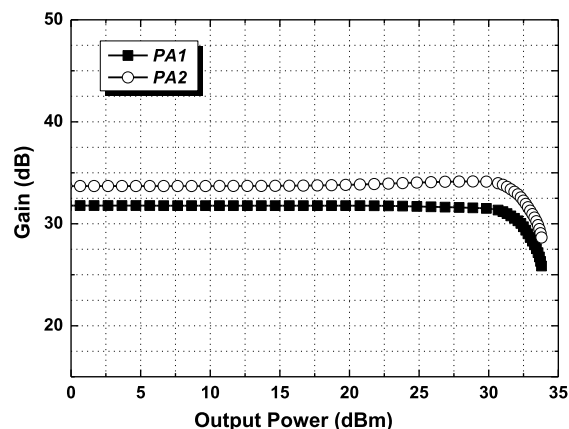

FIGURE 16. Simulated power gains of PA1 and PA2.

proposed transformer. Meanwhile, PA2 is connected to the middle of the secondary winding, which is the configuration of the single-winding transformer. The series capacitors C_S are added for the dc block of the output of PA1 and PA2. In addition, off-chip inductors and capacitors are added between PA1 and the primary winding to consider the additional tuning of output matching. To achieve IMD3 cancellation at the output, different values for R_b, R_{b1}, and C_{b1} are chosen through careful iterations of the ADS harmonic balance simulations. Fig. 12 shows the simulated results for the proposed two-stage HBT PA with IMD3 cancellation using a single- and two-winding transformer. A two-tone signal simulation was performed at a center frequency of 0.91 GHz with a tone spacing of 10 MHz. As shown in Fig. 12(a), the phases of the fundamental current components of the two input currents in the single- and two-winding transformer are almost identical. In contrast, the phase difference between the IMD3 components of the two input currents is approximately 180° until the output power reaches 28 dBm. To evaluate the linearity improvement with the proposed IMD3 cancellation method, the IMD3 results from the proposed PA are compared with the results from the PA design without IMD3 cancellation method under the same values for R_b, R_{b1}, and C_{b1}. As shown in Fig. 12(c), the total IMD3 of the PA is improved after applying the IMD3 cancellation method using a single- and two-winding transformer.

In addition, graphs of the Δ phase for different values of R_b, R_{b1}, and C_{b1} of PA1 and PA2 are compared in Figs. 13 and 14, respectively. No discernible change is visible in the phase difference of fundamental current components of the two input currents in the single- and two-winding transformer due to change in the values of R_b, R_{b1}, and C_{b1}. The phase difference between the IMD3 components of the two input currents changes with changes in the values of R_b, R_{b1}, and C_{b1}.

As shown in Fig 15, the bias conditions of PA1 and PA2 change with changes in the values of R_b, R_{b1}, and C_{b1}. The change in R_b, R_{b1}, and C_{b1} is related to the dc boosting
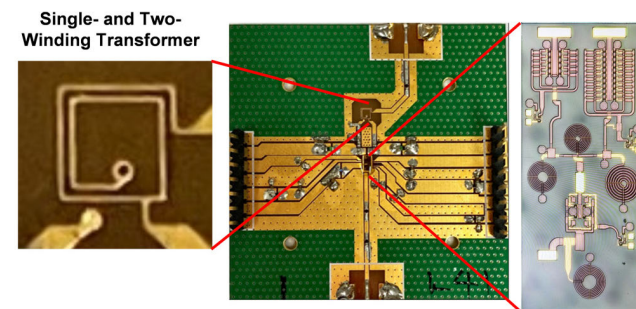

FIGURE 17. Photograph of the implemented PA.

effect. Moreover, the slope of the dc variation gets steeper for PA2 than for PA1 with an increase in the output power. As shown in Fig. 16, the gains of PA1 and PA2 are plotted. The gain difference between PA1 and PA2 is approximately 2 dB.

IV. MEASUREMENT RESULTS

The integrated PA was fabricated using Winsemi's InGaP/GaAs HBT process. The chip size, including the bond pads, is 3.24 mm². Fig. 17 shows photographs of the implemented PA including proposed transformer and off-chip elements. Measurements were performed using a supply voltage of 5 V. The measured S-parameters of the proposed PA are shown in Fig. 18. Fig. 19 depicts the measured power gain and PAE for a continuous-wave (CW) signal at 0.91 GHz. The measured saturated output power P_{SAT} is 33.3 dBm, with a PAE of 61.3%. By adopting the proposed low-loss high-Q single- and two-winding transformer, a high output power of more than 2 W is achieved with high efficiency. The measured power gain is 34.3 dB at 0.91 GHz. A two-tone signal measurement was performed at a center frequency of 0.91 GHz with a tone spacing of 10 MHz. As shown in Fig. 20, IMD3 values of less than −37 dBc have been obtained for output power up to 28 dBm. The proposed PA was also tested using an OFDM 64-quadrature amplitude modulation (QAM) signal with a bandwidth of 10 MHz and

TABLE 1. Performance comparison with linear PAs using PCB transformers.

| Reference	[26]	[27]	[28]	[29]	This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	InGaP HBT
Number of stages	1	1	1	1	2
Frequency (GHz)	1.85	1.85	1.85	0.88	0.91
Gain (dB)	15*	10*	13.0*	13.3	34.3
P_{SAT} (dBm)	N/A	30.2	N/A	31.8*	33.3
PAE_{SAT} (%)	N/A	48	N/A	56.2*	61.3
P1dB	28.2*	N/A	28.5*	30.8*	32.3
Signal	10-MHz 16-QAM (7.5 dB PAPR)	10-MHz 16-QAM (7.5 dB PAPR)	10-MHz 16-QAM (7.5 dB PAPR)	10-MHz 16-QAM (7.5 dB PAPR)	10-MHz 64-QAM (7.8 dB PAPR)
VDD/VCC	3.5	4.5	N/A	4	5
ACPR (dBc)	-31/-42	-32/-42	-31.0/-40	-33/-42	-31/-42
$P_{O, AVG}$ (dBm)	27.8/12*	26/ 13*	27.5/13.5*	27/ 8*	29.0/26.0
PAE_{AVG} (%)	41.0/5*	31.2/8*	38.5/7.5*	47.4/ 8*	38.8/26.8
PCB transformer topology	Two-winding transformer	Two-winding transformer	Two-winding transformer	Doherty transformer	Single- & two-winding transformer

*graphically estimated
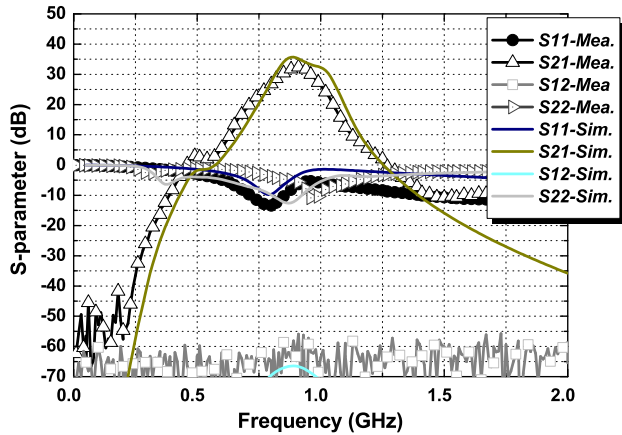
FIGURE 18. Measured small-signal performances.

FIGURE 20. Measured IMD3 results.

FIGURE 19. Measured power gain and PAE.

FIGURE 21. Measured ACLR and PAE for the 64-QAM OFDM signal with 10-MHz bandwidth.

PAPR of 7.8 dB at 0.91 GHz. Fig. 21 shows the measured ACLR and PAE with respect to the output power. The PA yields an output power of 26.0 dBm, with a PAE of 26.8% and current consumption of 297 mA, while achieving an ACLR of less than −42 dBc. Using the IMD3 cancellation method, a high linear output power with high efficiency is obtained.

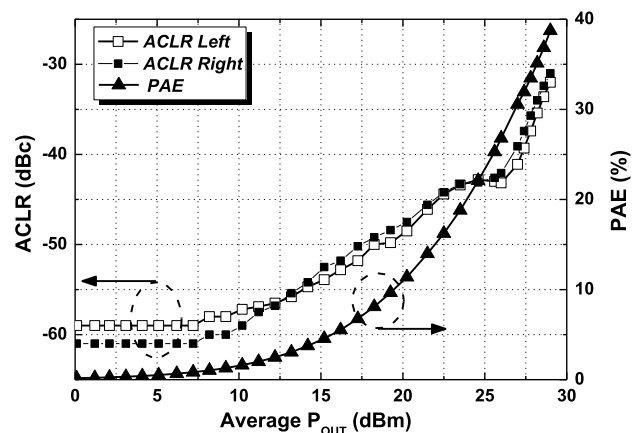**TABLE 2.** Comparison with linear femtocell PAs.

| Reference	Freq. (GHz)	Tech.	Signal	V_{CC}	P_{SAT} (dBm)	PAE_{SAT} (%)	Gain	P_{1dB}	Pout (dBm) @ -42dBc ACLR	PAE (Current) @ Pout	Output Topology
NXP MMZ09312B [30]	0.9	InGaP HBT	10-MHz LTE TM1.1	5	N/A	N/A	31.7	29.6	19.8*	14.0%* @ 19.8 dBm	Single-ended LC matching
SKY 65126-21 [1]	0.85	GaAs HBT	WCDMA 64DPCH	5	34.5*	N/A	31.8*	32.5	26.0*	(540mA) @ 25 dBm	Single-ended LC matching
[2]	0.88	InGaP HBT	10-MHz LTE (8.1dB PAPR)	5	33.5	46.1	29.2	30.5*	26.2*	20.3%* @ 26.2 dBm	Single-ended LC matching
[18]	2.3	InGaP HBT	10-MHz LTE (7.3dB PAPR)	4.7	31.0	27.6	26.0	29.1*	18.1*	4.7%* @ 18.1 dBm	On-chip Transformer
This work	0.91	InGaP HBT	10-MHz 64QAM (7.8dB PAPR)	5	33.3	61.3	34.3	32.3	26.0	26.8% (297mA) @ 26.0 dBm	PCB Single- & two-winding transformer

*graphically estimated
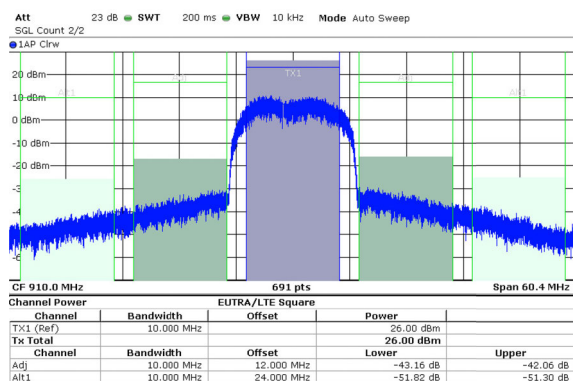
FIGURE 22. Measured ACLR for the 64-QAM OFDM signal with a bandwidth of 10 MHz at output power of 26.0 dBm.

Fig. 22 shows the measured ACLR at an output power of 26.0 dBm.

Table 1 presents a comparison of the measured results with the previously reported results of linear PAs using a PCB transformer. Among the PAs in Table 1, the proposed PA achieves the highest saturated output power, with the highest PAE. The reported performances of the linear femtocell PAs are summarized in Table 2. Compared with the reference PAs, the proposed PA achieves the highest PAE with an ACLR of less than −42 dBc.

V. CONCLUSION

A linear HBT PA is implemented using a single- and two-winding transformer. The proposed high-Q single- and two-winding transformer combines multiple unit amplifiers with low loss and compact form factors. An IMD3 cancellation technique is also proposed to cancel the nonlinear

components from the two-unit amplifiers. The measurement results prove that the proposed PA achieves the highest linear PAE of 26.8% at an average output power of 26.0 dBm with an ACLR of −42 dBc at 0.91 GHz.

REFERENCES

[1] Skyworks Solutions, Inc. *Part Number SKY65126-21*. Accessed: Aug. 5, 2020. [Online]. Available: https://www.skyworksinc.com

[2] S. Baek, H. Ahn, I. Nam, N. Ryu, H. D. Lee, B. Park, and O. Lee, "A linear InGaP/GaAs HBT power amplifier using parallel-combined transistors with IMD3 cancellation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 11, pp. 921–923, Nov. 2016.

[3] NXP Semiconductors Inc. *Part Number MMZ25332BT1*. Accessed: Aug. 5, 2020. [Online]. Available: https://www.nxp.com

[4] Skyworks Solutions, Inc. *Part Number SKY65120-21*. Accessed: Aug. 5, 2020. [Online]. Available: https://www.skyworksinc.com

[5] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371–383, Mar. 2002.

[6] E. Kaymaksut and P. Reynaert, "Dual-mode CMOS Doherty LTE power amplifier with symmetric hybrid transformer," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 1974–1987, Sep. 2015.

[7] G. Liu, P. Haldi, T.-J.-K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600–609, Mar. 2008.

[8] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu, and A. M. Niknejad, "A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1054–1063, May 2008.

[9] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, and A. M. Niknejad, "A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4 G WiMax applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393–3402, Dec. 2009.

[10] Y. Tan, H. Xu, M. A. El-tanani, S. Taylor, and H. Lakdawala, "A flip-chip-packaged 1.8 V 28 dBm class-AB power amplifier with shielded concentric transformers in 32 nm SoC CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 426–427.

[11] Y. Tan, J. Duster, C.-T. Fu, E. Alpman, A. Balankutty, C. Lee, A. Ravi, S. Pellerano, K. Chandrashekar, H. Kim, B. Carlton, S. Suzuki, M. Shafi, Y. Palaskas, and H. Lakdawala, "A 2.4 GHz WLAN transceiver with fully-integrated highly-linear 1.8 V 28.4 dBm PA, 34 dBm T/R switch, 240 MS/s DAC, 320 MS/s ADC, and DPLL in 32 nm SoC CMOS," in *Proc. Symp. IEEE VLSI Circuits Dig.*, Jun. 2012, pp. 76–77.

[12] E. Kaymaksut and P. Reynaert, "Transformer-based uneven Doherty power amplifier in 90 nm CMOS for WLAN applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659–1671, Jul. 2012.

[13] K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K. S. Yang, Y. Kim, J. J. Chang, W. Woo, C.-H. Lee, H. Kim, and J. Laskar, "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, May 2008.

[14] K. H. An, D. H. Lee, O. Lee, H. Kim, J. Han, W. Kim, C.-H. Lee, H. Kim, and J. Laskar, "A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 7, pp. 479–481, Jul. 2009.

[15] J. Kim, Y. Yoon, H. Kim, K. H. An, W. Kim, H.-W. Kim, C.-H. Lee, and K. T. Kornegay, "A linear multi-mode CMOS power amplifier with discrete resizing and concurrent power combining structure," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1034–1048, May 2011.

[16] V. A. Solomko and P. Weger, "A fully integrated 3.3–3.8-GHz power amplifier with autotransformer balun," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 9, pp. 2160–2172, Sep. 2009.

[17] H. Ahn, S. Baek, H. Ryu, I. Nam, and O. Lee, "A highly efficient WLAN CMOS PA with two-winding and single-winding combined transformer," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2016, pp. 310–313.

[18] H. Ahn, S.-E. Choi, H. Ryu, S. Baek, I. Nam, and O. Lee, "2.3-GHz HBT power amplifier with parallel-segmented on-chip autotransformer," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1140–1142, Dec. 2017.

[19] H. Ahn, S. Baek, I. Nam, D. An, J. K. Lee, M. Jeong, B.-E. Kim, J. Choi, and O. Lee, "A fully integrated dual-mode CMOS power amplifier with an autotransformer-based parallel combining transformer," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 9, pp. 833–835, Sep. 2017.

[20] P. Reynaert and M. S. J. Steyaert, "A 2.45-GHz 0.13-CMOS PA with parallel amplification," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 551–562, Mar. 2007.

[21] K. Choi, M. Kim, H. Kim, S. Jung, J. Cho, S. Yoo, Y. H. Kim, H. Yoo, and Y. Yang, "A highly linear two-stage amplifier integrated circuit using InGaP/GaAs HBT," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2038–2043, Oct. 2010.

[22] Y. S. Noh and C. S. Park, "PCS/W-CDMA dual-band MMIC power amplifier with a newly proposed linearizing bias circuit," *IEEE J. Solid-State Circuits*, vol. 2, no. 9, pp. 1096–1099, Sep. 2002.

[23] T. Yoshimasu, M. Akagi, N. Tanba, and S. Hara, "An HBT MMIC power amplifier with an integrated diode linearizer for low-voltage portable phone applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 9, pp. 1290–1296, Sep. 1998.

[24] T. Oka, M. Hasegawa, M. Hirata, Y. Amano, Y. Ishimaru, H. Kawamura, and K. Sakunoi, "A high-power low-distortion GaAs HBT power amplifier for mobile terminals used in broadband wireless applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2123–2127, Oct. 2007.

[25] K. W. Kobayasi, "High linearity dynamic feedback Darlington amplifier," in *Proc. IEEE Compound Semiconductor Integr. Circuits Symp.*, Oct. 2007, pp. 1–4.

[26] S. Jin, B. Park, K. Moon, M. Kwon, and B. Kim, "Linearization of CMOS cascode power amplifiers through adaptive bias control," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4534–4543, Dec. 2013.

[27] D. Kang, B. Park, D. Kim, J. Kim, Y. Cho, and B. Kim, "Envelope-tracking CMOS power amplifier module for LTE applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3763–3773, Oct. 2013.

[28] B. Park, J. Park, S. Jin, Y. Cho, J. Kim, and B. Kim, "CMOS power amplifier on top of embedded transformer for compact module," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 10, pp. 678–680, Oct. 2015.

[29] Y. Cho, K. Moon, B. Park, J. Kim, and B. Kim, "Voltage-combined CMOS Doherty power amplifier based on transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3612–3622, Nov. 2016.

[30] NXP Semiconductors Inc. *Part Number MMZ09312B*. Accessed: Aug. 5, 2020. [Online]. Available: https://www.nxp.com

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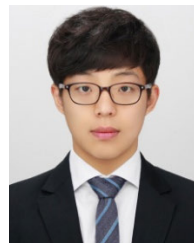
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