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Area and Power-Efficient Capacitively-Coupled Chopper Instrumentation Amplifiers in 28 nm CMOS for Multi-Channel Biosensing Applications

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ABSTRACT This paper presents two designs of a capacitively-coupled chopper instrumentation amplifier (CCIA) successfully implemented in 28 nm CMOS for biopotential sensing applications. The first design is a compact CCIA using offset-blocking for chopping ripple reduction, DC servo loop (DSL) for electrode offset (V_{EOS}) suppression, and a high pass filter (HPF) for handling common-mode (CM) artifacts. An inverter-based self-biased input stage is used for noise and power efficiency. The two gain stages of the CCIA achieve a low-frequency open-loop gain $>$ 80 dB. Realized in an area of 0.05 mm^2, the CCIA handles V_{EOS} up to 50 mV and tolerates CM artifacts up to 1.5 V_{pp}. The CCIA achieves a mid-band gain of 39.5 dB with a 1 kHz bandwidth by consuming 1 μW. The integrated input-referred noise (IRN) over 200 Hz bandwidth is 2.15 μV_{rms}. The second design presents a dual-channel CCIA (DCCIA) using an orthogonal frequency chopping for multi-sensor array applications. An inverter-based input stage is used for noise efficiency. The measured results show that the DCCIA achieves a low-frequency gain of 39.5 dB with a 3-dB bandwidth up to 1 kHz by consuming 0.71 μW per channel. The measured noise density is 136 nV/$\sqrt{}$Hz with an integrated noise of 2.67 μV_{rms} over 200 Hz bandwidth. The DCCIA suppresses V_{EOS} up to 50 mV using the DSL. Realized in a compact area of 0.04 mm^2 per channel, an excellent gain matching error of 0.29% is achieved with the crosstalk higher than 58 dB between the channels. This work is a measured report on the instrumentation amplifier using, to the best of the authors' knowledge, one of the smallest CMOS process nodes.

INDEX TERMS Chopper instrumentation amplifier, nanometer-scale CMOS, biopotential, multi-channel, electrode offset, DC servo-loop, neural signal recording.

I. INTRODUCTION

Neural and biopotential signal sensing using integrated circuits (ICs) has been an important research topic in various biomedical sensing applications [1]–[3]. Acquiring high-quality neural signals is important for rehabilitation, daily healthcare, sports activity monitoring, and brain-computer interfaces [4]–[6]. Biopotential signals, such as electroencephalogram (EEG), electrocardiogram (ECG), and electromyography (EMG), have an amplitude of tens of μV to a few mV, occupying a frequency band from 0.5 Hz to 1 kHz [7].

One of the critical requirements for the sensor frontend is low-noise performance. When a sensor array is considered for electronics implanted inside the body, subsequent design challenges include limiting the implant to a small area and low power consumption [8], [9]. Several approaches have been presented to address this issue [10]–[15]. The neural recording microsystem [13], which includes 32 recording channels, consumes 170 μW per channel to achieve an integrated noise of 12.6 μV_{rms} over a bandwidth from 300 Hz to 10 kHz. Work [14] achieves low power consumption

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of 3.77 μW per channel to achieve the input noise of 4.43 $\mu V_{\rm rms}$ over a bandwidth of 1 Hz to 12 kHz; however, it occupies a relatively large area of 0.35 mm^2 per channel. We note that the works [13], [14] do not use the chopping technique. Work [15], which uses the chopper, achieves a high area efficiency of 0.03 mm^2 per channel; however, the power consumption is relatively high with 40.5 μW per channel.

To address the area and power issues of previous works, we take advantage of CMOS process scaling and present two designs of the capacitively-coupled chopper instrumentation amplifier (CCIA), which are successfully fabricated in a 28 nm CMOS process. The first design of the CCIA uses a compact design approach for a DC-servo loop (DSL), chopping ripple reduction, and common-mode (CM) rejection. Ripple is suppressed using an offset-blocking capacitor. Using the DSL and a high pass filter (HPF), the CCIA can handle an electrode offset $V_{\rm EOS}$ up to 50 mV and common-mode (CM) artifacts up to 1.5 $V_{\rm pp}$. The CCIA realized in a compact area of 0.05 mm^2 achieves a mid-band gain of 39.5 dB with a 1 kHz bandwidth by consuming 1 μW. The input-referred noise (IRN) of 2.15 $\mu V_{\rm rms}$ over 200 kHz bandwidth is achieved. The second design realizes a dual-channel CCIA (DCCIA) for multi-sensor array applications. The DCCIA uses a shared inverter-based amplifier for the two channels, and an orthogonal chopping frequency is used to perform independent signal amplification for each channel. The DCCIA can block $V_{\rm EOS}$ up to 50 mV using the DSL. The DCCIA achieves a mid-band gain of 39.5 dB by consuming 0.71 μW per channel. An excellent gain mismatch of 0.29% and crosstalk of –58.3 dB between the channels is measured. The DCCIA achieves a high area efficiency of 0.04 mm^2 per channel, demonstrating improved area and power efficiency than previous works.

II. NANOMETER CMOS DESIGN ISSUES

The CMOS process's channel length has continued shrinking to increase speed and reduce power consumption. However, the nanometer-scale transistor suffers from various short-channel effects that impose many challenges for analog circuit design. Firstly, the channel length modulation becomes more critical in the small process node and increases the difficulty of implementing current bias schemes for the amplifier. The output impedance is also reduced by drain-induced barrier lowering (DIBL) [16], limiting the opamp gain. The amplifier design uses an increased channel length to counteract these effects.

Secondly, the nanometer CMOS process suffers from substantial process variability and mismatch effect. The variability is a discrepancy in characteristics between dies on the same silicon wafer, wafer-to-wafer, and lot-to-lot, whereas the random mismatch is local variation between transistors on the same die [17]. Besides, a systematic mismatch is introduced by layout-dependent effects (LDE) [18]. The typical LDE includes diffusion (OD) spacing effect (OSE), poly spacing effect (PSE), the well proximity effect (WPE), and the shallow trench isolation effect (STI). Extensive Monte Carlo simulations with global and local corners are required for the layout parasitic extracted (LPE) netlist to guarantee the worst-case expected performance.

Thirdly, the effect of the gate leakage current becomes exacerbated with a thinner oxide layer [19]. This unexpected current affects not only the power budget but also the noise performance. The gate leakage current causes an increase in the shot noise that is not usually considered in long-channel devices. The gate leakage affects the current gain ($i_{\rm D}/i_{\rm GS}$) and the mismatch of drain current $(\sigma_{\rm id}/i_{\rm D})^2$ [20]. The current gain decreases with process scaling via the increased tunnel conductance with gate leakage. The relative mismatch in the drain current becomes more severe due to the additional gate leakage.

Fourthly, the integrated circuit's reliability during the manufacturing process is a key concern, requiring a restricted design rule (RDR). The number of design rules continues to grow significantly, with about 2000 design rule check (DRC) counts for 28 nm node [21]. The designer spends much effort during the layout phase to meet the design rules related to the antenna, the latch-up, and the electrostatic discharge (ESD) protection. Layout techniques such as dummy poly insertion, shielding, blockage and guard ring are needed to maintain the performance under unexpected phenomena.

III. CAPACITIVELY-COUPLED CHOPPER INSTRUMENTATION AMPLIFIER

A. AMPLIFIER DESIGN

Fig.1 shows a schematic of the CCIA. The input stage $G_{\rm m1}$ is realized using an inverter-based input pair for noise efficiency. The second transconductor $G_{\rm m2}$ is realized using a common source (CS) amplifier to increase the output swing. The CM voltage $V_{\rm CM} = V_{\rm DD}/2$ is used to bias $G_{\rm m1}$ and $G_{\rm m2}$ using pseudo resistors $R_{\rm HP1,2}$ and $R_{\rm b1,2}$. The $G_{\rm m1}$ and $G_{\rm m2}$ consume 800 nA and 180 nA, respectively, to achieve a low-frequency open-loop gain of $A_{\rm V} > 80$ dB at $V_{\rm DD} = 1$ V. Two-stage opamp $G_{\rm m3}$ is used for the integrator in the DSL [22].

The input $V_{\rm in}$ is up-modulated to chopping frequency $f_{\rm CH} = 10$ kHz by the input chopper $\rm CH_{in}$ and down modulated to baseband by the output chopper $\rm CH_{out}$. The mid-band gain of 40 dB of the CCIA is defined by the ratio of the input $C_{\rm in1,2} = 4$ pF and feedback capacitor $C_{\rm fb1,2} = 40$ fF. The size of $C_{\rm fb1,2}$ is increased by 8$\times$ of the minimum to improve matching. The Miller capacitor $C_{\rm m1,2} = 3$ pF is used for stability. Considering $G_{\rm m1}$ bias current variation with the process corners, $C_{\rm m1,2}$ is sized larger than necessary. These capacitors are realized using a vertical natural capacitor (VNCAP) with a metal stack from metal-2 to metal-6, achieving area efficiency.

Significant CM artifacts can appear at the recording site in closed-loop neural recording systems [23]. The amplitude of these artifacts is in the hundreds of millivolts, which is relatively large, potentially leading to the amplifier saturation and a decrease of the dynamic range. Because the CM

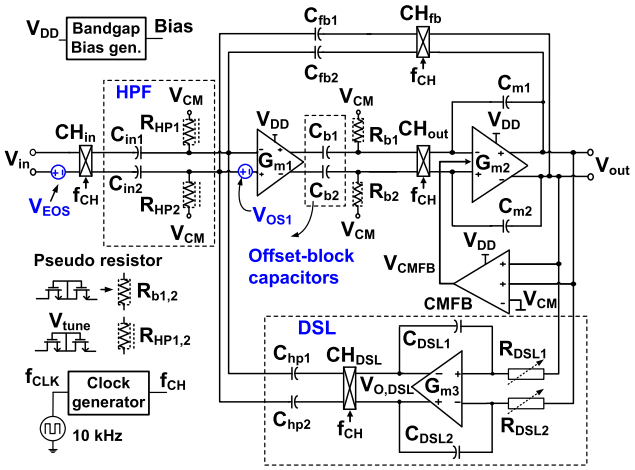

FIGURE 1. Schematic of the proposed CCIA.

artifacts pass through the chopper un-modulated, they still exist in the baseband at the output of CH_{in}. The $C_{in1,2}$ and $R_{HP1,2}$ forming an HPF with the cut-off frequency $f_{HPF} = 1/(2\pi R_{HP1,2}C_{in1,2})$ suppresses the CM artifacts at the virtual ground node. This idea of rejecting the CM artifacts is based on the biasing resistor commonly used for G_{m1} [24]; however, the value of $R_{HP1,2}$ is chosen to realize f_{HPF} attenuating the CM artifacts < 100 Hz. Besides, the value of $R_{HP1,2}$ is variable using the tuning voltage V_{tune}. Because $R_{HP1,2}$ is also used to bias G_{m1}, V_{tune} is set to ground when disabling the HPF.

Similar to the input, V_{EOS} is up-modulated to the f_{CH} band, and it is partially suppressed by $C_{fb1,2}$ at the virtual ground. The residual offset can be expressed as $V_{EOS,\omega} \cong V_{EOS}C_{in1,2}/(A_V C_{fb1,2})$ [22]. Then, G_{m1} converts $V_{EOS,\omega}$ into a current. The down-converted signal via CH_{out} is integrated to generate the output offset $V_{out,OS}$. The $V_{out,OS}$ is averaged and amplified by the integrator of DSL. The output $V_{O,DSL}$ of the DSL is up-modulated by CH_{DSL}, which is subsequently converted to a current by $C_{hp1,2}$, thus, canceling out the up-modulated offset current generated by the V_{EOS} [22]. The V_{EOS} depends on both the material and size of the electrodes, and it can be up to 50 mV [24]. Using the relation $C_{hp1,2} = V_{EOS}(C_{in1,2}/V_{DSL,max})$, we choose $C_{hp1,2} = 200$ fF to handle V_{EOS} up to 50 mV, where $V_{DSL,max} = 1$ V is the rail to rail of the DSL. When DSL is enabled, the high pass corner $f_{hp} = f_{ugb}(C_{hp1,2}/C_{fb1,2})$ is created, where $f_{ugb} = 1/(2\pi R_{DSL1,2}C_{DSL1,2})$ is the unity gain frequency of the integrator and $C_{DSL1,2} = 5$ pF is the capacitor in the integrator. The $R_{DSL1,2}$ is realized using a charge-sharing resistor (CSR).

The offset voltage V_{OS1} is converted to current and up-modulated by G_{m1} and CH_{out}, respectively, and integrated by $C_{m1,2}$ to generate the output ripple. Like the previous work [23], the offset-blocking capacitor $C_{b1,2} = 4$ pF is used at the output of the G_{m1} to mitigate the output ripple. With the high DC gain (~50 dB), V_{OS1} can saturate the output; however, the amplified offset appears as a DC current at the output of G_{m1}; therefore, output voltage saturation is not an issue.

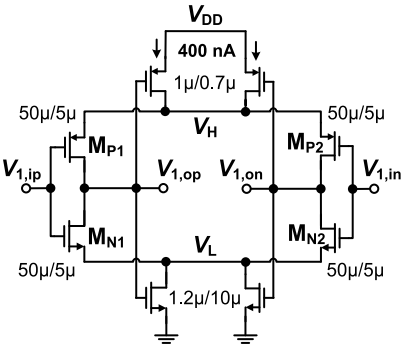

FIGURE 2. Schematic of the inverter-based self-biased input stage.

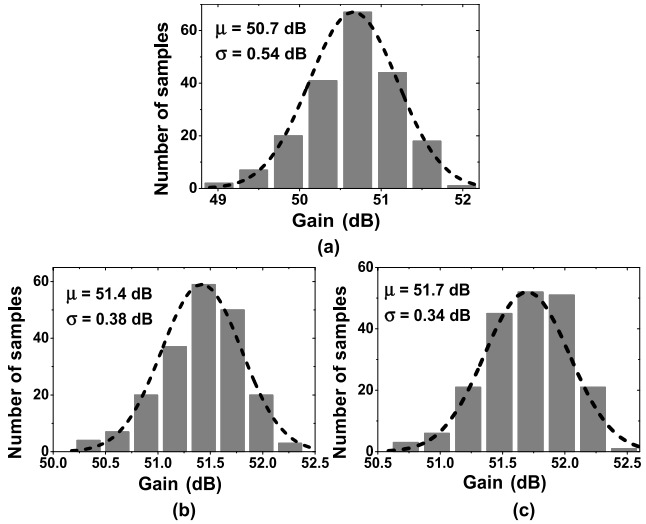

FIGURE 3. Statistical distribution of the gain of G_{m1} using (a) $V_{DD} = 0.9$ V, (b) $V_{DD} = 1$ V, (c) $V_{DD} = 1.1$ V.

B. CIRCUIT IMPLEMENTATION

Fig. 2 shows the schematic of the inverter-based input pair for G_{m1} biased at weak inversion. The current reuse improves noise efficiency via doubled transconductance. The differential outputs, $V_{1,op}$ and $V_{1,on}$, generate two equal magnitudes opposite change at V_H and V_L through $M_{P1,2}$ and $M_{N1,2}$. The output feedback operation achieves self-bias operation, stabilizing under the influence of the gate leakage.

Using the half-circuit, the low-frequency gain A_{V1} of G_{m1} can be expressed as:

$$A_{V1} \cong -\frac{2}{\lambda_{P1,2} + \lambda_{N1,2}} \tag{1}$$

where $\lambda_{P1,2} = 1/(g_{mP1,2}r_{oP1,2})$ and $\lambda_{N1,2} = 1/(g_{mN1,2}r_{oN1,2})$ are the DIBL parameter of $M_{P1,2}$ and $M_{N1,2}$, respectively [16]. The $g_{mP1,2}$ and $g_{mN1,2}$ are the transconductance of input transistors $M_{P1,2}$ and $M_{N1,2}$, respectively. The gain is increased by two, taking advantage of the current reuse. When each inverter is biased at 400 nA from a $V_{DD} = 1$ V, the parameters are $g_{mP1,2} = 10.4\ \mu$S, $g_{mN1,2} = 11.2\ \mu$S, $r_{oP1,2} = 52.1$ MΩ, and $r_{oN1,2} = 28.3$ MΩ. Using (1), we obtain $A_{V1} = 51.9$ dB.

Fig. 3 shows the statistical distribution of A_{V1} obtained using 200 Monte Carlo simulations. The result includes the

TABLE 1. Gain and bias current of G_{m1} depending on process corners.

Process corner	SS	SF	TT	FS	FF
Gain (dB)	49.9	50.9	51.4	51.6	51.9
Bias current (nA)	386	392	400	406	413

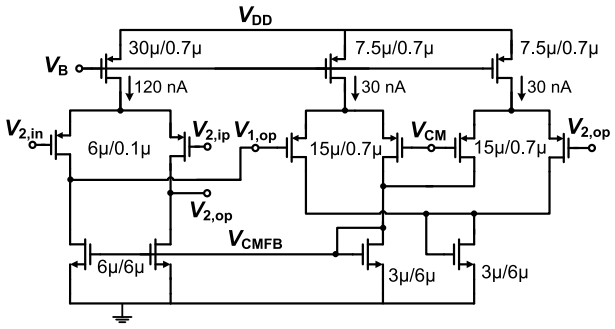

FIGURE 4. Schematic of the differential pair with CMFB circuit.

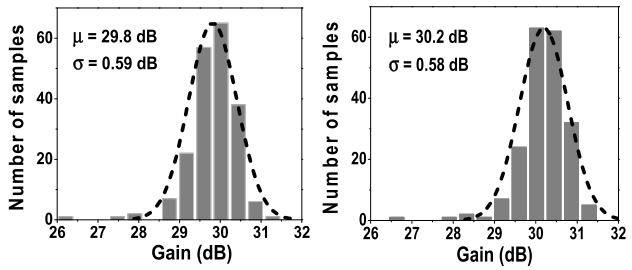

FIGURE 5. Statistical distribution of the low-frequency gain of G_{m2} at V_{DD} = 0.9 and 1.1 V.

local and global mismatches depending on process corners. The average gain is 51.4 dB, which agrees with the calculated result. When V_{DD} changes by 10%, the average gain varies from 50.7 to 51.7 dB. The results show that the self-bias operation provides a relatively constant gain under V_{DD} variations. The bias stability is achieved by the long-channel transistor (1.2 μm/10 μm) used in the tail current; however, G_{m1} lacks the mechanism to control its bias current under process variation. Because G_{m1} can be particularly sensitive to cross-corner, we investigate the gain and bias current variations. Table 1 shows that the change of gain across the corner is relatively small; gain depends mainly on the DIBL parameters.

Fig. 4 shows the schematic of G_{m2}. The input differential pair is biased at 120 nA. We consider a relatively high shift (~100 mV) in the threshold voltage V_{TH} under process, voltage, and temperature (PVT) variations. Active common-mode feedback (CMFB) is used to track the variation, which is realized using two differential pairs. The mean value of A_{V2} > 30 dB is achieved at V_{DD} = 1 V. Fig. 5 shows the statistical distribution of the low-frequency gain A_{V2} of G_{m2} when V_{DD} changes 10% from the 1 V. The mean value of A_{V2} varies from 29.8 dB to 30.2 dB, indicating a relatively small variation with V_{DD}.

Fig. 6 shows a schematic of the two-stage opamp G_{m3} for the integrator in the DSL. Because the DSL can

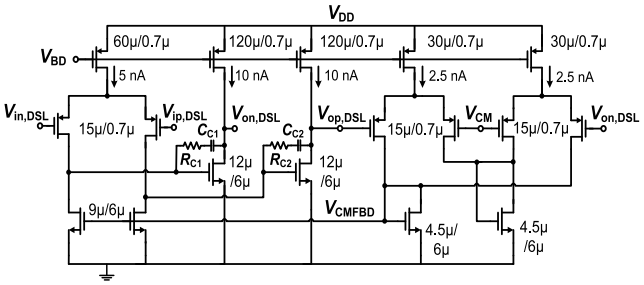

FIGURE 6. Schematic of a two-stage amplifier for the integrator. $C_{C1,2}$ = 2.5 pF, $R_{C1,2}$ = 1 MΩ.

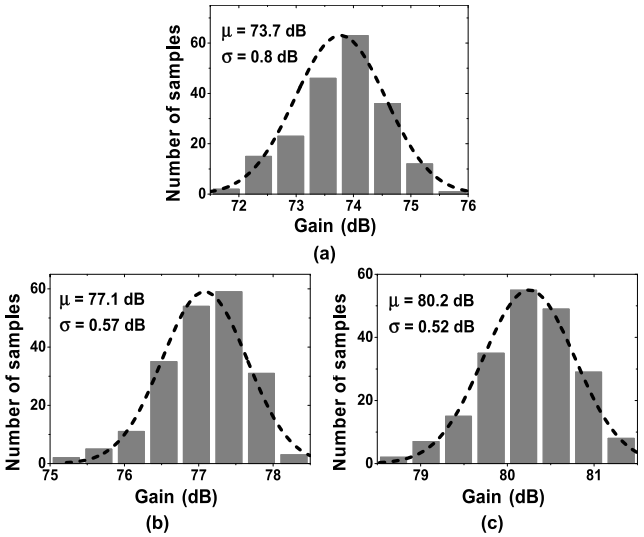

FIGURE 7. Statistical distribution of the low-frequency gain of two-stage opamp. (a) V_{DD} = 0.9 V, (b) V_{DD} = 1 V, (c) V_{DD} = 1.1 V.

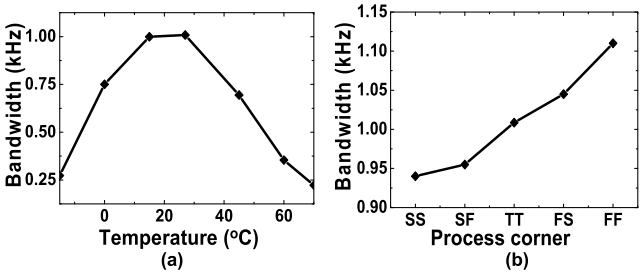

FIGURE 8. Bandwidth of the CCIA depending on (a) temperature, (b) process corner.

contribute significant noise [24], [25], we limit the bandwidth (~200 Hz) of the opamp by reducing the bias current; the input differential pair is biased at 5 nA. The common-source (CS) stage is biased at 20 nA to increase gain and output swing. Including CMFB, the opamp uses 30 nA. Fig. 7 shows that the opamp still provides a low-frequency gain > 70 dB when V_{DD} is reduced by 10% from V_{DD} = 1 V. The CCIA bandwidth depending on temperature and process corner is investigated using circuit simulations (Fig. 8). The CCIA achieves a 1 kHz bandwidth over normal body temperature. The bandwidth is larger than 700 Hz over the temperature from 0 °C to 40 °C. The bandwidth changes from 0.94 kHz to 1.11 kHz across the process corners.

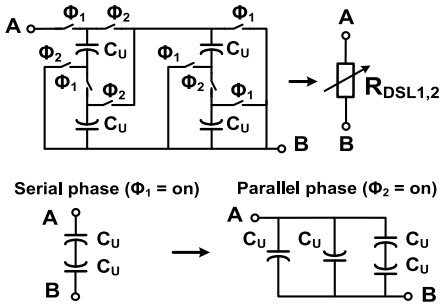

FIGURE 9. Schematic of the charge sharing resistor.

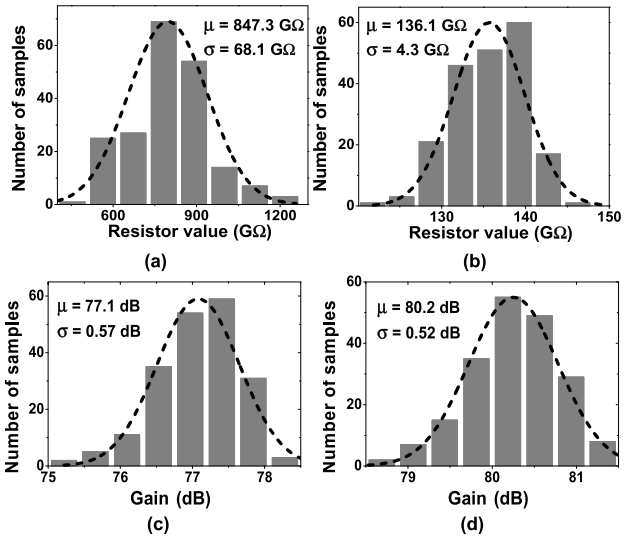

FIGURE 10. Statistical distribution of the $R_{DSL1,2}$ for different f_{CSR} of (a) 1.25 kHz, (b) 2. 5 kHz, (c) 5 kHz, (d) 10 kHz.

The $R_{DSL1,2}$ in the DSL is realized using a charge sharing resistor (CSR). Fig. 9 shows the schematic of CSR, where switches are controlled by complementary clocks $\Phi_{1,2}$ operating at f_{CSR}. By the serial-to-parallel charge sharing in the unit capacitor, $C_U = 40$ fF, the transferred charge in a clock cycle is reduced by a factor of ten, resulting in $R_{DSL1,2} \cong 10/(f_{CSR}C_U)$ [26]. Fig. 10 shows the statistical distribution of the $R_{DSL1,2}$ obtained using 200 Monte Carlo simulations. The mean value of $R_{DSL1,2}$ is tunable from 15.5 GΩ to 847 GΩ by varying f_{CSR} from 1.25 to 10 kHz. The f_{hp} is tunable from 0.2 Hz to 10.3 Hz. Fig. 11 shows the schematic of the clock generator. The D-F/F is used for a clock divider with an input clock $f_{CLK} = 10$ kHz, and f_{CSR} is selected by the 4-to-1 multiplexer using S[1:0].

C. NOISE ANALYSIS

The IRN of the CCIA, $\overline{V_{n,in}^2}$ can be expressed as

$$\overline{V_{n,in}^2} = \left(\frac{C_{tot}}{C_{in1,2}}\right)^2 \overline{V_{n,in,Gm1}^2} + 2\overline{I_{n,RHP}^2}Z_{Cin1,2}^2 + 12\overline{I_{n,shot}^2}Z_{Cin1,2}^2 + 2\overline{V_{n,out,DSL}^2}\left(\frac{C_{hp1,2}}{C_{in1,2}}\right)^2$$

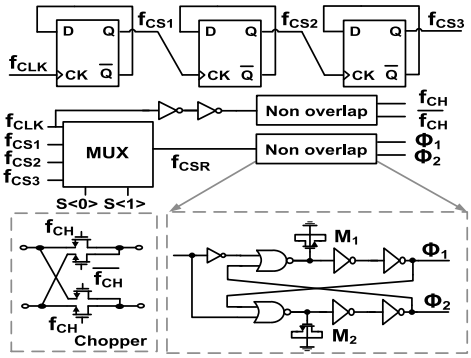

FIGURE 11. Schematic of the clock generator.

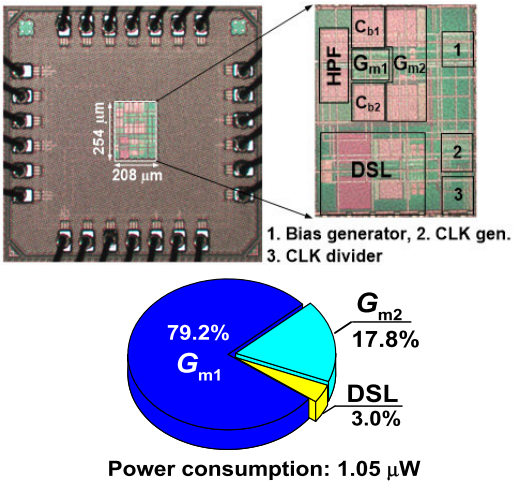

FIGURE 12. Microphotograph of the CCIA. The power breakdown of the CCIA is also shown.

$$+ 12\alpha q I_G \left(\frac{1}{\omega_{CH}C_{in1,2}}\right)^2 + 2\overline{V_{n,out,DSL}^2}\left(\frac{C_{hp1,2}}{C_{in1,2}}\right)^2 \quad (2)$$

where $C_{tot} = C_{in1,2} + C_{fb1,2} + C_{hp1,2} + C_P$ and C_P is parasitic capacitor at the virtual ground node. The $\overline{V_{n,in,Gm1}^2}$ is the input-referred noise of G_{m1}, and $\gamma = 4$ is the sub-threshold slope factor. The $\overline{I_{n,RHP}^2}$ is the noise current from the resistor $R_{HP1,2}$. Scaling down the oxide thickness ($t_{ox} < 20$ nm) increases the shot noise associated with the gate tunneling current [27]. $\overline{I_{n,shot}}^2 = \alpha q I_G \Delta f$ is the shot noise current density of the twelve switches in the choppers, where q is the elementary charge, $I_G \cong 0.25$ pA is the gate current, Δf is a 1 Hz bandwidth, and α is the constant between 0.5 and 1.5. The $Z_{Cin1,2}$ is the capacitive reactance of $C_{in1,2}$ at $\omega_{CH} = 2\pi f_{CH}$. The $\overline{V_{n,out,DSL}^2}$ is the output-referred noise of the DSL as:

$$\overline{V_{n,out,DSL}^2} = \left(\frac{f_{ugb}}{f_{CH}}\right)^2 \left(\overline{V_{n,in,Gm3}}^2 + \overline{V_{n,th}}^2 + \overline{V_{n,shot}}^2\right) = \left(\frac{f_{ugb}}{f_{CH}}\right)^2 \left(\overline{V_{n,in,Gm3}}^2 + \frac{4kT\gamma}{g_{m,SW}} + \alpha q I_G R_{on}^2\right) \quad (3)$$

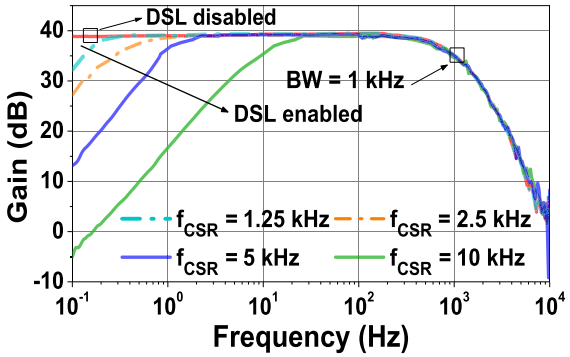

FIGURE 13. Measured frequency response of the CCIA.

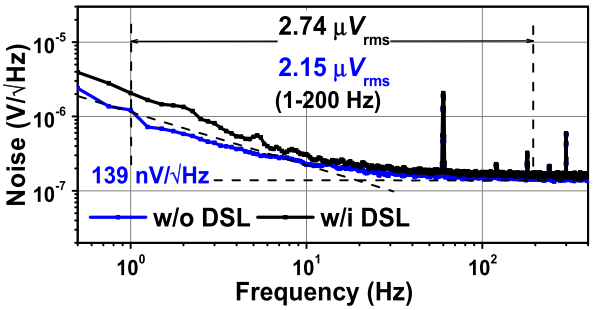

FIGURE 14. Measured input-referred noise of the CCIA.

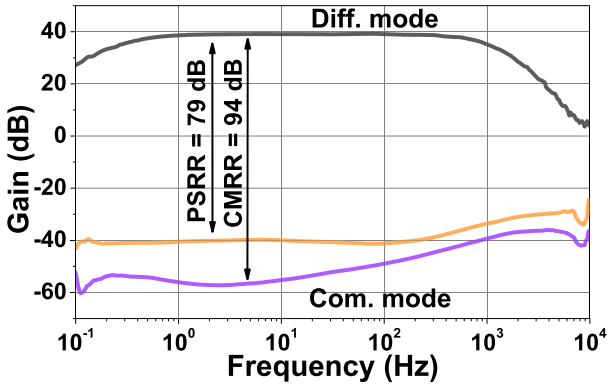

FIGURE 15. Measured CMRR and PSRR of the CCIA.

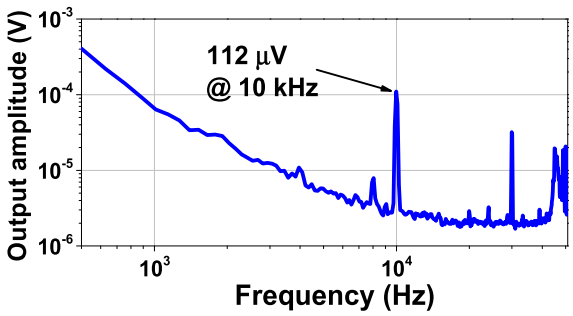

FIGURE 16. Measured output ripple of the CCIA.

where $\overline{V^2_{n,in,Gm3}}$ is the input-referred noise of G_{m3}. Because $R_{DSL1,2}$ is realized using the switched capacitors, the noise current consists of the thermal and the shot noise current density as $4kT\gamma g_{m,SW} + \alpha q I_G$, where $g_{m,SW}$ is the transconductance of the transistor in the CSR. Then, the corresponding noise voltages can be expressed as $4kT\gamma/g_{m,SW} + \alpha q I_G R^2_{on}$, where R_{on} is the channel resistance of the transistors in the CSR [28]. The simulation shows that $\overline{V^2_{n,out,DSL}}$ is 1.5×10^{-15} V^2/Hz. Using $g_{mP1,2} = 10.4$ μS, $g_{mN1,2} = 11.2$ μS, $R_{HP1,2} = 500$ MΩ, we obtain $\overline{V^2_{n,in}} = 125$ nV/$\sqrt{\text{Hz}}$ without the DSL. Including the DSL, the calculated $\overline{V^2_{n,in}}$ increases to 139 nV/$\sqrt{\text{Hz}}$.

D. MEASURED RESULT

Fig. 12 shows the microphotograph of the CCIA with a core area of 0.05 mm^2. The ESD protection part of the I/O pad is realizing using 1.8 V transistors. The power breakdown of the CCIA core shows that G_{m1}, G_{m2}, and DSL consumes 79.2%, 17.8%, and 3.0%, respectively.

Fig. 13 shows the frequency response of the CCIA measured using a 35670A dynamic signal analyzer. The high pass corner is successfully created, variable from 0.1 to 10.5 Hz using f_{CSR}. When the DSL is disabled, the high pass corner disappears as expected. The mid-band gain is 39.5 dB, affected by the parasitics. The result is similar to the gain realized using the metal-insulator-metal (MIM) capacitor in the 180 nm CMOS process [22], indicating the VNCAP has a relatively good matching in the 28 nm process. Fig. 14 shows the measured IRN of the CCIA. The noise spectra density is 139 nV/$\sqrt{\text{Hz}}$, and integrated rms noise over the 200 Hz bandwidth is 2.15 μV_{rms} when DSL is disabled. When DSL is enabled, the noise density increases to 160 nV/$\sqrt{\text{Hz}}$. The integrated noise is 2.74 μV_{rms}, which agrees with the simulated value of 2.45 μV_{rms}. Fig. 15 shows that the CMRR of 94 dB and PSRR of 79 dB is achieved at a low frequency. Fig. 16 shows the measured output ripple of 112 μV at 10 kHz. The result indicates the effectiveness of the offset-blocking technique for suppressing the chopping ripple.

The input CM range of G_{m1} is limited due to the inverter-based implementation and a relatively low V_{DD}; a small CM swing at the input of G_{m1} can easily cause distortion. Work [23] presents the method to characterize the CM tolerance; a small differential signal with a large CM interferer is used. Under this condition, the distortion at the output is observed with and without the CM filtering technique. As an alternative method, the distortion can be characterized by observing the harmonic amplitudes. Fig. 17 shows the output spectrum when a CM signal of 1.5 V_{pp} at 90 Hz is applied to the CCIA's input. The first and the second harmonic attenuation is 35.1 dB and 33.1 dB, respectively.

Fig. 18 shows the linearity characteristic of the CCIA for the 1.5 mV_{pp} differential input at 100 Hz. Considering the third harmonic as the dominant nonlinearity, the total harmonic distortion of CCIA is -52.6 dB. Fig. 19 shows the output of the CCIA for prerecorded human ECG.

Table 2 shows the performance comparison. The noise efficiency factor (NEF) captures the tradeoff between the noise,

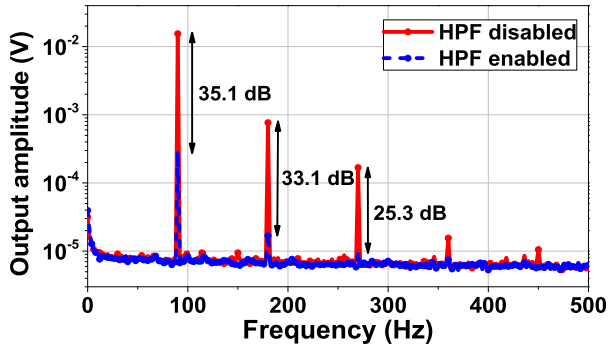

FIGURE 17. Measured output spectrum for an input CM interferer.

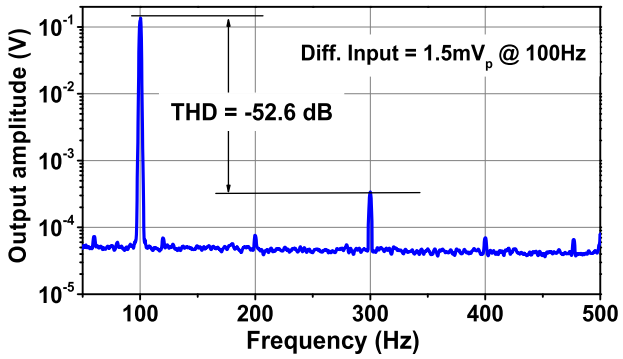

FIGURE 18. Measured linearity characteristic of the CCIA.

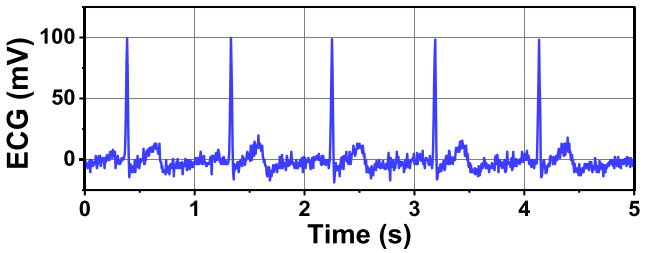

FIGURE 19. Output of the CCIA for the p rerecorded human ECG input.

current consumption, and bandwidth. The power efficiency factor (PEF) captures the tradeoff between the noise and power as:

$$\text{PEF} = V_{\text{ni, rms}}^2 \frac{2P_{\text{DC}}}{\pi V_{\text{TH}} 4kT \cdot BW} = \text{NEF}^2 \cdot V_{\text{DD}} \qquad (4)$$

where $V_{\text{ni,rms}}$ is the input-referred rms noise voltage, P_{DC} is the power consumption, and BW is the bandwidth. Work [23] achieves a noise density of 80 nV/$\sqrt{}$Hz by consuming 2.8 μW. That work handles CM artifacts of up to 0.65 V_{pp}, whereas ours handles artifacts of up to 1.5 V_{pp}. Work [24] shows a relatively high ripple of 0.3 mV and the integrated noise of 6.7 μV_{rms} when the DSL is enabled, resulting in NEF = 37.4. Work [29] achieves a low ripple of 0.01 mV using an offset-blocking capacitor similar to ours. The noise density of 100 nV/$\sqrt{}$Hz is achieved by consuming 2× more power than ours. Work [30] achieves a low noise density of 43 nV/$\sqrt{}$Hz by consuming 3.9× more power than ours without DSL. The output ripple of that work is suppressed only to 1.7 mV, whereas ours is suppressed to 112 μV. Work [31] achieves noise density similar to ours by consuming 3.8× more power than ours. Besides, the work in [31] can handle CM artifacts of only 0.4 V_{pp}. Our work is fabricated in a 28 nm CMOS process; both area (0.05 mm^2) and power consumption (1 μW) are the smallest. CM artifacts of up to 1.5 V_{pp} can be handled by our work, which is the highest among other mentioned works.

TABLE 2. Performance comparison.

	[23]	[24]	[29]	[30]	[31]	This work
Process (nm)	40	65	40	130	40	28
Area (mm^2)	0.07	0.2	0.07	0.28	N/A	0.05
Power (μW)	2.8	2.1	2	3.9	3.8	1.0
Supply (V)	1.2	1	1.2	1.2	0.6	1
Max. V_{EOS} (mV)	120	50	120	0	300	50
DSL	Y	Y	Y	N	Y	Y
Gain (dB)	25.7	40	26	40	30	39.5
BW (kHz)	5	0.5	5	N/A	0.15	1
Ripple (mV)	N/A	0.3	0.01	1.7	N/A	0.11
CM tolerance (V_{pp})	0.65	N/A	N/A	N/A	0.4	1.5
CMRR (dB)	78	134	N/A	N/A	87	94
PSRR (dB)	76	120	N/A	N/A	N/A	79
Noise density (nV/$\sqrt{}$Hz)	80	60	100	43	145*/ 240	139*/ 160
NEF	7.4	3.3*/ 37.4	7.0	3.8*	N/A	5.8*/ 7.5
PEF	65.7	10.9*/ 1399	58.8	17.3*	N/A	33.6*/ 56.3

* Without DSL.

IV. DUAL-CHANNEL CHOPPER AMPLIFIER USING ORTHOGONAL FREQUENCY CHOPPING

A. AMPLIFIER DESIGN

Fig. 20 shows a schematic of the DCCIA using the orthogonal frequency chopping technique. The DCCIA reuses the building blocks of the CCIA modified for low power suitable for multi-channel realization. The DCCIA uses a shared inverter-based input pair G_{m11} for noise efficiency. The input bias for G_{m11} is set to $V_{\text{CM}} = V_{\text{DD}}/2$ using $R_{1,2}$ realized using a pseudo resistor. The output stage G_{m21} (channel-1) and G_{m22} (channel-2) use a CS amplifier to increase the output swing.

The DCCIA provides an open-loop gain of 86 dB by consuming 1.23 μA from V_{DD} = 1 V. The two channels are symmetric, and each channel includes a negative feedback loop and a DSL. In channel-1, the mid-band gain is defined by the input capacitors $C_{\text{in11,12}} = 4$ pF and feedback capacitors $C_{\text{fb11,12}} = 40$ fF. The DSL consists of an integrator, capacitors $C_{\text{DSL11,12}} = 5$ pF, pseudo resistors $R_{\text{DSL11,12}}$,

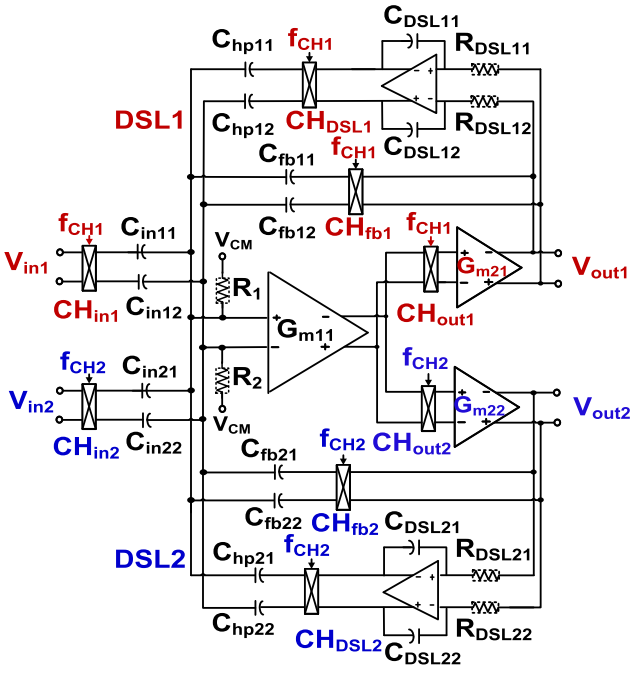

FIGURE 20. Schematic of the DCCIA using orthogonal frequency chopping technique.

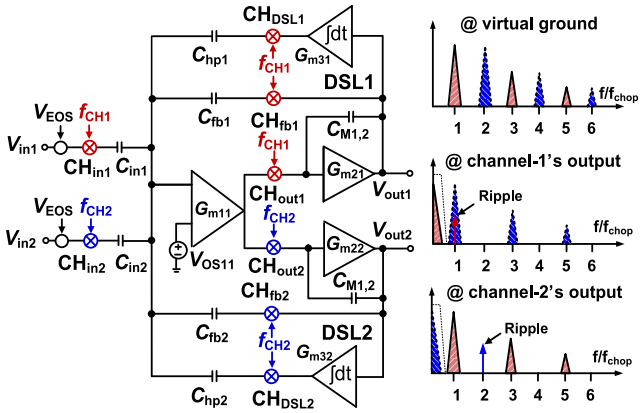

FIGURE 21. Simplified model of the proposed DCCIA.

and a two-stage opamp, a chopper $\mathrm{CH}_{\mathrm{DSL1}}$, and capacitors $C_{\mathrm{hp1,12}} = 0.2$ pF. The DSL can suppress V_{EOS} up to 50 mV.

Two orthogonal chopping frequencies, f_{CH1} and f_{CH2}, are used for channel-1 and channel-2, respectively. For the two-channel design considered in this work, we use $f_{\mathrm{CH1}} = f_{\mathrm{chop}}$ and $f_{\mathrm{CH2}} = 2f_{\mathrm{chop}}$, where f_{chop} is the lowest chopping frequency. The number of channels can be further increased for multi-sensor arrays using multiple of f_{chop}. Fig. 21 shows the simplified model of the DCCIA with the associated spectrums. The V_{in1} and V_{in2} are up-modulated to f_{chop} and $2f_{\mathrm{chop}}$ by $\mathrm{CH}_{\mathrm{in1}}$ and $\mathrm{CH}_{\mathrm{in2}}$, respectively. The closed-loop gain suppresses the signal at the virtual ground. The residual signal at the input of G_{m11} includes the odd harmonics of f_{chop} ($V_{\mathrm{in1},\omega}$, $V_{\mathrm{in1},3\omega}$, and $V_{\mathrm{in1},5\omega}$, ...) and $2f_{\mathrm{chop}}$ ($V_{\mathrm{in2},2\omega}$, $V_{\mathrm{in2},4\omega}$, and $V_{\mathrm{in2},6\omega}$, ...). These signals are converted to current by G_{m11}, and they are down-modulated to the baseband by $\mathrm{CH}_{\mathrm{out1,2}}$ and converted to output voltages V_{out1} and V_{out2}. Each channel's output includes the opposite channel's odd harmonics. Let us consider the output of channel-1, which includes the baseband signal of V_{in1} and harmonics generated by V_{in2}.

The harmonics of channel-2 modulated by $\mathrm{CH}_{\mathrm{out1}}$ generate signals at $f_{\mathrm{CH1}} \pm f_{\mathrm{CH2}} = (2n+1)f_{\mathrm{chop}} \pm 2f_{\mathrm{chop}}$ ($n = 0, 1, 2, 3, \ldots$) at the output of channel-1. The offset voltage V_{OS11} at the input of G_{m11} is converted to current and up-modulated by $\mathrm{CH}_{\mathrm{out1}}$. When converted to a voltage by the integrator, it generates an output ripple at f_{chop}. Similarly, the output of channel-2 includes the signals at the baseband and harmonic signals generated by V_{in1}. The harmonics exist at $f_{\mathrm{CH2}} \pm f_{\mathrm{CH1}} = 2(2n+1)f_{\mathrm{chop}} \pm f_{\mathrm{chop}}$. The output ripple exists at $2f_{\mathrm{chop}}$. Each channel's output is connected to an off-chip low-pass filter (LPF) to suppress the unwanted signals.

B. CIRCUIT IMPLEMENTATION

Fig. 22 shows the schematic of G_{m11} with the CMFB circuit. The inverter-based input stage achieves increased noise efficiency by the doubled transconductance. Because V_{TH} is about 500 mV, the input pair operates in the weak inversion with $V_{\mathrm{DD}} = 1$ V. The CM output voltage of the input pair can be directly affected by V_{TH}, which can shift more than 100 mV with the PVT variations [32]. The CMFB circuit based on active feedback is used to track the variation. The size of the current mirror (M_5 and M_6) is increased considering the effect of the gate leakage on the bias. The input pair and the CMFB network are biased at 1 μA and 100 nA, respectively.

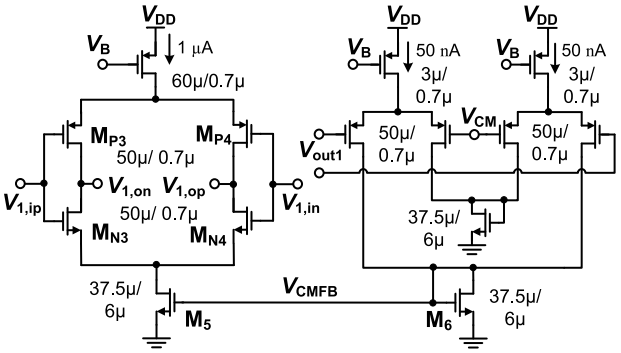

FIGURE 22. Schematic of the inverter-based amplifier with active CMFB circuit.

Fig. 23 shows the statistical distribution of the low-frequency gain of G_{m11} using 200 Monte Carlo simulations. The result shows the average gain of 55.1 dB at $V_{\mathrm{DD}} = 1$ V. When V_{DD} varies by 10%, the average gain changes from 54.2 to 55.3 dB. The relatively stable gain with V_{DD} change indicates that the gate leakage effect on the bias point can be handled using the active CMFB circuit. Fig. 24 shows the schematic of the G_{m21} and G_{m22} biased at 130 nA. The Miller capacitor $C_{\mathrm{M1,2}} = 2.5$ pF is used to achieve the phase margin $> 60^{\mathrm{o}}$. The Monte Carlo simulations show that the average gain of 31.3 dB at $V_{\mathrm{DD}} = 1$ V.

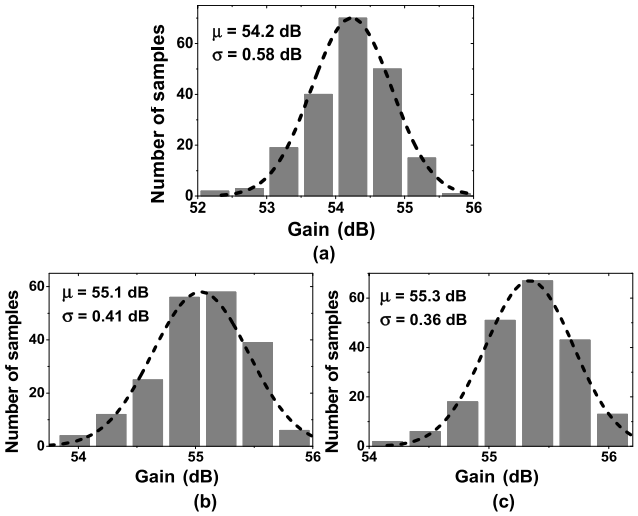

FIGURE 23. Statistical distribution of the gain of G_{m11} using (a) V_{DD} = 0.9 V, (b) V_{DD} = 1 V, (c) V_{DD} = 1.1 V.

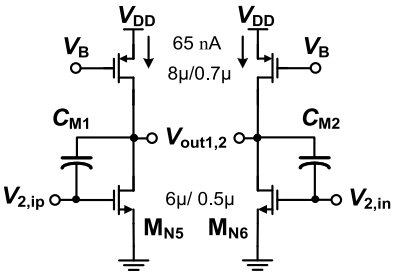

FIGURE 24. Schematic of the common-source amplifier.

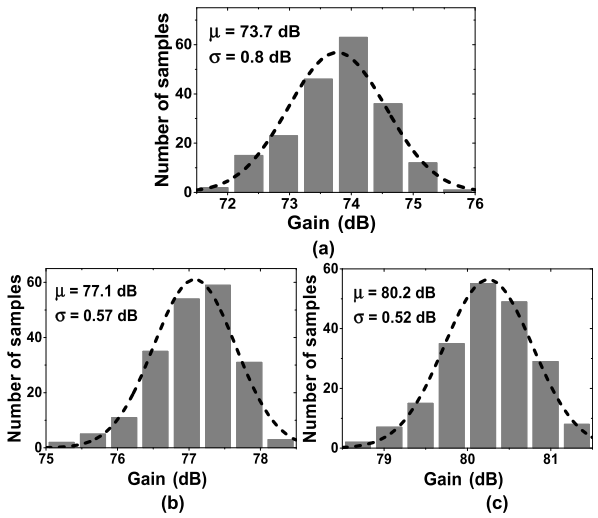

FIGURE 25. Statistical distribution of the gain of two-stage opamp. (a) V_{DD} = 0.9 V, (b) V_{DD} = 1 V, (c) V_{DD} = 1.1 V.

The two-stage opamp for the integrator in the DSL is similar to the one used for CCIA. The input differential pair is biased at 5 nA to limit the bandwidth. The second CS stage is biased at 10 nA to increase gain and output swing.

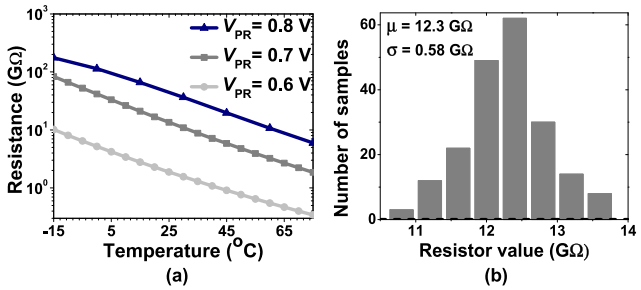

FIGURE 26. (a) Simulated value of the pseudo-resistor depending on temperature for different V_{PR}, (b) statistical distribution.

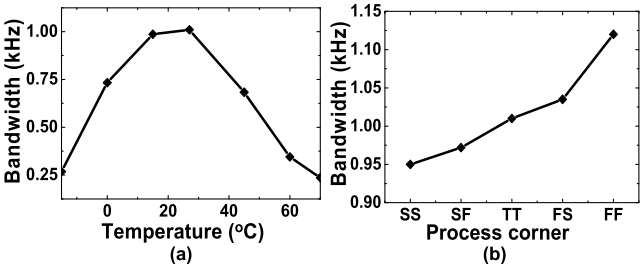

FIGURE 27. Bandwidth of the DCCIA depending on (a) temperature, (b) process corners.

Fig. 25 shows that the opamp under device mismatch still provides a low-frequency gain > 70 dB when V_{DD} is reduced to 10% from V_{DD} = 1 V. Here, R_{DSL} ($R_{DSL11,12}$ and $R_{DSL21,22}$) is realized using variable pseudo resistors with a size of W/L = 1μm/5μm. The external voltage V_{PR} controls the resistor value.

Fig. 26(a) shows the value of R_{DSL} as a function of temperature for various V_{PR}. The value of R_{DSL} decreases with temperature, and it increases with V_{PR}. Fig. 26(b) shows the statistical distribution obtained using 200 Monte Carlo simulations at 27 °C and V_{PR} = 0.7 V. The average value of R_{DSL} is 12.3 GΩ, with a standard deviation of 0.58 GΩ. Fig. 27 shows the effect of the temperature and process corner on the bandwidth of the DCCIA. The DCCIA achieves a 1 kHz bandwidth over normal body temperature. The bandwidth is larger than 750 Hz over the temperature from 1 °C to 41 °C. The dominant temperature-dependent parameters of the subthreshold current are mobility and the threshold voltage [33]. The increased threshold voltage with temperature reduces the gain and the bandwidth [34]. Because the bias current generated from constant-g_m current reference decreases with temperature, the bandwidth reduces with the decreasing temperature. The bandwidth changes from 0.95 kHz to 1.12 kHz across the process corners.

Fig. 28 shows the schematic of the clock generator. The two orthogonal chopping frequencies, f_{CH1} and f_{CH2}, are generated using an input clock f_{CLK}. The f_{CLK} is divided by half before applied to a non-overlap clock generator, which outputs the complementary chopping frequency f_{CH1} for channel-1. Because channel-2 uses $f_{CH2} = 2f_{CH1}$, f_{CLK} is directly applied to the non-overlap clock generator.

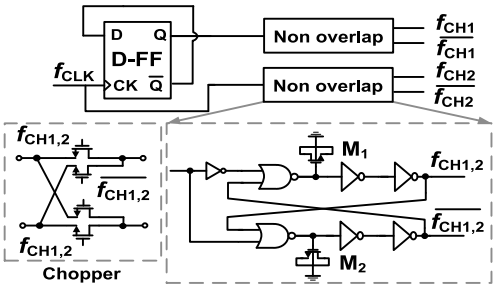

FIGURE 28. Schematic of the clock generator for the DCCIA.

C. NOISE ANALYSIS

The IRN of the DCCIA, $\overline{V_{\text{n,in}}^2}$ can be expressed as

$$\begin{aligned}\overline{V_{\text{n,i}}^2} &= \left(\frac{C_{\text{tot}}}{C_{\text{in11,12}}+C_{\text{in21,22}}}\right)^2 \overline{V_{\text{n,in,Gm1}}^2} \\ &+ 2\overline{I_{\text{n,R1,2}}^2} Z_{\text{Cin11,12}}^2 + 2\overline{I_{\text{n,R1,2}}^2} Z_{\text{Cin21,22}}^2 \\ &+ 12\overline{I_{\text{n,shot}}^2} Z_{\text{Cin11,12}}^2 + 12\overline{I_{\text{n,shot}}^2} Z_{\text{Cin21,22}}^2 \\ &+ 4\overline{V_{\text{n,out,DSL}}^2}\left(\frac{C_{\text{hp11,12}}}{C_{\text{in11,12}}}\right)^2 \\ &= \left(\frac{C_{\text{tot}}}{C_{\text{in11,12}}+C_{\text{in21,22}}}\right)^2 \left(\frac{8kT\gamma}{g_{\text{mP3,4}}+g_{\text{mN3,4}}}\right) \\ &+ \frac{8kT}{R_{1,2}}\left(\frac{1}{\omega_{\text{CH1}}C_{\text{in11,12}}}\right)^2 \\ &+ \frac{8kT}{R_{1,2}}\left(\frac{1}{\omega_{\text{CH2}}C_{\text{in21,22}}}\right)^2 + 12\alpha q I_{\text{G}}\left(\frac{1}{\omega_{\text{CH1}}C_{\text{in11,12}}}\right)^2 \\ &+ 12\alpha q I_{\text{G}}\left(\frac{1}{\omega_{\text{CH2}}C_{\text{in21,22}}}\right)^2 + 4\overline{V_{\text{n,out,DSL}}^2}\left(\frac{C_{\text{hp11,12}}}{C_{\text{in11,12}}}\right)^2 \end{aligned} \quad (5)$$

with $\overline{V_{\text{n,out,DSL}}^2} = \left(\frac{f_{\text{ugb}}}{f_{\text{CH1,2}}}\right)^2 \left(\overline{V_{\text{n,in,Gm31,32}}}^2 + \overline{V_{\text{n,R}_{\text{DSL}}}}^2\right) = \left(\frac{f_{\text{ugb}}}{f_{\text{CH1,2}}}\right)^2 \left(\overline{V_{\text{n,in,Gm31,32}}}^2 + 4kTR_{\text{DSL}}\right)$ where $C_{\text{tot}} = C_{\text{in11,12}} + C_{\text{in21,22}} + C_{\text{fb11,12}} + C_{\text{fb21,22}} + C_{\text{hp11,12}} + C_{\text{hp21,22}} + C_{\text{P}}$ and C_{P} is parasitic capacitor. The $V_{\text{n,in,Gm1}}^2$ and $V_{\text{n,in,Gm31,32}}^2$ represent the input-referred noise of G_{m11} and two-stage amplifier in DSL, respectively. The $I_{\text{n,R,1,2}}^2$ is the noise current from the bias resistor $R_{1,2}$, which is converted to noise voltage by f_{CH1} and f_{CH2}. $I_{\text{n,shot}}^2 = \alpha q I_G \Delta f$ is shot noise current density of the twelve transistors in the three choppers ($\text{CH}_{\text{in1,2}}$, $\text{CH}_{\text{fb1,2}}$, and $\text{CH}_{\text{out1,2}}$). The $Z_{\text{Cin11,12}}$ and $Z_{\text{Cin21,22}}$ are the equivalent resistance of $C_{\text{in11,12}}$ and $C_{\text{in21,22}}$ chopped at f_{CH1} and f_{CH2}, respectively. Using $g_{\text{mP3,4}} = 13\ \mu\text{S}$, and $g_{\text{mN3,4}} = 13.6\ \mu\text{S}$, we obtain $V_{\text{n,in}}^2 = 123\ \text{nV}/\sqrt{\text{Hz}}$ without the DSL. The simulated value obtained using the Cadence Spectre is 130 nV /$\sqrt{\text{Hz}}$, which is slightly lower than the measured value of 136 nV/$\sqrt{\text{Hz}}$. The calculated $V_{\text{n,in}}^2$ increases to 141 nV/$\sqrt{\text{Hz}}$ when the DSL is enabled. The result shows that the IRN of the DCCIA referred to either V_{in1} or V_{in2} is slightly increased compared to the noise of CCIA. This increase is attributed to the additional loading from the capacitive feedback network. Using an increased bias current (1 μA), however, the thermal noise density of DCCIA is slightly lower than that of CCIA. When we consider the overall noise of two channels, the IRN increases about a factor of two.

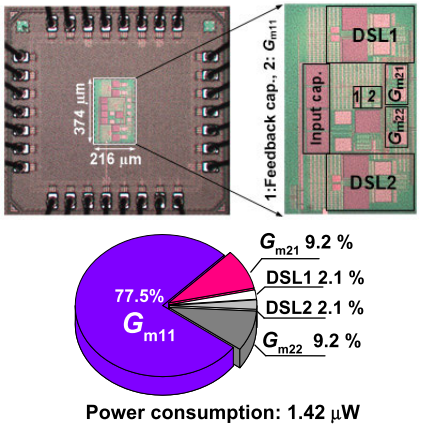

FIGURE 29. Microphotograph of the DCCIA fabricated using 28 nm CMOS. Power breakdown of the DCCIA is also shown.

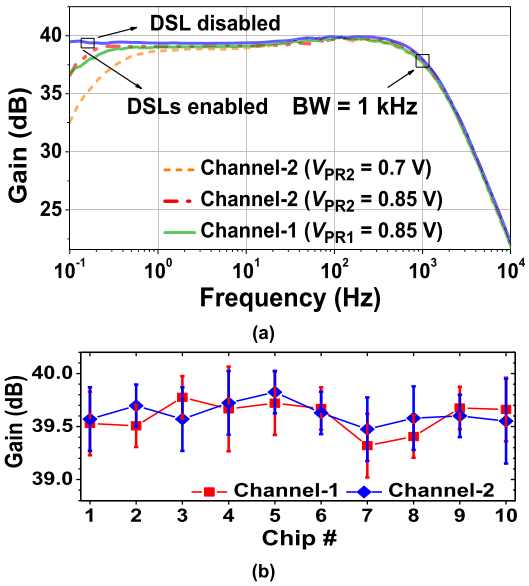

FIGURE 30. (a) Measured frequency response of DCCIA. (b) Measured gain distributions of ten chips. DSLs are enabled with $V_{\text{PR}} = 0.85$ V.

D. MEASURED RESULT

Fig. 29 shows the microphotograph of the DCCIA with a core area of 0.08 mm^2. The power breakdown of the DCCIA core shows that G_{m11} consumes 77.5% of the overall power of 1.42 μW. Fig. 30(a) shows the measured frequency response of the DCCIA. The low-frequency gain is 39.5 dB when the DSL is disabled. The 3-dB bandwidth is about 1 kHz. The high-pass corner is successfully created when DSLs are enabled. When V_{PR} is varied from 0.6 and 0.85 V, the high-pass corner frequency is tunable from 0.16 to 0.75 Hz. Fig. 30(b) shows the mid-band gain distribution obtained from ten samples. The result shows that the gain mismatch between the two channels is less than 0.3% indicating relatively good matching.

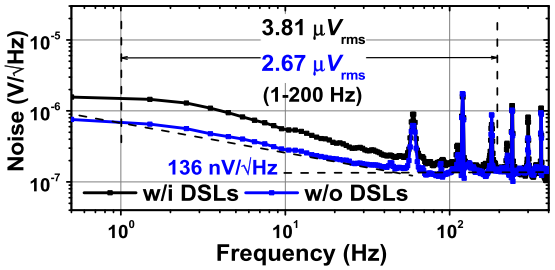

FIGURE 31. Measured input-referred noise voltage spectral density.

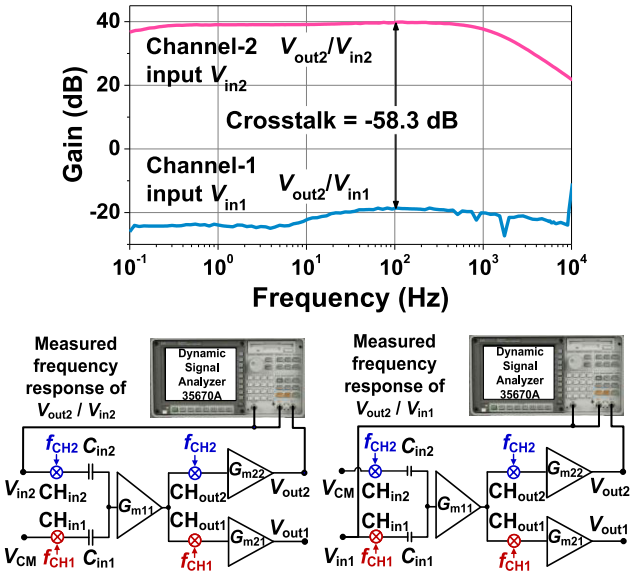

FIGURE 32. Measured crosstalk between the two channels of the DCCIA. Experimental setup for measured frequency response of V_{out2}/V_{in2} and V_{out2}/V_{in1} is also shown. The output of channel-2 is used for this characterization.

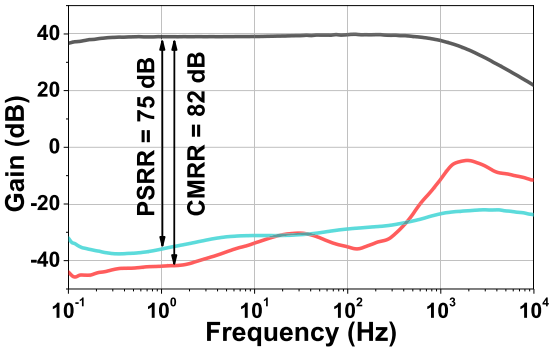

FIGURE 33. Measured CMRR and PSRR of the DCCIA.

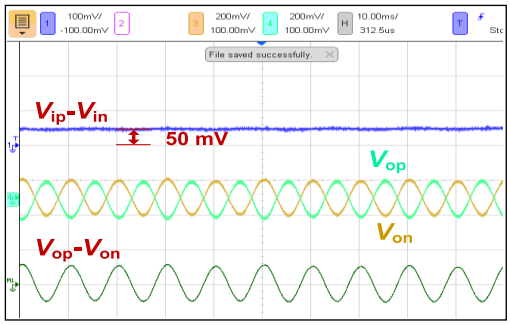

FIGURE 34. Measured waveforms of the DCCIA for the 50 mV electrode offset and 4 mV differential input signal.

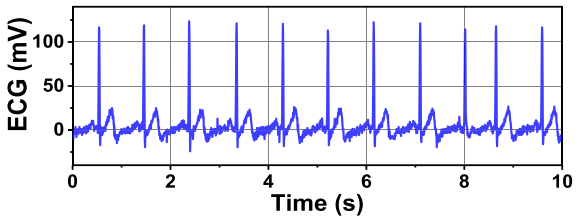

FIGURE 35. Output of the DCCIA for the p rerecorded human ECG input.

Fig. 31 shows the measured IRN of the DCCIA. Both inputs of the DCCIA is connected to ground, and one of output channel is connected to the signal analyzer. The measured output noise is divided by the gain of the DCCIA to obtained IRN. The noise density is 136 nV/$\sqrt{}$Hz, and the integrated noise over 200 Hz is 2.67 $\mu V_{\rm rms}$ when the DSLs are disabled. When the DSLs are enabled, the noise density increases to 168 nV/$\sqrt{}$Hz with the corresponding integrated noise of 3.81 $\mu V_{\rm rms}$. When the DSLs are enabled, the capacitor $C_{\rm hp11,12}$ used for current conversion increases the noise by the charge dividing effect. Besides, the low-frequency gain is reduced when the DSLs are enabled, increasing the flicker noise in the low-frequency band.

Fig. 32 shows the measured crosstalk between two channels of the DCCIA. The signal labeled channel-2 is the frequency response of channel-2's output when channel-1's input is connected to $V_{\rm CM}$. The signal labeled channel-1 is the response of channel-2's output for the input of channel-1 when channel-2's input is connected to $V_{\rm CM}$. The crosstalk between the two channels is –58.3 dB at 100 Hz. Fig. 33 shows that the low-frequency CMRR is about 85 dB, and the PSRR is about 75 dB. Fig. 34 shows the input and output waveforms of the DCCIA. The input consists of a 4 mV differential signal at 100 Hz with a 50 mV electrode offset. The result shows that the DSL tolerates a $V_{\rm EOS}$ up to 50 mV. Fig. 35 shows the measured output of the proposed DCCIA for the prerecorded human ECG input (∼ 1 mV). An off-chip LPF ($C = 0.1$ μF and $R = 2.2$ kΩ) is used at the output of each channel.

Table 3 shows the performance comparison. Work [15] achieves a low noise of 26 nV/$\sqrt{}$Hz and crosstalk of 83.2 dB; however, this work consumes a relatively high power of 40.5 μW per channel. Work [31] can simultaneously measure BioZ and ECG from the same electrode; however, it needs two chopper amplifier stages where the first stage modulates BioZ and ECG signals in different frequency bands before applied to the second stage, leading to increased power consumption. Work [35] achieves an area efficiency of 0.02 mm^2 by consuming 1.97 μW per channel; works [15] and [35] do not include the DSL for handling $V_{\rm EOS}$. Besides, the power

TABLE 3. Performance comparison.

	[15]	[24]	[31]	[35]	[36]	This work
Process (nm)	350	65	40	180	65	28
Area/ Ch. (mm^2)	0.03	0.2	N/A	0.02	0.03	0.04
Power/ Ch. (μW)	40.5	2.1	1.89	1.97	2.3	0.71
Num. of Ch.	2	1	2	15	64	2
Gain error (%)	0.55	N/A	N/A	0.43	15	0.29
Crosstalk (dB)	–83.2	N/A	–60	–51.5	–85	–58.3
Max. V_{EOS} (mV)	N/A	50	300	N/A	50	50
DSL	N	Y	Y	N	Y	Y
Gain (dB)	40	40	30	40	30	39.5
BW (kHz)	1	0.5	0.15	0.49	0.5	1
CMRR (dB)	110	134	87	N/A	88	82
PSRR (dB)	103	120	N/A	N/A	67	75
Noise density ($nV/\sqrt{Hz}$)	26	60	145*/ 240	155	58	136*/ 168
NEF/ Ch.	3.74*	3.3*/ 37.4	N/A	7.3*	4.8	3.0*/ 4.4
PEF/ Ch.	41.9*	10.9*/ 1398	N/A	63.1*	11.3	9*/ 19.1

* Without DSL.

consumption of these works exceeds 1 μW. Work [36] achieves an area efficiency of 0.03 mm^2 per channel, which is similar to ours; however, this work shows a relatively poor gain mismatch of 15%. Our work achieves an area efficiency of 0.04 mm^2 per channel using a 28 nm CMOS process. A mid-band gain of 39.5 dB is achieved using 0.71 μW per channel with the DSL included. The gain mismatch of 0.29% is the lowest among other works. The DCCIA achieves a NEF of 3.0 and 4.4 without and with the DSL.

The novelty of this work can be summarized as follows: the orthogonal frequency chopping technique is introduced in [10], [11]; however, the critical V_{EOS} issue is not addressed in these works. Previous works present the offset blocking capacitor [23] and charge-sharing resistor [26]. Based on similar techniques, however, our work is successfully realized in the advanced 28 nm CMOS process. This approach achieves a compact area (0.04 mm^2/channel) with an excellent gain matching (0.29% error). Besides, this work is the first instrumentation amplifier demonstration using the smallest CMOS process nodes, investigating the potential for the area and power-efficient biosensing systems.

V. CONCLUSION

In this paper, we present two CCIAs successfully implemented in a 28 nm CMOS process for advanced multi-channel biosensing applications. The first design realizes a compact CCIA using offset-blocking for chopping ripple reduction, DSL for V_{EOS} suppression, and an on-chip HPF for handling CM artifacts. The CCIA, which is realized in a compact area of 0.05 mm^2, achieves a mid-band gain of 39.5 dB by consuming 1 μW. The IRN of CCIA is 139 $nV/\sqrt{Hz}$ (without the DSL) and 160 $nV/\sqrt{Hz}$ (with the DSL), corresponding to the integrated noise of 2.15 and 2.74 μV_{rms}, respectively, over 200 Hz bandwidth. Using the on-chip HPF, the CCIA handles an electrode offset V_{EOS} up to 50 mV, tolerates the CM artifacts up to 1.5 V_{pp}, and suppresses the output ripple down to 112 μV. The CCIA achieves a NEF of 5.8 (without the DSL) and 7.5 (with the DSL). The second design demonstrates the DCCIA using orthogonal frequency chopping for multi-channel applications. The DCCIA, which is realized in a compact area of 0.04 mm^2 per channel, achieves a mid-band gain of 39.5 dB by consuming 0.71 μW per channel. The measured IRN is 136 $nV/\sqrt{Hz}$, and the integrated noise over 200 Hz bandwidth is 2.67 μV_{rms} when the DSL is disabled. When the DSL is enabled, the measured IRN is 168 $nV/\sqrt{Hz}$ with an integrated noise of 3.81 μV_{rms}. The DCCIA achieves a NEF of 3.0 (without the DSL) and 4.4 (with the DSL). An excellent gain matching error of 0.29% is achieved with the crosstalk higher than 58 dB between the channels. The results demonstrate the potential of deep nanometer-scale CMOS technology for realizing area and power-efficient biosensing systems.

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