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Impedance Modeling and Stability Analysis of Three-Phase Four-Leg Grid-Connected Inverter Considering Zero-Sequence

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ABSTRACT With the increasing applications of grid-connected voltage source converters, it is important to analyze the impedance characteristic of the grid-connected system to implement the stability analysis of the grid connection operation. Compared with the three-phase three-wire system, an additional zero-sequence path exists in the three-phase four-wire system. Therefore, it is necessary to consider the influence of the zero sequence when analyzing the stability of the system. In this paper, an impedance model including positive-sequence, negative-sequence and zero-sequence impedance of the three-phase four-leg grid-connected inverter is established. Through impedance characteristic analysis, the relationships between zero-sequence impedance and positive-sequence, negative-sequence impedance can be found which are decupled. Based on the developed zero-sequence impedance model, the main factors affecting the zero-sequence impedance model are revealed. Then, the system stability consisting of the grid and three-phase four-wire inverter is investigated, and the experimental results validate the theoretical analysis.

INDEX TERMS Impedance modeling, three-phase four-leg grid-connected inverter, zero-sequence, stability analysis.

I. INTRODUCTION

Grid-connected voltage source converters (VSCs) have been widely employed in power system for renewable energy generation, flexible power transmission, and energy-efficient power consumption. Since the integration of power electronic converters brings nonlinearity to the traditional grids, various stability problems were reported, which are caused by the interaction between the VSC and the grid [1]–[4].

Many methods are proposed to study the system stability characteristic, such as loop-gain [5]–[7], eigenvalues analysis based on system state-space [8], and passivity [9], [10], impedance-based method [11], [12]. Among these methods, the impedance-based analysis provides an attractive approach to analyze and resolve the stability problems caused by the interaction between the VSC and the grid [12]–[16]. Undrill and Kostyniak analyzed the sub-synchronous oscillations of power systems based on the impedances of generators and the transmission network in [13]. Reference [14] presents a stability criterion for grid-connected converters based on impedance models and Gershgorin's theorem, which consider the effect of the non-diagonal elements. In [15], the small signal stability of a three-phase ac system using measured d-q frame impedances and the generalized Nyquist stability criterion is investigated by the scholars. However, the above researches are based on the three-phase three-wire system.

In addition to three-phase three-wire system, three-phase four-wire system is also widely used in distribution network. The difference between a three-phase three-wire system and a three-phase four-wire system is whether there is a zero-sequence current path. Although many scholars have studied the stability problem in the three-phases three-wire system [12]–[16], [32], [33], the conclusions about stability based on the impedance analysis method cannot fully reflect the situation of the system due to the neglect of zero sequence component. Therefore, it is necessary to study zero-sequence stability and its relationship with positive, negative-sequence stability.

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In order to analyze the stability of the three-phase four-wire system including zero sequence stability, it is necessary to analyze the transmission path of the positive-sequence, negative-sequence and zero-sequence perturbation signals in each sequence loop. Then the frequency-domain relationship between the perturbation signal and the response can be obtained as the impedance model. Based on the impedance model, the stability issue can be analyzed. However, the relevant research on the zero-sequence is lacked.

In the three-phase four-wire system, the four-leg voltage source inverters are widely used in different standalone and grid-connected applications [17]–[24], which includes distributed generation [17], islanded microgrids [19], uninterruptible power supply [20], active power filter [21], [22] and voltage compensators [23], [24]. Compared to three-phase three-leg inverters with split dc links, the addition of the fourth leg provides extra advantage in terms of voltage rating. Indeed, reduced dc bus voltage is involved, and larger ac voltage may be supported (over 15%) [25]. Moreover, the additional leg provides zero-sequences current with an effective path, which sustains the converter ability to handle the critical conditions, such as the presence of single-phase or unbalanced phase loading [25].

Therefore, this paper established the impedance model of the three-phase four-leg grid-connected inverter, and the impedance models of positive-sequence, negative-sequence and zero-sequence are obtained. The derivation process of the admittance model including positive, negative and zero sequence is more complicated than that of the pure positive and negative sequence admittance model. The matrix dimension has increased from 2D to 3D, and the analysis of disturbance loop needs to consider the influence of the zero-sequence components. When performing stability analysis, it is not only necessary to consider the stability of the positive and negative sequences, but also need to consider whether the zero sequence will bring stability problems, which increases the complexity of the analysis process.

The rest of this paper is organized as follows: System description and impedance modeling of three-phase four-leg grid-connected inverter is given in Section II as a foundation of the following analysis. Then, the admittance model verification and the effect of AC side filter parameters as well as the zero-axis current loop parameters on zero-sequence admittance are studied in Section III. The grid-connected operation stability of the three-phase four-leg grid-connected inverter and the cases for validation is analyzed in Section IV. Finally, Section V gives the conclusion of the paper.

II. IMPEDANCE MODELLING OF THREE-PHASE FOUR-LEG GRID-CONNECTED INVERTER

For the sake of establishing the model of three-phase four-leg grid-connected inverter, firstly, it is necessary to analyze the transmission path of the positive-sequence, negative-sequence and zero-sequence perturbation signals in each sequence loop so as to obtain corresponding small-signal models. And then the impedance model can be derived.

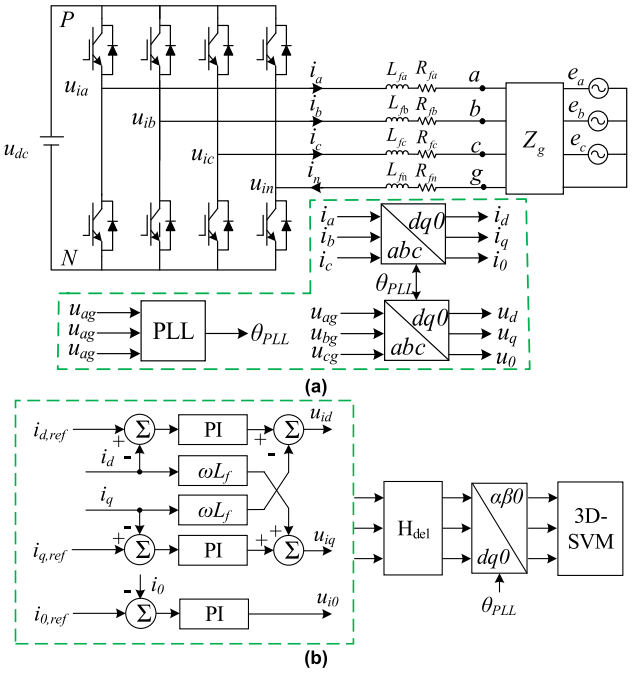


FIGURE 1. Block diagram of three-phase four-leg grid-connected inverter.

A. SYSTEM DESCRIPTION

The block diagram of the three-phase four-leg grid-connected inverter considered in this paper is shown in Figure 1. The control block diagram of the system includes the PLL, and the control delay, the inner current controller and 3D-SVM modulation module [26], [27].

The four control signals named as *Sa*, *Sb*, *Sc*, and *Sn* can be applied to denote a total of 16 (2^4) switching states of the converter. The voltages in each leg of the inverter, measured from the negative point of the dc-link N, can be expressed as,

$$\begin{bmatrix} u_{aN} \\ u_{bN} \\ u_{cN} \\ u_{nN} \end{bmatrix} = \begin{bmatrix} S_a \\ S_b \\ S_c \\ S_n \end{bmatrix} u_{dc} \tag{1}$$

From (1), the voltage model can be expressed as,

$$\begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = \begin{bmatrix} u_{aN} - u_{nN} \\ u_{bN} - u_{nN} \\ u_{cN} - u_{nN} \end{bmatrix} = \begin{bmatrix} S_a - S_n \\ S_b - S_n \\ S_c - S_n \end{bmatrix}$$
$$u_{dc} = \begin{bmatrix} d_a - d_n \\ d_b - d_n \\ d_c - d_n \end{bmatrix} u_{dc} \tag{2}$$

where, d_a, d_b d_c d_n are the duty ratio of the four legs respectively.

Then, the inverter voltages can be written as,

$$\begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = \begin{bmatrix} L_{fa} & 0 & 0 \\ 0 & L_{fb} & 0 \\ 0 & 0 & L_{fc} \end{bmatrix} \begin{bmatrix} pi_a \\ pi_b \\ pi_c \end{bmatrix}$$

$$+\begin{bmatrix} R_{fa} & 0 & 0 \\ 0 & R_{fb} & 0 \\ 0 & 0 & R_{fc} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L_{fn}\begin{bmatrix} pi_n \\ pi_n \\ pi_n \end{bmatrix} + R_{fn}\begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} + \begin{bmatrix} u_{ag} \\ u_{bg} \\ u_{cg} \end{bmatrix} \quad (3)$$

Under assumption $L_{fa} = L_{fb} = L_{fc} = L_f$, $R_{fa} = R_{fb} = R_{fc} = R_f$, $L_{fn} = L_n$, $R_{fn} = R_n$, the mathematical model in $dq0$-domain can be obtained as,

$$\begin{bmatrix} u_{id} \\ u_{iq} \\ u_{i0} \end{bmatrix} = \begin{bmatrix} L_f & 0 & 0 \\ 0 & L_f & 0 \\ 0 & 0 & 3L_n + L_f \end{bmatrix}\begin{bmatrix} pi_d \\ pi_q \\ pi_0 \end{bmatrix} + \begin{bmatrix} R_f & 0 & 0 \\ 0 & R_f & 0 \\ 0 & 0 & 3R_n + R_f \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} 0 & \omega L_f & 0 \\ -\omega L_f & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \quad (4)$$

where p represents the differential operator d/dt.

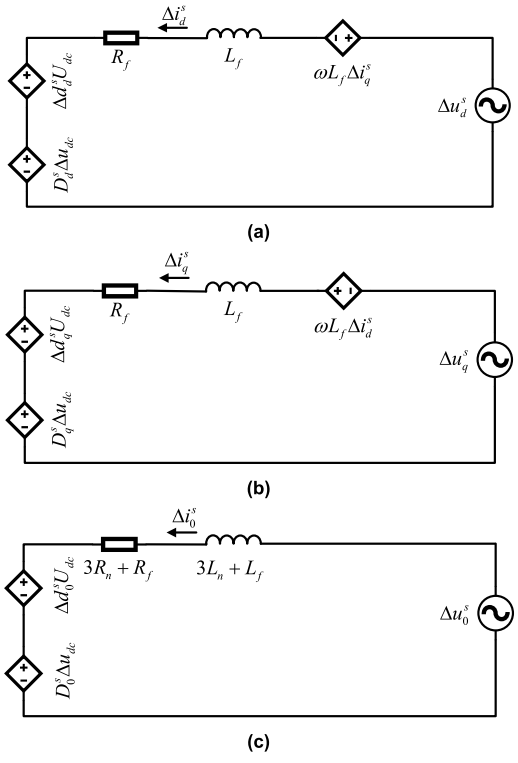


FIGURE 2. Small-signal circuit model of inverter in system $dq0$-domain. (a) d-axis small-signal circuit; (b) q-axis small-signal circuit; (c) 0-axis small-signal circuit.

Figure 2 shows its equivalent circuit used for developing the small-signal model, in which Δx denotes the small-signal perturbation of x and X represents corresponding steady state value. For instance, Δd_d^s denotes the small-signal perturbation of duty ratio and D_d^s is the steady-state value of duty ratio in d axis. In this paper, the dc voltage of inverter is assumed to be constant to simplify the modeling process. Based on the above small-signal model, the impedance model can be derived.

B. IMPEDANCE MODELING OF THE THREE-PHASE FOUR-LEG GRID-CONNECTED INVERTER

Since the synchronous reference frame phase-locked loop (SRF-PLL) is widely applied to obtain the grid phase information, and its dynamic characteristics influence the stability of the system. Therefore, it is necessary to consider the PLL when establishing the impedance model. the block diagram of SRF-PLL is shown in Figure 3.

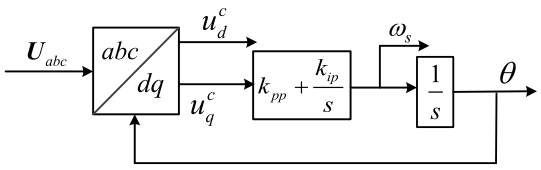


FIGURE 3. Block diagram of PLL.

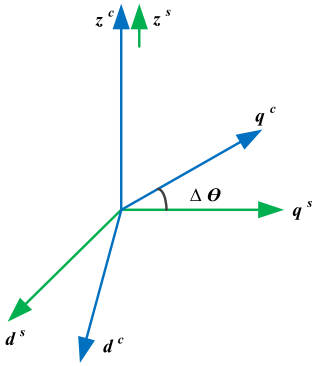


FIGURE 4. System and controller $d-q-0$ frames.

Figure 4 shows the system and controller $d-q-0$ frames. The system $d-q-0$ frame coincides with the controller $d-q-0$ frame in steady state. When there are perturbations in the grid voltage, due to the dynamic performance of the PLL, there will be an angular difference $\Delta\theta$ between the controller $d-q-0$ frames and the system $d-q-0$ frames in d-axis and q-axis, while the 0-axis is still coincident. The transfer function matrix from system $d-q-0$ frames to controller $d-q-0$ frames can be expressed by

$$\mathbf{F} = \begin{bmatrix} \cos(\Delta\theta) & -\sin(\Delta\theta) & 0 \\ \sin(\Delta\theta) & \cos(\Delta\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (5)$$

Then,

$$\begin{cases} \vec{u}^c = \mathbf{F}\vec{u}^s \\ \vec{i}^c = \mathbf{F}\vec{i}^s \\ \vec{d}^s = \mathbf{F}\vec{d}^c \end{cases} \quad (6)$$

where subscript s indicates the variable in the system $d-q-0$ frame as well as subscript c indicates the variable in the controller $d-q-0$ frame.

When the system operates in the steady state, the variables of system $d-q-0$ frame are equal to the variables of controller $d-q-0$ frame.

$$\begin{cases} \vec{U}^c = \vec{U}^s \\ \vec{I}^c = \vec{I}^s \\ \vec{D}^c = \vec{D}^s \end{cases} \tag{7}$$

The aforementioned equation indicates that the angle between vectors in the controller frame and the vector in system frame is 0; using the rotation matrix $\mathbf{F}$, (7) can be rewritten as

$$\begin{cases} \vec{U}^c = \begin{bmatrix} \cos(0) & -\sin(0) & 0 \\ \sin(0) & \cos(0) & 0 \\ 0 & 0 & 1 \end{bmatrix} \vec{U}^s \\ \vec{I}^c = \begin{bmatrix} \cos(0) & -\sin(0) & 0 \\ \sin(0) & \cos(0) & 0 \\ 0 & 0 & 1 \end{bmatrix} \vec{I}^s \\ \vec{D}^s = \begin{bmatrix} \cos(0) & \sin(0) & 0 \\ -\sin(0) & \cos(0) & 0 \\ 0 & 0 & 1 \end{bmatrix} \vec{D}^c \end{cases} \tag{8}$$

Add small-signal perturbation to (8)

$$\begin{bmatrix} U_d^c + \Delta u_d^c \\ U_q^c + \Delta u_q^c \\ U_0^c + \Delta u_0^c \end{bmatrix} = \begin{bmatrix} \cos(0+\Delta\theta) & -\sin(0+\Delta\theta) & 0 \\ \sin(0+\Delta\theta) & \cos(0+\Delta\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_d^s + \Delta u_d^s \\ U_q^s + \Delta u_q^s \\ U_0^s + \Delta u_0^s \end{bmatrix} \tag{9}$$

By doing a small angle approximation of trigonometric functions, and canceling the steady-state values, the relationship between voltage vectors in the controller frame, system frame, and PLL output angle can be derived as

$$\begin{bmatrix} U_d^c + \Delta u_d^c \\ U_q^c + \Delta u_q^c \\ U_0^c + \Delta u_0^c \end{bmatrix} \approx \begin{bmatrix} 1 & -\Delta\theta & 0 \\ \Delta\theta & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_d^s + \Delta u_d^s \\ U_q^s + \Delta u_q^s \\ U_0^s + \Delta u_0^s \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} \Delta u_d^c \\ \Delta u_q^c \\ \Delta u_0^c \end{bmatrix} \approx \begin{bmatrix} \Delta u_d^s + U_q^s \Delta\theta \\ \Delta u_q^s - U_d^s \Delta\theta \\ \Delta u_0^s \end{bmatrix} \tag{11}$$

Then, based on the block diagram of PLL in Figure3, $\Delta\theta$ can be obtained as,

$$\Delta\theta = \Delta u_q^c * \left(k_{pp} + \frac{k_{ip}}{s}\right) * \frac{1}{s} \tag{12}$$

Substituting (12) into (10), the relationship between small-signal perturbation from voltage in the system frame and in the controller frame can be achieved as,

$$\Delta u_q^s = \Delta u_q^c * \left(1 + U_d^s * \left(k_{pp} + \frac{k_{ip}}{s}\right) * \frac{1}{s}\right) \tag{13}$$

Combining (12) and (13), the relationship between angular difference $\Delta\theta$ and small-signal perturbation from voltage in the system frame can be expressed as,

$$\Delta\theta = \frac{k_{pp} + k_{ip}/s}{s + U_d^s * \left(k_{pp} + k_{ip}/s\right)} \Delta u_q^s \tag{14}$$

Defining

$$\Delta\theta = H_{PLL} * \Delta u_q^s \tag{15}$$

For duty ratio, the small-signal analysis can be done, which yields

$$\begin{bmatrix} \Delta d_d^s \\ \Delta d_q^s \\ \Delta d_0^s \end{bmatrix} \approx \begin{bmatrix} 0 & D_q^s H_{PLL} & 0 \\ 0 & -D_q^s H_{PLL} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \Delta u_d^s \\ \Delta u_q^s \\ \Delta u_0^s \end{bmatrix} + \begin{bmatrix} \Delta d_d^c \\ \Delta d_q^c \\ \Delta d_0^c \end{bmatrix} \tag{16}$$

The matrix $\mathbf{H_{PLL}^d}$ of the small-signal perturbation from voltage in the system frame to duty ratio in the controller frame can be expressed as,

$$\mathbf{H_{PLL}^d} = \begin{bmatrix} 0 & -D_q^s H_{PLL} & 0 \\ 0 & D_q^s H_{PLL} & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{17}$$

Similarly, for current, the matrix $\mathbf{H_{PLL}^i}$ of the small-signal perturbation from voltage in the system frame to the current in the controller frame can be can be defined as,

$$\mathbf{H_{PLL}^i} = \begin{bmatrix} 0 & H_{PLL} I_q^s & 0 \\ 0 & -H_{PLL} I_d^s & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{18}$$

From Figure 2, Assuming $\Delta d_d^s = \Delta d_q^s = 0$, the relationship between the small-signal perturbation voltage and the corresponding current in the system frame can be expressed,

$$\begin{bmatrix} \Delta u_d^s \\ \Delta u_q^s \\ \Delta u_0^s \end{bmatrix} = \begin{bmatrix} sL_f + R_f & \omega L_f & 0 \\ -\omega L_f & sL_f + R_f & 0 \\ 0 & 0 & s(L_f + 3L_n) + R_f + 3R_n \end{bmatrix} \times \begin{bmatrix} \Delta i_d^s \\ \Delta i_q^s \\ \Delta i_0^s \end{bmatrix} \tag{19}$$

Therefore, the transfer function matrix from perturbation voltage to current response can be expressed as,

$$\mathbf{Z_{out}} = \begin{bmatrix} sL_f + R_f & \omega L_f & 0 \\ -\omega L_f & sL_f + R_f & 0 \\ 0 & 0 & s(L_f + 3L_n) + R_f + 3R_n \end{bmatrix} \tag{20}$$

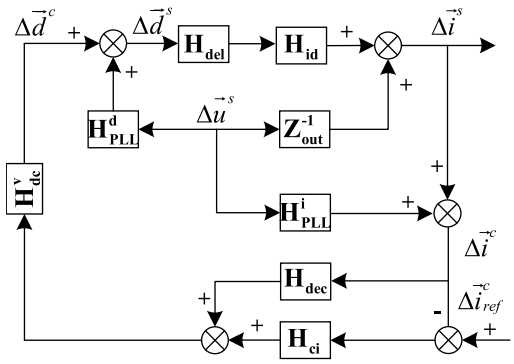


FIGURE 5. The block diagram of impedance model of the three-phase four-leg grid-connected inverter.

Similarly, in Figure 2, assuming $\Delta u_d^s = \Delta u_q^s = 0$, the transfer function matrix $\mathbf{H_{id}}$, from the small-signal perturbation from duty ratio to the corresponding current response in the system frame, can be obtained as,

$$\mathbf{H_{id}} = \begin{bmatrix} a & b & 0 \\ -b & a & 0 \\ 0 & 0 & c \end{bmatrix} \tag{21}$$

where,

$$a = \frac{-(sL_f + R_f)U_{dc}}{(sL_f + R_f)^2 + (\omega L_f)^2}$$
$$b = \frac{\omega L_f U_{dc}}{(sL_f + R_f)^2 + (\omega L_f)^2}$$
$$c = \frac{-U_{dc}}{s(3L_n + L_f) + 3R_n + R_f}$$

The block diagram of the impedance model of three-phase four-leg grid-connected inverter can be shown in Figure 5, in which $\mathbf{H_{del}}$ denotes a delay transfer matrix caused by the control delay, $\mathbf{H_{dec}}$ denotes the decoupling term matrix caused by the $d-q$ decoupling control, and $\mathbf{H_{ci}}$ denotes the current controller matrix.

$$\mathbf{H_{dec}} = \begin{bmatrix} 0 & -\omega L_f & 0 \\ \omega L_f & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{22}$$

$$\mathbf{H_{dc}} = \begin{bmatrix} 1/U_{dc} & 0 & 0 \\ 0 & 1/U_{dc} & 0 \\ 0 & 0 & 1/U_{dc} \end{bmatrix} \tag{23}$$

$$\mathbf{H_{del}} = \begin{bmatrix} \frac{1-0.75T_{del}s}{1+0.75T_{del}s} & 0 & 0 \\ 0 & \frac{1-0.75T_{del}s}{1+0.75T_{del}s} & 0 \\ 0 & 0 & \frac{1-0.75T_{del}s}{1+0.75T_{del}s} \end{bmatrix} \tag{24}$$

$$\mathbf{H_{ci}} = \begin{bmatrix} k_{dip} + \frac{k_{dii}}{s} & 0 & 0 \\ 0 & k_{qip} + \frac{k_{qii}}{s} & 0 \\ 0 & 0 & k_{0ip} + \frac{k_{0ii}}{s} \end{bmatrix} \tag{25}$$

According to Figure 5, the admittance from $\Delta\vec{i}^s$ to $\Delta\vec{u}^s$ can be expressed as,

$$\mathbf{Y_{idq0}} = \frac{\mathbf{H_{id}H_{del}H_{dc}}\left(\mathbf{H^i_{PLL}}(\mathbf{H_{dec}} - \mathbf{H_{ci}})\right)}{\mathbf{I} - \mathbf{H_{id}H_{del}} * \mathbf{H_{dc}}(\mathbf{H_{dec}} - \mathbf{H_{ci}})} + \frac{\mathbf{H_{id}H_{del}}\left(\mathbf{H^d_{PLL}} + (\mathbf{H_{id}H_{del}})^{-1}\mathbf{Z^{-1}_{out}}\right)}{\mathbf{I} - \mathbf{H_{id}H_{del}H_{dc}}(\mathbf{H_{dec}} - \mathbf{H_{ci}})} \tag{26}$$

According to the method that equivalently transforms the admittance in the dq-domain into the admittance in the sequence-domain in [28], the admittance model in sequence domain can be achieved as

$$\mathbf{Y_{ipn0}} = \mathbf{T_Z Y_{dq0} T_Z^{-1}} = \begin{bmatrix} \mathbf{Y_{ipn}} & \mathbf{0} \\ \mathbf{0} & \mathbf{Y_{i0}} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & 0 \\ Y_{21} & Y_{22} & 0 \\ 0 & 0 & Y_{33} \end{bmatrix} \tag{27}$$

$$\mathbf{T_Z} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j & 0 \\ 1 & -j & 0 \\ 0 & 0 & \sqrt{2} \end{bmatrix} \tag{28}$$

It should be noted that the elements in third column or third row in matrix $\mathbf{Y_{dq0}}$ and $\mathbf{Y_{pn0}}$ except the third element in the third column elements are zero, which means the relationship between positive-sequence admittance and zero-sequence admittance is decoupled, and the relationship between negative -sequence admittance and zero-sequence admittance is also decoupled.

III. IMPEDANCE ADMITTANCE MODEL VERIFICATION AND ZERO-SEQUENCE ADMITTANCE CHARACTERISTICS ANALYSIS

A. ADMITTANCE MODEL VERIFICATION

In order to verify the correctness of the analytical admittance model, the simulation based on MATLAB/Simulink is carried out. The simulation result of frequency scanning and the analytical model are presented in Figure 6, in which Y_{ij} denotes the i^{th} element in the j^{th} column. It can be seen that the measurement result matches the theoretical result well, which prove that the established model is accurate.

The magnitude of Y_{13}, Y_{23}, Y_{31} and Y_{32} is relatively small compared to other elements and can almost be neglected, which indicates the relationship between positive-sequence admittance and zero-sequence admittance is decoupled, and the relationship between negative-sequence admittance and zero-sequence admittance is also decoupled. It justifies the conclusion about the relationship between positive, negative and zero sequence admittance obtained in the above section, which means the zero-sequence admittance can be studied alone.

B. ZERO-SEQUENCE ADMITTANCE CHARACTERISTICS ANALYSIS

According to (27), the zero-sequence admittance is the third element in the third column elements of matrix $\mathbf{Y_{ipn0}}$, which

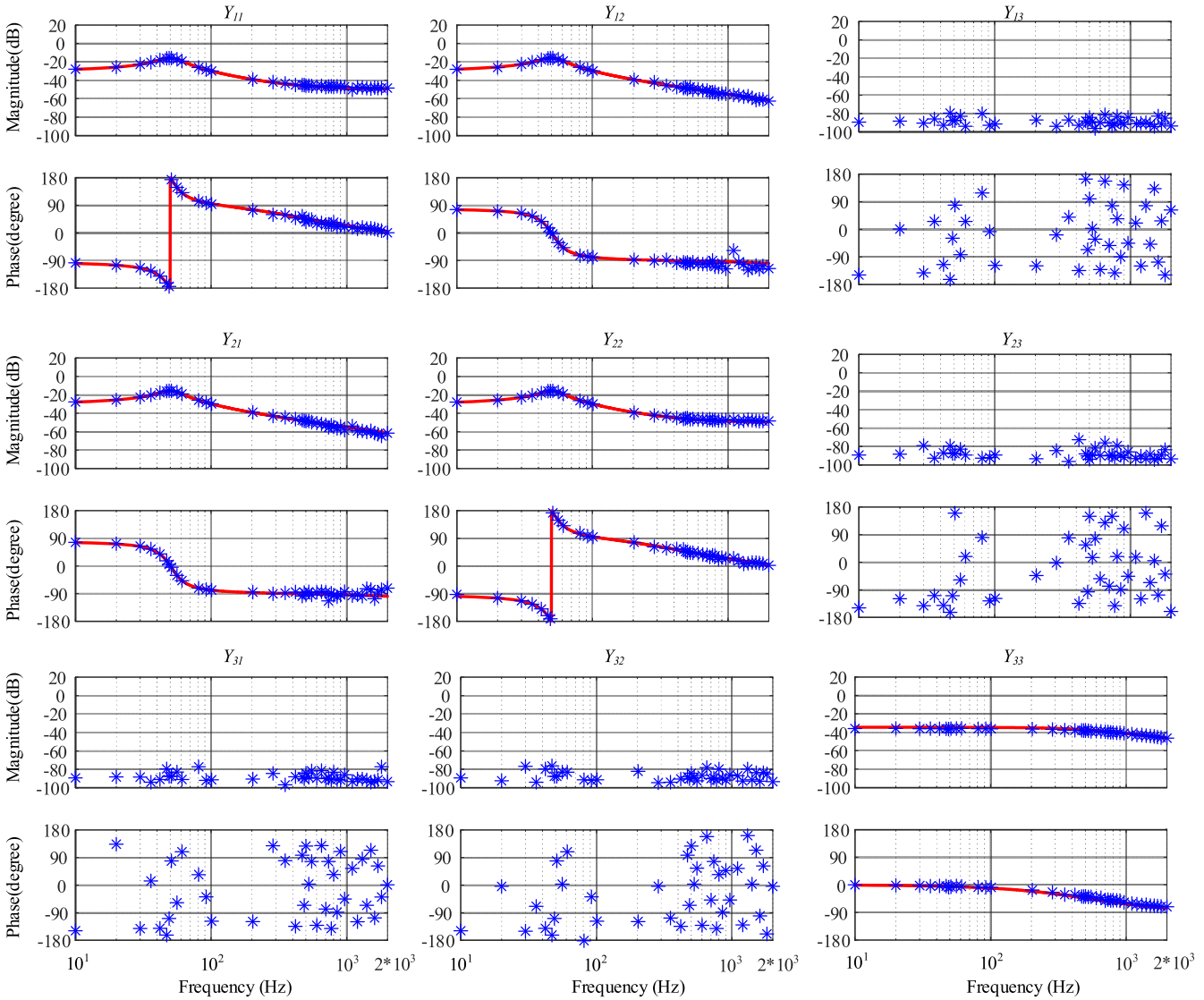


FIGURE 6. Bode diagrams of the output admittance of the inverter. (red curve denotes the model result and blue asterisk denotes the frequency scanning measurement result).

can be obtained as,

$$Y_{00} = 1/\left(s(3L_n + L_f) + 3R_n + R_f + \left(k_{0ip} + \frac{k_{0ii}}{s}\right)\right) \tag{29}$$

In (29), L_f *and* R_f respectively denote the inductance and parasitic resistance of the phase-a phase-b and phase-c, L_n *and* R_n denotes the instance and parasitic resistance respectively of the phase-n, k_{0ip}, k_{0ii} represent the proportional parameter and integral parameter of the zero-sequence current PI controller.

From (29), it can be seen that the zero-sequence admittance is relevant to the zero-sequence current PI controller parameters and *AC* side filter parameters. So it is necessary to analyze the influence of these two factors on the zero-sequence admittance.

Figure 7 shows bode diagrams of the zero-sequence admittance when the zero-axis current loop uses parameters with different current loop bandwidth. It can be seen that the zero-sequence admittance gradually transitions from resistive to inductive characteristic as the frequency increases. Compared with the red curve, the green curve has lager region with resistive characteristic. And the reason is that the bigger current loop bandwidth has stronger control ability to the zero-sequence current.

Figure 8 shows bode diagrams of the zero-sequence admittance when different ac side filter is applied. It can be seen that the zero-sequence admittance gradually transitions from resistive to inductive characteristic as the frequency increases. Compared with the red curve, the black curve has smaller region with resistive characteristic. And the reason is that the black curve corresponds to a larger AC side filter.

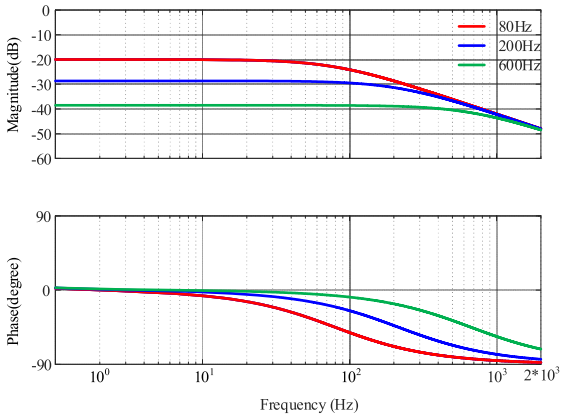


FIGURE 7. Bode diagrams of the zero-sequence admittance of the inverter when different bandwidth of the zero-axis current loop is applied.

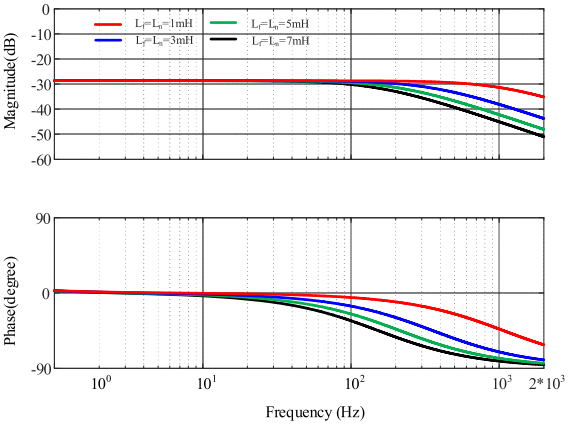


FIGURE 8. Bode diagrams of the zero-sequence admittance of the inverter when different AC side filter is applied.

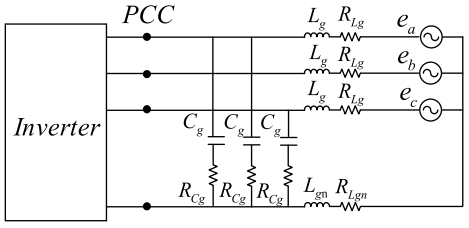


FIGURE 9. Equivalent circuit of grid impedance.

IV. STABILITY ANALYSIS AND EXPERIMENTAL VERIFICATION

A. STABILITY ANALYSIS

Based on the above analysis, the grid-connected operation stability of the three-phase four-leg grid-connected inverter will be discussed in the following. In order to investigate different impedances condition of the grid, the grid side impedance can be equivalent to the circuit in Figure 9. The impedance matrix of the grid can be achieved as,

$$\mathbf{Z_g} = \begin{bmatrix} Z_{gp} & 0 & 0 \\ 0 & Z_{gn} & 0 \\ 0 & 0 & Z_{g0} \end{bmatrix} = \begin{bmatrix} \mathbf{Z_{gpn}} & \mathbf{0} \\ \mathbf{0} & \mathbf{Z_{g0}} \end{bmatrix} \tag{30}$$

where,

$$Z_{gp} = Z_{gn} = \frac{\left(sL_g + R_{Lg}\right)\left(sC_gR_{Cg} + 1\right)}{R_{Cg}\left(sL_g + R_{Lg}\right) + sC_gR_{Cg} + 1}$$

$$Z_{g0} = \frac{\left(1 + \mathrm{s}C_gR_{Cg}\right)\left(s\left(L_g + 3L_{gn}\right) + R_{Lg} + 3R_{Lgn}\right)}{\mathrm{s}C_g\left(s\left(L_a + 3L_{gn}\right) + R_{Lg} + 3R_{Lgn}\right) + 1 + \mathrm{s}C_gR_{Cg}}$$

To analyze the system stability, the generalized Nyquist criterion is applied to the Nyquist plot of the eigenvalues of $\mathbf{Y_{ipn0}} * \mathbf{Z_g}$, where the impedance ratio matrix can be written as,

$$\mathbf{L} = \mathbf{Y_{ipn0}} * \mathbf{Z_g} = \begin{bmatrix} \mathbf{Y_{ipn}Z_{gpn}} & \mathbf{0} \\ \mathbf{0} & \mathbf{Y_{i0}Z_{g0}} \end{bmatrix} \tag{31}$$

From (31), due to the decoupled relationship between the positive-sequence admittance, negative-sequence admittance and zero-sequence admittance. The stability of the system is decided by the positive negative sequence sub system and the zero-sequence sub system, and the stability of these two sub systems can be analyzed respectively.

To analyze the zero-sequence sub system stability, the product of the zero-sequence admittance of inverter and the zero-sequence impedance of grid according to (30) and (29) can be achieved as,

$$\begin{aligned} L_0 &= Y_{i0} * Z_{g0} \\ &= \frac{\left(1+\mathrm{s}C_gR_{Cg}\right)\left(s\left(L_g+3L_{gn}\right)+R_{Lg}+3R_{Lgn}\right)}{s^2\left(L_g+3L_{gn}\right)C_g+\left(R_{Lg}C_g+3R_{Lgn}C_g+C_gR_{Cg}\right)s+1} \\ &\quad \times \frac{s}{s^2(3L_n+L_f)+\left(3R_n+R_f+k_{0ip}\right)s+k_{0ii}} \end{aligned} \tag{32}$$

The eigenvalue of L_0 can be expressed as,

$$l_1 = \frac{-\left(3R_n+R_f+k_{0ip}\right)}{2\left(3L_n+L_f\right)} \frac{\sqrt{\left(3R_n+R_f+k_{0ip}\right)^2-4(3L_n+L_f)k_{0ii}}}{2\left(3L_n+L_f\right)} \tag{33}$$

$$l_2 = \frac{-\left(3R_n+R_f+k_{0ip}\right)}{2\left(3L_n+L_f\right)} \frac{-\sqrt{\left(3R_n+R_f+k_{0ip}\right)^2-4(3L_n+L_f)k_{0ii}}}{2\left(3L_n+L_f\right)} \tag{34}$$

$$l_3 = -\frac{\left(R_{Lg}C_g+3R_{Lgn}C_g+C_gR_{Cg}\right)}{2\left(L_{ga}+3L_{gn}\right)C_g} - \frac{\sqrt{\left(R_{Lg}C_g+3R_{Lgn}C_g+C_gR_{Cg}\right)^2-4\left(L_g+3L_{gn}\right)C_g}}{2\left(L_{ga}+3L_{gn}\right)C_g} \tag{35}$$

By analyzing these formulas, it can be found that the real of l_1, l_2, l_3, l_4 are all less than zero, which indicate that the zero-sequence components will not result in stability problems in low frequency region. However, as the frequency increases, the impedance characteristics of the inverter are

mainly inductive, which may cause high frequency resonance when the grid impedance is capacitive.

$$l_4 = -\frac{\left(R_{Lg}C_g + 3R_{Lgn}C_g + C_gR_{Cg}\right)}{2\left(L_g + 3L_{gn}\right)C_g} - \frac{\sqrt{\left(R_{Lg}C_g + 3R_{Lgn}C_g + C_gR_{Cg}\right)^2 - 4\left(L_g + 3L_{gn}\right)C_g}}{2\left(L_g + 3L_{gn}\right)C_g} \tag{36}$$

To analyze the positive negative-sequence sub system, the eigenvalues of $\mathbf{Y_{ipn}}$ * $\mathbf{Z_{gpn}}$ should be studied. Many stability analyses of three-phase three-wire grid connected inverter based on positive and negative sequence admittance have been obtained and the conclusions about positive and negative sequence admittance are the same as the conclusions of this paper. To avoid repetitive discussion of the same content, detailed analysis will not be presented in this article.

FIGURE 10. Hardware platform of CHIL experiment.

To further verify the proposed conclusion, the hardware platform is established based on Control-hardware-in-loop (CHIL) as shown in Figure 10. The model of four-leg Grid-connected system is developed in Typhoon 602+ with the time step of 1 μs. And the controllers of DFIG are implemented in a TMS320F28335/Spartan6 XC6SLX16 DSP+FPGA control board. Applying the CHIL to analyze the stability of megawatt DFIG-grid interconnected system has been proposed in [29]–[31]. The parameters of the system are listed in Table 1 and Table 2 in section APPENDIX. In order to ensure one sub-system stable when analyzing another sub-system different grid parameter are used.

B. OCCURRENCE OF INSTABILITY IN THE POSITIVE NEGATIVE-SEQUENCE SUB SYSTEM

Figure 11 shows the characteristic root locus of $\mathbf{Y_{invpn}} \cdot \mathbf{Z_{gpn}}$, when the PLL using different parameters and the other parameters are listed in Appendix Table 2. Figure 11(a) shows the characteristic root locus of $\mathbf{Y_{invpn}} \cdot \mathbf{Z_{gpn}}$ without bypassing the point $(-1,0)$ when the proportional gain of PLL (k_{pp}) is 0.158, which means the positive-negative-sequence sub system is stable. Figure 11(b) shows the characteristic root locus of $\mathbf{Y_{invpn}} \cdot \mathbf{Z_{gpn}}$ when the proportional gain of PLL (k_{pp}) is 3.15. It can be seen from Figure 11(b) that the characteristic

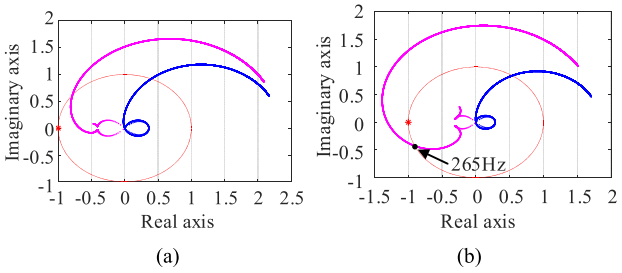


FIGURE 11. Characteristic root locus of $\mathbf{Y_{invpn}} \cdot \mathbf{Z_{gpn}}$. (a) when proportional gain of PLL (k_{pp}) is 0.158; (b) when proportional gain of PLL (k_{pp}) is 3.15.

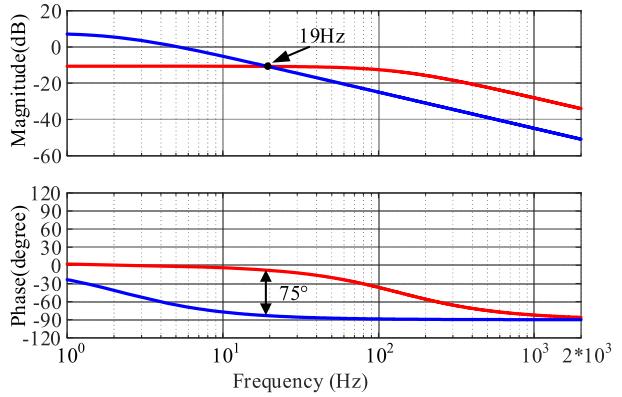


FIGURE 12. Bode diagrams of the zero-sequence admittances of the inverter and the grid (red curve denotes the zero-sequence admittances of the inverter and blue curve denotes zero-sequence admittances of the grid).

root locus Bypass the point $(-1,0)$, and the corresponding frequency through the unit circle is 165Hz. Therefore, according to the stability criterion, the positive negative sequence-sub system is unstable and will produce harmonic band at 165Hz and 265Hz due to the frequency coupling effect.

Figure12 shows the bode diagrams of the zero-sequence admittances of the inverter and the zero-sequence impedance of the grid. From Figure 12, the zero-sequence sub system has a large stability margin and has no stability problems caused by the zero-sequence impedance.

Figure 13 shows the voltage wave and current waveform at PCC where the proportional gain of PLL (k_{pp}) stepping from 0.158 to 3.15, the grid-connected phase currents gradually diverge, which indicates that the system is unstable. The FFT analysis of i_a, when $k_{pp} = 3.15$, is shown in Figure14, which reveals that there are considerable harmonic band at 165 Hz and 265 Hz in the phase currents. From Figure 14 it also can been seen that the zero-sequence current (i_0) is table, which means the instability of the positive and negative sequence loop will not affect the stability of the zero-sequence loop. The corresponding experiment parameters are listed in Appendix Table 2.

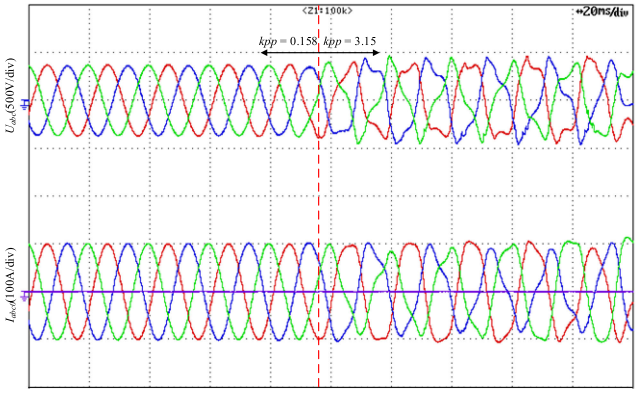


FIGURE 13. Time domain waveform of voltages and currents.

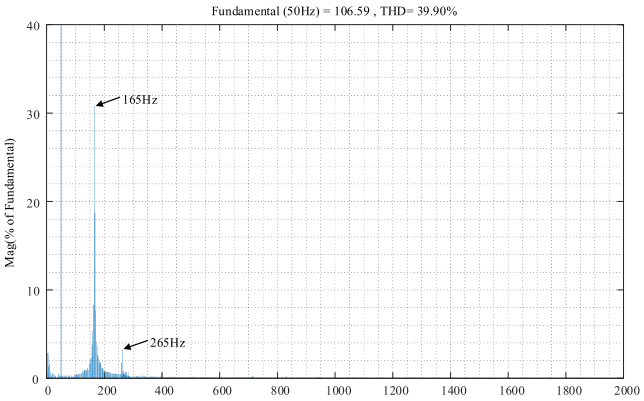


FIGURE 14. FFT analysis of the phase-a current (i_a).

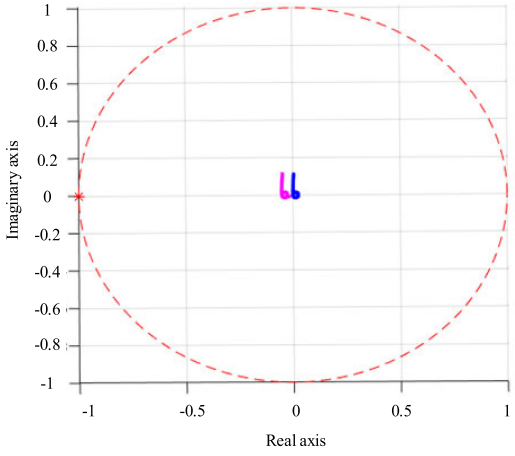
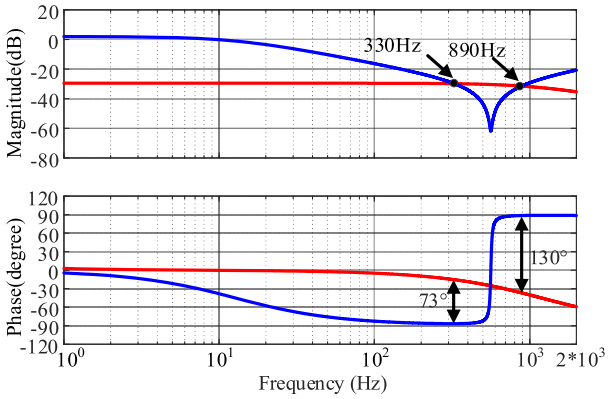


FIGURE 15. Characteristic root locus of $Y_{invpn} \cdot Z_{gpn}$.

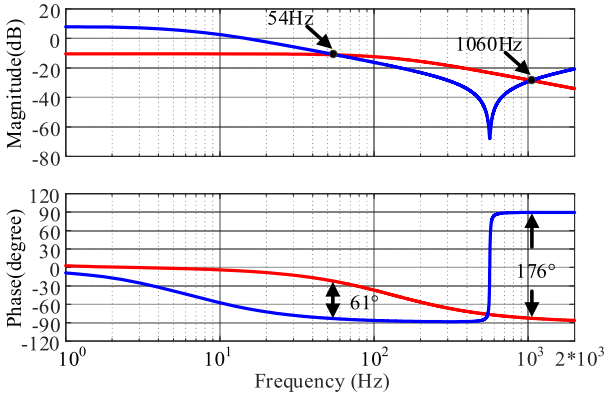
C. OCCURRENCE OF INSTABILITY IN THE ZERO-SEQUENCE SUB SYSTEM

Figure 15 shows the characteristic root locus of $\mathbf{Y_{invpn}} * \mathbf{Z_{gpn}}$, without bypassing the point (−1,0), which means the positive negative-sequence sub system is stable. The corresponding experiment parameters are listed in Appendix Table 3.

Figure 16 shows the bode diagrams of the zero-sequence admittances of the inverter and the zero-sequence admittances of the grid when the proportional gain of zero-axis current controller using different parameters and the other parameters are listed in Appendix Table 3. Figure 16(a) shows that the zero-sequence sub system has a large stability margin and has no stability problems caused by the zero-sequence impedance components when the proportional gain of zero-axis current controller (k_{0p}) is 30. From Figure 16(b), the magnitude of zero-sequence admittances of the inverter and grid intersect at 1060Hz and the phase difference is closed to 180°, which cause the system to oscillate at this



(a) when the proportional gain of zero-axis current controller(k_{0p}) is 30



(b) when the proportional gain of zero-axis current controller(k_{0p}) is 6

FIGURE 16. Bode diagrams of the zero-sequence admittances of the inverter and the grid (red curve denotes the zero-sequence admittances of the inverter and blue curve denotes zero-sequence admittances of the grid).

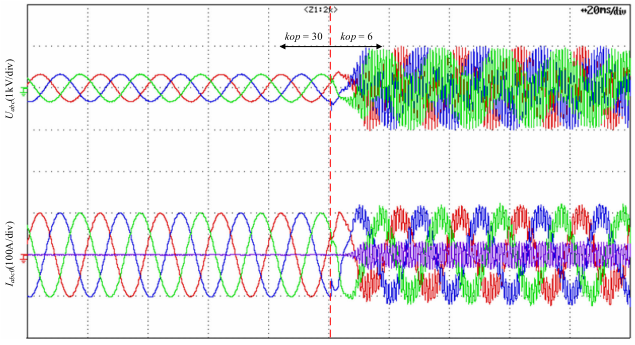


FIGURE 17. Time domain waveform of voltages and currents.

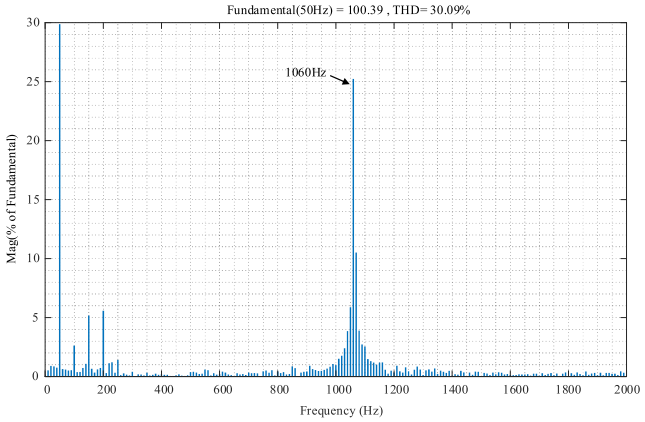


FIGURE 18. FFT analysis of the phase-a current(i_a).

TABLE 1. Iamplitude and phase of 1060Hz harmonic component in i_a, i_b, i_c and i_0.

Phase current	Magnitude(A)	Phase(°)
i_a	24.6	12.7
i_b	24.6	12.9
i_c	24.6	12.6
i_0	24.6	12.8

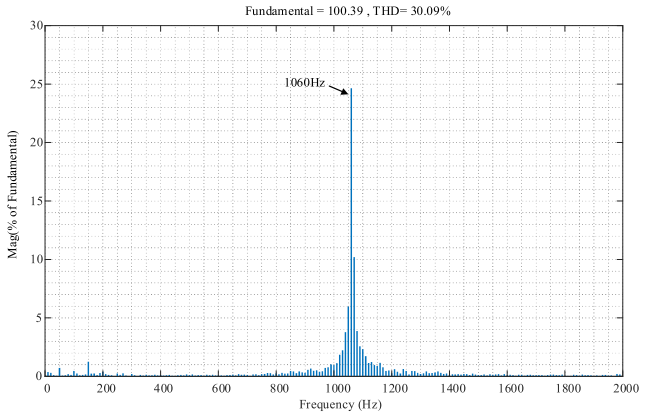


FIGURE 19. FFT analysis of the zero-sequence current(i_0).

frequency when the proportional gain of zero-axis current controller (k_{0p}) is 6.

Figure 17 shows the voltage wave and current waveform at PCC, where the proportional gain of zero-axis (k_{0p}) current controller stepping from 30 to 6 and the corresponding experiment parameters are listed in Appendix Table 3.

From Figure 17, high frequency oscillation occurs on the phase currents when k_{0p} is 6. The FFT analysis of i_a is shown in Figure 18, which reveals that there are considerable harmonic components at 1060Hz. Figure 19 shows the FFT analysis of zero-sequence current (i_0), and the frequency spectrum of i_0 is almost same with that of i_a in Figure 18. Table 1 shows the amplitude and phase of 1060Hz harmonic

TABLE 2. Experiment parameters when occurrence of instability in the positive negative sequence sub system.

Symbol	Parameter	Value
U_s	Rated voltage	380 V
P_s	Rated power	30kW
f_1	Fundamental frequency	50 Hz
f_s	Switching frequency	10 kHz
V_{dc}	Dc-link voltage	700 V
L_f	Filter inductance	1 mH
R_{Lf}	parasitic resistance of filter inductance	0.2Ω
L_g	Grid inductance	7 mH
R_{Lga}	parasitic resistance of Grid inductance	0.2Ω
k_{pi}	Integral gain of PLL controller	4.96
k_{dip}	Proportional gain of d-axis current controller	10
k_{dii}	Integral gain of d-axis current controller	180
k_{qip}	Proportional gain of q-axis current controller	10
k_{qii}	Integral gain of q-axis current controller	180
k_{0ip}	Proportional gain of zero-axis current controller	6
k_{0ii}	Integral gain of zero-axis current controller	2
SCR	Short circuit ratio	2.1

component in i_a, i_b, i_c and i_0, which means the 1060Hz oscillation is generated by the zero-sequence subsystem. From Figure 17, it also can be seen that the positive negative-sequence sub system is still stable, which means the instability of zero-sequence loop will not affect the stability of positive and negative sequence loop.

V. CONCLUSION

This paper analyzes the impedance characteristics of Three-phase Four-leg Grid-connected Inverter Considering Zero-sequence. The specific contribution of this paper can be concluded as follows:

1) An impedance model including positive-sequence, negative-sequence and zero-sequence impedance of the three-phase four-leg grid-connected inverter is established.

2) The paper reveals the relationship between zero-sequence impedance and positive-sequence, negative-sequence impedance is decupled.

3) The grid-connected operation stability of the three-phase four-leg grid-connected inverter have been discussed in the paper, which indicates that instability caused by the positive-sequence impedance or negative-sequence impedance and the instability caused by the zero-sequence impedance can be analyzed independently.

For the zero-sequence high-frequency oscillation problem mentioned in the paper, the solutions to this problem are not studied. Therefore, our next step will focus on the

TABLE 3. Experiment parameters when occurrence of instability in the zero-sequence sub system.

Symbol	Parameter	Value
U_s	Rated voltage	380 V
P_s	Rated power	30kW
f_1	Fundamental frequency	50 Hz
f_s	Switching frequency	10 kHz
V_{dc}	Dc-link voltage	700 V
L_f	Filter inductance	1 mH
R_{Lf}	parasitic resistance of filter inductance	0.2Ω
L_g	Grid inductance	2.5 mH
R_{Lga}	parasitic resistance of Grid inductance	0.2Ω
C_g	Grid capacitance	7.5uF
R_{Cg}	parasitic resistance of Grid capacitance	0.2Ω
k_{pp}	Proportional gain of PLL controller	3.15
k_{pi}	Integral gain of PLL controller	4.96
k_{dip}	Proportional gain of d-axis current controller	10
k_{dii}	Integral gain of d-axis current controller	180
k_{qip}	Proportional gain of q-axis current controller	10
k_{qii}	Integral gain of q-axis current controller	180
k_{0ip}	Proportional gain of zero-axis current controller	6
k_{0ii}	Integral gain of zero-axis current controller	2
SCR	Short circuit ratio	6

zero-sequence oscillation problem in the three-phase four-wire system.

APPENDIX

A. PARAMETERS OF SYSTEM

The parameters of the three-phase four-leg Grid-connected system sending terminal system are shown in Table 2 and Table 3.

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