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A Simple Space Vector Modulation Method With DC-Link Voltage Balancing and Reduced Common-Mode Voltage Strategy for a Three-Level T-Type Quasi-Z Source Inverter

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ABSTRACT Single-stage converters based on an impedance source (IS) network merged with a multilevel inverter remain a trending research topic, from both the topological and control perspectives, because of their potential in applications involving renewable energy. This paper presents a new, simplified space vector pulse-width modulation (SVPWM) for a three-phase three-level T-type quasi-impedance source inverter (3L-T-type qZSI). The benefits of the proposed modulation strategy include functionalities, such as boosting the input voltage and controlling the neutral-point (NP) voltage using the redundant small vectors, to mitigate the inner capacitors voltages imbalance. The proposed SVPWM guarantees a minimum common-mode voltage while preserving a very simple implementation, thus reducing the complex computations and cascaded proportional-integral (PI) control loops of the conventional SVPWM methods. The proposed algorithm can be applied to different multilevel inverter configurations combined with an IS network. A comprehensive simulation study and experimental results demonstrated the good performance of the proposed control method for dynamic response and imbalance conditions.

INDEX TERMS Space vector modulation (SVM), 3-level T-type inverter, impedance source (IS) network.

I. INTRODUCTION

Transformerless grid-connected inverters offer lower cost, smaller size and higher efficiency than inverters, including those with galvanic isolation. However, the mitigation of leakage currents is a large concern for a friendly grid integration of this family of inverters [1]–[4]. Solutions based on particular converter topologies, additional passive elements or advanced control techniques have been widely explored [3]–[7].

Multilevel single-stage configurations are considered suitable for connecting low-voltage applications such as renewable energy systems and medium-voltage AC-drives [8].

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Control algorithms for multilevel converters are primarily based on pulse-width modulation (PWM) techniques [9], [10]. Many PWM methods have been developed for multilevel converters, most of them can be classified into two large families: (a) carrier-based PWM modulation and (b) space-vector modulation (SVM). The first family includes carrier-based modulation techniques as level-shifted (LS) PWM, phase-shifted (PS) PWM, phase-disposition (PD) PWM or preprogrammed PWM modulation. All of them use high-frequency carrier waveforms, usually triangular, compared to the reference voltage to generate phase voltages. Output signal spectra contain harmonics related to the frequency modulation index, which must be filtered in power conversion applications [9]. The SVM method uses a vectorial representation of the voltage source inverters (VSIs) switching states, considering the modulations as an optimization of

a geometrical problem. The method determines a sequence of switching states and duty cycles, which are optimal for each reference voltage. The commutation states are determined for all phases, being a technique applicable to multiphase converters. SVM provides more flexibility regarding the redundant converter switching states, which can be used to compensate other variables such as common-mode voltages and neutral-point voltage balance [11]–[13].

An interesting multilevel single-stage configuration is the combination of a three-level T-type converter with an impedance-source (IS) network. The T-type converter has the merits of low components count, high efficiency, simple structure and reduced conduction losses [14], [15]. Regarding an IS network, the Z-source inverter was proposed in [16] as a novel single-stage solution. Since then, many other IS networks have been proposed as a further concept derivation. These solutions have overcome the limitation of the conventional inverters: they have a buck, a boost mode and do not suffer from shoot-through (ST) states. This boosting technique may enhance the inverter reliability in advance. References [17]–[20] present a good overview of the existing solutions. Over the years, IS networks have been verified in several applications [21]–[23]. In addition, several studies are devoted to IS use in the multilevel inverters [24]–[28]. It has all the inherent benefits of multilevel inverter use [29]. In advance, as shown in [30], IS networks, despite having more components, have no redundancy in terms of the overall size of passive components.

Fig. 1 shows several examples of IS networks suitable for 3-Level (3L) application. Fig. 1a shows that using two input voltage sources and a conventional Z-source (ZS) network, the 3L inverter can be configured, while Fig. 1b shows how to realize the two input voltage sources using a double ZS network. Despite the larger number of components, the overall size of the ZS network is expected to be the same because of the split voltage stress across the diode and passive components [30]. Fig. 1c shows how to use the LCCT Z-source network [31] for 3L application. A more detailed topological deviation of 3L LCCT solutions is addressed in [32]. Fig. 1d shows how to simplify this network using only one diode and only one input voltage source. Finally, Fig. 1d shows the symmetrical qZS network that has one input voltage source and middle point for neutral connection. Based on the concept illustrated in Fig. 1, almost any IS network can be adopted for a multilevel application, as shown for the qZS network and 3L-T-type branch (Fig.1e). Despite the remarkable number of studies dedicated to multilevel IS-based solutions, only a few of them discuss suitable modulation techniques in detail [14], [15], [33]–[35], particularly for leakage current mitigation.

An impedance source network stage with the 3L T-type inverter incorporates the continuous input current condition and the shoot-through immunity [36], [37]. Nevertheless, particular issues related to this topology arise, such as balancing the neutral point voltage, reducing the common-mode voltage (CMV) and obtaining sinusoidal current shaping in the output of the converter, which have imposed challenging tasks on the design of modulation techniques for the qZS T-type inverter.

Sinusoidal PWM has been applied in [33] for neutral point voltage control but neglecting CMV reduction. In [38], converter failure mode is included in the control algorithm. Improved SVPWM algorithms have been applied to transformerless 3L inverters in the literature incorporating capabilities regarding leakage currents [4], [5]. In [14] and [15], a modulation combining large, medium and small voltage vectors is applied to reduce the CMV, considering also zero vector and shoot-through time to balance the entire system. However, the numerical implementation of this technique is complex and no neutral point (NP) control is conducted. In [34], neutral point voltage is regulated, but it lacks the control of the CMV. An SVPWM algorithm, including the impedance source shoot-through state for three-level converters, was developed in [39]. In [40], neutral point voltage control is addressed and in [41], the PWM algorithm considers a common-mode voltage reduction that is directly associated with leakage currents, being an important variable in transformerless inverters.

Therefore, motivated by the aforementioned issues in existing SVPWM algorithms and based on preliminary work [42], this paper presents a simplified SVPWM algorithm incorporating NP voltage control and CMV reduction. This algorithm uses specific small vectors in the modulation to reduce naturally CMV values and includes internal capacitors balancing. Moreover, in this work the method is implemented for a 3L qZS T-type inverter, but it is also adapted for any other 3L-based inverter.

The structure of this paper is as follows: Section II describes in detail the conventional SVPWM modulation technique and the proposed technique. Section III presents the simulation results for different operation modes, which are verified experimentally in Section IV. Finally, conclusions are drawn in Section V.

II. MODULATION TECHNIQUES FOR A 3L-T-TYPE QZSI

A. THE BACKGROUND OF SVPWM ALGORITHM

The SVPWM strategy is, in essence, a variation of the PWM strategy. The former strategy computes the switching times based on the three-phase space vector representation of the reference voltage signal jointly with the available inverter switching states. Nevertheless, the latter strategy uses the per-phase amplitude in the time representation of the reference voltage signal, usually to be compared with a carrier.

In particular, for a 3L inverter with branch voltages $+v_{DC}/2$, 0 and $-v_{DC}/2$, 27 switching states are available because of the three-phase configuration. The main purpose will be to determine the three space vectors, their duty cycles or switching times and the sequence in which they will be generated to approximate the reference voltage vector ($\mathbf{V_{ref}}$) over the modulation period. Usually, the space vectors and switching times are calculated by using geometrical-based operations by projecting the reference space vector over the

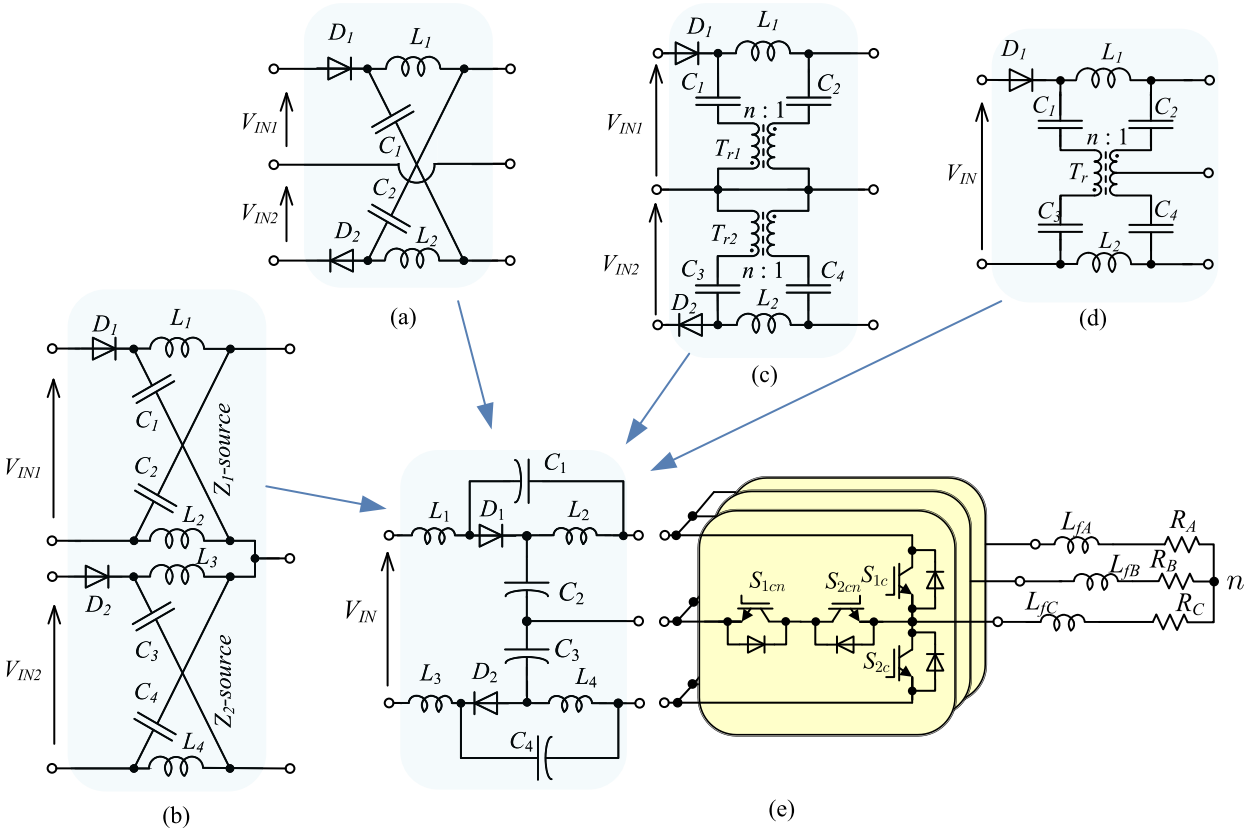

FIGURE 1. Example of IS networks for 3L configuration.

triangle formed by the nearest voltage space vectors available in the inverter at a certain moment [43].

The instantaneous three-phase voltages ($v_{\mathrm{AN}}(t)$, $v_{\mathrm{BN}}(t)$ and $v_{\mathrm{CN}}(t)$) can be defined in the complex plane by using the space vector transformation (1):

$$\mathbf{v(t)} = \frac{2}{3}(v_{\mathrm{AN}}(t) + v_{\mathrm{BN}}(t)e^{j\frac{2}{3}\pi} + v_{\mathrm{CN}}(t)e^{-j\frac{2}{3}\pi}) \qquad (1)$$

where $\mathbf{v(t)}$ is the voltage space vector. Fig. 2 shows the 27 space vectors and the corresponding 19 values of vectors ($\mathbf{V_{0-18}}$, as the remaining space vectors are considered redundant states), together with the division into six sectors (with a triangular shape). In addition, each sector is further divided into four smaller triangular regions.

At the same time, all vectors are divided into four groups: zero, small, medium and large vectors (i.e., [PPP], [POO], [PON], and [PNN], respectively).

To illustrate the operation principle of a conventional SVPWM, let us assume that $\mathbf{V_{ref}}$ is located in region 4 of sector 1, as shown in Fig. 2 in blue. The corresponding nearest three space vectors are ($\mathbf{V_2}$) (small: [PPO], [OON]), ($\mathbf{V_7}$) (medium: [PON]), and ($\mathbf{V_{14}}$) (large: [PPN]). The switching times in each branch are determined by using the volt-second balance equation (2):

$$\mathbf{V_{ref}} \cdot \mathrm{T}_s = \mathbf{V_2} \cdot \mathrm{T_{SV}} + \mathbf{V_7} \cdot \mathrm{T_{MV}} + \mathbf{V_{14}} \cdot \mathrm{T_{LV}} \qquad (2)$$

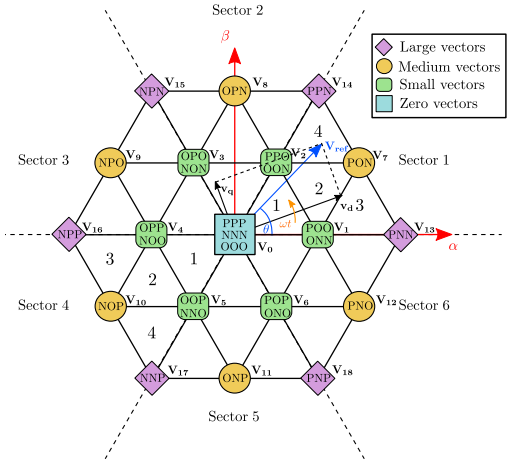

FIGURE 2. Space vector representation in a 3L inverter with divisions in sectors and regions.

with (3)

$$\mathrm{T}_s = \mathrm{T_{SV}} + \mathrm{T_{MV}} + \mathrm{T_{LV}} \qquad (3)$$

$\mathrm{T_{SV}}$,$\mathrm{T_{MV}}$ and $\mathrm{T_{LV}}$ correspond to the dwelling times of the small vector ($\mathbf{V_2}$), the medium vector ($\mathbf{V_7}$) and the large vector ($\mathbf{V_{14}}$), respectively. Assuming that $\mathbf{V_{ref}}$ is known and coming from the control strategy of the inverter, and T_s, $\mathbf{V_2}$, $\mathbf{V_7}$ and $\mathbf{V_{14}}$ and splitting (2) into a real and an imaginary part,

TABLE 1. CMV and classification of vectors in 3L-T-type qZSI. (P = Positive, N = Negative, O = Zero, F_{ST} = Full Shoot-Through).

Type vector	Vector	CMV
Large ($\mathbf{V}_{LV}$)	PPN, NPP,PNP	$-\frac{v_{DC}}{6}$
	PPN, NPP, PNP	$\frac{v_{DC}}{6}$
Medium ($\mathbf{V}_{MV}$)	PON,OPN,NPO NOP,OPN,PNO	0
Small ($\mathbf{V}_{SV}$)	ONN,NON,NNO	$-\frac{v_{DC}}{3}$
	OON, NOO,ONO	$-\frac{v_{DC}}{6}$
	POO,OPO,OOP	$\frac{v_{DC}}{6}$
	PPO,OPP,POP	$\frac{v_{DC}}{3}$
Zero ($\mathbf{V}_{ZV}$)	NNN	$-\frac{v_{DC}}{2}$
	OOO	0
	PPP	$\frac{v_{DC}}{2}$
Shoot-through ($\mathbf{V}_{ST}$)	F_{ST}OO,OF_{ST}O,OOF_{ST}	0

each individual dwelling time can be solved as (4):

$$\begin{aligned} T_{SV} &= T_s\left[2 - 2\cdot m\cdot \sin\left(\frac{\pi}{3}+\theta\right)\right] \\ T_{MV} &= T_s\left[2\cdot m\cdot \sin\left(\frac{\pi}{3}-\theta\right)\right] \\ T_{LV} &= T_s\left[2\cdot m\cdot \sin(\theta) - 1\right] \end{aligned} \tag{4}$$

where m represents the modulation index and is equal to $(\sqrt{3}V_{ref}/v_{DC})$ and θ is the phase angle of $\mathbf{V_{ref}}$.

B. PROPOSED MODULATION TECHNIQUE

The proposed algorithm SVPWM consists of a hybrid vector modulation that can address the application or neglect of the small vectors to perform an imbalance compensation voltage of the inner capacitors.

Our developed approach takes the basis proposed in [15] in the sense that a simple SVPWM for the same topology can be found in that work. Nevertheless, the proposed strategy adds functionalities, including the internal capacitors balancing and reducing the CMV. Using an impedance network adds the state of shoot-through (ST) that is inserted in the zero-vectors dwelling times without modifying the average volt-second equation. Furthermore, the modulation limits the common-mode voltage when only applying the blue vectors from Table 1, because they are associated with the lower CMV values (0 or $\frac{v_{DC}}{6}$). Because of this functionality, some benefits are derived as reduced leakage current. However, because the ST state is also applied during the zero vectors intervals, the priority of the modulation is given to this ST state over imbalance compensation.

For the proposed algorithm, the sector definition is shown in Fig. 3; where each sector is composed of LMZ (large, medium, zero) vectors with an angle of $\pi/6$. Analyzing all the sectors, an identical sequence of vectors can be identified between the odd sectors (1, 3, 5, 7, 9, 11) and the even sectors (2, 4, 6, 8, 10, 12), as detailed in the zoomed view in Fig. 4.

As an example, the reference vector $\mathbf{V_{ref}}$ is located in Sector 1 in Fig. 3 and its corresponding volt-second balance equation for SVPWM LMZ with ST is expressed by (5).

$$\mathbf{V_{ref}}\cdot T_s = \mathbf{V}_{LV}\cdot t_{LV} + \mathbf{V}_{MV}\cdot t_{MV} + \mathbf{V}_{ZV}\cdot t_{ZV} + \mathbf{V}_{ST}\cdot t_{ST} \tag{5}$$

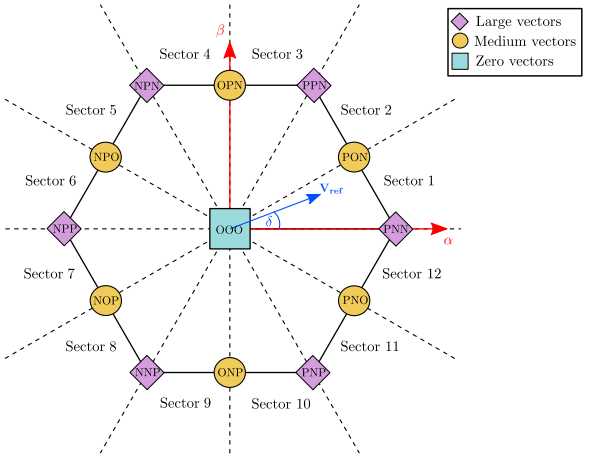

FIGURE 3. Sector divisions in the SVPWM LMZ [15].

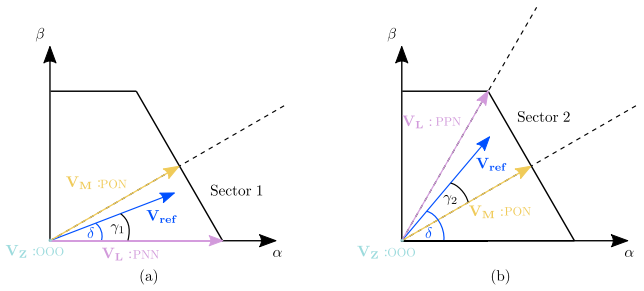

FIGURE 4. (a) Even sector (example sector 1); (b) Odd sector (example sector 2).

with

$$T_s = t_{LV} + t_{MV} + t_{ZV} + t_{ST} \tag{6}$$

where $\mathbf{V}_{LV}$, $\mathbf{V}_{MV}$ and $\mathbf{V}_{ZV}$ are the large, middle and zero vectors of each sector respectively, and $\mathbf{V}_{ST}$ is the applied shoot-through vector. t_{LV}, t_{MV}, t_{ZV} and t_{ST} are the dwelling times of the large, medium, zero and ST vectors, respectively. To generate the reference voltage in the odd sectors, the LMZ vectors nearest the reference vector are used. For example, in sector 1, the vectors PNN, PON and OOO are used, and the F_{ST}OO vector is applied for the ST state. The sequence of vectors in this sector is shown in Fig. 5 (b). To calculate the dwelling times, γ_i, which is the angle within the sector under study, is defined as:

$$\gamma_i = \delta - (i-1)\cdot\frac{\pi}{6} \tag{7}$$

where δ is the angle of the vector $\mathbf{V_{ref}}$, and i is the sector number with $i \in \{1, 2, \ldots, 12\}$. The value of the large, medium, zero and ST vectors is given by:

$$\mathbf{V}_{LV} = \frac{2}{3}V_{in}\cdot B \tag{8}$$

$$\mathbf{V}_{MV} = \frac{\sqrt{3}}{3}V_{in}\cdot B\cdot e^{j\frac{\pi}{6}} \tag{9}$$

$$\mathbf{V}_{ZV} = 0 \tag{10}$$

$$\mathbf{V}_{ST} = 0 \tag{11}$$

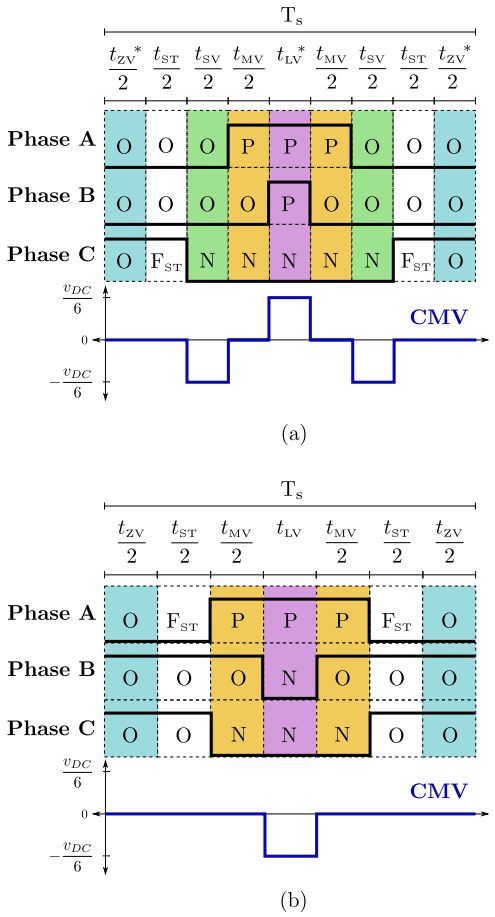

FIGURE 5. The switching sequence of the proposed SVPWM at $V_{C_3} > V_{C_2}$ at: (a) Sector 2, and (b) Sector 1.

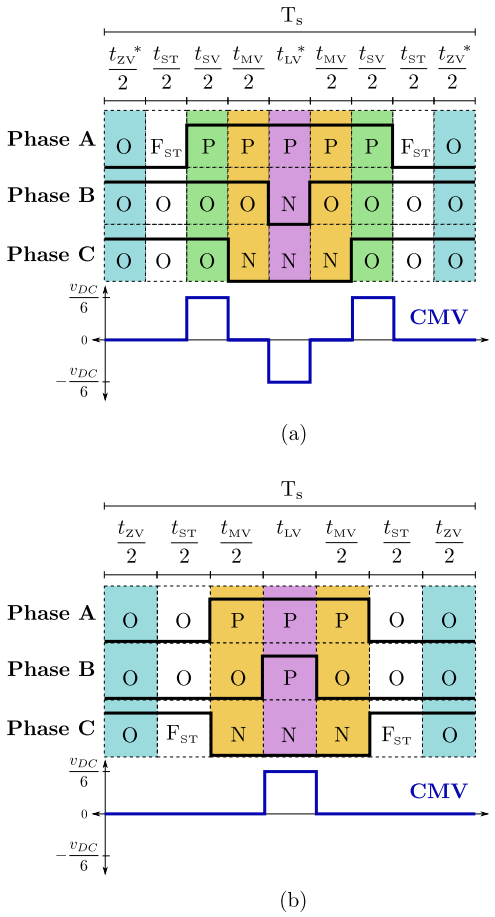

FIGURE 6. Switching sequence of the proposed SVPWM at $V_{C_2} > V_{C_3}$ at: (a) Sector 1, and (b) Sector 2.

where V_{in} is the input voltage to the impedance network and B is the boost factor, $B = 1/(1 - 2\,D_s)$. As expected, $\mathbf{V}_{\text{ZV}}$ and $\mathbf{V}_{\text{ST}}$ are null because they generate zero voltage. Then, with these values and Eqs. (5) and (6), the dwelling times in the case of odd sectors can be expressed as:

$$t_{\text{ST}} = D_s \cdot \text{T}_\text{s} \tag{12}$$
$$t_{\text{LV}} = \sqrt{3} m \text{T}_\text{s} \sin\left(\frac{\pi}{6} - \gamma_n\right) \tag{13}$$
$$t_{\text{MV}} = 2m\text{T}_\text{s}\sin(\gamma_n) \tag{14}$$
$$t_{\text{ZV}} = \text{T}_\text{s} - (t_{\text{ST}} + t_{\text{LV}} + t_{\text{MV}}) \tag{15}$$

where n is the odd sector number, $n \in \{1, 3, 5, 7, 9, 11\}$, D_s is the shoot-through duty cycle and T_s is the switching period. The modulation index m is defined as:

$$m = \frac{\sqrt{3} \cdot ||\mathbf{V_{ref}}||}{V_{\text{in}} \cdot B} = \frac{\sqrt{3} \cdot ||\mathbf{V_{ref}}||}{V_{\text{in}}} \cdot (1 - 2D_s) \tag{16}$$

In the case of even sectors, sector 2 is taken as an example, as shown in Fig. 4 (b), which uses the PON, PPN and OOO vectors, and the OOF_{ST} vector for the ST state. The sequence of vectors in this sector is shown in Fig. 6 (b). In this case, the value of the different vectors is:

$$\mathbf{V}_{\text{LV}} = \frac{2}{3} V_{\text{in}} \cdot B \cdot e^{j\frac{\pi}{6}} \tag{17}$$

$$\mathbf{V}_{\text{MV}} = \frac{\sqrt{3}}{3} V_{\text{in}} \cdot B \tag{18}$$
$$\mathbf{V}_{\text{ZV}} = 0 \tag{19}$$
$$\mathbf{V}_{\text{ST}} = 0 \tag{20}$$

and the dwelling times for even sectors are:

$$t_{\text{ST}} = D_s \cdot \text{T}_\text{s} \tag{21}$$
$$t_{\text{LV}} = \sqrt{3} m \text{T}_\text{s} \sin(\gamma_k) \tag{22}$$
$$t_{\text{MV}} = 2m\text{T}_\text{s}\sin\left(\frac{\pi}{6} - \gamma_k\right) \tag{23}$$
$$t_{\text{ZV}} = \text{T}_\text{s} - (t_{\text{ST}} + t_{\text{LV}} + t_{\text{MV}}) \tag{24}$$

where k is the even sector number $k \in \{2, 4, 6, 8, 10, 12\}$.

To include the compensation of possible capacitor imbalances, this modulation algorithm incorporates small vectors. Two situations must be considered: positive and negative imbalance. Positive imbalance occurs when the C_2 voltage exceeds the capacitor voltage: C_3 ($V_{C_2} > V_{C_3}$); and negative imbalance occurs in the opposite case ($V_{C_3} > V_{C_2}$).

As shown in Table 1, small vectors POO, OPO and OOP are applied to compensate positive imbalance, while in the negative case vectors NOO, ONO and OON are selected. Fig. 7, shows that the compensation of the positive imbalance

TABLE 2. Summary of dwelling time, switching sequence and imbalance compensation in all sectors in the proposed SVPWM modulation. ($t_{ST} = D_s \cdot T_s$).

Sector	$V_{C_2} > V_{C_3}$	dwell time large vector	dwell time medium vector (t_{MV})	dwell time zero vector	dwell time small vector	switching sequence
1	-	$t_{LV} = 2mT_s\sin(\gamma_1)$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_1)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OOF$_{ST}$-PON-PNN-PON-OOF$_{ST}$-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-F$_{ST}$OO-POO-PON-PNN-PON-POO-F$_{ST}$OO-OOO
2	+	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_2)$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_2\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-F$_{ST}$OO-PON-PPN-PON-F$_{ST}$OO-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OOF$_{ST}$-OON-PON-PPN-PON-OON-OOF$_{ST}$-OOO
3	+	$t_{LV} = 2mT_s\sin(\gamma_3)$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_3)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OF$_{ST}$O-OPN-PPN-OPN-OF$_{ST}$O-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OOF$_{ST}$-OON-OPN-PPN-OPN-OON-OOF$_{ST}$-OOO
4	-	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_4)$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_4\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OOF$_{ST}$-OPN-NPN-OPN-OOF$_{ST}$-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OF$_{ST}$O-OPO-OPN-NPN-OPN-OPO-OF$_{ST}$O-OOO
5	-	$t_{LV} = 2mT_s\sin(\gamma_5)$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_5)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-F$_{ST}$OO-NPO-NPN-NPO-F$_{ST}$OO-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OF$_{ST}$O-OPO-NPO-NPN-NPO-OPO-OF$_{ST}$O-OOO
6	+	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_6)$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_6\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OF$_{ST}$O-NPO-NPP-NPO-OF$_{ST}$O-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-F$_{ST}$OO-NOO-NPO-NPP-NPO-NOO-F$_{ST}$OO-OOO
7	+	$t_{LV} = 2mT_s\sin(\gamma_7)$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_7)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OOF$_{ST}$-NOP-NPP-NOP-OOF$_{ST}$-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-F$_{ST}$OO-NOO-NOP-NPP-NOP-NOO-F$_{ST}$OO-OOO
8	-	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_8)$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_8\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-F$_{ST}$OO-NOP-NNP-NOP-F$_{ST}$OO-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OOF$_{ST}$-OOP-NOP-NNP-NOP-OOP-OOF$_{ST}$-OOO
9	-	$t_{LV} = 2mT_s\sin(\gamma_9)$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_9)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OF$_{ST}$O-ONP-NNP-ONP-OF$_{ST}$O-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OOF$_{ST}$-OOP-ONP-NNP-ONP-OOP-OOF$_{ST}$-OOO
10	+	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_{10})$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_{10}\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OOF$_{ST}$-ONP-PNP-ONP-OOF$_{ST}$-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OF$_{ST}$O-ONO-ONP-PNP-ONP-ONO-OF$_{ST}$O-OOO
11	+	$t_{LV} = 2mT_s\sin(\gamma_{11})$	$\sqrt{3}mT_s\sin(\frac{\pi}{6} - \gamma_{11})$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-F$_{ST}$OO-PNO-PNP-PNO-F$_{ST}$OO-OOO
	-	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-OF$_{ST}$O-ONO-PNO-PNP-PNO-ONO-OF$_{ST}$O-OOO
12	-	$t_{LV} = \sqrt{3}mT_s\sin(\gamma_{12})$	$2mT_s\sin\left(\frac{\pi}{6} - \gamma_{12}\right)$	$t_{ZV} = T_s - t_{LV} - t_{MV} - t_{ST}$	-	OOO-OF$_{ST}$O-PNO-PNN-PNO-OF$_{ST}$O-OOO
	+	$t^*_{LV} = t_{LV} - \frac{r}{2}$		$t^*_{ZV} = t_{ZV} - \frac{r}{2}$	r	OOO-F$_{ST}$OO-POO-PNO-PNN-PNO-POO-F$_{ST}$OO-OOO

only occurs in sectors 1, 4, 5, 8, 9, and 12 while the negative imbalance is conducted in the remaining sectors. Therefore, depending on the type of imbalance and the sector where the reference voltage vector is located, an LMZ or an LMSZ modulation is used. Then the volt-second balance equation for LMSZ with ST modulation is:

$$\mathbf{V_{ref}} \cdot T_s = \mathbf{V_{LV}} \cdot t^*_{LV} + \mathbf{V_{MV}} \cdot t_{MV} + \mathbf{V_{SV}} \cdot t_{SV} + \mathbf{V_{ZV}} \cdot t^*_{ZV} + \mathbf{V_{ST}} \cdot t_{ST} \quad (25)$$

where

$$T_s = t^*_{LV} + t_{MV} + t_{SV} + t^*_{ZV} + t_{ST} \quad (26)$$

Some of these dwelling times remain unchanged, as t_{ST} and t_{MV}, but the others must be modified, as represented in Fig. 5(a) and Fig. 6(a), because of the consideration of zero vectors. Fig. 7 shows that regardless of the imbalance sign, each small vector is always in the same direction as one large vector, and their magnitudes are constant (Eq.(27) and (28)), as stated in Table 1. Therefore, the dwelling time of small vectors can be obtained from the large ones without an additional calculation because the magnitude of the large vector is twice that of the small one.

$$||\mathbf{V_{SV}}|| = \frac{1}{3} \cdot V_{in} \cdot B \quad (27)$$

$$||\mathbf{V_{LV}}|| = \frac{2}{3} \cdot V_{in} \cdot B \quad (28)$$

Therefore, to maintain the volt-second average, times are calculated as follows:

$$t_{SV} = r \quad (29)$$

$$t^*_{LV} = t_{LV} - \frac{r}{2} \quad (30)$$

$$t^*_{ZV} = t_{ZV} - \frac{r}{2} \quad (31)$$

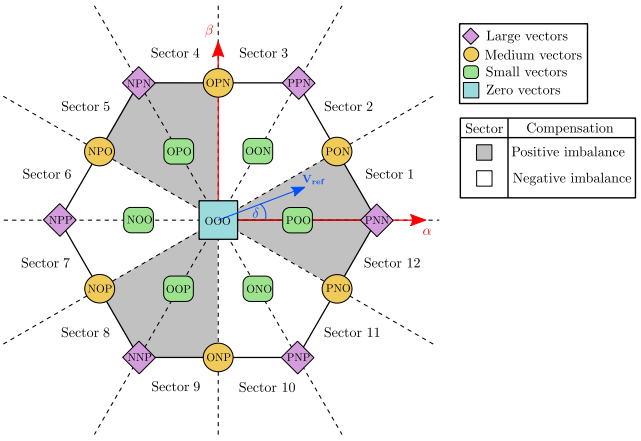

FIGURE 7. Sector divisions proposed in the SVPWM LMSZ.

r is an adjustment variable and its value is obtained from a proportional-integral (PI) controller. Calculation details for each sector are provided in Table 2, including the dwelling times for each vector and the corresponding switching sequence. Finally, all the dwelling times must meet Eq.(26).

In Fig. 8 the complete block diagram for the proposed control algorithm is represented, showing all the previously described stages.

III. SIMULATION RESULTS

In this section, simulation results are presented to verify the proper performance of the proposed modulation method in different conditions. Balanced and imbalanced systems have been studied, considering buck and boost converter operation in both cases. Furthermore, an additional case with a low modulation index and inductive load is analyzed. The passive element selection of the IS network is also indicated. Simulation parameters and passive element values are presented in Table 3.

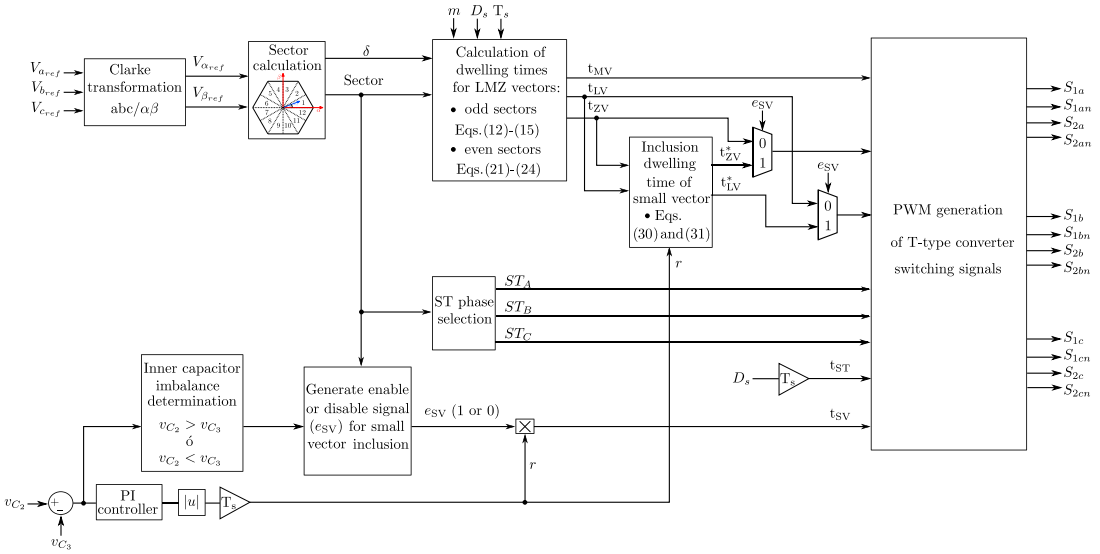

FIGURE 8. Block diagram of complete control algorithm.

TABLE 3. Values used in the converter design and simulation parameters.

Parameters	Value
Input voltage V_{in}	250 V
QZ-Source capacitors C_1, C_2, C_3, C_4	3.3 mF
QZ-Source inductors L_1, L_2, L_3, L_4	1.5 mH
AC frequency	50 Hz
Switching frequency (f_{sw})	10 kHz
Filter inductor L_f (per phase)	10 mH
Filter resistance R_f (per phase)	400 mH
Load Resistance R_L (per phase)	47 Ω
Maximum voltage ripple across the capacitors (K_C)	0.05 P.U
Maximum current ripple in (K_L)	0.05 P.U
Shoot-through duty cycle (D_s)	0.15 P.U

The passive element components were selected according to the guidelines provided in [44] and [45]. The main equations for the calculation are as follows:

$$L_{1,..,4} \leq \frac{V_{\text{in}} \cdot (1 - D_s) \cdot D_s}{2 \cdot I_{\text{in}} \cdot f_{\text{sw}} \cdot K_L \cdot (1 - 2D_s)} \tag{32}$$

$$C_{1,4} \leq \frac{2 \cdot P_{\text{out}} \cdot (1 - 2D_s)}{V_{\text{in}}^2 \cdot K_C \cdot f_{\text{sw}}} \tag{33}$$

$$C_{2,3} \leq \frac{2 \cdot P_{\text{out}} \cdot (1 - 2D_s)}{V_{\text{in}}^2 \cdot K_C \cdot f_{\text{sw}}} \cdot \frac{D_s}{(1 - D_s)} \tag{34}$$

where $L_{1,..,4}$ – are quasi IS network inductance values, $C_{1,4}$ – quasi IS network external capacitor values, $C_{2,3}$ – quasi IS network internal capacitor values, V_{in} – input voltage, I_{in} – input current, f_{sw} – switching frequency, K_L – maximum current ripple in I_{in}, P_{out} – output power and K_C – maximum voltage ripple across the capacitors.

A. WITHOUT IMBALANCE VOLTAGES

Because the converter topology allows buck and boost operation modes, both have been simulated. The difference lies in the inclusion or neglect of a voltage boost factor, through the ST state.

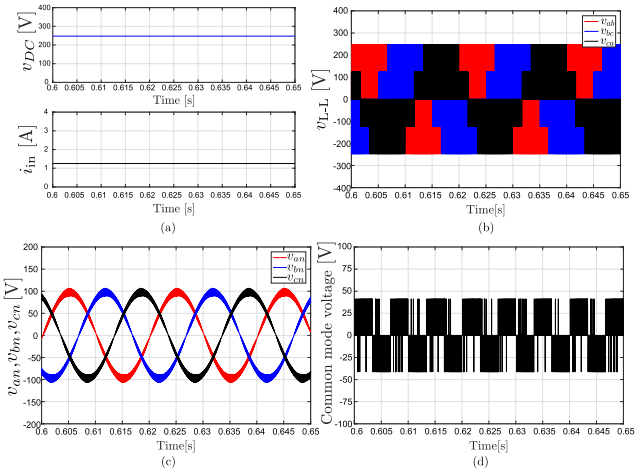

FIGURE 9. Simulation results with $m = 0.8$ and $D_s = 0$ without imbalance compensation: (a) Input current and dc-link voltage. (b) Line-to-line voltage before filter. (c) Load voltages. (d) Common-mode voltage.

1) BUCK OPERATION

This operation mode omits the ST state ($D_s = 0$) that is, this case represents the typical situation in which any three-level converter without IS is operating.

Fig. 9 shows the buck operation for an input voltage of 250 V and modulation index (m) of 0.8. This figure shows the current and voltage input variables (Fig. 9(a)) for the case of study. In Fig. 9(b) the line-to-line voltage before the filter is presented, indicating the correct operation of the 3-level converter. Fig. 9(c) presents the voltage on the resistive load, which provides the correct calculation of the volt-second average equation, demonstrating modulation performance. Fig. 9(d) displays the CMV with a value always within ($\pm 1/6\ v_{DC}$), which is one of the advantages of this modulation.

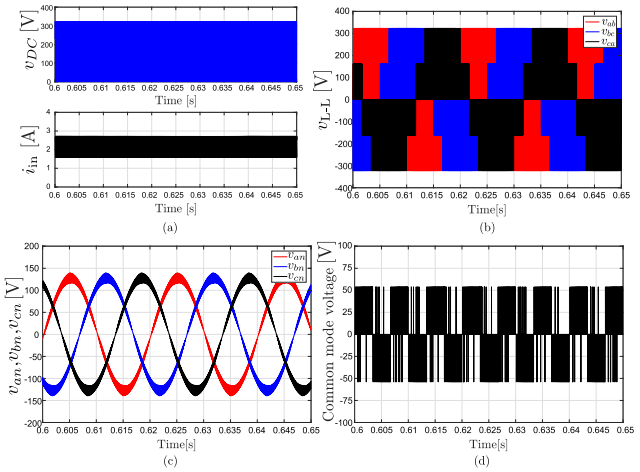

FIGURE 10. Simulation results with $m = 0.8$ and $D_s = 0.12$ without imbalance compesation: (a) Input current and dc-link voltage. (b) Line-to-line voltage before filter. (c) Load voltages. (d) Common-mode voltage.

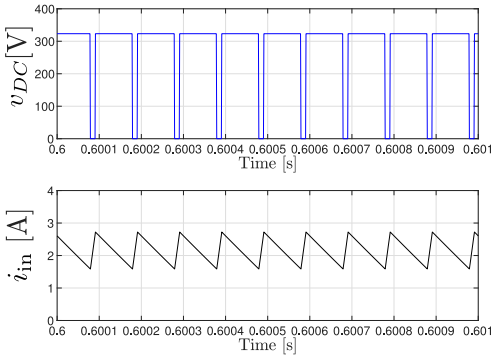

FIGURE 11. Waveform details for the input current and voltage of dc-link.

2) BOOST OPERATION

Boost operation is obtained with a non-zero ST state and the associated dwelling time. To show this converter operation mode, a D_s of 0.12 is chosen. In Fig. 10, the boost operation is shown for an input voltage of 250 V and modulation index (m) of 0.8, where the uniform distribution of the ST state in the modulation can be observed. For those conditions, the boost factor is given by $B = 1/(1 - 2 \cdot Ds) = 1.316$. Fig. 10(a) shows the input current and the dc-link voltage. Unlike the buck case, the dc-link voltage is switched at high frequency and reaches a higher voltage value when adding the ST state. The maximum value of the dc-link voltage complies with the theoretical value ($V_{\text{in}} \cdot B = 329\ V$). In Fig. 10(b), the line-to-line voltage before the filter is shown, where the 3-level voltages are observed. Fig. 10(c) presents the 3-phase equilibrated voltages in the resistive load, while Fig. 10(d) displays the common-mode voltage, again limited to reduced values.

Fig. 11 shows the dc-link voltage and input current for the case of study.

B. WITH IMBALANCE VOLTAGES

In this case, the proposed strategy includes the small vectors to compensate the NP imbalance, in addition to the ST states.

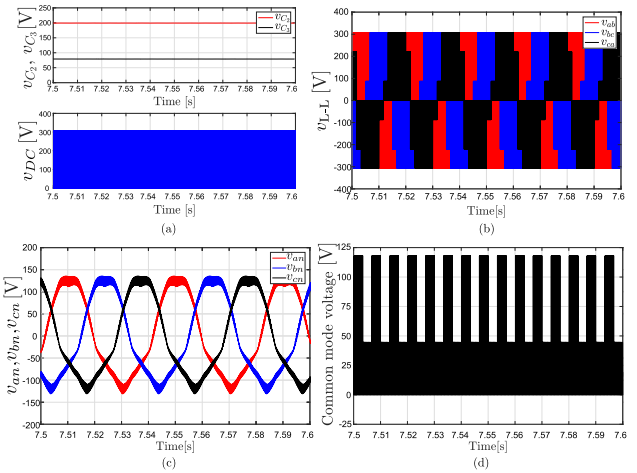

FIGURE 12. Simulation results with $m = 0.8$ and $D_s = 0.1$ without imbalance compensation: (a) voltage in inner capacitors (C_2 and C_3) and dc-link voltage. (b) Line-to-line voltage before filter. (c) Load voltages. (d) Common-mode voltage.

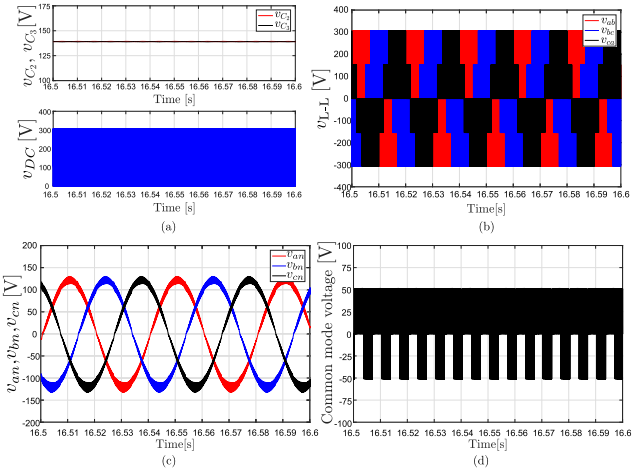

FIGURE 13. Simulation results with $m = 0.8$ and $D_s = 0.1$ with imbalance compensation: (a) voltage in inner capacitors (C_2 and C_3) and dc-link voltage. (b) Line-to-line voltage before filter. (c) Load voltages. (d) Common-mode voltage.

Then, in order to show the most general operation, the boost case is considered, demonstrating all the features and advantages of the developed modulation technique.

Figs. 12, 13 and 14 show the simulation results of the boost operation for an input voltage of 250 V, a modulation index of 0.8 and a duty cycle ST of 0.1. The boost factor for the case under study is given by $B = 1/(1 - 2 \cdot D_s) = 1.25$. The purpose of this simulation is to check the correct operation of the imbalance compensation. For this reason, a 470 Ω resistor is connected in parallel to the capacitor C_3, generating a high positive imbalance voltage between the inner capacitors (C_2 and C_3). Before 8.5 s., the imbalance compensation using the proper selection of the small vector is not activated.

Subsequently, the output voltage and currents are distorted, as can be appreciated in Fig. 12. A voltage difference of 120 V in the inner capacitors (C_2 and C_3) is observed in the top representation of Fig. 12(a). The switched dc-link voltage, depicted in the bottom, shows the maximum dc-link voltage

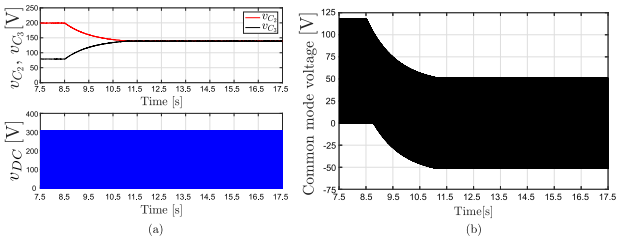

FIGURE 14. Simulation results with $m = 0.8$ and $D_s = 0.1$ with and without imbalance compensation: (a) voltage in inner capacitors (C_2 and C_3) and dc-link voltage. (b) Common-mode voltage.

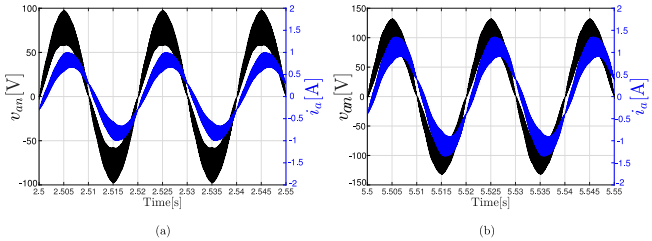

FIGURE 15. Simulation results with $m = 0.55$: (a) load voltage (v_{an}) and output current (i_a) without shoot-through; (b) load voltage (v_{an}) and output current (i_a) with shoot-through. ($D_s = 0.12$).

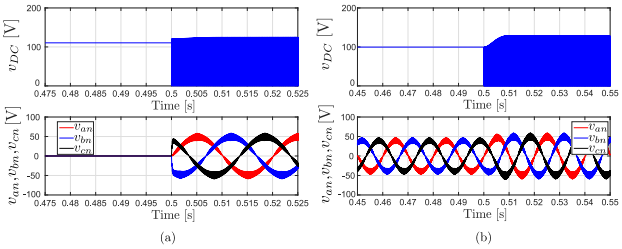

FIGURE 16. Simulation results under dynamic operating conditions with $m = 0.8$: a) Full DC-link voltage (v_{DC}) and load voltages (v_{an}, v_{bn} and v_{cn}) during the start-up process. b) Full DC-link voltage (v_{DC}) and load voltages (v_{an}, v_{bn} and v_{cn}) during the transient from buck to boost operation.

value, which complies with the theoretical value ($V_{\text{in}} \cdot B = 312.5\ V$). Fig. 12(b) illustrates line-to-line voltages, where additional voltage levels appear, because of the imbalance. Voltage in the resistive load can be seen in Fig. 12(c), showing a distortion in the sinusoidal waveform during the negative half-cycle. Moreover, the common-mode voltage is not within expected limits, as Fig. 12(d) shows.

Once the compensation algorithm is included (time > 8.5 s), the results reach the expected values, i.e., the voltage in the inner capacitors C_2 and C_3 is balanced at a value of approximately 139.1 V, as shown in Fig. 13(a). The dc-link voltage after activating the compensation is not modified because the value of D_s is unchanged. The line-to-line voltage before the filter recovers its symmetry and the expected 3-level waveform (Fig. 13(b)). Load voltage waveforms become sinusoidal again (Fig. 13(c)) and the common-mode voltage in Fig. 13(d) remains within the expected range.

In Fig. 14, the simulation time including the algorithm modification instant is shown, clearly appreciating the operation without imbalance compensation (time < 8.5 s) and with imbalance compensation (time > 8.5 s). The transient time for the capacitor balancing is lower than 3 s (Fig. 14(a)). Fig. 14(b) demonstrates how the common-mode voltage manages to remain within ($\pm 1/6\ v_{DC}$) once the capacitors are balanced.

C. LOW MODULATION INDEX ($m = 0.55$) AND INDUCTIVE LOAD

To demonstrate the performance of the proposed control strategy under different conditions, a simulation with low modulation index ($m = 0.55$) for low power factor (PF) conditions is presented. To generate the low PF an inductance is connected in parallel to a resistive load, for each phase ($L = 0.52$ H and $R = 100\ \Omega$ per phase). Phase a voltage (v_{an}) and output current (i_a) are depicted in Figs. 15 a) and 15 b) for buck and boost operations ($D_s = 0.12$), respectively. In both cases the voltage and current are not in phase, as expected for the reduced power factor due to inductive load (PF of approximately 0.85). The inclusion of the ST state has the effect of increasing load current and voltage for the boost case.

D. DYNAMIC CONDITIONS TEST

The behavior of the 3L-T-Type qZS inverter using the proposed modulation has been also tested under dynamic operating conditions. Two different tests are carried out, both setting a value of 100 V for the input voltage and a resistive load of 100 Ω (per phase).

Fig 16 a) shows the start-up process at t = 0.5 s., where the PWM and D_s signals are enabled ($D_s = 0.1$). Load voltages and DC-link voltage under these conditions are depicted. This test represents the sudden connection of any load or consumer. A very fast dynamic response without overvalues is observed, validating the control method for the studied conditions. The second dynamic test is depicted in Fig 16 b), showing the transition from buck to boost operation modes. To demonstrate the correct operation, D_s Value is changed from $D_s = 0$ to $D_s = 0.1$, at the time 0.5 s. This second dynamic test can represent a change in solar irradiance and the corresponding action to modify the input voltage. The dynamic response is again stable and voltages are controlled throughout the process.

IV. EXPERIMENTAL VERIFICATION

A 3L-T-Type qZSI was assembled to experimentally check the proper performance of the proposed SVM method and its main functionalities. In the following, the full laboratory setup (Fig. 17) and testing procedure with the main results are described. Notably, identical tests and main parameters (passive elements, testing power levels, etc.) similar to those in the simulations were conducted experimentally.

The 3L-T-Type power module is based on the 12MB150VX-120-50 IGBT module from FUJI. It is designed to have 1200 V and 50 A 12 RB-IGBT in one package with reduced size and substantial low power loss. Silicon carbide Schottky diodes C3D10060G from CREE are

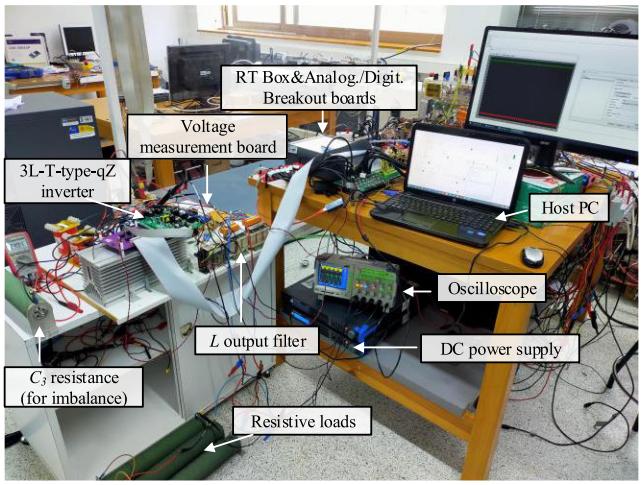

FIGURE 17. Full laboratory setup for experimental testing.

selected for the qZS network. The driver board AT-NPC 3-level 12in1 provided by FUJI is used to drive the power module. The driver chip is based on the ACPE-333J from Avago Technologies with a built-in function for short-circuit protection.

The control unit is the RT Box 1 from Plexim, used as a rapid prototype controller and equipped with analog and digital breakout boards. This controller operates a Xilinx Zynq Z-7030 system-on-chip that embeds two CPU cores on an FPGA. The proposed SVM was programmed in the PLECS standalone environment in the host computer, running at a sampling rate of 10 kHz. The measurement stage is equipped with LV-25-P for v_{C_2} and v_{C_3} inner voltages, both by LEM. These sensors perform with high precision, good linearity and low common-mode disturbance. The sensors are required for eliminating the voltage imbalance. Finally, the system is supplied by the BK XLN60026 DC power source. All our measurements were made by a Tektronix TPS2024B digital oscilloscope, Tektronix P5100A voltage probes and A622 current probes.

The switching signal generation is depicted in Fig. 18 a) and b). Fig. 18 a) shows the corresponding switching signals for each IGBT according to the sinusoidal modulation (S_{1a}, S_{1an}, ..., S_{2c} and S_{2cn}) and the shoot-through states (ST_A, ST_B and ST_C). It can be observed how the shoot-through states only short-circuit one inverter branch each time. These signals are presented from bottom to top in Fig. 18 a).

Fig. 18 b) shows the switching signals for each IGBT with embedded shoot-through states that directly interface with the 3L-T-Type driver board. This stage is performed in a PCB composed of OR and AND chips.

A. WITHOUT IMBALANCE VOLTAGES

Our first tests aimed at validating the proper switching during the buck and boost capability of the 3L-T-Type power inverter but with balanced inner capacitor voltages v_{C_2} and v_{C_3}. The main waveforms are shown and discussed below.

FIGURE 18. Switching and control signal generation a). Digital outputs from RT box 1. b) Control signals from PCB.

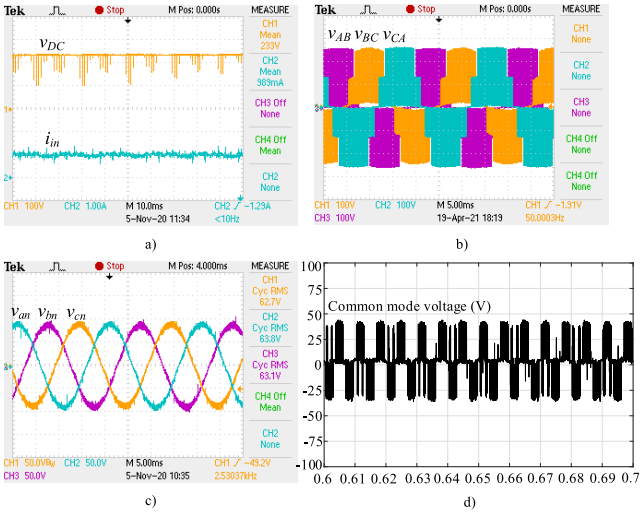

FIGURE 19. Main experimental waveforms with $m = 0.8$ and $D_s = 0$. a) DC-link voltage (v_{DC}) and input current (i_{in}). b) Line-to-line voltages (v_{ab}, v_{bc} and v_{ca}) before filtering stage. c) Load voltages (v_{an}, v_{bn} and v_{cn}) and d) common-mode voltage.

1) BUCK OPERATION ($D_s = 0$)

Fig. 19 shows the experimental waveforms without shoot-through and $m = 0.8$, i.e., the power inverter operates in buck mode in balanced conditions.

Fig. 19 a) presents the dc-link voltage and input current. v_{DC} corresponds to the input voltage equal to 250 V, but a voltage drop is appreciated. Voltage spikes are also observed. This phenomenon is justified because no dead-time was implemented in the pulses generation, as this is one of the main characteristics of the impedance-based power converter family. Fig. 19 b) shows the line-to-line voltages and their corresponding DC voltage levels before filtering (0, $\pm$ $V_{\text{in}}/2$ and $\pm$ V_{in}). Finally, Fig. 19 c) and d present the output load voltages and common-mode voltage respectively. Quite good sinusoidal voltages (v_{an}, v_{bn} and v_{cn}) were obtained (with THD around the 2%), and the common-mode voltage is limited at $v_{DC}/6$.

2) BOOST OPERATION ($D_s = 0.12$)

The same electrical magnitudes were measured and are shown for the boost case, i.e., with $D_s = 0.12$ and $m = 0.8$.

The DC-link voltage and input current are depicted in Fig. 20 a). Fig. 20 b) is a detailed zoom view of the previous one. As can be observed, v_{DC} drops to zero uniformly because

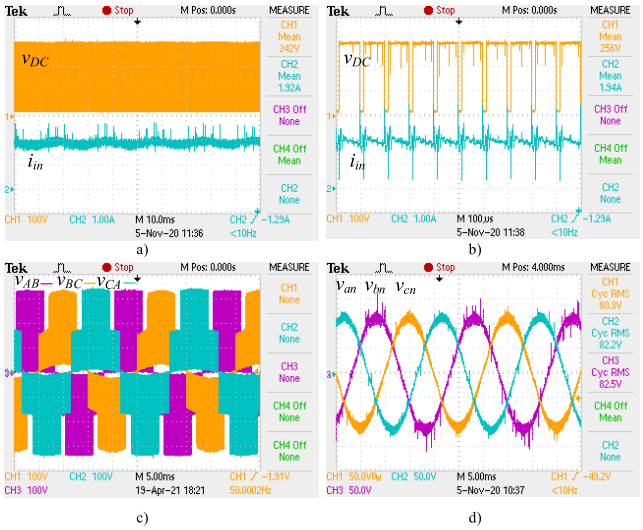

FIGURE 20. Main experimental waveforms with modulation index equal to 0.8 and $D_s = 0.12$. a) DC-link voltage (v_{DC}) and input current (i_{in}). b) Detailed view of v_{DC} and i_{in}. c) Line-to-line voltages (v_{ab}, v_{bc} and v_{ca}) before filtering stage and d) load voltages (v_{an}, v_{bn} and v_{cn}).

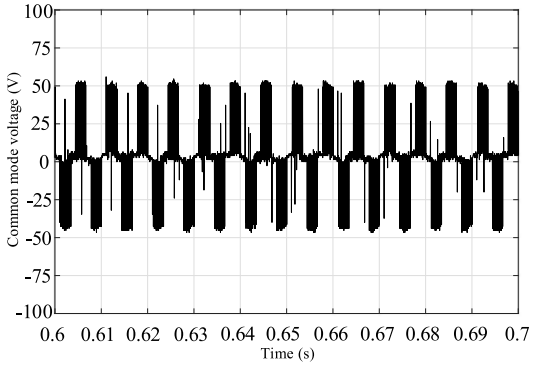

FIGURE 21. Common-mode voltage $((V_{AO} + V_{BO} + V_{CO})/3)$.

of the shoot-through insertion. The i_{in} waveform demonstrates the continuous conduction operation mode of the 3L-T-Type qZSI. The maximum value of the DC-link voltage is approximately 315 V, the theoretical value being 328 V. This value is produced by the voltages drop (of approximately 4%) in magnetic components.

New voltage levels were achieved (0, $\pm BV_{in}/2$ and $\pm BV_{in}$), as demonstrated in Fig. 20 c). Fig. 20 d) depicts the output voltage in the load for this boosting case. In these signals, a THD below 5% was achieved. Finally, Fig. 21 shows the common-mode voltage waveform limited to $v_{DC}/6$, as the voltage vectors that produce higher CMV are avoided. This feature would reduce the leakage currents and increase the security level against indirect contacts.

B. WITH IMBALANCE VOLTAGES

To perform the DC-link inner voltages control in the case of possible imbalances, a resistor was connected to C_3 ($R = 470\ \Omega$). This case would produce a hard positive imbalance ($v_{C_2} > v_{C_3}$). For generalization, this test was also conducted during the boost operation with identical parameters.

TABLE 4. Experimental load voltage THD (phase A).

	V_{an} THD$_v$ (before imbalance compensation)	V_{an} THD$_v$ (after imbalance compensation)
Phase A	15.78%	5.5%

Fig. 22 shows the main signals before and after the control loop activation, for mitigating the voltage imbalance. First, Fig. 22 a) depicts the response of the proposed SVPWM method for controlling the voltage imbalance. In this figure, an effective voltage compensation is demonstrated with a fast transient, without any undesired overvoltage or overcurrent. This capability improves the entire inverter reliability. Moreover, the output voltage quality is substantially improved once the voltage imbalance is eliminated. Table 4 shows the voltage total harmonics distortion (THD$_v$) before and after imbalance compensation. As expected, after the imbalance compensation the THD value is quite reduced.

C. LOW MODULATION INDEX ($m = 0.55$) AND INDUCTIVE LOAD

In this case, the system operates at m equal to 0.55, supplying an inductive load. A pure inductance with value equal to 0.52 H per phase is connected in parallel to a resistive load with 100 Ω per phase. With the same power and voltage testing parameters, the load corresponds to a power factor of approximately 0.85. Fig. 23 shows the waveforms of v_{DC}, v_{an} and the load current of phase a (i_a). In Fig. 23 a) and in Fig. 23 b), the 3L-T-Type qZSI is working in buck mode and in boost mode respectively ($D_s = 0.12$). In the buck mode, i_a presents a low THD (15.18%), but in the boost mode the current i_a is slightly more distorted because of the shoot-through states insertion (THD = 22.84%) and the low modulation index.

D. DYNAMIC CONDITIONS TEST

In order to validate the 3-level T-Type q-ZS inverter behaviour in dynamic conditions operation with the proposed modulation, two different tests were conducted for its analysis. In these cases, the input voltage was set at 100 V. First the start-up process is shown in the Fig. 24 a), where the PWM signals are enabled and the D_s value is equal to 0.1. The transition from the buck to the boost mode was also studied and depicted in Fig. 24 b). This second dynamic condition may correspond to a change in the solar irradiance, and the corresponding action to boost the input voltage. Meanwhile, the first case can be intended as the sudden connection of any load or consumer. The Fig. 24 a) shows the output voltages and the DC-link voltage during the start-up process, where the D_s is included from the beginning. The power converter presents an stable behaviour without any dangerous transient in the voltages. The Fig. 24 b) depicts the transient from

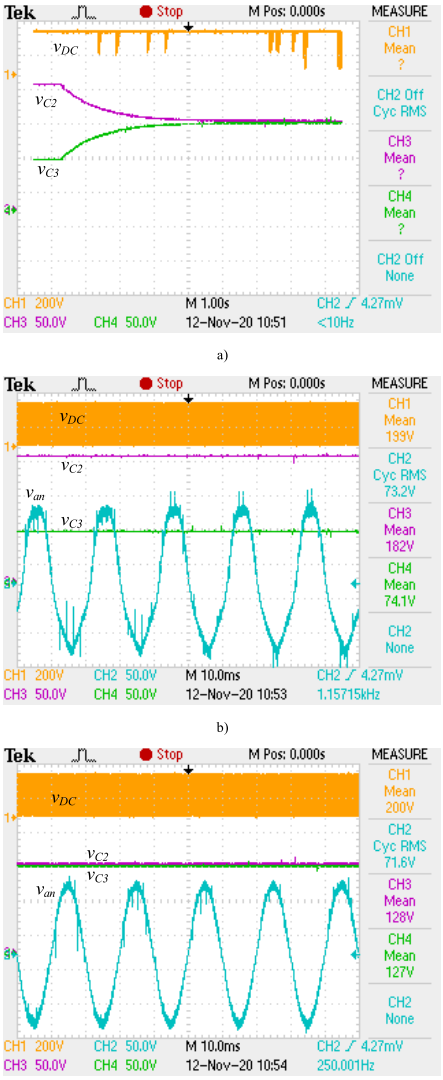

FIGURE 22. Main experimental pictures during unbalance condition. a) Full DC-link voltage (v_{DC}) and capacitor voltages (v_{C_2} and v_{C_3}) evolution during imbalance control. b) Detailed view of v_{DC}, v_{C_2}, v_{C_3} and v_{an} before imbalance compensation. c) Detailed view of v_{DC}, v_{C_2}, v_{C_3} and v_{an} after imbalance compensation.

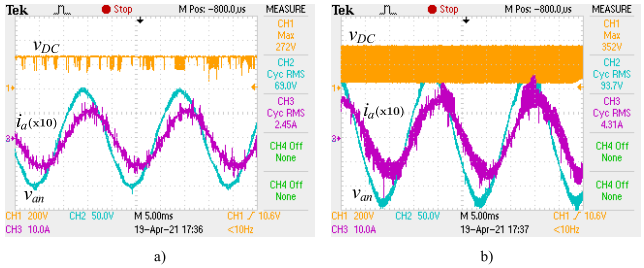

FIGURE 23. Main experimental pictures with $m = 0.55$ and an inductive load. a) Full DC-link voltage (v_{DC}), load voltage (v_{an}) and output current (i_a). b) Full DC-link voltage (v_{DC}), load voltage (v_{an}) and output current (i_a) with shoot-through ($D_s = 0.12$).

the buck to the boost operation ($D_s = 0.1$) and the same voltage waveforms. Again, the output voltage shows a robust behaviour during the dynamic evolution.

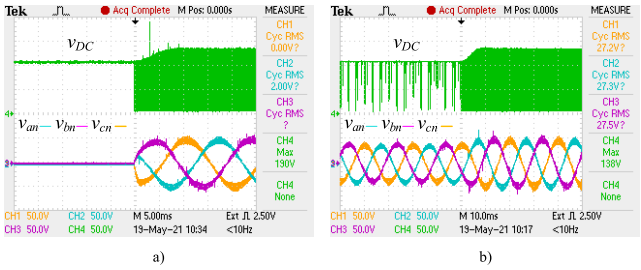

FIGURE 24. Dynamic conditions operation with $m = 0.8$: a) Full DC-link voltage (v_{DC}) and load voltages (v_{an}, v_{bn} and v_{cn}) during the start-up process. b) Full DC-link voltage (v_{DC}) and load voltages (v_{an}, v_{bn} and v_{cn}) during the transient from the buck to the boost operation.

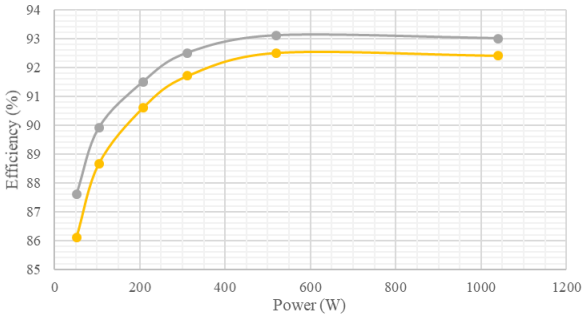

FIGURE 25. Efficiency curves in balanced conditions for buck operation (grey line) and boost operation (yellow line).

E. EFFICIENCY ANALYSIS

Finally, Fig. 25 shows some 3-level T-Type q-ZS inverter efficiency curves depending on the output power, and using the proposed modulation technique. The measurement of the efficiency was done in the laboratory with the Newtons4th PPA5500 equipment, dedicated for this purpose. The efficiency was tested in six different power points for the buck (grey line) and for the boost case (yellow line) in balanced conditions. As expected, the use of the shoot-through states increases the system losses, but the efficiency is still good above the 90% for both cases.

V. CONCLUSION

This paper presents a simplified version of SVPWM modulation for a 3-level T-Type q-ZS inverter, allowing a reduced common-mode voltage operation. This algorithm can be applied to any 3-level converter combined with an impedance network. It has been verified by simulation and experimental implementation, showing correct operation in different operating points, voltage boost regulation and inner capacitors voltage balancing.

The main application field considered was the PV energy conversion systems. Further works will be conducted to optimize the power converter hardware, aiming at higher power density by means of the use of wide-band semiconductors and higher switching frequencies. Besides, new application fields will be explored for the proposed system, as for example, its applicability in fast-charging electric-vehicle infrastructures, [46].

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