IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received May 12, 2021, accepted June 3, 2021, date of publication June 7, 2021, date of current version June 16, 2021.

*Digital Object Identifier 10.1109/ACCESS.2021.3086867*

# Manufacturing Issues of BEOL CMOS-MEMS Devices

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This work was supported in part by the Spanish Ministry of Science, Innovation and Universities, under Project RTI2018-099766-B-I00, in part by the State Research Agency (AEI), in part by the European Social Fund (ESF), and in part by Baolab Microsystems, S.L.

**ABSTRACT** In this paper we present a comprehensive report on the issues found during the manufacturing of high-yield CMOS-MEMS sensors based on vapor-phase hydrogen fluoride (vapor-*HF*) oxide etching. During the study we have identified the main issues affecting CMOS-MEMS high-yield manufacturing regarding the silicon oxide as a sacrificial material, the passivation as a release mask, the BEOL as structural material for MEMS design and the aluminum-sputtering as a sealing layer for the MEMS cavity. This study has been carried out by systematically analyzing over 100 full wafers in 10 different runs on four different foundries using 0.5 µm, 0.18 µm and 0.15 µm CMOS processes, containing both test structures and full-sensor designs.

**INDEX TERMS** CMOS-MEMS, design techniques, hydrogen fluoride, silicon oxide, vapor-HF, release, reliability, yield.

## I. INTRODUCTION

Complemetary-Metal-Oxide-Semiconductor (CMOS) technology is by far the most common semiconductor manufacturing technology. Today, many commercial circuits incorporate Micro-Electro-Mechanical-Systems (MEMS) that are manufactured using their own processes in a separate die. The CMOS and the MEMS dice must be later integrated into a single package, process known as hybrid integration. For several applications, building the MEMS in the same die as the CMOS circuitry has important benefits such as lower cost, size and parasitics, which in turn means lower power consumption and higher performance. This is known as CMOS-MEMS monolithic integration.

Numerous CMOS-MEMS monolithic integration approaches have been developed. A good explanation is given by Baltes *et al.* [1], [2]. Monolithic integration of CMOS and MEMS may be achieved by three general approaches, depending on when the MEMS devices are fabricated with respect to CMOS FEOL (Front-End-Of-Line) and BEOL (Back-End-Of-Line) processes [3], [4]:

- **Pre-CMOS or MEMS before CMOS**: Yasaitis *et al.* [5], Smith *et al.* [6], M3EMS from Sandia National Laboratories [7]. The processing temperatures of the MEMS do not need to be CMOS-compatible [8]. However, the main drawback of this approach is that it is very difficult to pursue given that CMOS foundry requirements for acceptance of externally processed wafers are very demanding.
- **Intra-CMOS or MEMS between FEOL and BEOL**: iMEMS from Analog Devices [9], Nanomech from Cavendish Kinetics [10]–[13], Cornell University [14]. The CMOS process is stopped and the MEMS parts are processed before finishing the standard CMOS process.
- **Post-CMOS or MEMS after CMOS**
  - **MEMS on top**: Microstructures are built on top of the finished CMOS die [15], [16]. This approach was followed by several foundries like XFAB, TSMC, UMC and DALSA, and also in the processes IMEC's SiGe MEMS [17], and DMD from Texas Instruments [18]. For CMOS compatibility, thermal budget limits need to be taken into account as described in Takeuchi *et al.* [8].
  - **CMOS micromachining or BEOL CMOS-MEMS**: MEMSIC [19], Bosch [20],

The associate editor coordinating the review of this manuscript and approving it for publication was Agustin Leobardo Herrera-May.

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Abadal *et al.* [21], Baolab Microsystems [22] and UPC [3], [23]–[28] are good examples. It uses the Back-End-Of-Line (BEOL) layers of the finished CMOS process to create the MEMS. Micromachining techniques are used to release the structures already manufactured with the CMOS process, thus minimizing the number of additional steps added to the standard CMOS manufacturing approach. This study is based on this approach.

In a BEOL CMOS-MEMS process, once the standard CMOS processing is finished, the structural parts need to be released either with wet or dry etching. Although wet etching has been used by many groups [29]–[37], dry etching draws a clearer path towards high volume production given its advantages over liquid release [3], [38], [39]. CMOS-MEMS integration with silicon removal with gaseous xenon difluoride ($XeF_2$) has been reported in Eyre *et al.* [40], for example. Another option is to release the BEOL metal layers by etching the BEOL silicon oxide. One typical example of commercially available dry etching applicable to silicon oxide removal is vapor-phase hydrofluoric acid (Vapor-*HF* or *vHF*) etching [39]. This option is the one discussed in this study and it is described in section II.

Usually, research papers focus on the final achievements but omit the arduous development and trial and error process that usually is needed to reach a stable and repeatable process. In this work, we discuss the main manufacturing issues of the BEOL CMOS-MEMS approach, and how they can be prevented. This study has been carried out by analyzing over 100 full wafers in four different CMOS foundries. The results have been classified in four sections: In section III we identify the main issues affecting silicon oxide as a sacrificial material, in section IV the issues using the passivation as a release mask, in section V the BEOL as a structural material for MEMS design and in section VI the aluminum-sputtering process as a sealing layer for the MEMS cavity.

## II. THE BEOL CMOS-MEMS PROCESS WITH VAPOR-HF RELEASE

### A. CMOS PROCESS CROSS-SECTION

The CMOS-MEMS experiments encompassed the following standard CMOS processes: 0.5 µm 1Poly-3 Metal (1P3M) from MHS, 0.15 µm 1P6M from LF and 0.18 µm 1P6M from GF and TSMC. The typical cross-section of a 6-metal process is shown in figure 1a. The active area elements (CMOS-area) are always connected between them and to the outer world using the BEOL interconnection layers. The six layers and the vias that join them may be used for creating the MEMS device. In 0.18 µm processes, the typical thickness of these layers is $0.40 - 0.60$ µm, although CMOS foundries usually allow the option of a few micron-thick top metal. The vertical spacing between layers is around $0.40 - 1.00$ µm. This means a vertical separation between the first level (metal 1 or M1) to the top metal (metal 6 or M6) of around $5 - 10$ µm. This separation is important for establishing the etch time/length needed to reach metal 1. Each metal layer by itself is a stack of several materials, which is further explained in section V.

### B. CMOS-MEMS PROCESS FLOW

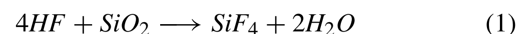
The CMOS integrated circuits (ICs) can be designed as usual. The MEMS structures are designed using the same masks as the ICs. They can be placed next to (as shown in figure 1a) or on top of the CMOS area if the number of metals used by the MEMS sensor is small. Once the CMOS process is finished, the wafers undergo a selective silicon oxide ($SiO_2$) etching with vapor-*HF* to release the MEMS structures (figure 1b) using the passivation layer of silicon nitride ($Si_3N_4$) as a release mask. Finally, the MEMS cavity is sealed using an aluminum-sputtering process deposited on top of the MEMS (figure 1c). Given the characteristics of the process, it is also convenient to deposit the sealing layer over the pad regions, as the patterning and etching of the sealing layer could damage the aluminum pads if left exposed.

As it can be observed, the top metal layer is used as a support for the sealing layer, and vent/release holes are used for allowing the penetration of the *vHF* into the MEMS cavity. This will be discussed further in section VI. Passivation openings are also needed to allow *vHF* penetration, which will be discussed in section IV.

### C. VAPOR-HF RELEASE

Vapor-*HF* release of MEMS structures avoids stiction-related failures, common to liquid *HF* release, provided the etching reaction is properly controlled [38], [39]. Therefore, the use of super-critical-drying process is not necessary with *vHF*. Its etching uniformity on BEOL CMOS-MEMS wafers is excellent for creating repeatable CMOS-MEMS structures [26]. As a matter of fact, it is already employed for successful commercial products that release MEMS structures by etching silicon oxide [41], [42].

The key chemical reaction in which the silicon oxide is etched is as follows:



$$4HF + SiO_2 \longrightarrow SiF_4 + 2H_2O \tag{1}$$

Water acts as an aggressive catalyzer for the *vHF*, so etching rate, gas flow, pressure and temperature have to be controlled to keep the water in vapor state and prevent condensation. We have also found dependencies with the oxide volume to be etched (with depends itself on the particular MEMS design, the number of dies per wafer and the number of wafers etched per batch).

Given the high number of process variables involved, the etching is performed in specific machines. During our experiments we have tested etching tools from Memsstar and SPTS Primaxx. With SPTS Primaxx, the typical value for the chamber pressure is 125 Torr, for the *vHF* partial pressure is 33.3 Torr and for the temperature is 44 °C [26].

### D. SELECTIVITY

The metallization in the CMOS processes we used is composed of aluminum ($Al$) with some small percentage of

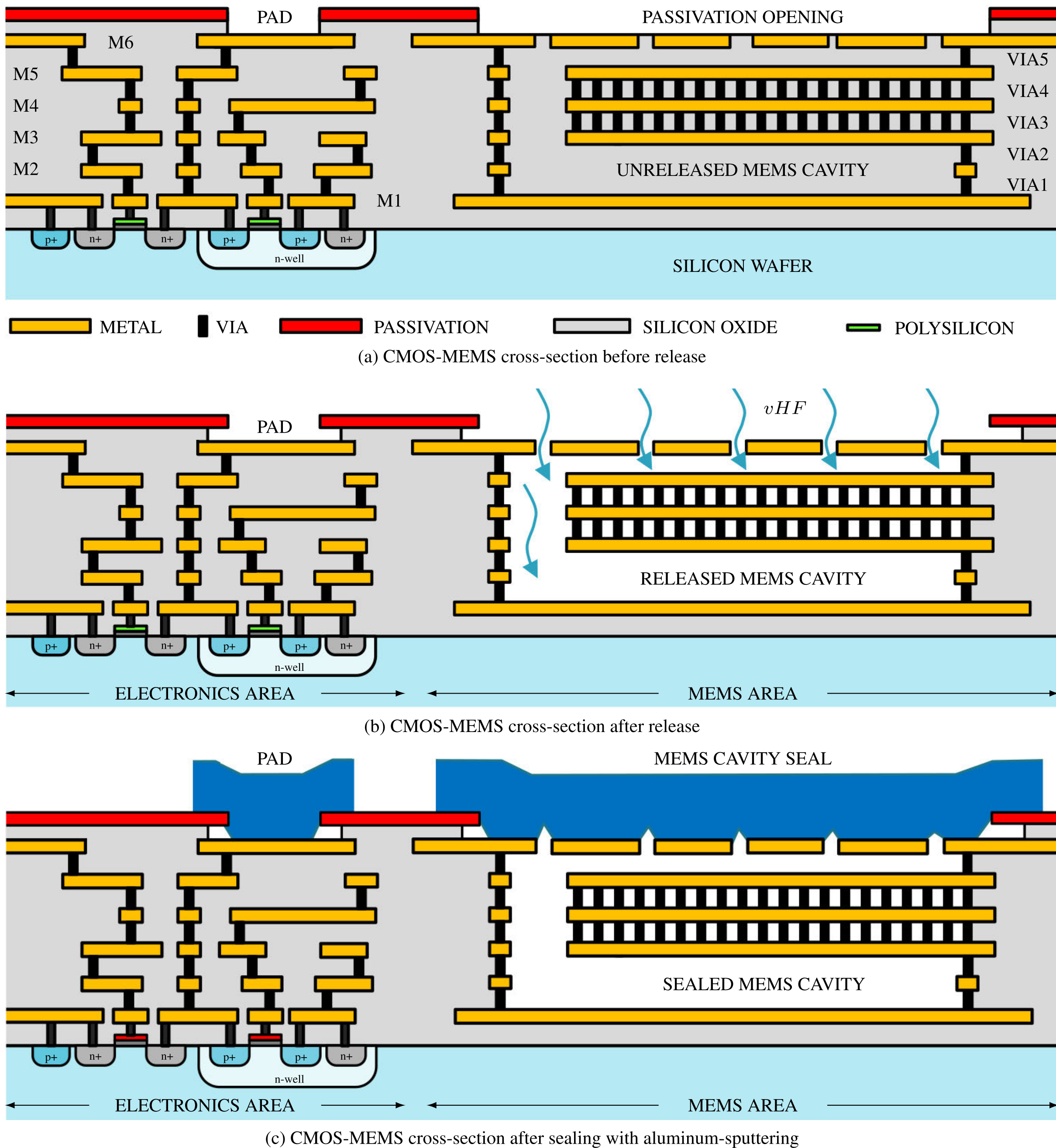



**FIGURE 1. CMOS-MEMS process cross-section before release (a), after release (b), showing the CMOS area and the MEMS cavity defined by the passivation opening, and after sealing (c).**

copper ($Cu$) and a thin ($10 \sim 70$ nm) coating of titanium/titanium nitride ($Ti/TiN$). Aluminum is barely etched by *vHF* and the alumina that is formed on the surface of the aluminum also helps as a protective layer [43]. In order to compare the etch characteristics of aluminum, titanium and titanium nitride, tests on 50 nm-thick films blanket wafers were carried out. Results showed that titanium and titanium nitride etch slightly, and titanium nitride, in particular, showed a roughened surface after the etch. This had been previously observed [43]. In our case, close inspection revealed that the roughness mainly comes from small fluoride residues that appear on the *TiN* surface. Interestingly, these residues are not observed in full CMOS wafers. The reason for this difference is not well understood, but it is known that the presence of other materials may affect the etch results. Samples that resemble closely real process conditions should be used in accurate studies. The blanket aluminum wafers showed no film thickness reduction or roughness increase. Similarly to aluminum, tungsten is highly resistant to *vHF*. Finally, low temperature Plasma Enhanced CVD (PECVD)

silicon nitride is known to have a relatively high etch rate in *vHF* [43], but by increasing its silicon content, the etch rate can be substantially decreased [26], [44]. The etch rate and selectivity of silicon oxide compared to other materials can be tailored by modifying some etching process parameters [39], [45]: for example, it is known that silicon oxide *vHF* etch rate varies inversely with temperature. In addition, surface contaminants or adsorbed moisture may alter the etching speed.

In any case, the different types of Inter-Metal Dielectric (IMD) silicon oxides tested, i.e., Undoped-Silicate-Glass (USG), Fluoro-Silicate Glass (FSG) and Tetra-Ethyl-Oxy-Silane (TEOS), were etched substantially faster than the other structural materials, i.e., aluminum ($Al$), titanium ($Ti$), titanium nitride ($TiN$), tungsten ($W$) and silicon-rich passivation nitride ($Si_3N_4$). This makes silicon oxide a good potential candidate as sacrificial material.

## III. THE SILICON OXIDE AS SACRIFICIAL MATERIAL

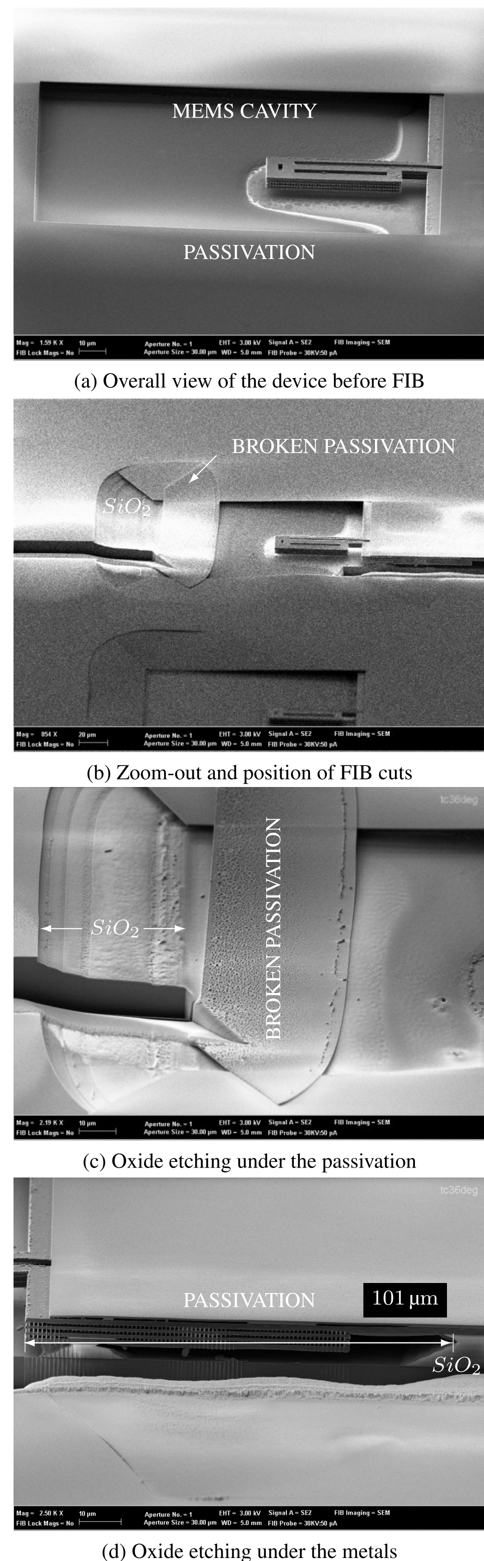
### A. GENERAL CONSIDERATIONS

A sacrificial material needs to combine several characteristics [46]: good selectivity, sufficiently high etch rate, good etch uniformity and ease of release. The selectivity of silicon oxide, compared with the BEOL metals is sufficient in our experience, as mentioned in previous section II-D.

The structure and doping of the silicon oxide ($SiO_2$) used in the CMOS process as insulating material is not uniform over the BEOL stack, as it depends on the specific deposition process. Different deposition techniques are used during the different FEOL and BEOL manufacturing steps. For example, Chemical-Vapor Deposition (CVD) is commonly used for the IMD oxide layers, like USG or doped FSG, that separate the different metal tracks. Thermally-grown oxide is used for the gate insulation, and doped CVD oxides, like Phospho-Silicate Glass (PSG) or Boro-Phospho-Silicate Glass (BPSG), are used in the Pre-Metal-Dielectric (PMD) between polysilicon and the bottom metal. Although we limit ourselves to the IMD oxide present in the CMOS metal stack, there are also differences between the oxide between different metal layers and the oxide between metal tracks on the same layer, as well as differences among the different layer levels. Some oxide layers are deposited using High Density Plasma (HPD) CVD. In addition, Silane ($SiH_4$) or TEOS ($Si(OC_2H_5)_4$) precursors may be used for oxide deposition. This lack of vertical uniformity in the oxide structure and composition leads to oxide layers with potential different etching rates that must be taken into account when performing the MEMS design.

### B. VERTICAL AND HORIZONTAL ETCHING RATES

Figure 2 shows a test structure used to demonstrate the different etching rates of the release agent. A multi-layer cantilever is released under a big passivation opening, as depicted




(a) Overall view of the device before FIB

(b) Zoom-out and position of FIB cuts

(c) Oxide etching under the passivation

(d) Oxide etching under the metals

**FIGURE 2. Anomalies of the etching speed under the SEM/FIB microscope. (a) Shows an overall view of a released cantilever under a big passivation opening. (b) Position of the FIB cuts used to investigate the etching on the same device. Note that the passivation was broken during the measurements due to the heavy underetch. (c) Etching below the passivation. (d) Etching in a narrow metal passage.**

in Figure 2a. Then, two FIB cuts are performed at both sides of the passivation opening, as shown in Figure 2b. The cut on the left shows how the oxide is etched under the passivation (see the zoom-in in Figure 2c) while the cut in the right shows how the oxide is etched in between the metals (see the zoom-in in Figure 2d). As it can be seen in Figure 2c, there is a slope in the etch profile with an angle smaller than 10°, pointing out to an etching speed 7× faster in the horizontal than in the vertical direction. In fact, even the different oxide layers can be readily identified in the picture.

The lateral etching speed may be affected by many factors, but the vertical etching speed was relatively stable, between $250\,\mathrm{nm\,min^{-1}}$ and $300\,\mathrm{nm\,min^{-1}}$. Typical release times for the 0.18 µm processes ranged from $25-35$ min in LF to around $45-55$ min in GF. These times match the expected etch length imposed by the vertical distance from metal 1 to the passivation opening, with some additional necessary lateral etch.

If the release process is performed outside the main CMOS foundry, it is important to carry out a pre-bake that will eliminate moisture (etch acceleration) and organic contaminants (etch deceleration) prior to release. Otherwise, non-repeatable results can be obtained.

### C. CAPILLARITY EFFECT

Capillarity, or capillary action, is defined in classical physics as the ability of a liquid to flow in narrow spaces or porous materials without any assistance. We use this term to refer to the accelerated etching reaction that we have observed when the vapor-*HF* release agent becomes in contact with the side walls of the metal layers. This happens around the edges of the metals, and not on the top or bottom of the metal plates: these are usually coated with a titanium (*Ti*) or titanium nitride (*TiN*) film. The coating layers are usually a few tens of nanometers thick and they are used as seed/adhesion layer or anti-reflective coating (ARC) to prevent reflections during mask photolithography. The effect of this capillarity on a MEMS cavity can be observed in figures 2a and 2d. As it can be seen, around the cantilever no oxide remains, but further from it there is still oxide in the substrate. In figure 2d, the *vHF* advanced between the electrodes of the device, traveling a distance of 100 µm (from the left to the right of the figure), and reaching the right side of the electrodes. It should be noted that no aluminum is etched, so this appears to be a catalytic reaction in which no structural material is lost. This effect is accelerated if two metals are separated by a small gap, and is particularly exacerbated if metal fillers are present (see Section IV-C) as they provide a significant lateral surface area and small gaps that catalyze the reaction.

In order to contain this effect within the MEMS cavity, no continuous lines that expose the sidewall of metal lines should be used to connect the MEMS with the electronics. Vias must be used to force the etching agent to move up and down, making its progress substantially slower as no acceleration occurs between different metal levels. Failure to do so is depicted in Figure 3, where the top metal is used for

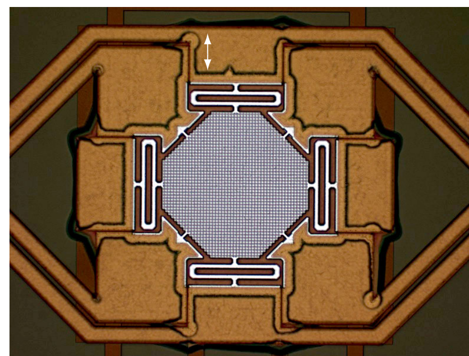


**FIGURE 3. Capillarity effect as seen under the optical microscope. Note that the release agent has progressed faster along the edges of the top metal covered by the passivation (shown in brown color), as indicated by the double arrow, in comparison with the oxide etched around the passivation opening.**

routing (shown in brown color). As it can be seen, the release agent has followed the metal edges far beyond the oxide etching around the passivation opening, compromising the structure and making the result unpredictable.

### D. THE PMD OXIDE

The Pre-Metal-Dielectric (PMD) oxide is placed below the bottom metal. In 0.5, 0.18 and 0.15 µm processes, at least part of this oxide is doped. The implantation process produces damages in the oxide lattice, breaking covalent bonds and enhancing the reactivity to hydrofluoric acid [46]. It is known that doped oxide is etched in vapor-*HF* two orders of magnitude faster than undoped oxide [39], [46], [47]. We have also observed that PSG and BPSG oxides etch very fast with vapor-*HF*. In our experiments this triggered an uncontrolled reaction that damaged the wafer. As doped PMD oxide is required for CMOS electronics manufacturing, the bottom of the MEMS cavity has to be sealed by a metal plate in order to prevent the release agent from reaching the PMD under any reasonable circumstance. Figure 4 shows the wafer damage as the etching agent reaches the PMD oxide. As it can be seen, the passivation is seriously damaged and whole metal plates are released away.

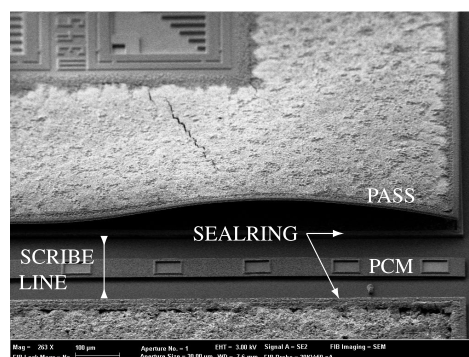



**FIGURE 4. Damage as result of the etching agent reaching the PMD oxide.**

### *E. WAFER ETCHING UNIFORMITY AND REPEATABILITY*

The *vHF* etching uniformity has been discussed in detail by the authors in a previous work [26]. Etching through release holes ranging from 0.48 µm$^2$ to 1 µm$^2$ produced a uniformity better than 3.3%. Note that this was achieved by preventing uncontrolled reaction caused by the so-called capillarity effect or PMD oxide etching.

## IV. THE PASSIVATION LAYER AS A RELEASE MASK

The passivation layer is used as a means to protect the CMOS die from external moisture and contaminants once the manufacturing is finished. Holes (passivation openings) are opened in standard CMOS processes in order to contact the top metal in the pads area, so wirebonding or bumping can be performed and the die can be electrically-connected to the external world. In the BEOL CMOS-MEMS approach, the passivation is also used as a release mask to define what areas are to be released by the etching agent. This approach has the lowest possible costs as it does not require any additional mask nor process step, but it must be used with care in order to avoid manufacturing issues.

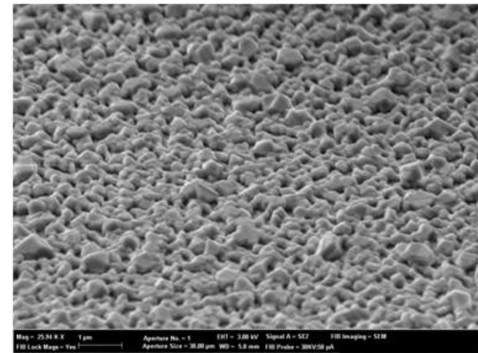
### *A. PASSIVATION SELECTIVITY*

The passivation is composed of silicon nitride, $Si_3N_4$. Standard silicon nitride is known to partially etch by the hydrogen fluoride, $HF$ and leave residues in the wafer [48]. However, its resilience against vapor-$HF$ can be greatly improved by increasing its silicon contents [44], which results on an increase of its optical refractive index (RI). In our experiments, when the refractive index increased to 2.45, additional protection was obtained. Without this additional protection, the passivation is heavily compromised, as depicted in Figure 5. As it can be seen in the zoom-in, the passivation becomes a granular, porous structure, unable to work anymore as a release mask and generating significant residues in the wafer and MEMS structures.

### *B. RELEASE RESIDUES*

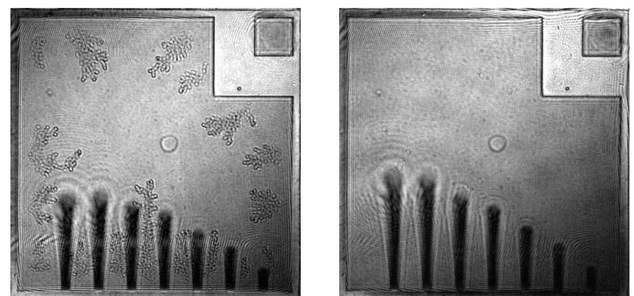
Even with increased silicon contents, a small part of the passivation is etched during the release process, leaving some residues in the wafer as byproducts of the chemical reaction between the different materials. The most abundant residue is ammonium fluoride ($NH_4F$), as result of the reaction between the passivation layer (silicon nitride, $Si_3N_4$) and the release agent (hydrogen fluoride, $HF$). Fortunately, ammonium fluoride decomposes upon heating in ammonia and hydrogen fluoride gases, following the reaction $NH_4F \rightarrow NH_3 + HF$. Figure 6 shows a microphotograph before and after heating up for 30 s at 200 °C a test structure composed of cantilevers, proving that the residues indeed disappear. This heating step does not significantly change the residual stress of the structures (see Fig. 9 in Valle *et al.* [49]).

(a) Damage to the standard passivation



(b) Zoom-in

**FIGURE 5. SEM image of a standard passivation damaged during the release with vapor-*HF* (a) and zoom-in revealing its new porous structure after the release (b).**



(a) Release residues before baking

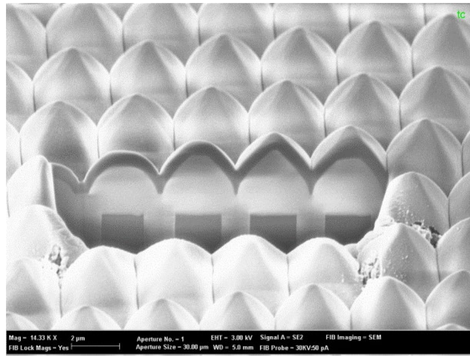
(b) Release residues after baking

**FIGURE 6. Microscope image of the release residues before baking process (a) and after baking in a hot plate for 30s at 200°C (b).**

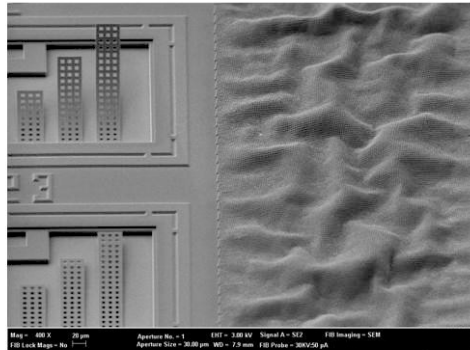
### *C. FILTRATION*

For the release, it is important that the passivation in planarized and non-conformal, that is, its surface cannot have a pattern depending on what it is below. This is also an important requirement when a pad RDL (Re-Distribution Layer) is needed, so CMOS foundries usually offer this as an option by depositing silicon oxide on top of the top metal, performing a CMP (Chemical-Mechanical-Polishing) planarization and then depositing the passivation on top.

If the passivation is conformal instead of planar, it no longer works as an effective etching barrier or release mask if there are structures immediately below it, that is, in the top

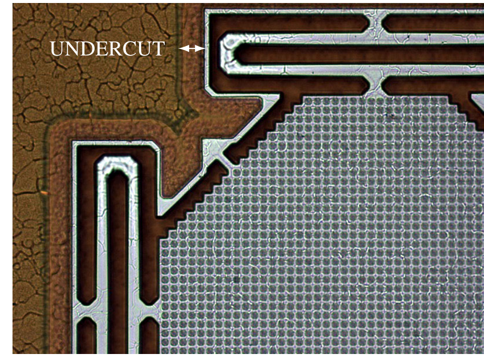


(a) Conformal passivation before etching

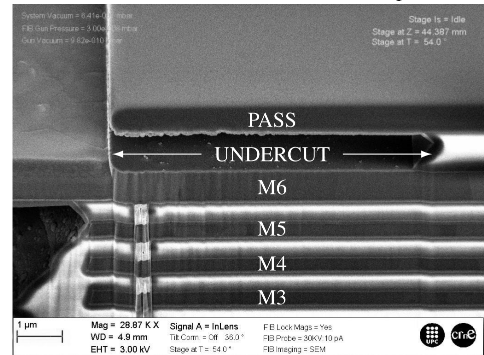


(b) Conformal passivation etching result

**FIGURE 7. Conformal passivation etching example: (a) FIB cut before etching, revealing how the top metal filling affects the passivation planarity. (b) After etching, showing how the release agent has penetrated the passivation over the metal filling area.**




(a) Undercut as seen with a microscope




(b) Undercut as seen with a SEM

**FIGURE 8. Images of the passivation undercut near an opening as seen with an optical microscope (a) and with SEM after a FIB cut is performed (b).**

metal. This can be seen in Figure 7a, where a metal filling pattern of little squares was placed in top metal in order to guarantee appropriate metal density for manufacturing. This pattern, as the passivation was conformal, was translated to the passivation surface as small bumps. This topography was proven to be very weak as *HF* barrier, as the release agent filtered through it and compromised everything below, as it can be seen in Figure 7b. Note that the passivation itself was not damaged, neither this had any effect outside the metal filling area, effectively revealing the nature of this phenomenon. The underlying reasons for the filtration are unknown, but it could be related to the poor step-coverage capability of the passivation and to its reduced thickness when deposited over a non-flat surface. This could cause the *vHF* to leak into some weak spots and have a reaction catalyzed by the limited flow of water-binding agents and carrier gas into these spots.

### D. UNDERCUT

As shown in Figure 1, in most 0.18 μm processes there is a layer of silicon oxide between the passivation and the top metal. This layer allows planarizing the passivation, but it is etched as any other oxide, causing the passivation to become unattached and hang from the wafer around the passivation openings. Figure 8 shows this effect as seen under an optical microscope and under a SEM. This effect causes the passivation to be weak near the passivation openings, breaking easily as there is nothing below to support it. Likely, the material will fall into the cavity (see Figures 2b and 2c), causing a malfunction of the MEMS or a tool contamination that limits production yield. There is no design solution to overcome this problem, becoming necessary either a process modification so the oxide is not exposed or a sealing step so the passivation is protected against damage. As seen in previous section IV-C, depositing the passivation directly over the metal without any oxide in between is not an option either, as the deposition will become conformal and the release agent will filtrate through it.

Passivation undercut has a significant impact on pads also. The metal under the passivation opening needs to be extended, so the release agent does not travel beyond the pad head and reaches the electronics or interconnections below. With our MEMS designs, this distance was set to 20 μm to safely account for all process variations. Alternatively, in order not to loose too much area in the pad ring, a process modification can be implemented so the passivation openings of the pads is done after the release has taken place, effectively requiring an additional process mask and step. The pad passivation undercut can be optically measured and has been previously used for estimating the etch oxide ratio [26].

### E. SCRIBE LINES

In some CMOS processes, the scribe lines are patterned in order to generate a deep trench between the dice and thus allow easier die singulation. However, leaving the scribe lines without a protective passivation layer on top may cause important damages to the wafer during the *vHF* release step. Figure 4 shows the result of *vHF* etch on a wafer with scribe lines not covered with passivation. Clearly, all the oxide down to the silicon wafer has been etched, and an uncontrolled reaction has taken place, yielding the wafer unusable.

If scribe lines are not protected, a ring of continuous vias around the CMOS die is necessary in order to protect the die from the *vHF* coming from scribe line region. In some foundries, the die seal ring already implements such structures in order to prevent contaminants to penetrate it after singulation.

### F. PCM TEST STRUCTURES

In production environments, CMOS foundries place PCM (Process Control Monitoring) structures between the dies in order to verify that the wafer passes the corner criteria, that is, that the CMOS circuits are manufactured within specification. Unfortunately, these structures have passivation openings, hence, they get etched, generating a significant amount of residues and an uncontrolled etched reaction when the release agent reaches the doped oxide of the PMD below the bottom metal, as shown in Section III-D. Figure 4 shows PCM structures placed by the foundry between two dies. Figure 9 shows damaging effects of PCM structures with pasivation openings after MEMS release.

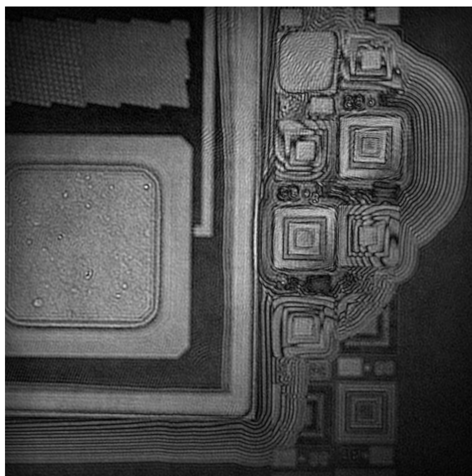
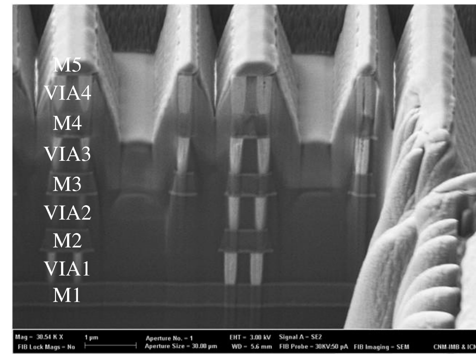


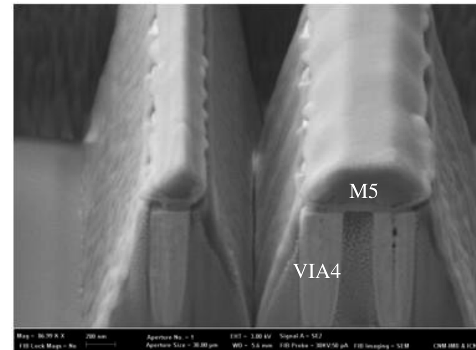
**FIGURE 9.** Uncontrolled release of unprotected PCM structures close to a pad. Image taken with an optical holographic microscope.

### G. PASSIVATION OVERETCH AFFECTING BEOL METAL STRUCTURES

Passivation overetch and undesired metal etch is a potential side effect of using the passivation as a release mask.




(a) Metal overetch




(b) Zoom-in

**FIGURE 10.** SEM image of an unreleased MEMS device without protective metal top (metal 6) showing metal 5 and oxide overetch (a). Zoom-in showing the little remaining metal (b).

Passivation openings are intended and designed for pad openings, and therefore expected to have top metal in below, acting as a etch stoppers for the passivation etch. If no metal is present, the etching will penetrate down below and may affect the mechanical properties of the exposed metals under the oxide. Usually the top metal is used only as a cavity seal and it is significantly thicker than the metals below it, making this overetch unimportant. However, overetching of the metals in below, which have a reduced thickness and belong to the structural parts of the MEMS, may have a much significant impact on the MEMS characteristics. Figure 10 shows the impact of metal overetching. In the picture, the top metal was not present over the MEMS device, so the passivation etching took away a significant portion of the metal below it (metal 5) and the oxide around.

It should be noted than in most cases the overetching does not have such a serious impact as depicted in Figure 10. However, in certain process corners it does, so it requires monitoring. By experimenting with different processes, we have found that, the thicker the oxide below the passivation is, the more control is required in the passivation etch. Therefore, thin passivation oxide is preferred in order to pattern the passivation and oxide reliably without affecting metals below. Additionally, adding a top metal protective capping with small release holes helps to greatly reduce this effect.

## V. THE BEOL AS STRUCTURAL MATERIAL

Structural materials are used to build the MEMS itself. When only a vapor-*HF* agent is used for release, there are three main structural materials that can be used in the CMOS-MEMS design, namely:

- Metals, mainly a metallization layer composed of aluminum ($Al$) with some small percentages of copper ($Cu$) and, sometimes, silicon ($Si$). Each metallization layer is coated by a thin ($10 \sim 70\,\mathrm{nm}$) titanium/titanium nitride ($Ti/TiN$) layer on both top and bottom, used, among other reasons, as seed layer and anti-reflective coating (ARC) to prevent reflections during subsequent masking steps.
- Vias, usually made of tungsten ($W$). In the pure CMOS process they are used for electrical connection between different metal layers. Again, a seed layer of titanium/titanium nitride is usually deposited before the tungsten.
- Unreleased silicon oxide ($SiO_2$), generally enclosed within metal and continuous via ring structures, so the release agent cannot etch it. If desired, silicon oxide may be the main material of the MEMS structure.

Silicon is not available as a structural material, as it is unaffected by vapor-*HF* and thereby it cannot be patterned. However, other groups [50], [51] have used polysilicon for building resonators with $0.35\,\mu\mathrm{m}$ processes, for instance. Additional materials are those included in the Metal-Insulator-Metal (MIM) capacitor options offered in standard CMOS processes, which generally use silicon nitride as a dielectric layer.

### A. RESIDUAL STRESS OF METALS AND COMPOSITE LAYERS

One of the major hurdles when designing CMOS-MEMS with the BEOL layers is dealing with the high residual stress gradient and associated curling of the structures. Both the large curvature displayed by BEOL structures and, more importantly, its poor repeatability, pose an important challenge to CMOS-MEMS designers. In addition, it was found that surpassing certain time-dependent temperature conditions after release lead to important curvature shifts. In particular, temperatures higher than 300 °C caused a noticeable effect even with exposure times as small as 1 minute. The density of vias between two metal layers does not change the curvature. However, a ring of continuous via between two metal layers was found to strongly affect the curvature of cantilevers. Fortunately, the curling issue can be greatly improved by using composite stacks of layers of metal, tungsten and oxide. In figures 11a and 11b the metal stack M5-M6 is clearly much less curved than a single metal stack. This has already been discussed extensively in a previous work of the authors [49]. Interestingly, in some cases, the large curvature can lead to bi-stable structures that may display completely different shapes after the release: one case is a cantilever folded along its length (bottom cantilever in figure 11c), and the second stable shape is when it is in an extended state and it is folded in a tube-like manner (two top cantilevers in figure 11c). This second case results in a very straight structure given the increased bending stiffness of the final geometry.

It was found that the effective stress is tensile. This was initially observed qualitatively with test structures using rotary pointers [52], as depicted in figure 11d and later confirmed by measuring the resonance frequency of clamped-clamped (c-c) beams of different lengths. The resonance frequency versus the length curve matched very well the one of axially stressed c-c beams with a certain tensile stress, independent of the beam length.

### B. DETACHED VIAS

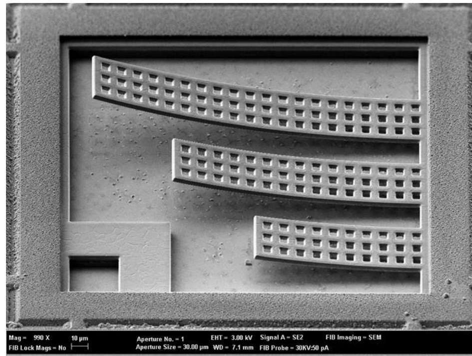
Vias are an important structural material for keeping metal lines mechanically attached together. However, it is important to keep in mind that vias are attached to the bottom metal layer with a $TiN$ layer. Although titanium nitride is very slowly etched, long etch times may decrease the via structural integrity. Additionally and more importantly, due to the structural material stress, they can be easily detached from their structure, as shown in Figure 12. Depending on the stress, on a fully etched structure a minimum via density has to be reached in order to keep metal lines together. Maximum via density is generally recommended in order to maximize structural robustness. An alternative and preferred option is to have a ring of continuous vias, between two metal layers, that encloses and protects the oxide from being etched. The increased adhesion provided by the oxide to the top and bottom metals confers a much greater structural robustness, and no detached layers have been observed in this case.

## VI. ALUMINUM SPUTTERING AS CAVITY SEALING

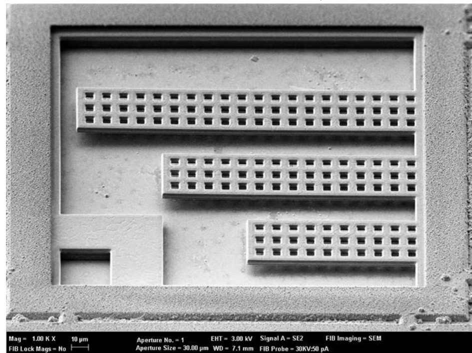
Most MEMS sensors require sealing in order to prevent moisture and contaminants to enter the cavity, or to allow for a standard, low-cost, CMOS-compatible wafer handling and packaging or even to allow operation in vacuum. Lowest-cost sealing is aluminum sputtering, that is, the deposition and patterning of an aluminum layer on top of the passivation, as if another regular CMOS metal layer or Re-Distribution Layer (RDL) was deposited. Be aware that, as the patterning of the sealing layer could affect the aluminum pads, they need to be covered by the aluminum-sputtering sealing layer. Figure 13 shows a FIB cut of a CMOS-MEMS sensor before and after sealing. Note that all holes have been covered. Also note that, due to the insufficient step coverage of the sealing, placing cavity holes near the passivation-opening edge could prevent a hermetic seal, which was observed in some of the tests.

### A. SPUTTERING PRESSURE AND TEMPERATURE

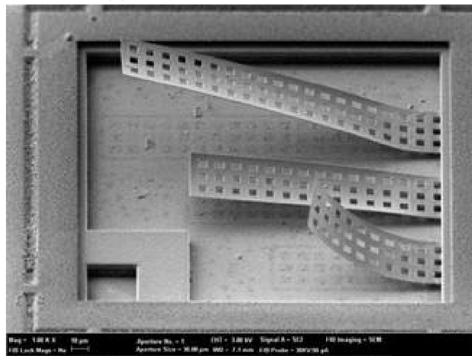
The sputtering deposition was carried out at a very low pressure (less than $10\,\mu\mathrm{bar}$) in Argon ($Ar$) plasma. Obtained film adhesion was excellent as no film detachment was observed. Two sputtering deposition temperatures were tested: 180 °C



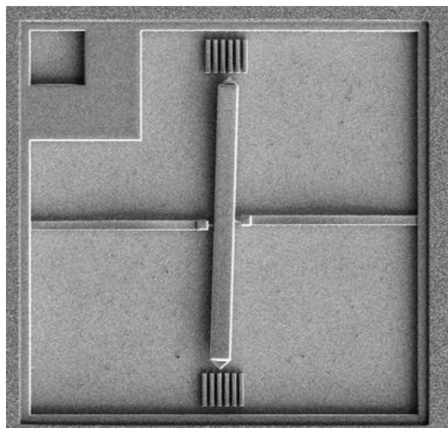
(a) Cantilevers with only M5



(b) Cantilevers with M5 and M6

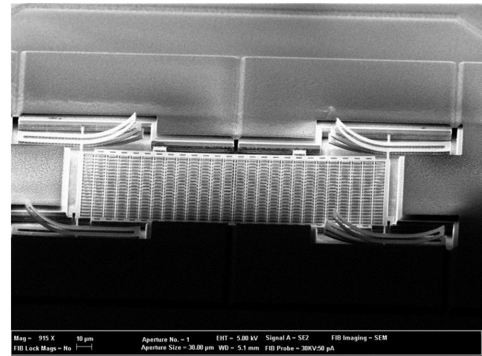


(c) Bistable cantilevers

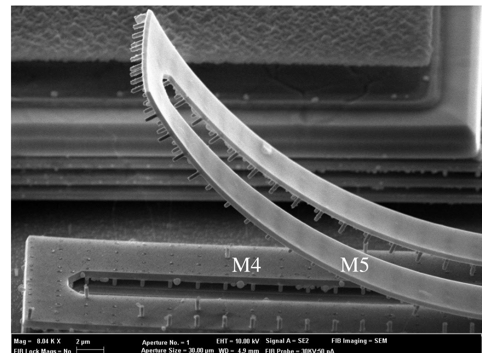


(d) Rotary pointer (M345)

**FIGURE 11. SEM images of test cantilevers with different metal compositions (a)-(c) and a rotary pointer of a M345 stack that shows deformation compatible with tensile stress (d).**



(a) Detached vias



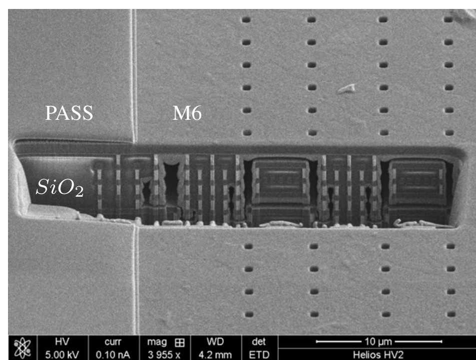

(b) Zoom-in

**FIGURE 12. Detached vias on MEMS device arms as seen through a SEM (a). Zoom-in showing the individual vias (b).**

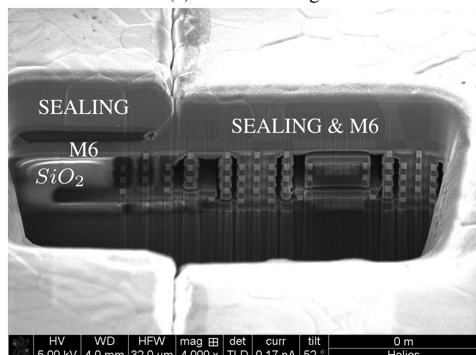
and 350 °C. The highest temperature yielded the best results in terms of sealing. For example, the highest deposition temperature led to improved step coverage. This is an important feature for sealing release holes, which have vertical sidewalls. However, the maximum deposition temperature will be limited by the released MEMS ability to withstand the thermal budget with minimal yield loss. Lower temperatures will probably require a thicker sealing layer. Also, higher deposition temperature may lead to higher residual stress and premature out-gassing that yields higher cavity pressure. This, although expected, was not confirmed experimentally.

### B. TOP-METAL HOLE SIZE

In addition, top-metal hole size has a direct effect on the sealing reliability. Figure 14 shows a sealed test structure with different release hole sizes. The smallest hole did not comply with the design rules and was not opened correctly, so the oxide below could not be etched by the *vHF*. Larger holes were correctly opened, but significant aluminum was deposited below the largest hole. For this reason, it is important to use the smallest release hole size allowed by the design rules. Choosing smaller holes will not have an impact on the *vHF* etching rate [26]. In addition, placing the release




(a) Before sealing




(b) After sealing

**FIGURE 13. SEM image after FIB cuts of a CMOS-MEMS before aluminum-sputtering sealing (a) and after it (b).**

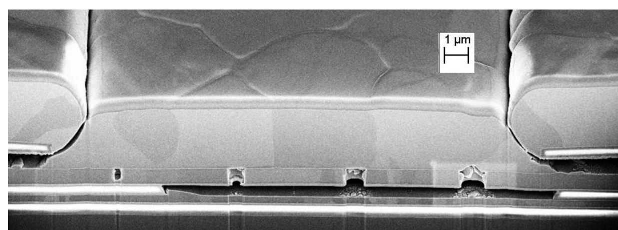
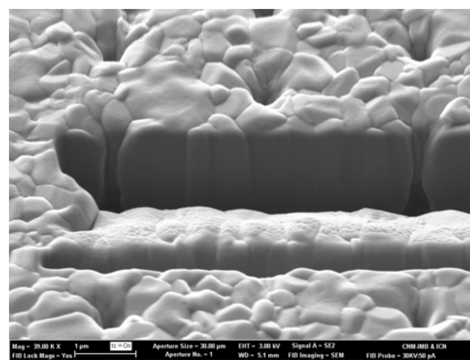
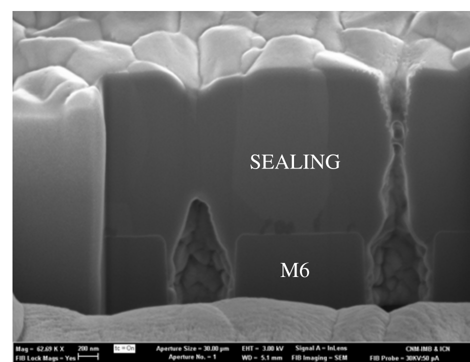


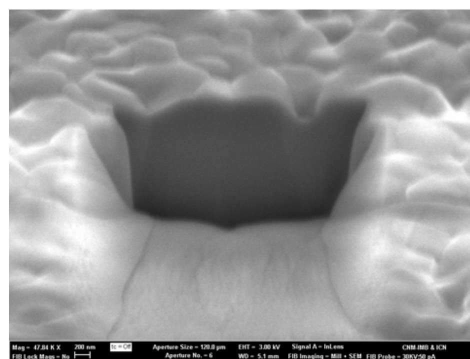

**FIGURE 14. Test structure for release hole sizing and aluminum sputtering sealing. Sealing is 3 μm-thick. Holes are of 0.4, 0.6, 0.8 and 1.0 μm size.**



(a) 1.0 μm-thick deposition. Most holes not sealed.




(b) 1.5 μm-thick deposition. Some holes not sealed.



(c) 2.0 μm-thick deposition. All holes sealed.

**FIGURE 15. Reliability and hermeticity of the sealing as a function of layer thickness.**

holes over areas with no movable structures below was found beneficial: failure to do so may lead to reduced performance and lower yield.

Once the release hole was fixed to 0.9 μm (minimum allowed size), several sealing thickness were tested, as shown in figures 15a to 15c. With a total deposited thickness of 2.0 μm all the release holes were correctly sealed. This was assessed by measuring the Q factor of several sealed resonators. In order to improve the safety margin and reliability of the sealing process, thicknesses of $3.0 - 3.5$ μm were routinely successfully used. The release hole topography was still observed on the top surface of the sealing layer with a 2.0 μm-thick deposition, but a flat surface was obtained with $3.0 - 3.5$ μm-thick layers (see figure 14).

### C. OUTGASSING AND FINAL PACKAGING

Some MEMS devices require operation on high-vacuum, like resonator structures. During our research, we observed that pressures inside the MEMS cavity after sealing were over 1 mbar. In order to reduce this pressure, a pre-outgassing step, consisting on raising the temperature to several hundred degrees Celsius for a given period of time, was added prior to sealing. This allowed to achieve average cavity pressures around a few hundred μbar. We have also observed that devices with higher surface of oxide exposed to the cavity compared to the total cavity volume, consistently yielded higher pressure levels. This indicated that the oxide is the main responsible for the observed out-gassing. In order to

achieve lower cavity pressure, the oxide area should be minimized, or the cavity volume increased. It should be noted, that similarly to the maximum sputtering temperature, the released MEMS devices need to be able to withstand the pre-out-gassing thermal budget. So, it is very important to fabricate MEMS devices that show no yield drop nor significant performance loss after high temperature profiles are applied. A clean cavity is crucial for a good sealing process, as similar commercial sealing processes have shown [42].

Some tests were also carried out with QFN packages in order to assess the out-gassing temperature-time dependence. The cavity pressure was inferred from the Q factor of the devices. For this calculation, the gas in the cavity was assumed to be nitrogen, although it may be argon or a mixture of moisture and other species. Results indicated that out-gassing was exacerbated over $125 - 175\,^{\circ}$C. Some samples were kept at 150 °C for 1000 hours. Results showed a cavity pressure increase from 200 µbar to 900 µbar after 200 hours and to 2 mbar after 1000 hours. Similar samples underwent 85 °C for 8000 hours, and the cavity pressure only increased from 200 µbar to 1 mbar. Finally, some samples have been kept at room temperature for more than six years showing no Q factor decrease. Final measured yield was above 95% in packaged samples.

## VII. CONCLUSION

In this paper we have shown the main issues regarding high-volume production of BEOL CMOS-MEMS devices and how they can be prevented. From the experience obtained during years in design and test of CMOS-MEMS wafers, several guidelines have been pointed out to obtain robust devices capable of attaining more than 95% yield after packaging. We have classified the main issues we encountered in four main categories, namely, those related to the sacrificial material (section III), to the release mask (section IV), to the MEMS structure (section V) and to the cavity sealing (section VI). We have shown the main manufacturing techniques for low-cost fabrication along with the associated failure mechanisms and how to prevent them. Extensive SEM imaging and FIB cuts have been performed in order to pinpoint the issues and test the implemented solutions.

Results indicate that low-cost manufacturing of high-yield CMOS-MEMS devices is certainly possible, although many problems can arise during the sensor design and process definition that will require a thorough scientific investigation to overcome. By means of the disclosed results and the proposed guidelines, it is our hope that this study will help process and MEMS engineers in speeding-up the research and development of their own CMOS-MEMS devices as well as increasing their manufacturing yield.

## ACKNOWLEDGMENT

The authors would like to thank Laura Barrachina and Sandra Aguilar from Baolab Microsystems, S.L., for their assistance during the measurements.

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