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Design Optimization and Electro-Thermal Modeling of an Off-Board Charging System for Electric Bus Applications

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ABSTRACT This paper proposes a co-design optimization procedure of a high-power off-board charger for electric vehicle (EV) applications. The primary purpose is to design a 175 kW SiC DC-charging system with high power density to achieve high efficiency at a wide operating range. For the active part of the DC off-board charger, a three-phase active front end (AFE) rectifier topology is considered in the design optimization and the modelling. The design methodology focuses on the optimal design of the passive filters, accurate electro-thermal modelling of the converter, inductor design, capacitor selection, loss and geometric modelling of the passive filters and control system design. The design optimization of the high-power charging system is performed in MATLAB Simulink using a closed-loop dynamic electro-thermal simulation of the off-board charger. The switching frequency, loss and temperature-dependent efficiency of the charger is investigated in parallel. Through this proposed technique, efficiency greater than 96% is achieved at a switching frequency of 40 kHz, along with a smaller size and lower weight of the system. Moreover, it operates with a current total harmonic distortion (THDi) below 3% and a power factor (PF) above 99% at rated power condition.

INDEX TERMS Co-design, thermal modelling, AFE rectifier, wide bandgap, SiC, passive filter, electric vehicles, fast DC charger.

I. INTRODUCTION

In the current era, battery electric vehicle (EV) technology has become popular because of its positive effects on climate change. In cities, public transport operators are integrating battery electric buses (BEBs) into their traditional fleets, but to be operational, they need to be charged frequently [1], [2]. In practice, there are two common strategies to charge BEBs: overnight charging or opportunity charging [3]. Overnight (depot) charging is typically used for BEBs, which have a large battery on board and do not need to be recharged during the day. Opportunity charging requires the BEB to charge during operation at end stations or bus stops. In this case, the BEB is generally equipped with smaller batteries in order to have it charged in only several minutes. However, both strategies require DC chargers. Such chargers consist of power electronic converters (PECs), which convert AC power from the grid to DC power to charge batteries, as depicted in Figure 1 and Figure 2. Unidirectional or bidirectional PECs can be used for the off-board charger depending on whether Vehicle-to-Grid (V2G) features are desired or not [4].

In this paper, two topologies are discussed, which can be considered for high power Off-board charger design. The first topology converts three-phase incoming AC power to a variable DC output power. This topology consists of a low frequency (LF) isolation transformer, an LCL filter, an AC/DC bidirectional converter and a DC link LC filter, as shown in Figure 1(a). The second topology consists of converting incoming AC power to a fixed DC output, which is then

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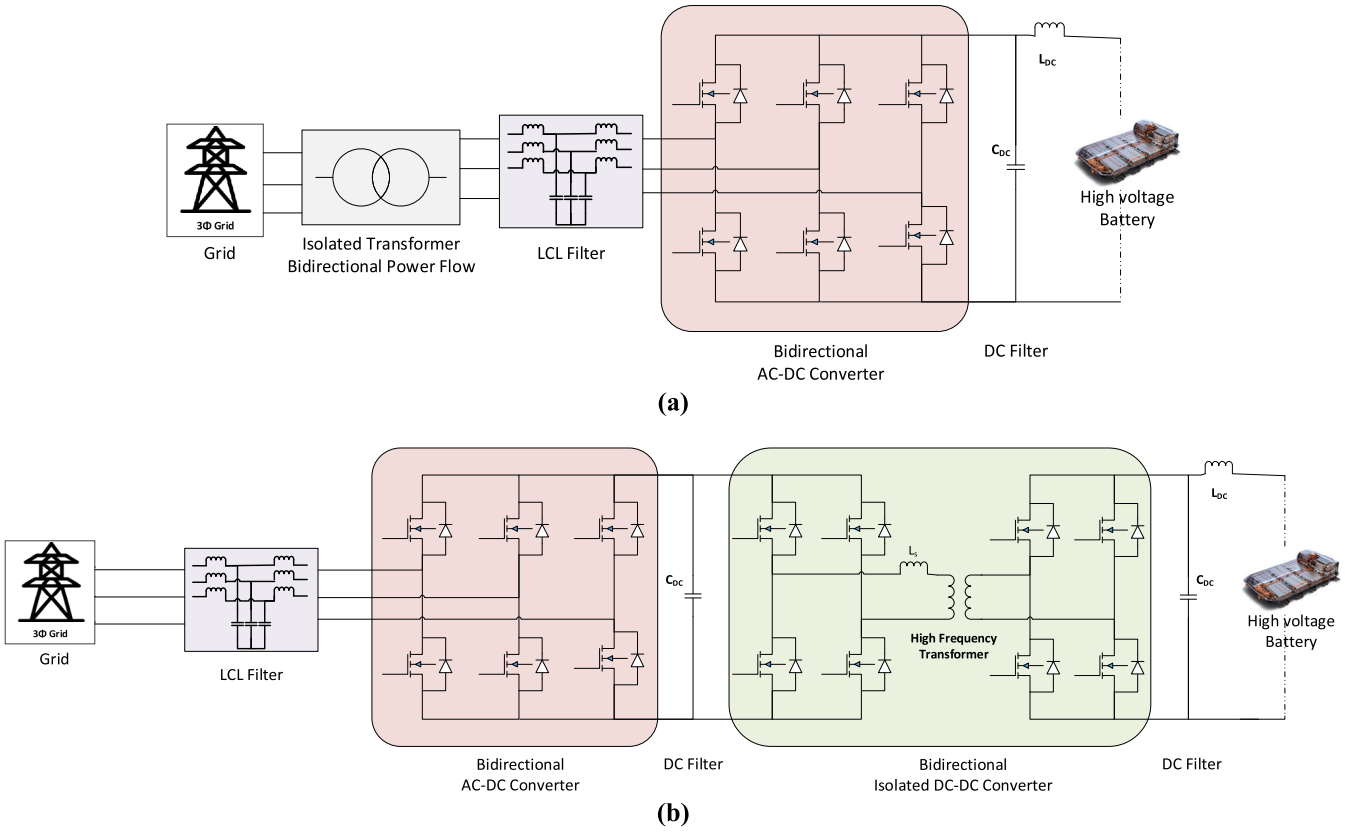

FIGURE 1. Multifunctional off-Board charger; without DC-DC converter (a), with isolated DC/DC converter (b).

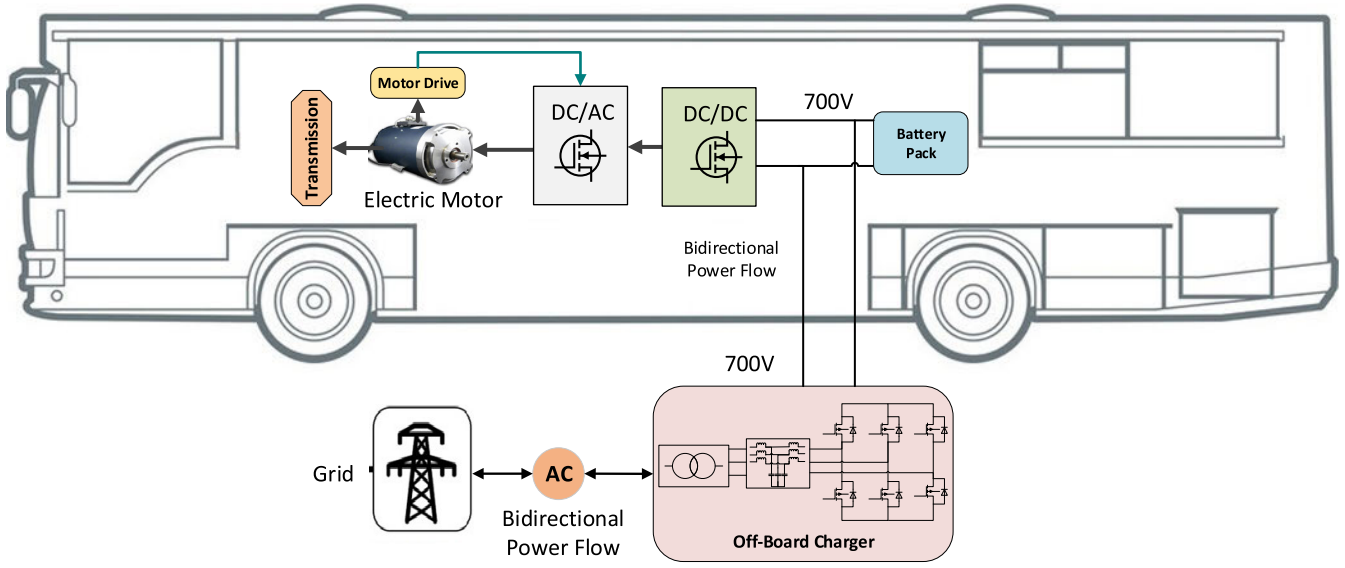

FIGURE 2. Off-Board charging arrangement for fast DC charging of BEBs.

converted to the demanded voltage of the EV using a DC/DC converter. This topology contains an LCL filter, an AC/DC bidirectional converter, a DC filter, an isolated DC/DC bidirectional converter with a high frequency (HF) transformer and a DC link LC filter [5] as shown in Figure 1(b). Both methods are equally valid and have no prime advantage or disadvantage [6]. However, this research only focuses on designing the DC off-board fast-charging system using a LF grid transformer. The presence of passive filters greatly affects the size and weight of the charger; hence size and weight of passive filters are calculated with power modules, gate drivers, sensors and heatsink.

TABLE 1. Type of chargers [9].

Type of Chargers	Location of Charger	Power Supply/Output
Level 1	Single phase On-board	Vac: 230 Output: 12-16 A (~1.44 kW to ~1.92 kW)
Level 2	Single / 3 phase On-board	Vac: 400 Output: 15-80 A (~3.1 kW to ~19.2 kW)
Level 3 DC Fast Chargers (DCFC)	Three-phase Off-board	Uses a three-phase Vac: 208-600 AC circuit converted to DC to the vehicle. Output: Up to 500 A (50kW up to 350 kW)
Next Generation: Ultra-Fast Charger (UFC)	Three-phase Off-board	Uses a three-phase Vac: 208-600 AC circuit converted to DC to the vehicle. Output: 800V, 400kW or more

The three-phase front-end AC/DC PEC can include a diode rectifier, an active buck/boost rectifier or a Vienna rectifier [7]. The simplest and most cost-effective approach for the AC/DC conversion is a diode rectifier. However, the fixed output voltage depends heavily on the three-phase supply voltage. The disadvantage of this method is an unfavorable total harmonic distortion (THD). Implementing a multi-pulse rectifier can enhance the THD of the line current, but it requires a more complex transformer and rectification diodes. A three-phase active front-end (AFE) rectifier tackles the issue of THD by generating a three-phase sine shaped input current with improved power factor and efficiency and offers a variable DC output voltage. The Vienna rectifier becomes increasingly popular, and it can be adequate where unidirectional power flow is essential [10]. Among all these three-phase AC/DC conversion techniques, the AFE boost rectifier is the best option for an off-board charger [11]. From the design point of view, it is necessary to consider several elements in the development of the AC/DC PEC, i.e., high efficiency, high power factor, cost-effectiveness, small system size and weight, distortion-free operation with limited grid impact and high reliability. The existing types of EV charging systems are briefly described in Table 1. The level-1 and level-2 chargers are used as on-board converters for running power to the batteries, but the level-3 charger typically works as an external converter, and it can effectively manage the flow of high power. The fast DC charger is associated with level-3 and next-generation charging [7], [8].

The most essential components of the PEC are the switches. At charging stations, the switches of the PEC convert AC voltage into DC voltage for the BEBs, allowing them to connect and charge their batteries, as depicted in Figure 2. In Figure 2, the bidirectional off-board charger connects to the 700V high voltage battery pack of BEBs. The high-voltage battery pack is connected with a buck DC/DC converter inside the vehicle, which feeds the inverter to drive the electric motor. A lot of research is going on semiconductor materials based on which the switches are built. Nowadays, the switches inside the PECs are based on silicon (Si) IGBT semiconductor technology. However, new insights in switching technology have stimulated the development of wide bandgap (WBG) semiconductor materials like Silicon Carbide (SiC) and Gallium Nitride (GaN) [6], [7]. These new WBG semiconductor materials provide interesting characteristics and advanced material properties compared with traditional Si semiconductors, i.e. operating at higher voltages and lower leakage current, higher electron mobility, electron saturation velocity and higher thermal conductivity. They require more than 1eV or 2eV of bandgap energy to transfer an electron from the highest energy level of the valence band to the lowest energy level of the conduction band within the semiconductor. A comparison of material properties between Si, SiC and GaN is shown in Figure 3. The enhanced material properties of WBG semiconductors will allow the new generation of PECs to achieve higher efficiency at a reduced size and weight [10]–[12]. Even today, innovative research is still required to integrate these WBG devices into existing applications.

High power charging systems require more enhanced thermal management solutions to avoid dangerous thermal runaways and anomalies at high power operation points. Therefore, researchers are highly interested in exploring innovative techniques for the high-precision thermal distribution and system losses using high-speed simulation models for long-time mission profiles [13]. Accurate thermal investigation of a PEC can be achieved using PLECS, SPICE and SABER based simulations.

There are several generic techniques for optimization; in such a generic technique, the equation-based script is designed at a static value to estimate the converter current,

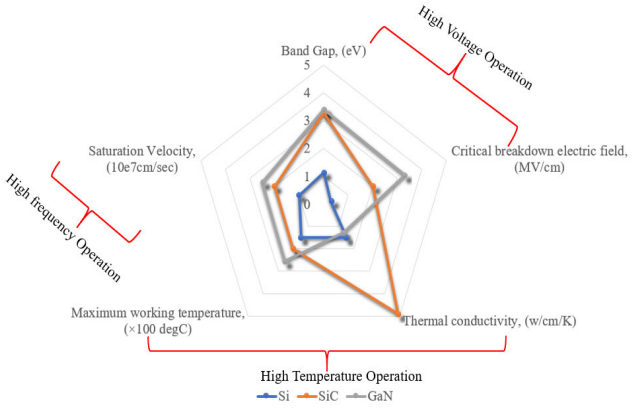

FIGURE 3. Material properties comparison of Si, SiC and GaN.

passive filters, power loss, efficiency, and weight and volume. The suitable devices and components are selected from the database using an optimization algorithm. The design optimization is carried out using a multi-objective algorithm based on an improved genetic algorithm (IGA) to quickly search for the optimal parameters [14]. In comparison with conventional single-objective optimization, the non-dominated sorting genetic algorithm (NSGA-II) is able to solve a complex design with multiple objectives [14], [15]. The main principle of NSGA-II is to alter the optimization variables with crossover and mutation operators and select the next generation's population based on the Pareto front dominance [17]. The system ripples, non-linear switching characteristic during turn-on and turn-off, and accurate power losses estimation with respect to the instantaneous current and voltage are not included in the generic framework, but the proposed technique has some advantage over it.

This paper proposes an approach for the co-design optimization of a 175kW off-board charger based on SiC technology, using a dynamic electro-thermal simulation model. The purpose is to achieve high efficiency, a high-power factor, a minimum THD of current, lower weight, and smaller PEC size compared with existing solutions in the market.

In Section II of this paper, the co-design optimization framework is clearly illustrated using the dynamic simulation model. In Section III, the design procedure of the off-board charger and all information regarding its topology are described together with the optimal design strategy of the passive filters, i.e. LCL filter and DC filter. The devices and components with their part numbers, which will be used for the development, are also stated. Section IV explains the design procedure of the electro-thermal modelling of the converter using mathematical equations and parameterization based on a datasheet. Thermal modelling of the power module and heatsink modelling are also included here. Section V is dedicated to passive filter design and modelling. The detailed route of inductor design i.e. core selection and core winding, loss modelling of the inductor and the capacitor and an estimation of the mass and volume of the PEC are illustrated. The DC bus voltage control approach of the AFE converter and the efficiency estimation using the total charger losses are arranged in section VI and VII, respectively. In section VIII, the optimized parameters of the off-board charger are achieved in terms of switching frequency, passive filters, efficiency, losses, power density, specific power, size and weight. Next, a system stability analysis is performed in section IX. Finally, the performance of the off-board charger is shown in Section X, and the main conclusions are described in Section XI.

II. CO-DESIGN OPTIMIZATION FRAMEWORK

The AFE rectifier topology consists of a transistor and anti-parallel diodes, a three-phase boost passive filters (L, LC or LCL) on the AC side to compensate the harmonics of line current and to achieve sinusoidal waveforms, and a DC capacitor for filtering of ripples at DC side. Moreover, electro-magnetic interference (EMI) chokes can also be added to filter unwanted noise due to the switching [4].

The proposed technique is applied in the same way as a generic framework of optimization works. However, this methodology has some advantages over the generic framework. Every component and device are modelled in a dynamic simulation to add the effect of the switching frequency and the system's ripples on power losses, temperature, and efficiency. In the electro-thermal simulation design, it is presumed that every component is behaving like an actual component. Therefore, extra features have been added in the simulation, i.e. closed-loop control, accurate loss and thermal model of a power module, accurate passive filter loss model (inductor core, inductor winding and capacitor) and heatsink model with their size and weight. After developing the closed-loop electro-thermal simulation model, it is then applied for design and optimization.

This optimization technique is performed with an integrated dynamic electro-thermal simulation model of the off-board charger. Numerous calculations are conducted to estimate the required passive components, losses, efficiency, mass, and volume with respect to the switching frequency, AC frequency, AC/DC voltage-current and power. The different steps in the co-design and optimization process of a high-power charging system are listed below. The methodology is shown in the block diagram in Figure 4.

1. Mathematical calculation of the passive filters
2. Accurate closed-loop electro-thermal simulation design of the AFE converter
   a. Parameterization of the power modules using a datasheet
   b. Loss and thermal modelling of the power module
   c. Loss modelling of the passive filters
   d. Cooling system modelling
   e. Closed-loop control of the AFE converter
   f. Efficiency estimation
   g. Mass and volume calculation
3. Initialization with the off-board charger specifications
4. Running optimization algorithm

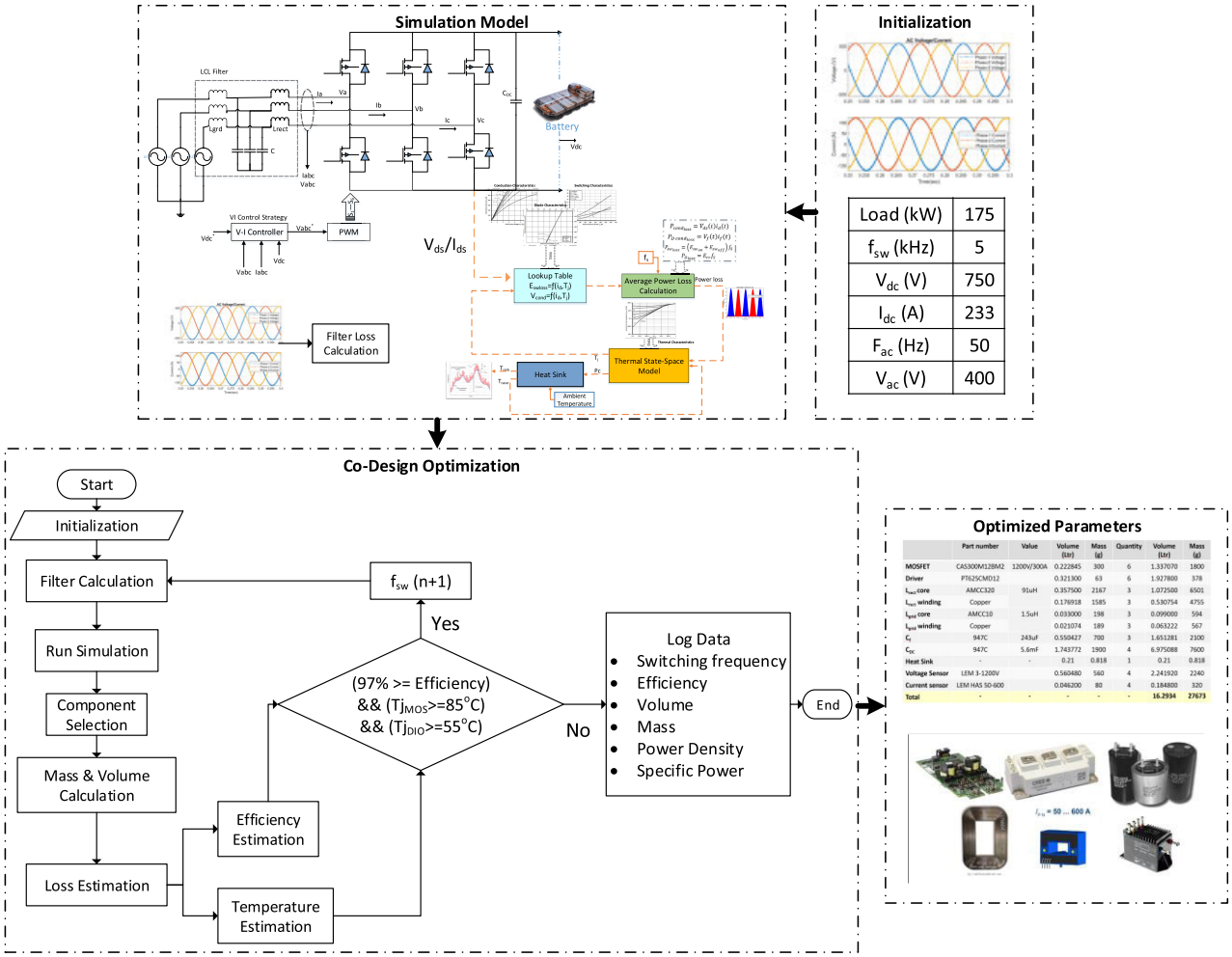

FIGURE 4. Co-design optimization procedure for the SiC-based off-board charger.

5. Collecting optimized parameters
   a. Efficiency
   b. Maximum switching frequency
   c. Filter components
   d. Mass, volume, power density and specific power

The flow chart consists of four main blocks: the simulation model, the initialization, simulation model, the co-design optimization, and optimized parameters. This methodology is compulsory to make a database of devices and components; it contains information about all electrical, thermal, mechanical, and geometrical characteristics of switching devices (SiC MOSFET), diodes, inductors capacitors, transformers, gate drivers and heatsinks. An automated algorithm is used to select the best database components. The calculations of the current, voltage, power losses, mass and volume of the transistors, diode, heatsink and passive components are being solved in the optimization process. In this way, the optimal solution is obtained to design a 175kW off-board charger with a low-frequency transformer.

In this approach of simulation-based co-design optimization, the first step is the simulation modelling according to the topology and specifications of the charger. The design specifications of the off-board charger is shown in the initialization block in Figure 4. The optimization algorithm is initialized with the parameters according to these specifications and calculates the filter parameters. Then, the simulation model is run, and the components are selected from the database according to the specified switching frequency. Next, the mass and volume of the off-board charger are calculated, and the losses are estimated. The MOSFET's and diode's efficiency and junction temperature are measured at the end of each simulation run. If the efficiency is greater than the constraint efficiency, and the junction temperature of the MOSFET and the diode are less than the set value. In that case, the next iteration of the simulation takes place with a higher switching frequency and new filter parameters. If the efficiency and the junction temperatures do not meet the set condition. In that case, the simulation will be stopped, and all parameters will be logged, i.e. switching frequency, efficiency, volume, mass, power density and specific power. After the completion of the optimization algorithm, the optimal parameters are obtained, together with the selected components and devices.

TABLE 2. Off-board charger design.

Parameter	VALUE
Efficiency	>96%
Power Factor	>0.99
Input Current Harmonics (THD)	<5%
Output Voltage (V)	600-800V
Output Current	200-300A
Output Power	175kW

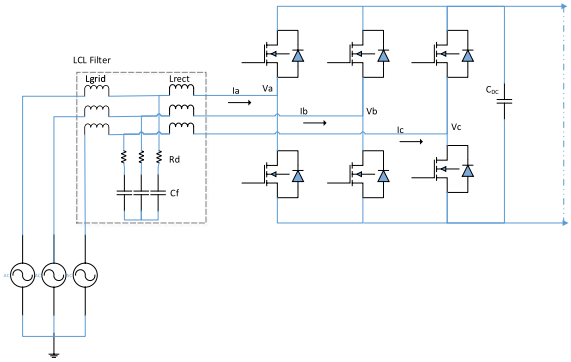

FIGURE 5. Three-phase AFE rectifier with the passive filters at AC and DC sides.

III. DESIGN PROCEDURE OF CHARGER

A. CONSTRAINTS OF THE OBJECTIVE FUNCTION

The objective of this research is to design an optimal high power off-board charger. The constraints are shown in Table 2, including efficiency, power factor, THD of line current, output voltage range, maximum output current and power rating.

B. PASSIVE FILTERS DESIGN

The high-power AC/DC converter should have a high-power factor and low THD. This can be achieved by adding filters to the PEC. In addition, an intelligent design of these filters ensures that they are neither bulky nor expensive [18].

The passive filters applied to the three-phase AFE rectifier are depicted in Figure 5.

The specifications of the devices and components selected for the design of the off-board charger are summarized in Table 3 and Table 4. Table 3 comprises the power modules that satisfy the specifications of the off-board charger. The CREE devices have been considered for preliminary design because they can operate at the maximum current rating of the charger, R_{ds} is small, and a compatible gate driver is easily available. Information about the gate drivers, inductor core, capacitor, voltage, and current sensors with their part number are mentioned in Table 4 and used in the co-design optimization algorithm.

An LCL filter with a damping resistor is designed to reduce the ripples at the AC side, while a DC link capacitor is designed to minimize the ripples at the DC side. The LCL filter consists of two inductors, one resistor and one capacitor, L_{rect} [uH] is the rectifier side inductor, L_{Grid}[uH] is the grid side inductor, R_d [Ω] is the damping resistance and C_f [uF] is the parallel capacitor between the two inductors [19]. The rectifier side inductor can be calculated as described in Eq. (1). At a switching frequency of 40kHz, the calculation of the filter is performed and increased with twenty percent of the computed value of the inductor to obtain the desired THD.

$$L_{rect} = \frac{V_{DC}}{nf_s I_{grid_{rated}} \%ripple} = \frac{1000 \times 1.2}{4 \times 40kHz \times I_{grid_{rated}} \times 40\%} = 90.9\text{uH} \quad (1)$$

$$I_{grid_{rated}} = \frac{\sqrt{2}P_{load}}{3V_{AC}} = \frac{\sqrt{2} \times 175kW}{3 \times 400} = 206.24 \quad (2)$$

For a 2-level converter, the value of n is 4, and for a 3-level converter, the value of n is 8. $I_{grid_{rated}}$ [A] is the rated current at grid side, P_{load} [W] is the load power, V_{DC} [V] is DC link voltage, V_{AC} [V] the phase voltage, and f_S [Hz] is the operating switching frequency. The AC side filter capacitor for three phases can be calculated in Eq. (3) [20].

$$C_f = \frac{1\% \frac{P_{rated}}{3}}{\frac{2\pi f_{AC} V_{AC}^2}{3}} = \frac{1\% \times \frac{175kW}{3}}{\frac{2\pi \times 50 \times 400^2}{3}} = 34.8uF \quad (3)$$

where, f_{AC} [Hz] is the grid frequency and P_{rated} [W] the three-phase rated power.

The attenuation factor (I_{att}) which indicates the allowable ripple in the grid inductor and switching inductor is represented in Eq. (4). This factor needs to be minimized while maintaining a stable and cost-effective filter [21].

$$I_{att} = \left| \frac{1}{1 + r(1 - L_{rect} C_f (2\pi f_s)^2)} \right| \% \quad (4)$$

For this design, I_{att} is 10 %. The factor "r" is derived by rearranging the above equations and expressed in Eq. (5).

$$r = \left| \frac{\frac{1}{I_{att}} - 1}{(1 - L_{rect} C_f (2\pi f_s)^2)} \right| = \left| \frac{\frac{1}{10}\% - 1}{(1 - 90.9uH \times 34.8uF \times (2\pi \times 40kHz)^2)} \right| = 4.52\% \quad (5)$$

The grid side inductor L_{Grid} is determined by multiplying r with L_{rect} as in Eq. (6).

$$L_{grid} = rL_{rect} = 4.52\% \times 90.9uH \times 1.2 = 4.94uH \quad (6)$$

It is also necessary to calculate the resonance frequency F_{res} [Hz] (Eq. (7)), which should be within a stable region. The stable region of F_{res} lies between ten times the line

TABLE 3. Power electronic modules.

Manufacturer	Part Number	Vds [V]	Id [A]	Rds [mOhm]	Eon [mJ]	Eoff [mJ]	Err [mJ]	RthM [°C/W]	RthD [°C/W]	Weight [g]
Cree	CAS300M17BM2	1700	225-325	8	13	10	0.2	0.071	0.065	300
Cree	CAS300M12HM2	1200	300-423	4.2	5.8	6.1	0.2	0.075	0.076	300
Infineon	FF3MR12KM1	1200	375-500	2.83	16	13.5	-	0.113	0.1	340
Semikron	SKM260MB170SCH17	1700	301-378	8.1	7.59	6.21	-	0.065	0.055	300
Semikron	SKM350MB120SCH15	1200	380-478	5.6	2.31	2.07	-	0.055	0.05	300
Microsemi	-	1200	300-600	6.5	9.5	10.5	-	0.08	0.1	350

TABLE 4. Charger components.

	Part Number	Voltage (V)	Current (A)	Max. Freq. (Hz)	ESR [mOhm]	Weight [g]
Gate Driver	PT62SCMD	-6/+20	±20	125k	-	63
	CGD15HB62P1	0/+5	±9	64k	-	44
	62EM1	-0.5/+16	±20	200k	-	63
Metglas Inductor core (Amorphous)	AMCC-320-630	-	-	-	-	2167-3678
	AMCC-10	-	-	-	-	198
	AMCC-8	-	-	-	-	172
947C Capacitor DC	947C152K801DLHS	1300 DC	100	-	1.8	1900
TDK Capacitor AC	B32362A4257J080	480 AC	30	-	2.3	1800
LEM Voltage Sensor	LEM 3-1200V	3-1200	-	-		2240
Current Sensor	LEM HAS 50-600	-	50-600	-	-	320
Grid Transformer	3-Phase 175kW (D/Y)	400	-	50/60	2530W Loss	600,000

frequency and half of the switching frequency. This criteria avoid issues in the upper and lower harmonic spectrums [19].

$$F_{res} = \frac{1}{2\pi\sqrt{\frac{L_{grid}L_{rect}}{L_{grid}+L_{rect}}C_f}} = \frac{1}{2\pi\sqrt{\frac{4.94uH\times 90.9uH}{4.94uH+90.9uH}\times 34.8uF}} = 12.47kHz \quad (7)$$

Finally, the damping resistor R_d can be calculated from the resonance frequency and filter capacitor as in Eq. (8).

$$R_d = \frac{1}{6\pi F_{res}C_f} = \frac{1}{6\pi \times 12.47kHz \times 34.8uF} = 0.122\Omega \quad (8)$$

The DC-link capacitance of the AC/DC converter can be quantified according to the average power Eq. (9) [22], [23].

$$C_{DC} = \frac{I_{DC}V_{DC}}{f_s\Delta V_{1\%}V_{DC}} = \frac{175kW}{40kHz \times 10 \times 1000} = 438uF \quad (9)$$

where I_{DC} [A] is the DC current, V_{DC} [V] is the maximum DC link voltage and ΔV [V] is the amplitude of allowable DC link voltage ripple, set at 1% [24].

The filter's frequency response is executed using the transfer function of LCL filter Eq. (10), as shown at the bottom of the page, to prove the damping resistance in the passive filter at the AC side [25]. This resistance is placed in series with the capacitor, which can eliminate the gain spike and smoothen the overall response [26]. The results are shown in Figure 17.

IV. ELECTRO-THERMAL MODELLING OF CONVERTER

The estimation of losses and the thermal characteristics of the PEC are a principal concern in the design of an off-board charger due to their influence on the system efficiency and reliability. Hence, the PEC dynamic electro-thermal model is designed in the MATLAB/Simulink environment and described hereunder.

A. LOSSES MODELLING

Power losses due to the PWM switching cycle of a semiconductor device can be divided into conduction losses and switching losses (turn-on loss and turn-off loss), as shown in Figure 6 [27]–[29]. An overview of the electro-thermal model is shown in Figure 7.

1) CONDUCTION POWER LOSSES

The conduction power losses of the PECs depend on the voltage-current characteristic of the transistor and the diode

$$G_d(s) = \frac{r_dC_fs+1}{L_{rect}L_{grid}C_fs^3 + (L_{grid}+L_{rect})r_dC_fs^2 + (L_{rect}+L_{grid})s} \quad (10)$$

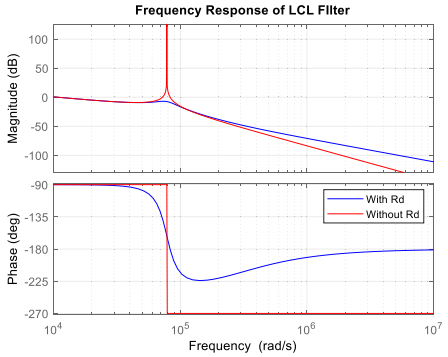

FIGURE 6. Frequency response of LCL filter.

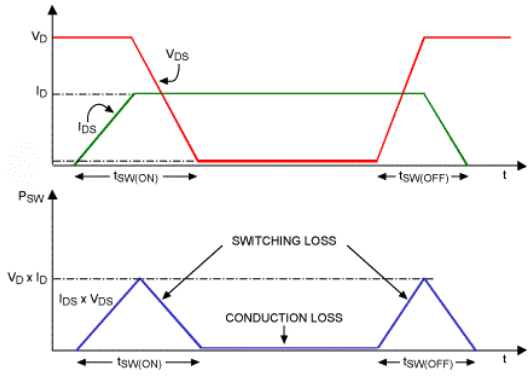

FIGURE 7. Typical switching and conduction loss in a PEC.

and can be calculated using Eqs. (11) and (14) [30]–[34].

$$P_{cond_{loss}} = V_{ds}\,(t)\,i_d(t) \tag{11}$$

V_{ds}[V] and i_d [A] represent the forward saturation voltage and drain current of the MOSFET. V_{ds} is obtained as a function of i_d and the junction temperature T_j [°C] (Eq. (12)).

$$V_{ds}(t) = f\left(i_d\,(t)\,, T_j\right) \tag{12}$$

This voltage can be estimated by using an interpolation technique on the datasheet characteristics of the PEC module. Hence, every simulation step can give information according to the datasheet of the module. Through this manner, power conduction losses of the MOSFET can be obtained by multiplying sample-to-sample data of V_{ds} with i_d.

Integrating the instantaneous power losses over a switching cycle T_{sw} [seconds] gives an average value of the MOSFET conduction losses as in Eq. (13) [30].

$$P_{CM} = \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{cond_{loss}}\,(t)\,dt \tag{13}$$

The conduction losses of the anti-parallel diode are calculated using Eq. (14).

$$P_{Dcond_{loss}} = V_f\,(t)\,i_f(t) \tag{14}$$

V_f [V] and i_f [A] represent the forward saturation voltage and current of the diode, respectively. V_f is again a function of the junction temperature T_j and the current i_f as expressed in Eq. (15).

$$V_f(t) = f\left(i_f\,(t)\,, T_j\right) \tag{15}$$

The average diode conduction losses across the switching period T_{sw} are expressed in Eq. (16).

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{Dcond_{loss}}\,(t)\,dt \tag{16}$$

At last, the total conduction losses are calculated by adding up the average power losses of the MOSFET and the diode, as represented in Eq. (17).

$$P_{total_C} = P_{CM} + P_{CD} \tag{17}$$

2) SWITCHING POWER LOSSES

An accurate estimation of the switching losses in the device is done by using datasheet values. A complex strategy with a small step size is necessary to estimate the losses that occur during the device's turn-on and turn-off transients. However, due to the complicated physics of the switching process, a lookup table method is more feasible and easier to implement for the estimation of the switching power losses. This is possible using the switching energies present in the component's datasheet, i.e. E_{swon} [mJ] and E_{swoff} [mJ]. The switching energies of MOSFETs are defined as functions of drain current, junction temperature and drain voltage [26], [30]–[32], [34], [29], [35] as expressed in Eqs. (18) and (19).

$$E_{sw_{on}}\,(k) = f(i_d\,(k)\,, T_j\,(k)\,, V_{dd}(k)) \tag{18}$$

$$E_{sw_{off}}\,(k) = f(i_d\,(k)\,, T_j\,(k)\,, V_{dd}(k)) \tag{19}$$

where k represents the k^{th} PWM switching pulse. The total switching energy is computed following Eq. (20).

$$E_{total} = E_{sw_{on}} + E_{sw_{off}} \tag{20}$$

Hence, the switching power losses can be estimated from the energy losses expressed in Eq. (21).

$$P_{Msw_{loss}} = \left(E_{sw_{on}} + E_{sw_{off}}\right) * f_S \tag{21}$$

where, f_S is the operating switching frequency.

The switching losses for a diode are defined by the reverse recovery characteristics but can also be calculated from the reverse recovery charge and reverse recovery time. However, in many cases, the switching losses of the diode are negligible [36]. Hence, the switching losses across the diode are considered very small. If the reverse recovery characteristic features are present in the datasheet, which is the case for an IGBT, it is necessary to calculate these losses in MATLAB/Simulink according to the relation expressed in Eq. (22).

$$E_{rr}\,(k) = f(i_f\,(k)\,, T_j(k)) \tag{22}$$

where i_f is the forward current of the diode. The switching power losses in the diode are calculated as in Eq. (23).

$$P_{Dsw_{loss}} = E_{rr} f_S \tag{23}$$

TABLE 5. SiC power module parameters.

	4TH ORDER THERMAL IMPEDANCES	VALUES
Diode	Resistance (R_1, R_2, R_3, R_4) [K/W]	0.008, 0.02, 0.024, 0.025
	Capacitance (C_1, C_2, C_3, C_4) [J/K]	0.05, 0.17, 0.44, 3.64
MOSFET	Resistance (R_1, R_2, R_3, R_4) [K/W]	0.008, 0.018, 0.02, 0.028
	Capacitance (C_1, C_2, C_3, C_4) [J/K]	0.07, 0.24, 0.52, 6.37

TABLE 6. Cooling system parameters.

	Parameters	Values
TIM	Thermal Conductivity [W/m/K]	3.6
	Thickness (mm^2)	0.178
Cold Plate	Thermal Resistance [°C/W] @ flow rate of 0.076LPS	0.025

The total average power losses of the MOSFET and anti-parallel diode can be computed with Eq. (24).

$$P_{total_{sw}} = P_{Dsw_{loss}} + P_{Msw_{loss}} \tag{24}$$

B. THERMAL MODELING

Semiconductor switches are very sensitive to their working temperature, and thermal cycling is the main cause of many power components' failure and lifetime reduction. The maximum temperature of the switch impacts the design of the PECs, and the heatsink or other cooling systems influence the overall size of the converter. The maximum operating temperature of the MOSFET influences the importance of the cooling and what type of cooling will be needed, e.g. air cooling or liquid cooling. The complexity of the cooling system can increase due to the requirement of an additional hydraulic system for the circulation of cooling liquid [37]. In the operation of semiconductor devices, the conduction and switching losses depend on the device's temperature. Therefore, careful design is necessary to ensure the correct functionality with all temperature-dependent conditions over the entire expected temperature range.

1) THERMAL STATE-SPACE MODEL

The thermal loss estimation is presented by a state-space model consisting of one cell Cauer network model with an equivalent thermal capacitance C_{th} [J/K], equivalent thermal resistance R_{th} [K/W] and time constant τ [seconds]. For the case of the PEC module, a fourth-order thermal impedance is considered. Its parameters are tabulated in Table 5. This compact thermal model has two inputs, the total power loss P_{Tloss} [W] and the case temperature T_c [°C] of the rectifier, and two outputs, the junction temperature T_j [°C] and the heat flow Pc [W] [37], [38].

The state-space thermal model is represented in Eqs. (25) and (26).

$$\frac{dx}{dt} = \left[-\frac{1}{\mathrm{R_{th}C_{th}}}\right]x + \left[\frac{1}{\mathrm{R_{th}C_{th}}}\ \frac{1}{\mathrm{C_{th}}}\right]\begin{bmatrix}\mathrm{T_c}\\ P_{Tloss}\end{bmatrix} \tag{25}$$

$$\begin{bmatrix}T_j\\ Pc\end{bmatrix} = \begin{bmatrix}1\\ \frac{1}{R_{th}}\end{bmatrix}x + \begin{bmatrix}0 & 0\\ -\frac{1}{R_{th}} & 0\end{bmatrix}\begin{bmatrix}\mathrm{T_c}\\ P_{total_{loss}}\end{bmatrix} \tag{26}$$

R_{th} is the thermal resistance of the MOSFET or diode, and usually its values can be found in the datasheet. C_{th} is the thermal capacitance of the MOSFET or diode and can be calculated from the thermal impedance Z_{th}[K/W] graph using Eqs. (27) and (28).

$$Z_{th} = R_{th}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{27}$$

where,

$$\tau = R_{th}C_{th} \tag{28}$$

After discretization with the sampling time, this state-space thermal model is implemented in the simulation (together with the non-linear rectifier loss model described in Section IV-A). It provides a link between the total power losses of the system and the junction temperature, as shown in Figure 7. This thermal model of the MOSFET and diode is also validated with the built-in thermal model of the PLECS software. It is observed from the responses of the heat flow and the junction temperature that both models behave in a similar way, as shown in Figure 8.

2) HEAT SINK MODELLING

A liquid heat sink is more appropriate for cooling purposes in the design and development of high-power charging systems. A Wakefield-vette liquid cold plate with thermal interface material (TIM) is considered in this paper and modelled in the simulation with a liquid flow rate of 0.076 LPS. The parameters of the cooling system are displayed in Table 6.

This heat sink is modelled in MATLAB/Simscape and incorporated with the thermal model. It allows to measure the case temperature of the PEC module and the sink temperature based on the heat flow and the ambient temperature as depicted in Figure 7.

V. PASSIVE FILTER DESIGN AND MODELLING

A. INDUCTOR DESIGN & CORE SELECTION

In this paper, the inductor design and loss modelling are also considered to accurately determine the total losses of the system. The selection of the core and calculations of the winding are performed in simulation.

The following steps are essential for selecting the core and the complete design of the inductor [39]–[41].

Step-1: Initial inductor area product estimation

$$A_p[mm^4] = \frac{2W_m}{K_u J_{m_{asum}} B_{pk}} 10^6 \tag{29}$$

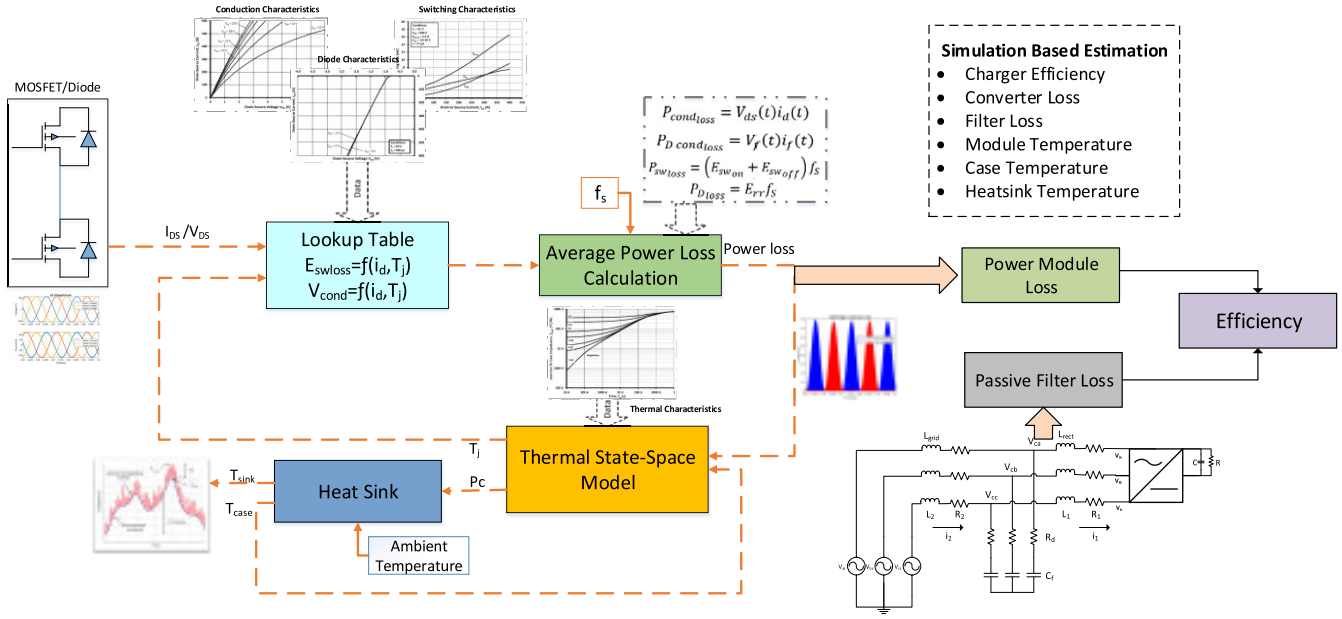

FIGURE 8. Overview of the off-board charger electro-thermal model.

In Eq. (29), B_{pk} [T] is assumed to be 80% of the flux density of the core, which is taken from the amorphous alloy material of the core (2605SA1), $J_{m_{asum}}$ $[\frac{A}{mm^2}]$ is the current density, and is equal to 6 for air forced cooling conditions, K_u is a window utilization factor with a value of 0.4 and W_m [J] is the stored energy of the inductor. To obtain a compact inductor, W_m needs to be minimized. It is computed as expressed in Eq. (30).

$$W_m = \frac{1}{2}LI_{pk}^2 \tag{30}$$

L [uH] is the inductor that needs to be designed. Its value comes from the filter calculation of L_{rect} and L_{grid} in Section III-B. I_{pk} [A] is the peak current passing through the inductor. After the estimation of the area product A_p of the inductor, it needs to be compared with a core selection lookup table where all the related parameters like W_a[mm^2], A_c[mm^2], l_m [mm] and the core dimensions can be found.

Step-2: Wire selection for the core winding

Selecting the winding wire for the inductor design is related to the wire area, which depends on the RMS current passing through the inductor and current density.

The area of wire can be calculated using Eq. (31).

$$A_w[mm^2] = \frac{I_L}{J_{m_{asum}}} \tag{31}$$

Next, a wire can be selected by matching the wire area with the American wire gauge (AWG) standard table. Then, the current density according to the selected wire can be recalculated, as in Eq. (32).

$$J_m[A/mm^2] = \frac{I_L}{A_w(m)}10^{-6} \tag{32}$$

Finally, the final area product for the core selection can be recalculated using Eq. (33). This is also a final confirmation of the inductor selection.

$$A_p[mm^4] = \frac{2W_m}{K_u J_{m_{asum}} B_{pk}}10^6 \tag{33}$$

Step-3: Number of turns and core volume estimation

The maximum allowable number of turns N_{max} for a specific inductor core and window size is computed by Eq. (34). The required number of turns for the specific inductor design are represented in Eq. (35), it should be less than N_{max}. The required numbers N of turns is used for the loss calculation of the inductor.

$$N_{max} = \frac{K_u W_a}{A_w}10^6 \tag{34}$$

$$N = \frac{LI_{pk}}{B_{pk}A_c k_{c_{core}}} \tag{35}$$

where, $k_{c_{core}}$ is the core fill factor, which value is mentioned in the amorphous core's datasheet. The volume of the inductor core can be calculated as Eq. (36)

$$core\ volume(mm^3) = l_m 10^3 A_c 10^6 \tag{36}$$

Step-4: Length of air gap calculation

The length of the air gap can be found using Eq. (37).

$$l_{ag}[mm] = \left(\frac{N^2\mu_o A_c}{2L} - \frac{l_m}{2\mu_r}\right)10^3 \tag{37}$$

where μ_o is the permeability of air (i.e. $4\pi 10^{-7}$[H/m]) and μ_r the relative permeability [-] of the amorphous material (i.e. 5000).

Step-5: Wire length calculation

The length of the wire for each turn l_{we} is calculated using the core dimensions, A [mm] and D [mm] (see Figure 9) the

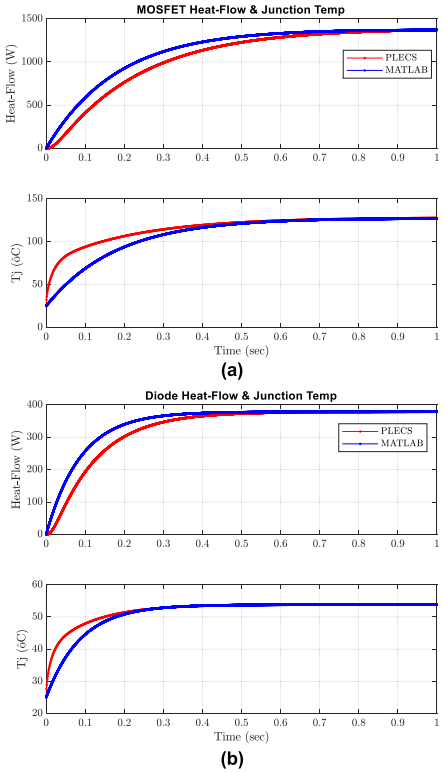

FIGURE 9. Thermal model comparison of MOSFET (a) and diode (b).

bobbin thickness B_t [mm] and the nominal diameter of wire d_{out} [mm]:

$$l_{we}[mm] = 2A10^3 + 2D10^3 + 4B_t10^3 + 4d_{out} \tag{38}$$

The total length of wire is calculated in millimeters by multiplying the number of turns with each wire turn length:

$$l_w[mm] = Nl_{we} \tag{39}$$

B. PASSIVE FILTER LOSSES, MASS AND VOLUME

The passive filters have a major contribution to the size and weight of the off-board charger design. Therefore, it is necessary to ensure that the individual passive components are correctly sized. The required inductance decreases with an increasing switching frequency. As a result, the cross-sectional area of the core and the number of winding turns will also decrease. Thus, the total mass and the cross-sectional area of the inductor will be reduced.

1) INDUCTOR LOSSES CALCULATION

The inductor's total losses depend on the power losses in the windings and the core. It can be determined by Eq. (40) [28].

$$P_{ind_{Total\ loss}} = 3P_{ind_{loss}} + 3P_{ind_{core}} \tag{40}$$

The power losses in the inductor windings are represented in Eq (41).

$$P_{ind_{loss}} = I_L^2 R_{LDC} + \Delta I_L^2 R_{LAC} \tag{41}$$

where I_L [A] is the inductor current, ΔI_L [A] is the inductor current ripple, R_{LDC} [mΩ] is the inductor resistance and R_{LAC} [mΩ] is the AC winding resistance due to the skin effect.

R_{LDC} is quantified by Pouillet's law as shown in Eq. (42) [4], [39], [40].

$$R_{LDC} = \frac{\rho N l_T}{A_w} \tag{42}$$

where, ρ [mm. Ω] is the wire resistivity, N is the number of turns, l_T [mm] is the length of the turn and the cross-sectional area of the wire is denoted by A_w. The wire for the inductor core can be selected, according to A_w and by the current passing through the inductor [39], [41].

R_{LAC} can be calculated based on the skin depth S_d [mm], as expressed in Eqs. (43)-(46). Skin depth can also be used for the selection of Litz wire with strand size not bigger than three times the skin depth.

$$R_{LAC} = R_{LDC} F_R \tag{43}$$

$$F_R = \frac{A_0\left(e^{2A_0} - e^{2A_0} + 2Sin\left(2A_0\right)\right)}{e^{2A_0} - e^{2A_0} - 2Cos\left(2A_0\right)} + \frac{2\left(N^2-1\right)}{3}\frac{e^{A0} - e^{A0} - 2Sin\left(A_0\right)}{3\left(e^{A0} - e^{A0} - 2Sin\left(A_0\right)\right)} \tag{44}$$

$$A_0 = \frac{\left(\frac{\pi}{4}\right)^{\frac{3}{4}} d_{out}}{S_d}\sqrt{\frac{d_{out}}{p}} \tag{45}$$

$$S_d = \sqrt{\frac{\rho}{\pi f_s \mu_o \mu_{rw}}} \tag{46}$$

where, F_R is the winding resistance ratio, f_s [kHz] is the power stage switching frequency, μ_o the wire permeability, μ_{rw} the winding relative permeability, d_{out} is the nominal diameter of wire and p the distance between two adjacent conductors is equal to the diameter of the wire, which is generally mentioned in the core datasheet.

Another factor on which the total inductor losses depend are the core losses, represented by Eq. (47).

$$P_{ind_{core}} = kf_s\left(\frac{2}{\pi^2}4f_S\right)^{\alpha-1} B_{pk}^{\beta} V_{core} \tag{47}$$

where k, α, β are the Steinmet'z parameters and V_{core} [L] is the volume of the core, which can be extracted from the datasheet of the inductor core material. B_{pk} is a peak magnetic flux density, which can be determined by Eq. (48). It depends on A_c which indicates the core cross-sectional area, number of turns, average inductor current and inductor current ripple:

$$B_{pk} = \frac{L\left(I_L + 0.5\Delta I_L\right)}{NA_c} \tag{48}$$

2) INDUCTOR MASS AND VOLUME

The mass and volume of the inductor take an important share in the overall mass and volume of the charger. The total mass of the inductor is the sum of mass of winding and the mass of the inductor core, and the total volume of inductor is sum of volume of the winding and volume of inductor core

as expressed in Eqs. (49) and (50).

$$m_{total} = m_{T_{wire}} + m_{core} \tag{49}$$
$$V_{total} = V_{T_{wire}} + V_{core} \tag{50}$$

$V_{T_{wire}}$ [L] is the total volume of wire and depends on the total wire length and the diameter of a wire, as in Eq. (51).

$$V_{T_{wire}} = \frac{l_w \pi d_{out}}{2} \tag{51}$$

The total mass of wire $m_{T_{wire}}$ [kg] depends on copper density ρ_{cpr} (i.e. 8960 $\frac{kg}{m^3}$) and the total volume of wire (Eq. (52)).

$$m_{T_{wire}} = \rho_{cpr} V_{Twire} \tag{52}$$

3) CAPACITOR LOSSES CALCULATION

The values of the DC link capacitor and AC link capacitor also need to be calculated. In the simulation, a lookup table of different capacitors is created. The simulation can automatically pick the mass and the dimensions of the capacitor according to the system's requirements. Moreover, it also considers the equivalent series resistance (ESR [mΩ]) from the datasheet for the capacitor losses estimation.

The power losses of the capacitor are calculated using Eq. (53) [39].

$$P_C = I_{CRMS}^2 ESR + I_{leak} V_C \tag{53}$$

where, I_{CRMS} [A] is the RMS current passing through the capacitor, V_C [V] is the average capacitor voltage and I_{leak} [A] is the leakage current passing through the capacitor. The latter value can be determined from the characteristic equations in the datasheet.

4) CAPACITOR MASS AND VOLUME

The mass and volume of the capacitor also take part in the charger's overall mass and volume. The volume of the capacitor can be calculated by using the dimensions of the cylindrical capacitor and the mass of the capacitor, generally mentioned in the datasheet. The capacitor volume is calculated using Eqs. (54) and (55).

$$V_{T_{cap}} = A_{cap} H_{cap} \tag{54}$$
$$A_{cap} = \pi \left(\frac{d_{cap}^2}{4}\right) \tag{55}$$

where A_{cap} [mm^2] is the capacitor area and H_{cap} [mm] the height of the capacitor and d_{cap} [mm] is the diameter of the capacitor.

VI. CONTROL SYSTEM DESIGN

The low-level control approach provides DC voltage regulation. With the implementation of control, it is possible to adjust the required voltage according to the charging demand and check the amount of line current passing through the converter and its ripple. The control system derives signals for the six switches of the three-phase AC/DC AFE converter inside the off-board charger. It consists of an outer DC bus voltage control loop and an inner dq-current control loop [42],

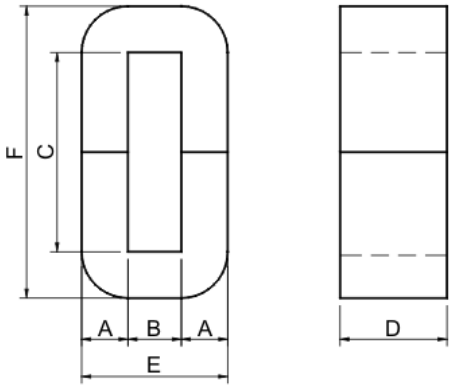

FIGURE 10. Amorphous inductor core dimensions [40].

as shown in Figure 10. For the control loops, a proportional integral (PI) controller is designed. The proportional gain (K_p) and integral gain (K_i) of both the voltage and current controllers are expressed in Eqs. (56) and (57). The performance can be enhanced by tuning the controller using an optimization algorithm to minimize overshoot, rise time, settling time and integral time absolute error (ITAE) etc. [43].

$$PI_{voltage} = 0.03 + \frac{112}{s} \tag{56}$$
$$PI_{current} = 0.7 + \frac{900}{s} \tag{57}$$

The PI controller is designed using the state-space model of the AFE converter. The state-space model of AFE converter is derived in the reference dq frame using the first-order differential equation [44]. The sensos and PWM delays are included in close loop control design, i.e. 8us for voltage sensor (LEM 3-1200V) delay, 3us for current sensor (LEM HAS 50-600) and 0.5us for PWM. After close-loop analysis, the controller is tuned according to margins and frequencies. The gain margin (gM) at gain crossover frequency (ωcg) and phase margin (PM) at phase crossover frequency (ωcp) of voltage control ($75.3dB$ at $(7.84\times10^4 rad/sec)$ and 52^o at $(417 rad/sec)$) and current control ($10dB$ at $(8.23\times10^4 rad/sec)$ and 30^o at $(4\times10^3 rad/sec)$. A static disturbance rejection analysis is executed for the closed-loop control, which specifies the controller performance in the presence of input disturbances (faults in the system) and output disturbances (faults in sensors). The step response and disturbance rejection response of the system with the integration of the control are shown in Figure 11. It can be seen that the system reacts very fast to disturbances. This control system is implemented with the electro-thermal simulation model of the charger and used for the co-design optimization.

VII. EFFICIENCY ESTIMATION

The system efficiency is a very important variant for the observation of the overall performance of the system. This efficiency will play a major role in the design and optimization. In this paper, the efficiency is estimated using the complete power losses of the system, such as power losses of

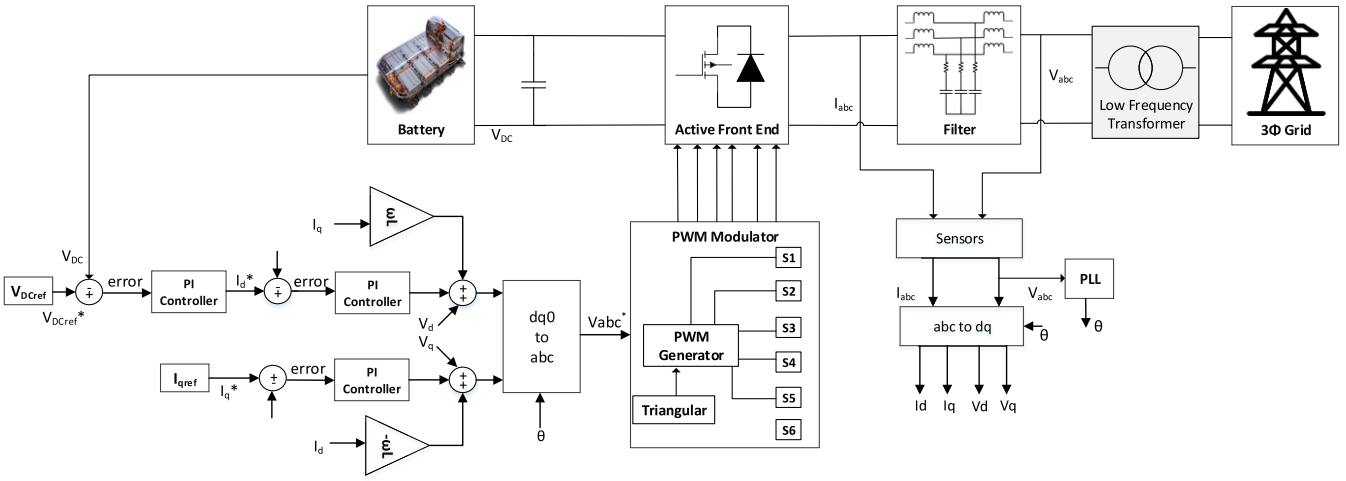

FIGURE 11. DC bus control system of the Off-board charger.

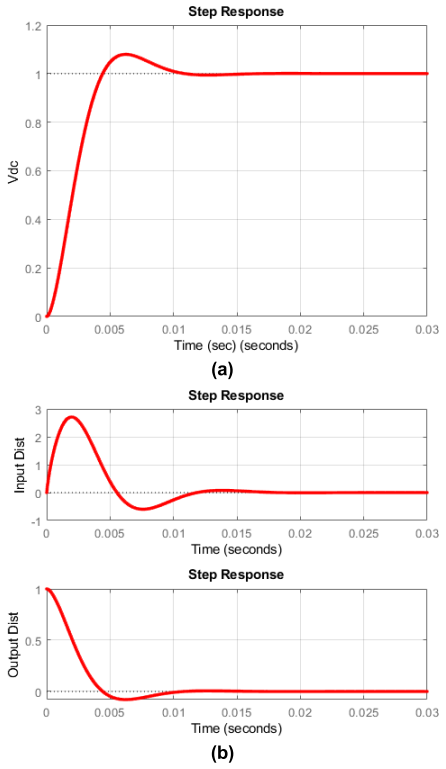

FIGURE 12. Closed loop step response (a) and disturbance rejection responses (b).

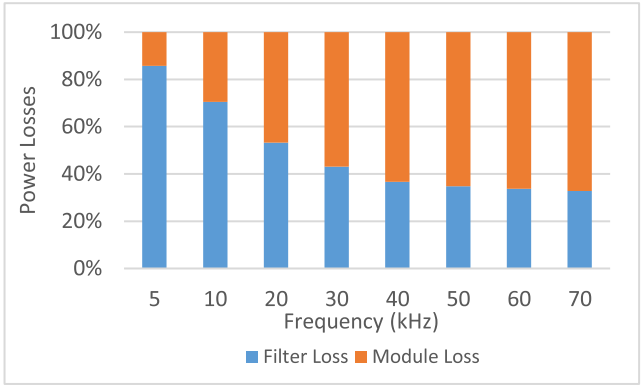

FIGURE 13. Power losses of PEC versus switching frequency.

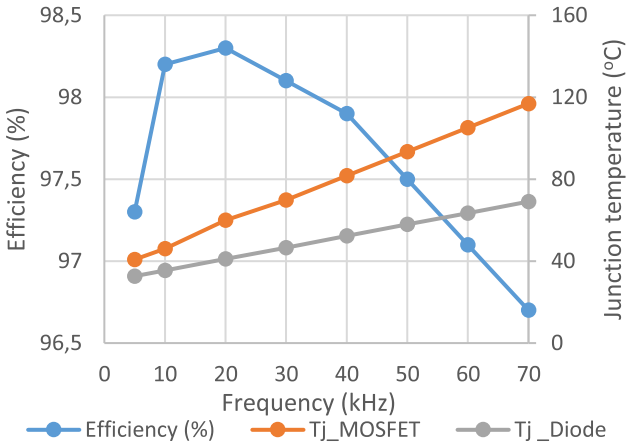

FIGURE 14. PEC Efficiency and junction temperature versus frequency.

the transistors, losses in the passive filters and line frequency transformer loss. The loss of line frequency transformer is fixed for total primary and secondary side. According to the manufacturer's specification, it contributes about 1.5% to the overall efficiency of the charger at full load. The efficiency in percentage is calculated using the DC output power and the total average power losses of the converter according to Eqs. (58) and (59).

$$P_{DC} = I_{DC} V_{DC} \tag{58}$$

$$\eta = \frac{P_{DC}}{P_{DC} + P_{loss} + P_{loss_{psve}} + P_{lossTR}} 100(\%) \tag{59}$$

VIII. OPTIMIZED PARAMETERS OF CHARGER

The closed-loop electro-thermal simulation model of the high-power off-board charger, described in Sections IV to VI, will be used in the optimization process. The efficiency of

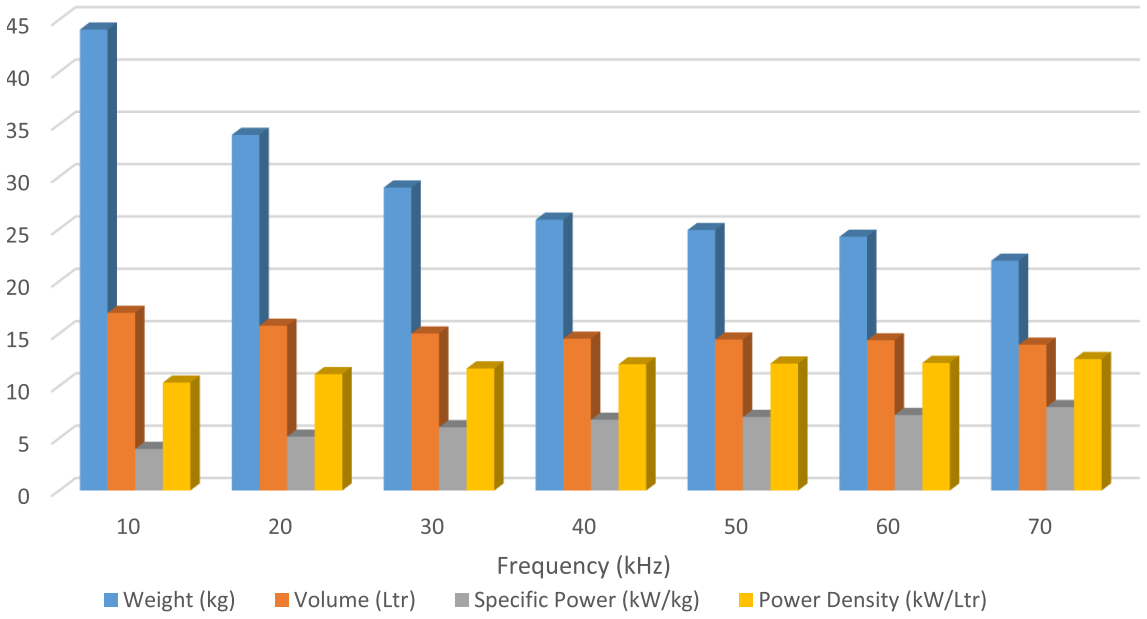

FIGURE 15. Weight and volume PEC versus switching frequency.

the charging system is estimated in a dynamic simulation by considering all the system losses, i.e. from the power module, inductor core, inductor winding and capacitor. The efficiency also depends on the junction temperature, the cooling system, TIM and the case temperature. The WBG SiC technology-based power module has some benefits; it can operate at a high switching frequency and high power. The switching frequency plays a major role in the system's performance because it affects the ripples and harmonics. When the switching frequency increases, the ripple decreases and reducing the passive filter requirement.

Additionally, the switching frequency will also have an impact on the size, volume, and weight of the system, and as a result, the power density and the specific power will be affected. Therefore, an analysis has been done by performing multiple iterations of the dynamic simulation with varying switching frequency to achieve the system's best performance at rated power. The results can be seen in Figure 12, Figure 13 and Figure 14. In Figure 13, the efficiency of the charging system in function of the switching frequency can be observed. It can be observed that the efficiency of the system increases until 20 kHz and then decreases again. This means that the losses in the power module increase at higher switching frequencies and impact the overall efficiency of the system. Furthermore, it can also be noticed that the junction temperatures of the MOSFET and the diode increase at higher switching frequencies. Figure 14 shows the weight and volume of the system at different switching frequencies. It can be observed that the weight and volume will be reduced by increasing the switching frequency. This is more detailed in Table 7, where the values of the passive filter come from the filter calculation in Section III-B. When the system is operated at a switching frequency of 10 kHz, the ripple of the system is higher, and a big filter is required for minimizing it.

TABLE 7. Passive components with frequency variation.

Sr. No.	Frequency (kHz)	L_{rect} (uH)	L_{grid} (uH)	C_f (uF)	R_d (Ω)	C_{dc} (uF)	F_{res} (kHz)
1	10	363.7	80.2	35	0.46	1800	3.3
2	20	181.8	19.8	35	0.24	875	6.4
3	30	121.2	8.8	35	0.16	583	9.4
4	40	90.9	4.94	35	0.12	438	12.5
5	50	72.7	3.2	35	0.1	350	15.5
6	60	60.6	2.2	35	0.08	292	18.6
7	70	52	1.6	35	0.07	250	21.6

Figure 12 clearly shows that the filter losses decrease with an increasing switching frequency because of the filter's size reduction. On the other side, the module losses increase with increasing switching frequency, resulting in lower efficiency.

Therefore, a trade-off is required. From Figure 14, it can be seen that drastic changes in size and weight occur up to a switching frequency of 40 kHz, but that at higher frequencies the variation becomes relatively small. Moreover, at 40 kHz, the efficiency (excluding line frequency transformer loss, weight and volume) is still greater than the requested 97%, while the junction temperatures of the MOSFET and the diode are less than 85°C and 55°C respectively. However, the loss of line frequency transformer is 2530 [W] at 175kW load, dimension (L × W × H [mm]) is (680 × 470 × 680) and weight is 600 [kg]. The 1.5% efficiency of the transformer will be reduced from Figure 14 efficiency, 217.3 litres of volume and 600kg of weight will be increased with reducing their power density and specific power in Figure 15. Therefore, a switching frequency of 40 kHz is selected by the optimization algorithm for the design of the 175 kW off-board charger. The filter parameters and resonance frequency associated with the switching frequency can also be found in Table 7.

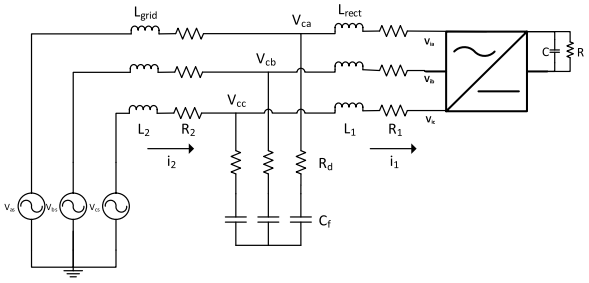

FIGURE 16. Three-phase rectifier with LCL filter.

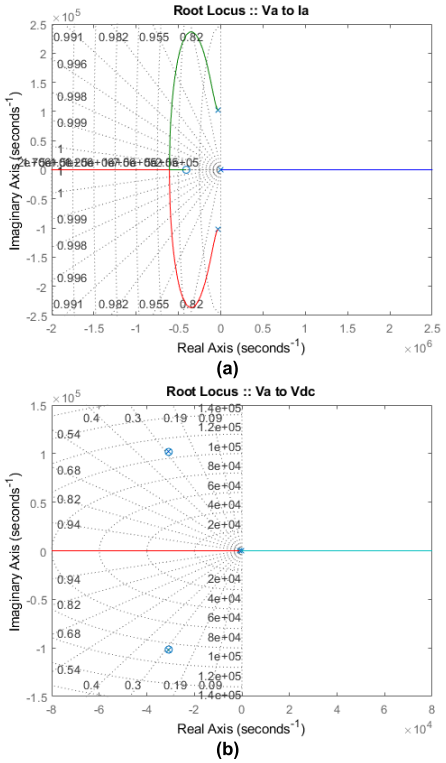

FIGURE 17. Root locus plots; line current (a) and DC voltage (b).

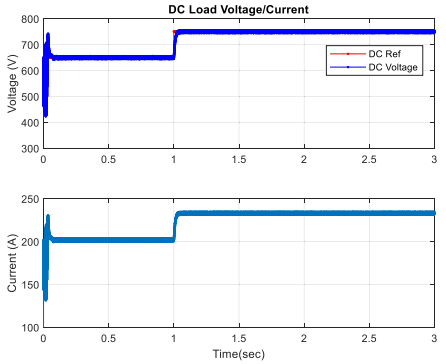

FIGURE 18. DC voltage tracking and current of charger.

IX. SYSTEM STABILITY ANALYSIS

A linear model is constructed based on the generalized off-board charger model achieved after the optimization process in the form of state-space or transfer function equations.

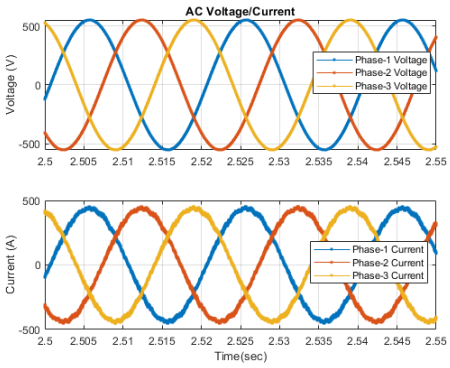

FIGURE 19. 3-phase voltage and current.

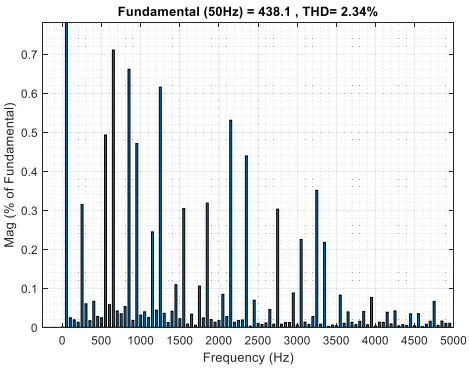

FIGURE 20. THD of input AC current.

This model is then utilized for a stability analysis to determine whether the system is stable or not.

Eqs. (60)-(72) have been derived in *abc* reference frames for the three-phase AFE AC/DC rectifier as shown in Figure 15 [45]–[47]. These first-order differential equations of the LCL filter and the DC filter will be used for the creation of the state-space model [44].

$$V_{as} = (R_l + r_d)i_{2a} + L_2\frac{di_{2a}}{dt} + V_{ca} - R_l i_{1a} \quad (60)$$

$$V_{bs} = (R_l + r_d)i_{2a} + L_2\frac{di_{2b}}{dt} + V_{cb} - R_l i_{1b} \quad (61)$$

$$V_{cs} = (R_l + r_d)i_{2c} + L_2\frac{di_{2c}}{dt} + V_{cc} - R_l i_{1c} \quad (62)$$

$$C_f\frac{dv_{ca}}{dt} = -i_{1a} + i_{2a} \quad (63)$$

$$C_f\frac{dv_{cb}}{dt} = -i_{1b} + i_{2b} \quad (64)$$

$$C_f\frac{dv_{cc}}{dt} = -i_{1c} + i_{2c} \quad (65)$$

$$V_{ca} = (R_l + r_d)i_{1a} + L_1\frac{di_{1a}}{dt} + V_{ia} - R_l i_{2a} \quad (66)$$

$$V_{cb} = (R_l + r_d)i_{1b} + L_1\frac{di_{1b}}{dt} + V_{ib} - R_l i_{2b} \quad (67)$$

$$V_{cc} = (R_l + r_d)i_{1c} + L_1\frac{di_{1c}}{dt} + V_{ic} - R_l i_{2c} \quad (68)$$

$$C\frac{dV_{dc}}{dt} = d_a i_{1a} + d_b i_{1b} + d_c i_{1c} - \frac{V_{dc}}{R} \quad (69)$$

Using the expressions above, $V_{i_{abc}}$ can be calculated.

$$V_{ia} = \left(\frac{2}{3}d_a - \frac{1}{3}d_b - \frac{1}{3}d_c\right)V_{dc} \tag{70}$$

$$V_{ib} = \left(\frac{2}{3}d_b - \frac{1}{3}d_a - \frac{1}{3}d_c\right)V_{dc} \tag{71}$$

$$V_{ic} = \left(\frac{2}{3}d_c - \frac{1}{3}d_a - \frac{1}{3}d_b\right)V_{dc} \tag{72}$$

V_{as}, V_{bs}, V_{cs} [V] are the voltages of phases A, B and C, while ϕ_v is the voltage phase angle, ω [rad/sec] is the angular frequency of the line voltage, V_{ia}, V_{ib}, V_{ic} [V] are the three-phase input voltages of the converter, i_a, i_b, i_c [A] are the AC line currents, V_{dc} [V] and I_{dc} [A] are the DC voltage and current of the rectifier, respectively, M_a, M_b, M_c are the modulation indexes of the three phases and d_a, d_b, d_c are the duty cycles.

After solving Eqs. (60) - (72), the generalized state-space model of the AC/DC converter is represented in A, B, C and D matrices.

$$\frac{dx}{dt} = Ax + Bu \tag{73}$$

$$y = Cx + Du \tag{74}$$

with

$$x = [i_{2a} i_{2b} i_{2c} V_{ca} V_{cb} V_{cc} i_{1a} i_{1b} i_{1c} V_{dc}]^T,$$
$$u = [V_{ia} V_{ib} V_{ic} V_{as} V_{bs} V_{cs}]^T$$

The matrix representation of the state-space model is shown in Eqs. (75) – (78), as shown at the bottom of the page.

The modulation index and duty cycle can be calculated using $M_a = 2d_a - 1$, $M_b = 2d_b - 1$ and $M_c = 2d_c - 1$ [26]. However, this state-space model is dependent on the duty cycle.

With the linear model, a stability analysis is performed. Figure 16 shows the root locus plot of the line current and DC voltage. The poles and zeros of the system are in the negative axis, which indicates that the system is stable.

$$\mathrm{A} = \begin{bmatrix}
-\frac{R_l+R_d}{L_2} & 0 & 0 & -\frac{1}{L_2} & 0 & 0 & \frac{R_d}{L_2} & 0 & 0 & 0 \\
0 & -\frac{R_l+R_d}{L_2} & 0 & 0 & -\frac{1}{L_2} & 0 & 0 & \frac{R_d}{L_2} & 0 & 0 \\
0 & 0 & -\frac{R_l+R_d}{L_2} & 0 & 0 & -\frac{1}{L_2} & 0 & 0 & \frac{R_d}{L_2} & 0 \\
\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_f} & 0 & 0 & 0 \\
0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_f} & 0 & 0 \\
0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_f} & 0 \\
\frac{R_d}{L_1} & 0 & 0 & \frac{1}{L_1} & 0 & 0 & -\frac{R_l+R_d}{L_1} & 0 & 0 & 0 \\
0 & \frac{R_d}{L_1} & 0 & 0 & \frac{1}{L_1} & 0 & 0 & -\frac{R_l+R_d}{L_1} & 0 & 0 \\
0 & 0 & \frac{R_d}{L_1} & 0 & 0 & \frac{1}{L_1} & 0 & 0 & -\frac{R_l+R_d}{L_1} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{d_a}{C_{DC}} & \frac{d_b}{C_{DC}} & \frac{d_c}{C_{DC}} & -\frac{1}{RC_{DC}}
\end{bmatrix} \tag{75}$$

$$\mathrm{B} = \begin{bmatrix}
0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}, \tag{76}$$

$$\mathrm{C} = [1]_{10\times 10}, \tag{77}$$

$$\mathrm{D} = [0]_{10\times 6} \tag{78}$$

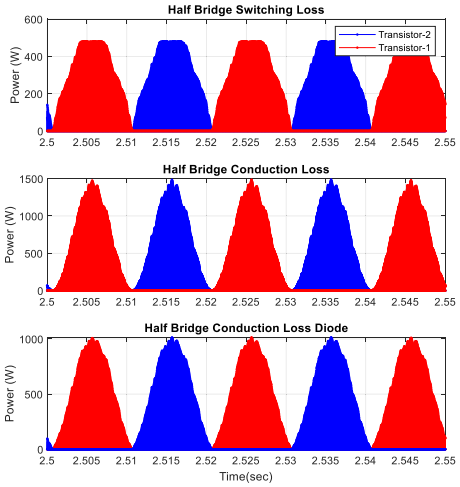

FIGURE 21. Power losses in a MOSFET module.

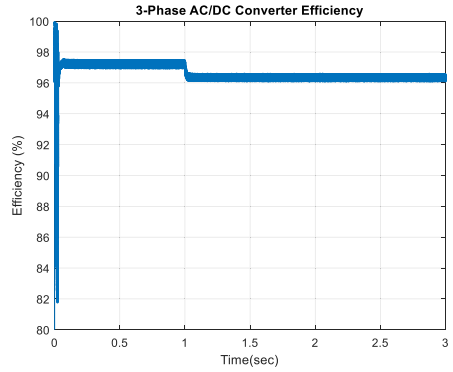

FIGURE 22. Efficiency of the 3-phase SiC AC/DC converter.

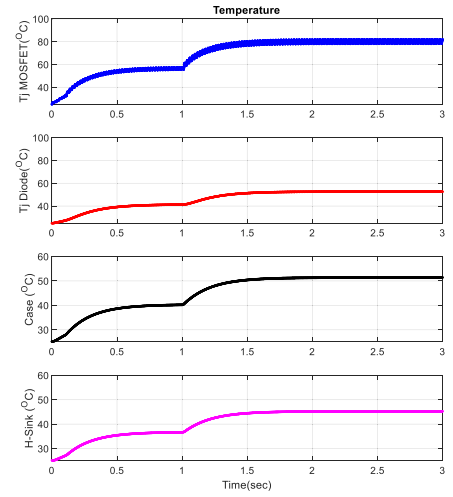

FIGURE 23. Temperature across MOSFET and diode.

X. RESULTS

This research aims to design an optimal 175 kW off-board charging system and achieve maximum efficiency, low THD and ripples of AC current, and unity PF. The passive filter design calculation is proposed to achieve these goals. After the design and optimization, the dynamic simulation results of the DC voltage/current, AC voltage/current, THD of input AC current, conduction power losses, switching power losses, efficiency, case and heatsink temperatures of the off-board charger are presented in Figures 18 to 23. The implemented control, tracking the reference DC voltage and DC load current, is shown in Figure 18. The three-phase line current and phase to phase voltage are shown in Figure 19. The achieved THD of the line current, which is less than 3%, is shown in Figure 20. The instantaneous switching power loss and conduction power loss of upper and lower MOSFET and anti-parallel diode are shown in Figure 21. The efficiency of the SiC converter at 175kW is greater than 96%, as shown in Figure 22 from 1 to 3 seconds. The junction temperature of the MOSFET and the diode, the case temperature and heatsink temperature are shown in Figure 23 and do not exceed the allowable range.

XI. CONCLUSION

This paper proposes a co-design optimization of a 175 kW off-board charger based on SiC technology. To achieve this, a dynamic simulation model of the converter is developed in MATLAB for the accurate estimation of power losses, i.e. conduction and switching losses of the power module and passive filter losses. Passive filter design and its mass and volume predictions were also presented, which vary with the switching frequency on the rated power. A thermal model of the power module with a heatsink was developed to estimate the temperature of the system. The developed model can be used to monitor and estimate the efficiency at different switching frequencies. This scalable parametrization based electro-thermal simulation design is very useful for developing highly efficient charging systems by configuring devices and components and key parameters such as filter impedance, switching frequency and control design. After the co-design optimization using the dynamic simulation model, the proposed design of the off-board charger was achieved at a frequency switching of 40 kHz. The final results show that the THD of line current is less than 3%, the PF above 99% and the rated power efficiency is higher than 96%. Experimental testing will be performed in the future to have a more accurate view of the total efficiency of your proposed system. In addition, thanks to WBG-based devices, the size and weight of the off-board charger has been reduced due to the higher switching frequency.

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