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Inductorless Multi-Mode RF-CMOS Low Noise Amplifier Dedicated to Ultra Low Power Applications

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ABSTRACT This work presents and analyses the design of a multi-mode Low Noise Amplifier (LNA) dedicated to 2.4 GHz Wireless Sensor Network (WSN) applications. The proposed inductorless LNA, implemented in a 28 nm FDSOI CMOS technology, is based on a common-gate configuration imbedded with a common-source stage to boost the overall transconductance of the circuit. The LNA is specifically designed, and optimized, to address three modes of operation. The reconfiguration is performed through current tuning, combined with switching the back gate of the amplification transistors. The proposed implementation allows the figure of merit (FOM) to be maintained constant in the different modes of operation. In the low power mode, the LNA only consumes 350 uW. It achieves a voltage gain (G_v) of 16.8 dB and a noise figure (NF) of 6.6 dB. In the medium performance mode, the gain and the NF are respectively improved to 19.4 dB and 5.4 dB, the power consumption is 0.9 mW. In the high-performance mode, the gain is maximum, 22.9 dB, and the noise figure is minimum, 3.6 dB, for a power consumption of 2 mW. The linearity represented by the input referred third-order intercept point (IIP3) is constant, close to −16 dBm. The reported LNA occupies only 0.0015 mm^2.

INDEX TERMS RF low power, low noise amplifier, inversion coefficient.

I. INTRODUCTION

At the edge of the Internet Of Things (IOT) deployment, the implementation of Wireless Sensor Networks (WSN) has to address two challenges: the energy saving and the low-cost development. In a wireless sensor node, 70% of the power consumption is generally dedicated to the radiofrequency (RF) module [1]. More specifically, 60% of the power dedicated to the receiver (Rx) part of an RF module is consumed by the frequency synthesis and the RF amplification, thus compromising the node's lifetime [2]. To address this issue, a channel-aware solution is proposed in [3]. Based on the IEEE802.15.4 standard and a given scenario of WSN deployment, the probability distribution of the received power signal is derived in Fig. 1. The lifetime of a node can be multiplied by a factor of 5 if the receiver front end (RFFE) features three modes of operation, with the specifications reported in Table 1 [3]. Focusing on the amplification stage, the investigations derive a set of specifications for the Low Noise Amplifier in each mode of operation. This paper aims to implement such multi-mode LNA.

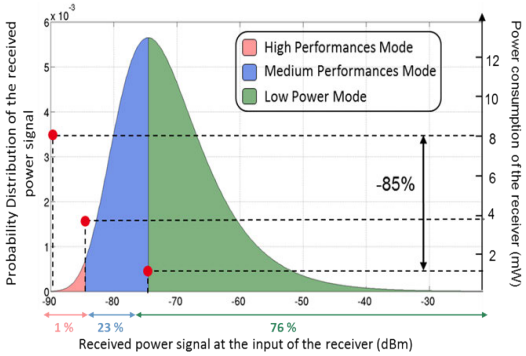

FIGURE 1. Probability Distribution of the received power signal at a wireless sensor node [3].

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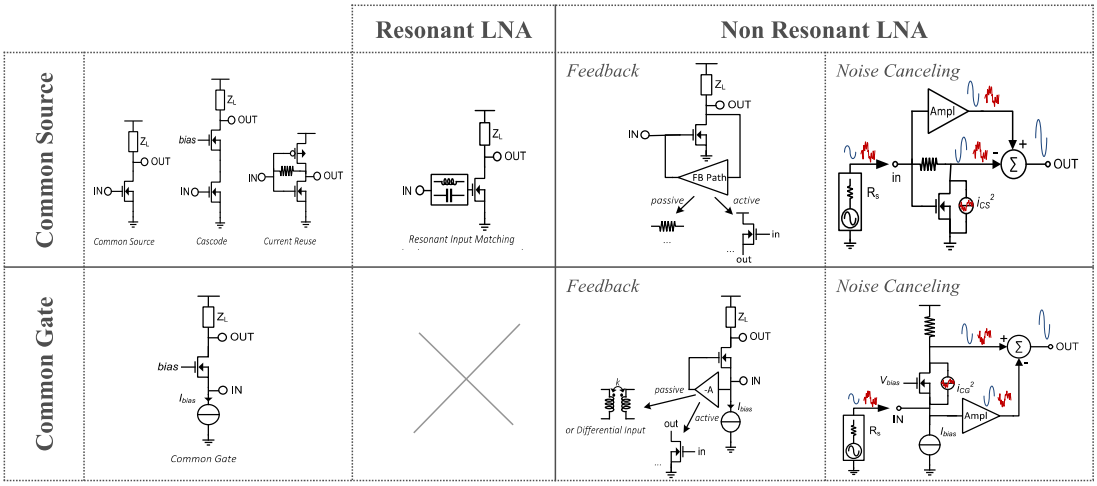

FIGURE 2. LNA architecture basics.

TABLE 1. Specifications for multi-mode RFFE and LNA dedicated to WSN.

	Mode	*Low Power*	*Medium Performance*	*High Performance*
RFFE	P_{sens} (dBm)	-75	-85	-90
	Usage (%)	76	23	1
	P_{DC} (mW)	<1.2	<4	<8
LNA	S_{11} (dB)	<-10	<-10	<-10
	NF (dB)	7	5	3
	G_V (dBv)	15	20	25
	IIP3 (dBm)	-16	-16	-16
	P_{DC} (mW)	<0.5	<1	<2

In Ultra Low Power (ULP) applications, such as WSNs, power saving can be achieved by relaxing the performance in terms of data-rate and sensitivity. Interestingly, a wireless node would scarcely (1% of time) have to achieve a high sensitivity (−90dBm), and most of the time (76% of usage) a sensitivity close to −75dBm as illustrated in Fig. 1. This feature is exploited to relieve the NF and linearity specifications of the LNA as reported in Table 1. Up to now, the design of ULP LNA has only focused on reducing the power consumption for a fixed mode, with no specific consideration for reconfiguration nor multi-mode operation. The purpose of this paper is to address this, by firstly investigating a design guide based on the Inversion Coefficient (IC) to work out a design of LNA suited for each mode of operation.

The back gate of the 28nm FD-SOI technology is further exploited to implement the reconfigurability of the circuit. This technique offers an interesting solution for the switching of analog/RF transistors operating in the sub-threshold region. The last section presents measurement results, and a comparison with the state of the art.

II. LNA CONSIDERATIONS

LNA basics are first briefly discussed in this section. Afterwards, the proposed topology is introduced, along with the analytic derivations of the input impedance, the noise factor and the voltage gain.

A. LNA ARCHITECTURE BASICS

Only two topologies of amplification are exploited in the design of LNA: the common-source configuration (CS), including cascode and current reuse arrangements, and the common-gate configuration (CG). The input matching, which contributes to the voltage gain and the noise figure, can be either of the resonant type or the non-resonant type, as illustrated in Fig. 2. Resonant LNAs embed an LC-based network, which not only achieves input matching, but also voltage pre-amplification. This passive pre-amplification contributes to the reduction of the noise figure (NF) and increases the overall voltage gain (G_v). Presenting a highly capacitive input impedance, the CS configuration is preferred for the implementation of a resonant LNA. Indeed, the gate to source capacitor is absorbed in the synthesis of the input matching network. A classic solution is the use of a cascode topology with inductive degeneration [4]. Resonant LNAs provide (very) good performance in terms of voltage gain and noise figure [5]. However, they are narrowband due to the limited bandwidth of the LC input matching. In terms of integration, the inductors embedded in the input network require a large area of silicon, preventing the development of highly integrated, and low cost, RFFEs.

To perform the input matching, non-resonant LNAs add a (local) feedback path, in the case of CS configuration, or exploit the natural resistive input impedance, in the case of CG configuration. These techniques do not achieve voltage pre-amplification, which limits the NF performance

compared to resonant LNAs. As illustrated in Fig. 2, non-resonant LNA architectures can be classified in two categories. The first one embeds a feedback between the output and the input for the CS configuration, between the input and the gate for the CG configuration. The feedback path can be active or passive. It is usually dedicated to improve the current efficiency [15], or to relax the trade-off between the gain-bandwidth product, the noise figure, and the condition for input matching [17]. The second type of architecture exploits the technique of noise canceling. In this approach, the thermal noise of the main amplification stage is cancelled out by an auxiliary path, which performs out-of-phase processing of the input signal, and in-phase processing of the noise, as illustrated in Fig 2. The technique of noise canceling ensures a flat band behavior of the circuit response over a significant bandwidth [6], but does not guarantee noise input matching. Non-resonant LNAs are particularly suited for wideband operation and can be highly integrated.

Considering the relatively relaxed NF specification and the constraint on the development cost of the targeted application, a solution based on an inductorless, non-resonant LNA is preferred. The noise canceling architecture is not suited for low power applications due to its dual path processing and the conditions required for noise cancelation. The proposed LNA exploits a feedback architecture with an emphasis on current efficiency and reconfiguration capability.

B. COMMON GATE CONFIGURATION WITH ACTIVE Gm-BOOSTED

Referring to Table 1, as the linearity (IIP3) is relaxed, and therefore does not require any design effort. However, the voltage gain specification is challenging if we consider the associated P_{DC}. To overcome this issue, a topology with a high current efficiency is recommended. A simplified schematic of the proposed LNA architecture is presented in Fig. 3(a). The core of the circuit is based on a CG configuration (M_1, R_1) whose transconductance is boosted by the voltage gain of the CS stage (M_2, R_2). The separate paths of the CS and CG stages are further exploited to adjust the performance of the circuit through bias control. Based on the equivalent schematic proposed in Fig. 3(b), the voltage gain, the input impedance and the noise factor are derived in (1), (2) and (3) respectively. For the noise analysis, only the thermal noise contributions are considered. The noise model of the MOS transistor is given in the Appendix.

$$G_V = \frac{\left[1 + g_{m1}.Z_{ds1}\frac{(1+g_{m2}.Z_{R2})}{(1+Z_{R2}/Z_{gs1})}\right]}{(1 + \frac{Z_{ds1}}{Z_{R1}})} \tag{1}$$

$$Z_{in} = \frac{1}{\left[jC_{gs2}\omega + g_{m1}.\frac{(1+g_{m2}.Z_{R2})}{(1+Z_{R2}/Z_{gs1})} + \frac{(1-G_V)}{Z_{ds1}} + \frac{(1+g_{m2}.Z_{R2})}{(Z_{gs1}+Z_{R2})}\right]} \tag{2}$$

$$F = 1 + \frac{4}{(1 + g_{m2}\,|Z_2|)^2.R_s} \cdot \left[\frac{\left[|Z_2|^2\left(\frac{1}{R_2}+\gamma_n.g_{m2}+g_{m2}^2.r_{g2}\right)+r_{g1}+\frac{\gamma_n}{g_{m1}}\right]}{\left[1+g_{m1}\,|Z_s|\,(1 + g_{m2}\,|Z_2|)\right]^2} + \frac{1}{R_1}\right] \tag{3}$$

With:

$$\begin{aligned}
\frac{1}{Z_{ds1}} &= g_{ds1} + jC_{ds1}\omega \\
\frac{1}{Z_{R2}} &= g_{ds2} + jC_{ds2}\omega + \frac{1}{R_2} + jC_{gd1}\omega, \\
\frac{1}{Z_{gs1}} &= j\left(C_{gs1} + C_{gd2}\right)\omega, \\
\frac{1}{Z_2} &= Y_{R2} + Y_{gs1} \\
\frac{1}{Z_{R1}} &= \frac{1}{R_1} + jC_{gd1}\omega + jC_L\omega
\end{aligned}$$

In Fig. 4, the analytic expressions (1), (2) and (3) are compared with Cadence simulations for the design of the 2.4GHz LNA with different power budgets. We first note that the performance is consistent with the expected specifications for each mode. The topology is suited for the targeted application. Furthermore, both the analytical and simulation results exhibit similar responses over an order of magnitude of DC power consumption. The proposed derivations can be further exploited to optimize the design.

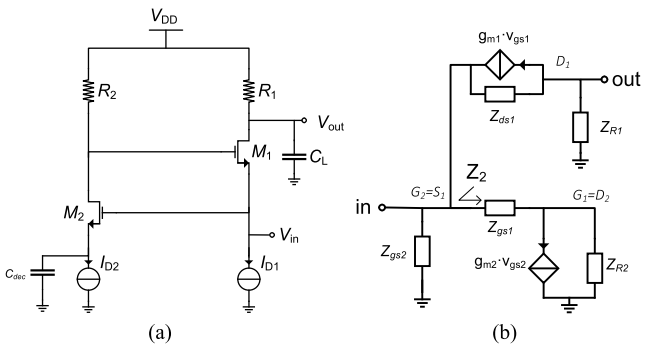

FIGURE 3. Active Gm-Boost CG LNA topology (a) equivalent small signal schematic (b).

III. LNA SYNTHESIS

To optimize the LNA for different modes of operation, the performance of the circuit is analyzed over a large design space. To address this purpose an algorithmic approach is proposed.

A. EKV MODEL AND DESIGN SPACE EXPLORATION

To explore the design space of the Gm-boosted LNA, the EKV model [7], offering a continuous and simple description of the MOS device from the Weak Inversion (WI) to the Strong Inversion (SI) regions, is exploited. In the EKV model, the drain current, I_D, in saturation mode is defined by the transistor aspect ratio W/L, the Inversion Coefficient (IC) and

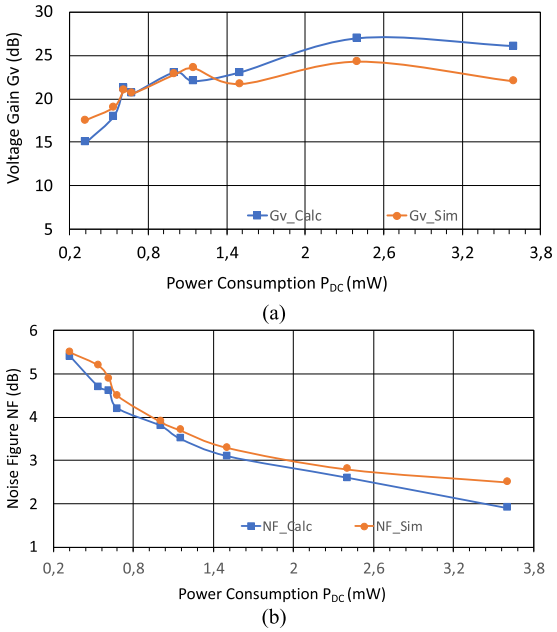

FIGURE 4. Comparison of the analytic model and Cadence simulations of the Voltage Gain (Gv) (a) and the Noise Figure (NF) (b) at 2.4GHz in 28nm FDSOI.

the specific current I_{spec_sq} according (4).

$$I_{Dsat} = \frac{W}{L}.I_{spec\_sq}.IC \tag{4}$$

where W and L are, respectively, the gate length and width of the device, I_{spec_sq} is a technological parameter, and the IC represents the level of channel inversion. The MOS transistor described with the IC operates in WI when IC<0.1, in the Moderate Inversion (MI) when 0.1<IC<10, and in SI when IC>10. The small signal model of a MOS transistor, reported in Appendix [12], is used to exploit the analytic derivations (1), (2) and (3). To explore the design space of the circuit, the algorithm illustrated in Fig. 5 is implemented in MatLab. This algorithm is not specific to the design of LNA, it can be used for any analog/RF circuit described with the IC. It works out a set of dimensions ($\overrightarrow{X_{opt}}$), and the associated performance ($\overrightarrow{Perf_{opt}}$), which address a set of specifications ($\overrightarrow{Spec}$) while achieving a maximum amount of optimization criteria (Crit_Opt).

B. Gm-BOOSTED LNA SYNTHESIS

The algorithm described in Fig. 5 is used to generate several LNA designs, which address the specifications defined in Tab 1. The algorithm is run for each set of specifications.

The design space is defined as follows:

- IC_i range is 0.05 to 20 with 10 values per decade
- R_i range is 400 to 1400 Ohm with a step of 100 Ohm
- W_i range is 10um to 120um with a step of 10um
- L_i are limited to 28nm, 45nm and 60nm
- C_L is fixed to 50fF

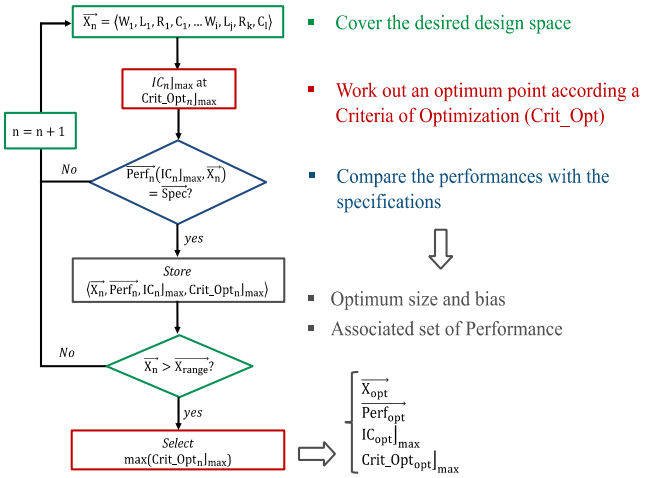

FIGURE 5. Algorithm for design space exploration of an analog/RF circuit.

- Crit_Opt is defined in (5)

$$FOM = \frac{G_V\rfloor_{lin} \cdot BW\rfloor_{GHz}}{P_{DC}\rfloor_{mW} \cdot (F\rfloor_{lin} - 1)} \tag{5}$$

The FOM (5) is typical of a low power LNA [11]. The linearity, IIP3, is not included, since the targeted performance, −16dBm, is not an issue here. Table 2 reports the dimensions and the associated performance for each configuration. The time required to explore the design space, and to work out the data for each configuration, does not exceed 850 sec (15 min.).

We observe a moderate variation (+15%) in the resistor values, from 600Ω to 700Ω for R_1, and from 850Ω to 1000Ω for R_2. Interestingly the ratio R_2/ R_1, close to 1.4, is almost constant over the different design sets. The optimization of the circuit for each mode is more dependent on the width of the transistors (W_{M1}, W_{M2}), and the associated bias conditions represented by (IC_{M1}, IC_{M2}). Reconfiguring the LNA performance would focus on adjusting both the drain current and the size of M_1 and M_2.

IV. IMPLEMENTATION

Based on the circuit analysis and the first-cut design proposed in section III, the implementation of the LNA is now discussed. More specifically, the strategy of reconfiguration and its consequences on the overall performance are investigated.

According Table 2, the optimization of the LNA for each mode is mainly supported by adjusting the geometry of M_1 and M_2, and the associated bias conditions. Hence the implementation of the multi-mode LNA focuses on the tuning of the transistor's width and bias. The reconfiguration of analog/RF circuits is usually steered by current DAC composed of CMOS switches and weighted current mirrors. Stacked with the RF function between the supply rails, Fig. 6(a), the current DAC requires an increase in the nominal supply, and as a consequence, consumes an extra DC power ($V^*_{DD\_iDAC} I_{DD}$). Interestingly, the FDSOI technology features

TABLE 2. LNA sizing and performance based on algorithm.

	Mode	Low Power	Medium Performance	High Performance
Device Sizes	W_{M1} (um)	20	40	45
	L_{M1} (nm)	28	28	28
	IC_{M1}	0.25	0.30	0.35
	W_{M2} (um)	30	80	100
	L_{M2} (nm)	28	28	28
	IC_{M2}	0.4	0.3	0.4
	R_1 (Ω)	600	650	700
	R_2 (Ω)	850	900	1000
Performances	S_{11} (dB)	<-10	<-10	<-10
	NF (dB)	5.8	4.5	2.8
	G_V (dBv)	15	21	26.2
	P_{DC} (uW)	300	850	1950

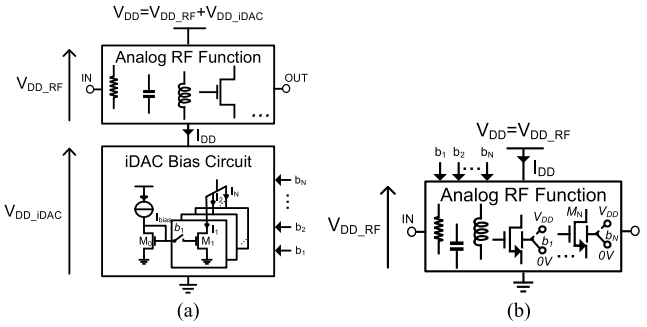

FIGURE 6. Principle of circuit reconfiguration with an iDAC (a) back gate switching (b).

an isolated access of transistor back-gates, which can be manipulated under specific bias conditions, further discussed, in order to switch the device on and/or off. This technique does not need to implement any additional circuitry with the RF function, nor any supplemental DC power, as illustrated in Fig. 6(b).

In Fig. 7 $I_D(V_{GS})$ is drawn as a function of the back-gate voltage V_{BG} of a NMOS transistor, in a 28nm FDSOI technology. Commuting V_{BG} from 0V to +2V reduces the transistor threshold voltage (V_T) from 365mV to 170mV. Hence, a transistor operating in the MI region ($0.1<IC<10$) with $V_{GB} = +2V$, illustrated by square marks in Fig. 7, has its gate to source voltage, V_{GS}, close to 170mV. If V_{BG} is grounded (0V), as shown by triangle marks in Fig. 7, the V_T is shifted to 365mV and the transistor, now operating in the WI region with an $IC<0.1$, is almost turned off.

For the 3 designs proposed in Table 2, the transistors operate in the MI region ($0.25<IC_{Mi} < 0.4$), and can be reconfigured through back-gate control. We first discuss the impact of such a technique on the circuit performance and its implementation. To illustrate this, we consider in Fig. 8, a multi-gate transistor featuring N elementary devices M_i,

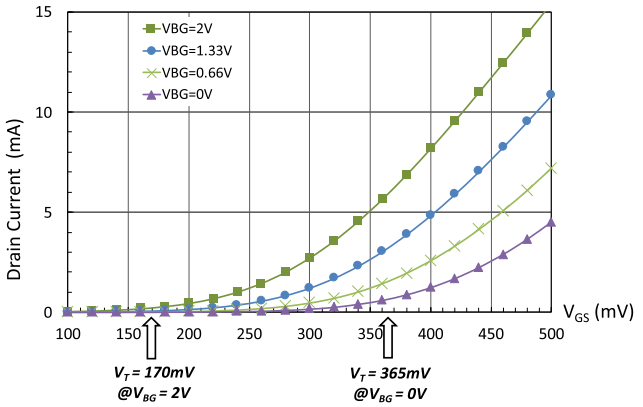

FIGURE 7. Drain current of a 50um/28nm FDSOI NMOS transistor versus V_{GS} as a function of V_{BG}.

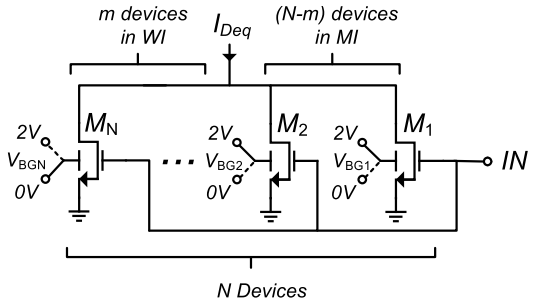

FIGURE 8. An N-gate common source configuration of a NMOS transistor with a back gate control VBGi.

with the same size (W_0, L_0), controlled by the back-gate voltage V_{BGi}. For the proposed configuration we further assume:

- M_i operates in the MI region at IC_{MI} if $V_{BGi} = 2V$, "on-state"
- M_i operates in the WI region at IC_{WI} if $V_{BGi} = 0V$, "off-state"
- $IC_{MI} \gg IC_{WI}$ -i.e. typ. $IC_{MI} > 0.2$ and $IC_{WI} < 0.01$-m transistors operate in the WI region with $0<m<(N-1)$, and at least one transistor operates in the MI region

For a given configuration of the back gate control, the small signal model (see Appendix) of the equivalent transistor M_{eq} (Fig.8) depends on the number of devices operating respectively in the MI region and the WI region. The model parameters are derived in Table 3, expressions (6) to (12) accounting for m, the number of transistors operating in the WI region. Since $IC_{MI} \gg IC_{WI}$, we can assume that the equivalent inversion coefficient IC_{eq} (6), drain current I_{Deq} (7), transconductance g_{meq} (8), and output conductance g_{dseq} (9), are determined by the number of transistor operating in the MI region (N-m). The parasitic capacitors are defined by the geometry of the device, and are weakly dependent on bias conditions. Indeed, we observe in Fig. 9 a variation of less than 16% of C_{gs}, 2% of C_{gd} and 10% of C_{bd} when the back gate (V_{BG}) of an NMOS transistor ranges from 0V (WI region) to 2V (WI region). The values of C_{gseq}, C_{gdeq} and C_{dseq} are determined by the total number of parallel devices N.

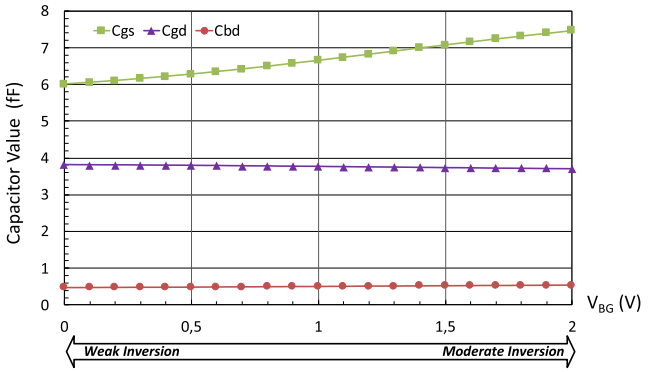

FIGURE 9. Simulated Parasitic Capacitors, Cgs, Cgd, Cbd versus V_{BG} for an NMOS transistor biased at VGS=300mV and VDS=500mV (W=20μm/L=28nm).

TABLE 3. Parameters and metrics of the equivalent N-gate transistor with m devices operating in weak inversion region.

Param	*Theoretical expression*	*Approx.*	*Eq.*
IC_{eq}	$= (N-m).IC_{MI} + m.IC_{WI}$	$\approx (N-m).IC_{MI}$	(6)
I_{Deq}	$= [(N-m).IC_{MI} + m.IC_{WI}].I_{spec\square}.\frac{W_0}{L_0}$	$\approx (N-m).IC_{MI}.I_{spec\square}.\frac{W_0}{L_0}$	(7)
g_{meq}	$= (N-m).g_m(IC_{MI}) + m.g_m(IC_{WI})$	$\approx (N-m).g_m(IC_{MI})$	(8)
g_{dseq}	$= g_{ds11}(IC_{11}) + g_{ds12}(IC_{12})$	$\approx g_{ds11}(IC_{11})$	(9)
C_{gseq}	$= (N-m).C_{gsMI}(W_0) + m.C_{gsWI}(W_0)$	$\approx NC_{gsMI}(W_0)$	(10)
C_{dseq}	$= (N-m).C_{dsMI}(W_0) + m.C_{dsWI}(W_0)$	$\approx NC_{dsMI}(W_0)$	(11)
C_{dgeq}	$= (N-m).C_{dgMI}(W_0) + m.C_{dgWI}(W_0)$	$\approx NC_{dgMI}(W_0)$	(12)
Current Efficiency	$\frac{g_{meq}}{I_{Deq}}$	$\frac{g_m(IC_{MI})}{IC_{MI}.I_{spec\square}.\frac{W_0}{L_0}}$	(13)
Transit Frequency	$f_{Teq} = \frac{g_{meq}}{2\pi C_{gseq}}$	$\frac{\left(1-\frac{m}{N}\right).g_m(IC_{MI})}{2\pi.C_{gsMI}(W_0)}$	(14)

Two metrics are considered to illustrate the impact of the multi-gate configuration with back bias control on the performance of the equivalent transistor: the current efficiency (g_m/I_D) and the transit frequency (f_T).

As long as $IC_{MI} \gg IC_{WI}$, the equivalent current efficiency (13) is not affected by the multi-gate configuration. However the transit frequency (14) depends on the ratio between the number of devices operating in the WI (N-m) and MI regions (m):

- if $(\frac{m}{N}) \ll 1$, f_{Teq} is the same as a single transistor, featuring an aspect ratio $\left(\frac{W_0}{L_0}\right)$ and a drain current I_{Deq}.
- if the number of devices m operating in the WI region is not negligible compared to the number of devices operating in the WI region (N-m), f_{Teq} is reduced by a factor $\left(1-\frac{m}{N}\right)$.

The multi-gate configuration is equivalent to a scalable transistor, which steers the DC current and the transconductance. However, the frequency performance (f_{Teq}) of the equivalent transistor is more affected than a standalone equivalent device if the number of devices operating in the WI region (off-state mode), is not negligible compared to the number of devices operating in the MI region (on-state mode). This frequency degradation must be considered for the design of RF circuits.

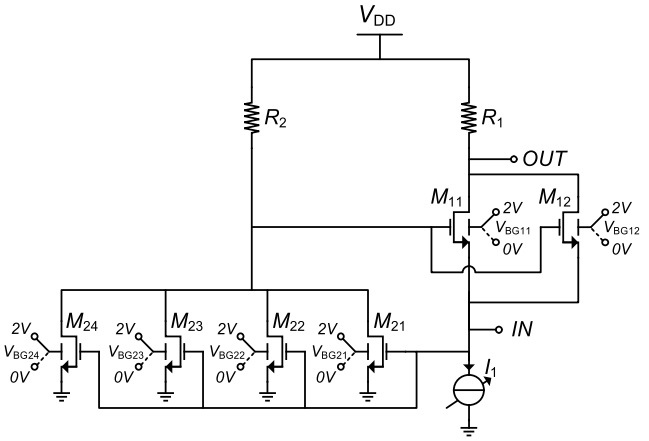

FIGURE 10. Architecture of the proposed multi-mode LNA.

The architecture of the multi-mode LNA implemented in a 28nm FDSOI CMOS technology is reported in Fig. 10. As discussed in section III, the tuning of the resistor value has a moderate impact on the optimization of the reconfiguration. R_1 and R_2 are respectively fixed to 850Ω and 1250Ω which respects the ratio condition 1.4. The tuning of the current and the IC is performed by

- the current source (I_1) and by resizing M_1 throughout V_{BG1i} in the CG branch.
- the supply voltage (V_{DD}) and resizing M_2 throughout V_{BG2i} in the CS branch.

The current source in the CS branch is removed in order to keep the supply voltage below 1.2V in the high-performance mode. To reduce the mismatch, each branch is implemented with a replica of a unit transistor: M_{2i} geometry is (30um/28nm), and M_{1i} geometry is (20um/28nm). The equivalent device sizes and bias conditions for each mode, based on post-layout simulations and accounting for the impact of the multi-gate configuration on frequency performance, are reported in Table 4.

V. MEASUREMENT RESULTS

A chip micrograph and a layout snapshot are presented in Fig. 11(a) and (b) respectively. The silicon footprint of the multi-mode LNA is only 0.0015 mm^2. The implemented circuit includes a buffer based on a source follower. The contribution of the buffer is de-embedded from the reported results.

TABLE 4. Final LNA sizing based on post-layout simulations.

	Mode	*Low Power*	*Medium Performance*	*High Performance*
Device Size & Bias	W_{M1} (um)	20	40	40
	IC_{M1}	0.27	0.27	0.27
	W_{M2} (um)	30	60	120
	IC_{M2}	0.32	0.32	0.32
	R_1 (Ω)	850	850	850
	R_2 (Ω)	1250	1250	1250
	I_1 (uA)	180	360	360
	I_2 (uA)	320	640	1280
	V_{DD} (V)	0.6	0.9	1.2

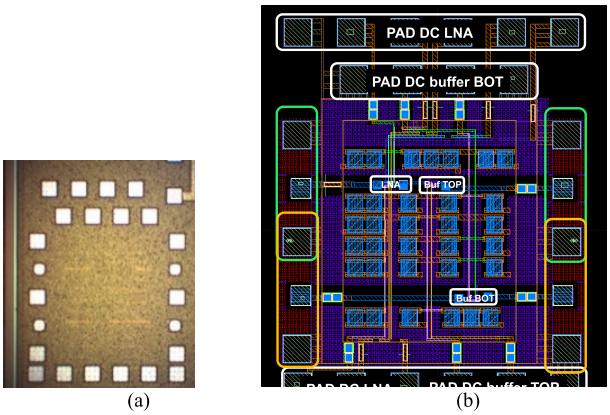

FIGURE 11. Chip micrograph (a) Layout snapshot (b).

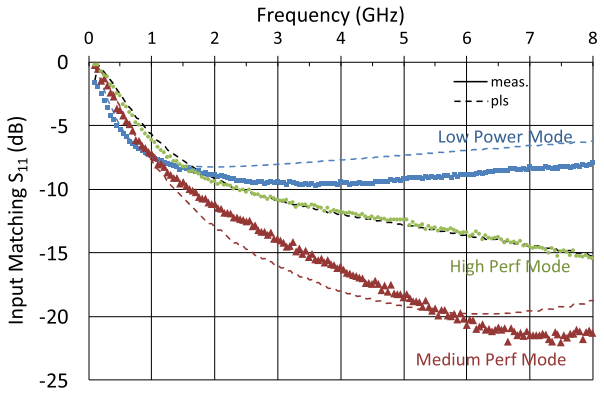

FIGURE 12. Measured and PLS input return loss S_{11} for the 3 modes of operation.

The measurement results and the post layout simulations (PLS) of the LNA are presented for the 3 modes of operation. According to (2), the input impedance of the circuit is dominated by the transconductance g_{m1} of the CG stage (M_1, R_1). The equivalent transconductance g_{m1eq} is changed when switching modes, as is the input matching. The input return loss S_{11}, Fig. 12, is kept below −9dB from 1.8GHz to 8GHz in medium and high performance modes, and from 2GHz to 5GHz in low power mode. We observe a very close form between the measurement and PLS results.

In the proposed Gm-boosted topology, most of the gain is achieved through the CS branch (M_2, R_2). The voltage gain,

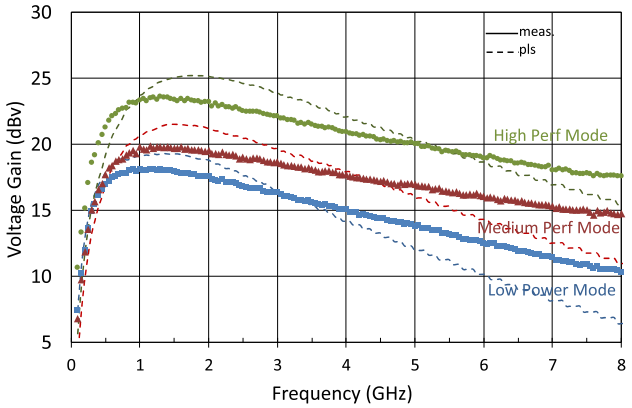

FIGURE 13. Measured and PLS Voltage Gain for the 3 modes of operation.

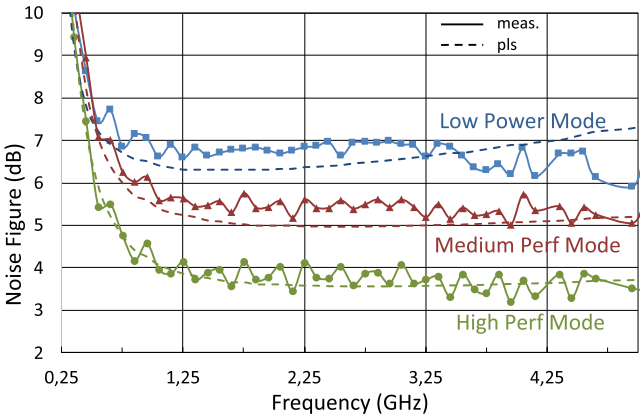

FIGURE 14. Measured and PLS Noise Figure for the 3 modes of operation.

Fig. 13, is obtained from S_{21} data. In high performance mode, it is 23.6dB at 1.3GHz, in medium power mode it is 19.8dB at 1.6GHz, and in low power mode it is 18.1dB at 1.4GHz. We can observe the impact of the multi-gate configuration on the frequency performance of the circuit. The −3dB cut-off frequencies are respectively 4.35GHz, 5.2GHz and 4GHz. For the 3 modes of operation, the measured peak of Gv almost occurs at the same frequency, but it is 1 to 2 dB lower with respect to the PLS. The measured forms remain consistent with the PLS.

The noise figure (NF), Fig. 14, exhibits a flat response which is typical for inductorless LNAs. The measured performance is in good agreement with PLS. In this topology, the NF is limited by the transconductance of the CG branch, which also adjusts the input matching as previously discussed. The NF is 3.3dB at 3.45GHz in high performance mode, 4.7dB at 4.25GHz in medium performance mode and 5.9dB at 3.95GHz in low power mode. In any mode, the NF ripple does not exceed +0.5dB from 1GHz to 3.25GHz, and is less than 0.8dB from 1GHz to 4.85GHz. The increase of NF for frequencies below 500MHz is due to the gain roll-off, induced by the coupling capacitor at the input of the circuit.

As discussed in the introduction, this LNA is originally dedicated to 2.4GHz WSN applications, and is expected to address the specifications reported in Table 1. In low power

TABLE 5. State of the art of low power inductorless LNAs.

Ref	LP Mode	MP Mode	HP Mode	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[12]	[15]	[16]	[17]	[12]	[18]
Gain (dBv)	16.8	19.4	22.9	18	15	16.8	12.3	15	14.7	21.2	14.5	20	23	19	17	20.8
NF (dB)	6.6	5.4	3.6	4.2	5.2	7.2	4.9	4.7	4.8	3.5	4.6	4	1.85	2.4	3	2.2
IIP3 (dBm)	-16.4	-16.8	-17.2	-14	-9	-16	-11	-6.5	2	-2	-1	-12	-2.8	8.6	7.9	-11
P_{DC} (mW)	0.35	0.9	2	0.2	0.2	0.3	0.4	0.55	0.6	1	1.2	1.3	2.8	3.1	3.7	3.8
BW (GHz)	4	5.2	4.5	1	2.2	5.5	2.2	2.4	2.5	2.7	2.7	2.7	1.7	2	5.8	3.5
Techno. (nm)	28	28	28	180	180	28	130	28	180	65	65	130	90	130	28	130
Area (mm2)	0.0015	0.0015	0.0015	0.3	1.5	0.001	0.005	0.005	0.4	0.05	0.005	0.006	0.03	0.007	0.005	0.0017
FOM (GHz/mW)	22	21.8	24	24	26	29	10.8	12.5	11.2	25	6.4	13.5	9.5	3.9	11	15

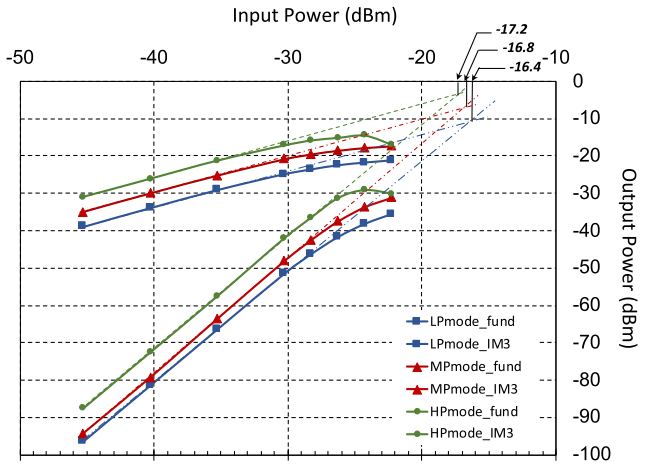

FIGURE 15. Measured IIP3 for the 3 modes of operation.

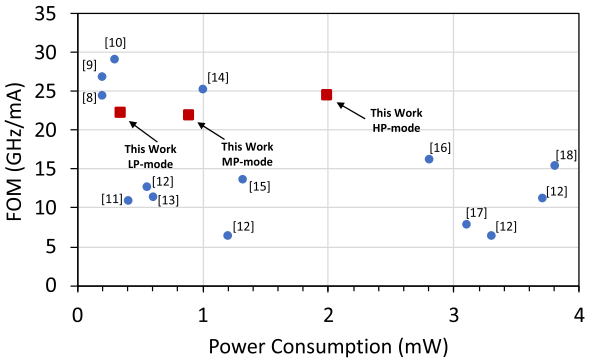

FIGURE 16. FOM comparison for the state-of-the-art references.

mode, at 2.4GHz, the voltage gain and noise figure are respectively 16.8dB and 6.6dB. In medium performance mode, they are 19.4dB and 5.4dB, respectively. For these two modes of operation, the LNA addresses the set of specifications. In high performance mode, the voltage gain is 22.9dB, expected at 26dB in theory, and the NF is 3.6dB, expected at 3dB in theory. Based on the investigation proposed in [3], the estimated sensitivity of the receiver in high performance mode is −89.9dBm, expected at −90dBm in theory. We can assume that the LNA addresses the targeted scenario of application in the three modes of operation.

To determine the IIP3, a two tone test with 2.40GHz and 2.41GHz is applied at the input of the LNA. Interestingly, the intermodulation products remain constant over the 3 modes of operation. We observe, Fig. 15, a degradation of only 0.8dB between the LP mode, at −16.4dBm, and the HP mode, at −17.2dBm. The active Gm-boosted configuration is less linear than a single-stage common source, or common gate, topology. Indeed, the distortions generated by the CS stage M_{2i} in Fig. 10 are directly applied on the gate of M_{1i}, and further distorted.

Table 5 reports some state-of-the-art inductorless LNAs, except [9], which exploits inductive degeneration. Considering the scenario of application, it only contains some circuits with a power consumption which does not exceed 4 mW. The proposed LNA achieves the highest voltage gain in HP-mode with [16], and among the lowest power consumption (350uW) in LP-Mode with [8]–[10]. We observe the limitation on the power consumption strongly impacts the noise figure, which remains above 4dB for a P_{DC} below 600uW [8]–[13]. Interestingly, the noise figure limitation seems to be technology independent. Unlike the bandwidth and the gain-bandwidth, the in-band noise performance does not improve with shrinking technology. As mentioned, an active Gm-boosted configuration remains limited in terms of linearity. The proposed LNA exhibits the lowest IIP3, but it is consistent with the specifications (Table 1) for the case of application.

For the works reported in Table 5, the associated FOM, defined in (5), is represented as a function of the power consumption in Fig. 16. It is important to note that the LNAs

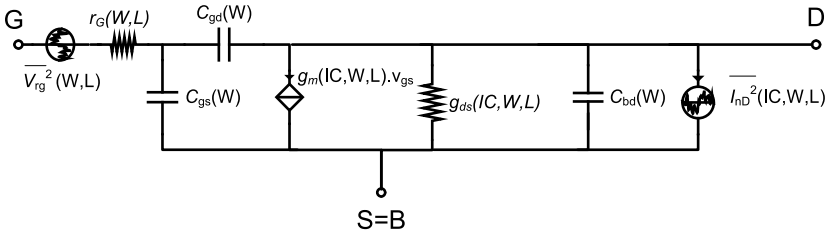

FIGURE 17. Small signal model of a MOS transistor including thermal noise source.

reported so far are optimized for a single bias point. The proposed LNA not only achieves among the best values of the FOM, but it maintains the FOM at a constant level over a large range of power consumption.

VI. CONCLUSION

In this paper, a multi-mode inductorless LNA is analyzed and implemented in a 28nm CMOS FDSOI technology. The Gm-boosted architecture, featuring a common gate configuration and a common source stage, achieves a high current efficiency, allowing for low power design. To optimize the trade-off between performance and current consumption in each mode of operation, a design algorithm based on the inversion coefficient is used to explore the design space of the LNA. This approach leads to three design configurations which are further combined and implemented. The reconfiguration is performed by adjusting the IC and the size of the transistors through a combination of current steering and back bias switching of some multi-gated transistors. The LNA achieves among the best FOM, between 22 and 24 GHz/mA, reported so far, for inductorless configurations over a large range of power consumption, from 0.35mW to 2 mW. To the knowledge of the authors, none of the circuits reported so far in the literature are capable of such behavior. The measured performance at 2.4GHz addresses the set of specifications defined for a multi-mode RFFE dedicated to WSN applications. In the high-performance mode, the gain is maximal, 22.9dB, and the NF is minimal, 3.6dB. In the low power mode, the LNA only consumes 0.35mW, and still achieves a gain of 16.8dB and a noise figure of 6.6dB. The IIP3 remains constant, close to −16dBm, in any mode of operation.

APPENDIX

This appendix introduces the equivalent small signal model of the MOS transistor described with the inversion coefficient according [7], including thermal noise sources reported in Fig. 17.

For the small signal model:

$$g_m\,(IC, W, L) = \frac{G_m\,(IC,\lambda_c)\,.I_{spec\square}}{U_T}.\frac{W}{L}$$

$$\text{with}: G_m\,(IC,\lambda_c) = \frac{1}{n}.\frac{\sqrt{(IC.\lambda_c+1)^2+4.IC}-1}{\lambda_c.(IC.\lambda_c+1)+2}$$

$$g_{ds}\,(IC, W, L) = \frac{IC.I_{spec\square}}{\alpha_{G_{ds}}.L}.\frac{W}{L}$$

$$C_{ij}\,(W) = C_{ij\_W}.W$$

$$r_G\,(W, L) = R_{G\square}.\frac{W}{L}$$

For the noise sources:

$$\bar{i_{nd}^2}\,(IC, W, L) = 4kT.\gamma_n\,(IC)\,g_m.\,(W, L, IC)$$

$$\bar{v_{r_g}^2}\,(W, L) = 4kT.r_G$$

The technological parameters for the 28nm FD SOI CMOS technology from ST are extracted with Cadence. They are reported in the following table:

Parameter	NMOS (svtlp)
$I_{spec\square}$ (nA)	930
n	1.55
λ_c	0.42
C_{gs_w} (fF/µm)	0.46
C_{gd_w} (fF/µm)	0.22
C_{bd_w} (fF/µm)	0.20
$R_{G\square}$ (Ohm/m^2)	21.3
γ_{wi}	0.87

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