IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 8, 2021, accepted May 29, 2021, date of publication June 3, 2021, date of current version June 10, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3085826

A Current-Mode Four-Phase Synchronous Buck Converter With Dynamic Dead-Time Control

JUN TANG, TIAN GUO, JUNG SIK KIM, AND JEONGJIN ROH, (Senior Member, IEEE)
Department of Electrical and Electronic Engineering, Hanyang University, Ansan 15588, South Korea

Corresponding author: Jeongjin Roh (jroh@hanyang.ac.kr)

This work was supported in part by the Ministry of Science and ICT (MSIT), South Korea, under the Information Technology Research Center (ITRC) Support Program supervised by the Institute for Information Communications Technology Planning Evaluation (IITP) under Grant IITP-2020-2018-0-01421, in part by the National Research Foundation (NRF) of Korea Grant through the Korea Government (MSIT) under Grant 2019R1A2C2085189, and in part by the BK21FOUR Program through the National Research Foundation of Korea within the Ministry of Education.

ABSTRACT A current-mode four-phase synchronous buck converter with a dynamic dead-time control (DDTC) method is presented in this work. A brief analysis of the multiphase buck converter power efficiency in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is performed to provide design guidelines for minimizing power losses. In synchronous converters, the power efficiency can always be improved by optimizing the dead-time. Therefore, a gate driver with DDTC is designed to optimize the dead-time in every switching cycle, thereby improving power efficiency particularly under heavy load conditions. The proposed buck converter has the ability to deliver a maximum load current of 6.0 A at a typical output voltage of 1.2 V from a power supply of 3.0 V. A power efficiency improvement of over 1.0% is achieved when the load current is over 2.0 A, and an improvement of about 2.4% is obtained at a load current of 4.0 A. A peak power efficiency of 92.8% is measured at an output voltage of 1.8 V.

INDEX TERMS Dynamic dead-time control, high efficiency, multiphase, synchronous buck converter.

I. INTRODUCTION

Portable and battery-powered electronic devices are in great demand in the modern consumer electronic market. This demand has led to the rapid rise in requirements for high efficiency power management systems. Inductor-type switching mode DC-DC converters with synchronous switches are widely used for their high efficiency and high power delivery capabilities [1]–[6]. Compared to single-phase DC-DC converters, the multiphase topology is much more attractive and advantageous in low-voltage high-current applications, exhibiting the advantages of ripple reduction at both the input and output, fast load transient performance, and flexible control strategies.

A block diagram of a basic four-phase synchronous buck converter is presented in Fig. 1. The power efficiency (η) is determined by the output power (P_{OUT}) and the total power loss (PL_{tot}) in the following manner:

$$\eta = \frac{P_{OUT}}{P_{OUT} + PL_{tot}} = \frac{I_{OUT} \times V_{OUT}}{I_{IN} \times V_{IN}}, \tag{1}$$

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

where I_{IN}/I_{OUT} is the input/load current and V_{IN}/V_{OUT} is the input/output voltage.

The PL_{tot} must be minimized to achieve a higher efficiency as in (1), which implies that the power losses of each sub-converter must be minimized. In synchronous buck converters, the discontinuous conduction mode (DCM) instead of the continuous conduction mode (CCM) is applied to prevent the reverse inductor current when the average inductor current $I_{L(avg)}$ is smaller than half of the peak-to-peak inductor current ΔI_L. Moreover, various top-level strategies can be also applied in the multiphase converters, such as phase-shedding techniques [1], [2].

In synchronous buck converters, the dead-time is essentially required to prevent the unwanted shoot-through current caused by simultaneous conduction of the switches, as depicted in Fig. 1. However, additional power losses are incurred during the dead-time period, and the dead-time may introduce current unbalance in a multiphase converter [3]. Thus, the dead-time should be appropriately optimized. The optimal dead-time T_{DT_opt} is heavily dependent on the load conditions, since the switching node voltage V_{SW} is discharged by the inductor current [16], as in (2), which makes

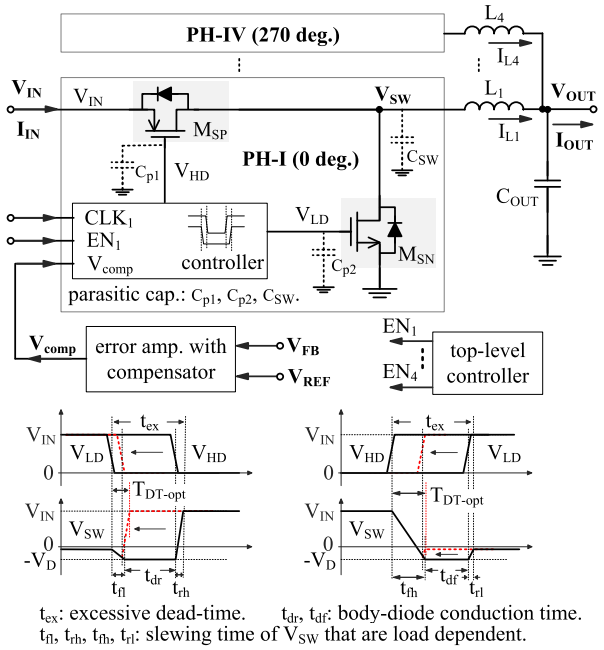

FIGURE 1. Block diagram of a basic four-phase synchronous buck converter, and the dead-time issues in its sub-converters at the on/off transition of the switching node.

its optimization a challenging goal.

$$T_{DT\_opt} \approx C_{SW} \times V_{IN}/I_{L(avg)}, \tag{2}$$

where C_{SW} is the parasitic capacitance at the switching node in a sub-converter.

According to (2), a long dead-time is required for light load conditions, whereas a short dead-time is adequate for heavy load conditions. With a fixed dead-time gate driver, an adequate long dead-time is required for all load conditions, thereby resulting in a long body-diode conduction time under heavy load conditions, which greatly degrades the power efficiency. Therefore, numerous dead-time optimization methods have been reported to adaptively or dynamically adjust the dead-time, not only for improving the power efficiency [11]–[16], but also for helping the current balancing compensation [3], [17]. The sensorless optimization approaches in [3] and [11] are implemented with complex digital algorithms, which are not applicable to analog control-based power converters. An analog automatic dead-time control system is presented in [12], which presents an undershoot voltage detection technique to adjust the dead-time only for the off-transition of the switching node and leaves a fixed dead-time for the on-transition interval. An accurate and fast dead-time error voltage sensor and integrator are used to adjust the on/off dead-time, independent of the duty cycle in [13], but it is not easy to achieve an ultra-fast response time of the sensor and integrator. In [14] and [15], switched capacitors are applied for dead-time adjustment, which requires additional capacitors and switches, and the adjusted dead-time is employed in the next switching cycle. The asymmetrical dead-time control driver in [16] exhibits

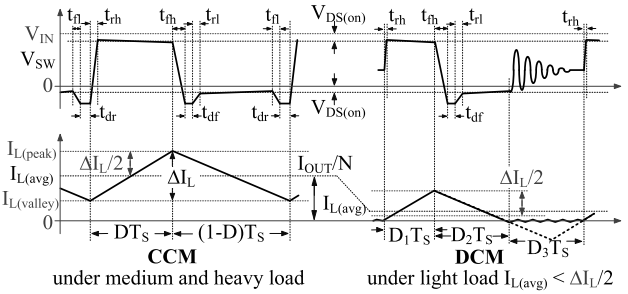

FIGURE 2. Switching node voltage and inductor current waveforms of an identical sub-converter in an active N-phase synchronous buck converter in CCM/DCM mode.

a compact structure that merges a dead-time controller with a gate driver for CCM operation. The dead-time is achieved by the designed asymmetrical rising (falling) slopes of the high-side and low-side switches, which are heavily dependent on the supply voltage and process.

In this paper, a current-mode four-phase synchronous buck converter is presented. A dynamic dead-time control (DDTC) method based on an ultra-fast body-diode conduction sensor (BDCS) is proposed to optimize the dead-time. Therefore, a near-optimal effective dead-time is achieved immediately in every switching cycle. Moreover, DCM operation is applied to prevent the reverse inductor current for light load conditions. A brief analysis of the synchronous buck converter power efficiency is provided in Section II, which provides design guidelines for the proposed buck converter discussed in Section III. The experimental results are presented in Section IV, and the conclusion is presented in Section V.

II. EFFICIENCY ANALYSIS

Similar to the efficiency analysis in [2] and [9], the power losses of an identical sub-converter in an active N-phase interleaving synchronous buck converter are reviewed here.

As indicated in Fig. 2, the switching node voltage V_{SW} and inductor current waveforms of the identical sub-converter are presented. The sub-converters have the same inductor (L) and switching frequency (F_S), and share the output capacitor (C_{OUT}). The on and off transition dead-time are found as $(t_{fl}+t_{dr}+t_{rh})$ and $(t_{fh}+t_{df}+t_{rl})$, respectively. DCM operation is applied to prevent the reverse inductor current under light load conditions whenever $I_{L(avg)} < \Delta I_L/2$, where $I_{L(avg)}$ and ΔI_L are as given below:

$$\begin{aligned} \Delta I_L &= \frac{V_{IN} - V_{OUT}}{L \times F_S} \times \frac{V_{OUT}}{V_{IN}} \\ I_{L(avg)} &= I_{OUT}/N. \end{aligned} \tag{3}$$

The steady-state conversion ratio is $V_{OUT}/V_{IN} = D$ in CCM or $V_{OUT}/V_{IN} = D_1/(D_1+D_2)$ in DCM [27]. In a buck converter with a fixed V_{OUT} and V_{IN}, the relationships of D_1, D_2, and D can be found as in (4). The critical value $(1-D)$ of the nameless parameter K is found to be the boundary of CCM and DCM. Namely, when the load resistance R_L increases to $[2L/(N \cdot R_L \cdot T_S)] < (1 - V_{OUT}/V_{IN})$, the buck

converter will operate in DCM mode.

$$\begin{aligned} D_1 &= \sqrt{K/(1-D)} \cdot D \\ D_2 &= \sqrt{K(1-D)} \\ K &= 2L/(N \cdot R_L \cdot T_S) \ \leq \ (1-D), \end{aligned} \tag{4}$$

where the T_S is the switching period, which is the reciprocal of the switching frequency F_S in the sub-converter.

The effective inductor current $I_{L(rms)}$ is given as

$$I_{L(rms)} = \begin{cases} \sqrt{I_{L(avg)}^2 + \dfrac{\Delta I_L^2}{12}} & \text{(in CCM)} \\ \sqrt{\dfrac{4}{3(D_1+D_2)} \cdot I_{L(avg)}^2} & \text{(in DCM).} \end{cases} \tag{5}$$

Once the switch is on, there will be conduction loss PL_{con_hs} of the high-side switch during DT_S and PL_{con_ls} of the low-side switch during $(1-D)T_S$ in CCM, as given in (6). The R_{on_hs} (R_{on_ls}) is the drain-source on-resistance of the high-side (low-side) switch, which is inversely proportional to the switch size. In DCM, as both switches are off during D_3T_S, the PL_{con_hs} and PL_{con_ls} can be simply determined by modifying D to D_1 and $(1-D)$ to D_2 in (6) and using the DCM value of $I_{L(rms)}$.

$$\begin{aligned} PL_{con\_hs} &= I_{L(rms)}^2 \cdot R_{on\_hs} \cdot D \\ PL_{con\_ls} &= I_{L(rms)}^2 \cdot R_{on\_ls} \cdot (1-D). \end{aligned} \tag{6}$$

The switching loss PL_{sw_hs} of the high-side switch and PL_{sw_ls} of the low-side switch are given in (7). V_D is the forward-direction voltage of the low-side switch body diode. The rising time t_{rh} (t_{rl}) and falling time t_{fh} (t_{fl}) of V_{SW} are dependent on the inductor current and the drain current of the power switches; hence, the values of t_{rh} (t_{rl}) and t_{fh} (t_{fl}) are dependent on the load current.

$$\begin{aligned} PL_{sw\_hs} &= V_{IN} \cdot I_{L(avg)} \cdot F_S \cdot (t_{rh} + t_{fh})/2 \\ PL_{sw\_ls} &= V_D \cdot I_{L(avg)} \cdot F_S \cdot (t_{rl} + t_{fl})/2. \end{aligned} \tag{7}$$

The parasitic output capacitances of the power switches also cause switching loss, PL_{OSS}, as in (8). The total parasitic capacitance C_{SW} at the switching node is proportional to the power switches size.

$$PL_{OSS} = C_{SW} \cdot V_{IN}^2 \cdot F_S/2. \tag{8}$$

The reverse recovery power loss PL_{rr} and conduction loss PL_{con_bd} of the low-side switch body diode are given in (9). The t_{dr} (t_{df}) is the conduction time of the body diode at the on (off) transition of V_{SW}; the Q_{rr} is the reverse recovery charge, which is linearly proportional to the body diode conduction time when the dead-time is less than the diode reverse recovery time (i.e. typically 50-150 ns) [3].

$$\begin{aligned} PL_{rr} &= V_{IN} \cdot F_S \cdot Q_{rr} \\ PL_{con\_bd} &= V_D \cdot F_S \cdot I_{L(avg)} \cdot (t_{dr} + t_{df}). \end{aligned} \tag{9}$$

The gate charge loss PL_G of the power switches is given in (10), where C_{p1} (C_{p2}) is the gate parasitic capacitance of the high-side (low-side) switch, and V_G is the gate driver voltage that is generally equal to V_{IN}.

$$PL_G = (C_{p1} + C_{p2}) \cdot V_G^2 \cdot F_S. \tag{10}$$

The power loss of the output inductor comprises the core loss due to the magnetic properties of the inductor core [2], and the conduction loss PL_{con_L} in (11) caused by the DC resistance (DCR) R_{DCR} of the inductor.

$$PL_{con\_L} = I_{L(rms)}^2 \cdot R_{DCR}. \tag{11}$$

The power loss PL_{con_C} of the output capacitor C_{OUT} is caused by its equivalent series resistance (ESR) R_{ESR}, as given in (12), where ΔI_C is the current of C_{OUT}.

$$PL_{con\_C} = \frac{\Delta I_C^2}{12} \cdot R_{ESR} \tag{12}$$

$$\frac{\Delta I_C}{\Delta I_L} = \frac{[m - floor(m)] \cdot [1 - m + floor(m)]}{N \cdot D \cdot (1-D)}, \tag{13}$$

where $m = N \cdot D$, the $floor(m)$ is the integer of m.

The power loss PL_{trace} of the bonding wires and print circuit board (PCB) traces can be estimated as in (14), which is caused by the parasitic resistance R_{trace}.

$$PL_{trace} \approx I_{OUT}^2 \cdot R_{trace}. \tag{14}$$

Moreover, there are power losses caused by the controller and the input capacitors. Usually, low-power controllers are designed to efficiently control power switches; the ceramic capacitors are then selected for both the input and output capacitors because of their low ESR properties.

Among the power losses above, the conduction and switching losses of the power switches result in major power loss of the buck converter. As in (6)–(10), conduction losses can be reduced by decreasing ΔI_L or the on-resistance of switches, whereas switching losses can be reduced by decreasing F_S or the rising (falling) time. However, there are certain trade-offs between these parameters, power losses, and the performance. An ultra-wide size is required to reduce the on-resistance of the switches, which not only occupies a large chip area but also increases the parasitic capacitance. Consequently, the conduction losses in (6) are reduced at the penalty of the increased switching losses in (7)–(8) and the gate charge loss in (10). Decreasing F_S will reduce the switching losses and the losses caused by the body diode at the penalty of the increased conduction loss and the degraded transition performance. Therefore, the power switches, the output inductor (capacitor), and F_S must be carefully designed to meet the output (voltage, current, and ripple) requirements at a balance point between the conduction loss and switching loss. Regardless of these trade-offs, the body-diode-related power losses in (9) can be minimized by a well-designed gate driver that obtains the optimal dead-time.

III. PROPOSED MULTIPHASE BUCK CONVERTER

A. CIRCUIT DESIGN AND IMPLEMENTATION

As depicted in Fig. 3, the proposed buck converter consists of four identical sub-converters, a clock generator, and a

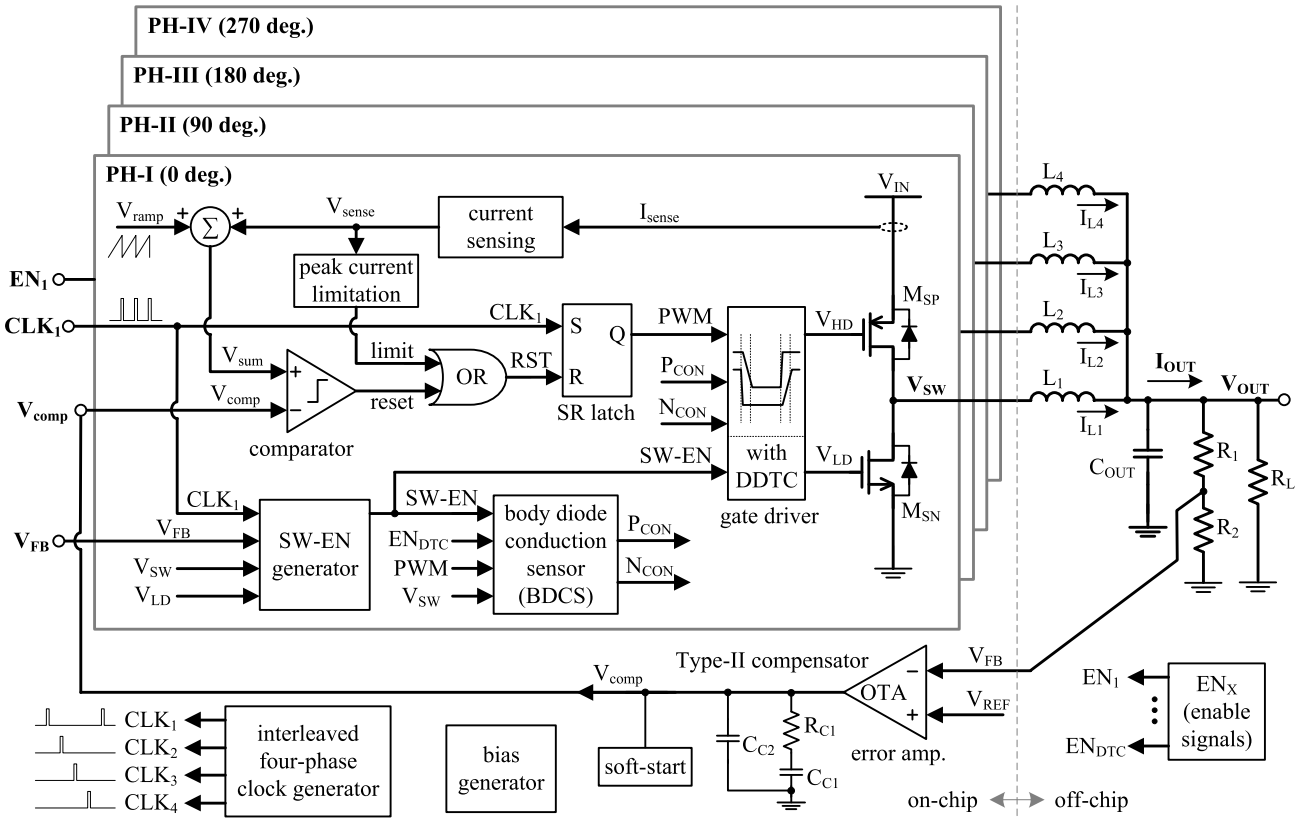

FIGURE 3. Block diagram of the proposed four-phase buck converter.

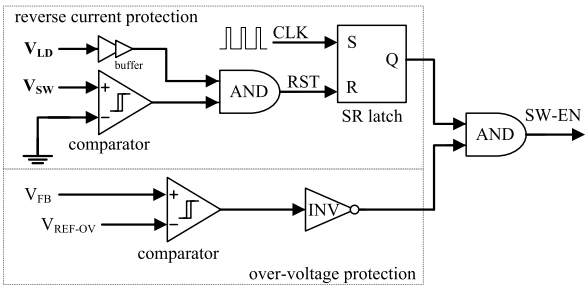

FIGURE 4. SW-EN generator.

high-gain operational transconductance amplifier (OTA) with type-II compensator. The sub-converters are implemented in the current mode. The peak current control scheme is applied for current sharing among the phases because of the simple design and small effects on device parameters [5], [10], [17]. The clock generator generates four short-pulse clocks, CLK_1–CLK_4, that have 90° phase differences from each other, which ensures that the four sub-converters operate in an interleaved manner. Therefore, the ripple cancellation property is achieved, which indicates that the power loss caused by the output capacitor in (12) is reduced. Since the inner current loop compensates the voltage feedback loop, the type-II compensator that introduces a pole and a zero is adequate for the current-mode buck converters [22].

The identical sub-converter consists of a gate driver with dynamic dead-time control (DDTC), a body-diode conduction sensor (BDCS), a current sensing circuit, an artificial ramp generator, and a pulsewidth-modulator (PWM). The gate driver with DDTC is designed to dynamically optimize the dead-time, which will be discussed in detail later. The instantaneous current sensing circuit senses the current flowing through the high-side switch, and forms the inner current loop and peak current control. An artificial ramp signal V_{ramp} is generated and added to the current sensing signal V_{sense} for generating the reset signals, thereby avoiding the oscillation problem whenever the steady-state duty cycle is greater than 0.5 in the current-mode buck converters. The PWM signal is generated via a clocked SR latch that involves the reset signals, then it is enhanced by the gate driver to adequately control the wide-size power switches. To prevent the reverse inductor current in synchronous buck converters when $I_{L(avg)} < \Delta I_L/2$, the SW-EN generator is designed and applied to disable the power switches under such conditions. As depicted in Fig. 4, the output over-voltage protection is also implemented in the SW-EN generator.

B. GATE DRIVER WITH DDTC

A gate driver is essentially required to not only adequately control the power switches but also consume less power, as in (9) and (10), since the ultra-wide size power switches

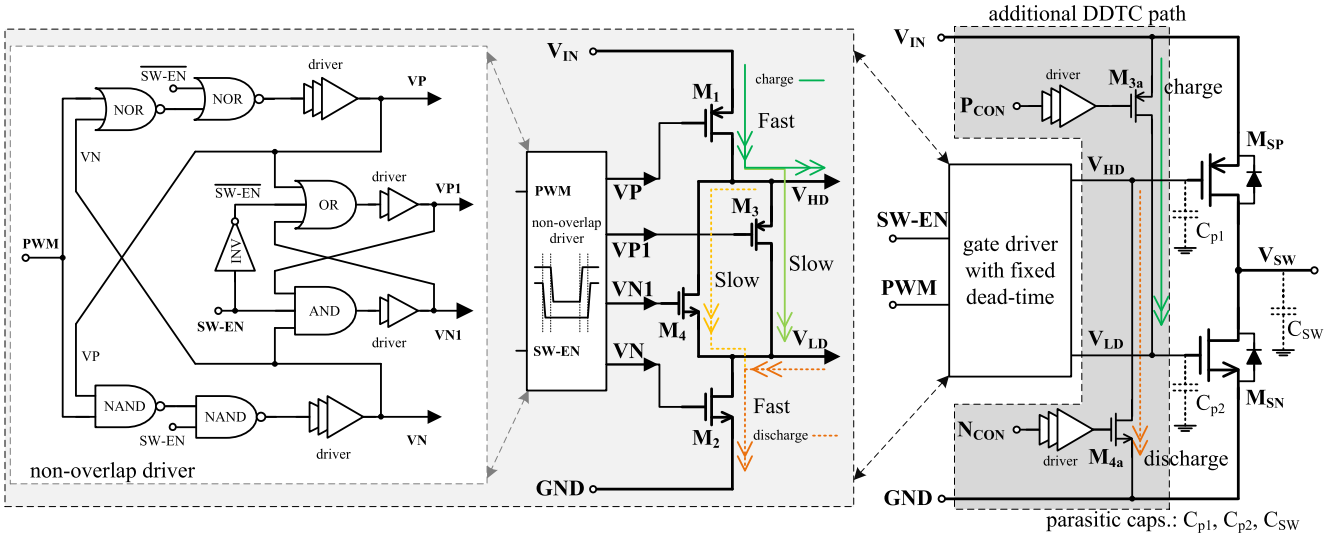

FIGURE 5. Proposed gate driver with dynamic dead-time control (DDTC).

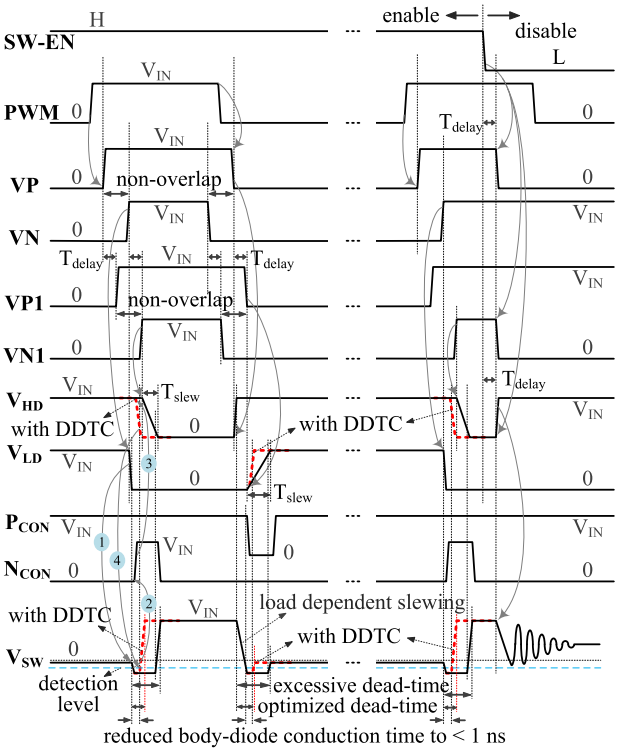

FIGURE 6. Waveforms of the proposed gate driver (with DDTC effects represented by the dashed lines).

are applied to support a large load current and to obtain small on-resistance for less conduction loss, as in (6).

The proposed gate driver with DDTC is depicted in Fig. 5 and its corresponding waveforms are presented in Fig. 6. Unlike the dead-time optimization methods in [12]–[15] that utilize complex circuit implementations and/or require additional capacitors and switches, the proposed DDTC method can be easily inserted into the conventional fixed dead-time gate driver in the synchronous buck converters via the additional DDTC path and BDCS circuit, which can dynamically optimize the effective dead-time at both on and off transitions of V_{SW} in every switching cycle for efficiency improvement.

A fixed dead-time gate driver is firstly designed based on the fast and slow paths, which relieves the requirements of the inverter-based driving chains and requires no delay capacitors [1]. The dead-time is generated by the propagation delay of the driving chains and the slewing time (T_{slew}) of the gate voltages V_{HD} and V_{LD}, where T_{slew} accounts for the major proportion and is controlled by the size of M_{1-4}. The size of the fast path transistor M_1 (M_2) is designed to around one-twenty-fifth of the power switches M_{SP}(M_{SN}), and the size of the slow path transistor M_3 (M_4) is set to around one-tenth of M_1 (M_2). An adequate fixed dead-time is generated via the fast and slow paths, whereas the switching noise and power loss of the gate driver are reduced [1]. However, a long body-diode conduction time will occur under medium and heavy load conditions, as discussed according to (2), which will cause large power losses, as in (9).

Therefore, the additional DDTC path controlled by the BDCS circuit is designed and inserted into the gate driver, which dynamically optimizes the effective dead-time by adjusting T_{slew} of V_{LD} (V_{HD}) via M_{3a} (M_{4a}). The additional DDTC path requires no quiescent current, and only consumes little switching power when it is activated at the on/off transition of V_{SW}. The size of M_{3a} (M_{4a}) is set to one-third of M_1 (M_2), which is about three times larger than the size of M_3 (M_4). The T_{slew} of V_{LD} (V_{HD}) is reduced once M_{3a} (M_{4a}) is activated by the control signal P_{CON} (N_{CON}); hence, the switching speed of the power switches is increased and the effective dead-time is reduced, as depicted in Fig. 6.

As illustrated in Fig. 6, at the on transition of V_{SW}, once VN becomes high, V_{LD} will be discharged down to ground quickly via the fast path (M_2) to turn off M_{SN} immediately. After a short delay, VN1 becomes high to attempt to turn

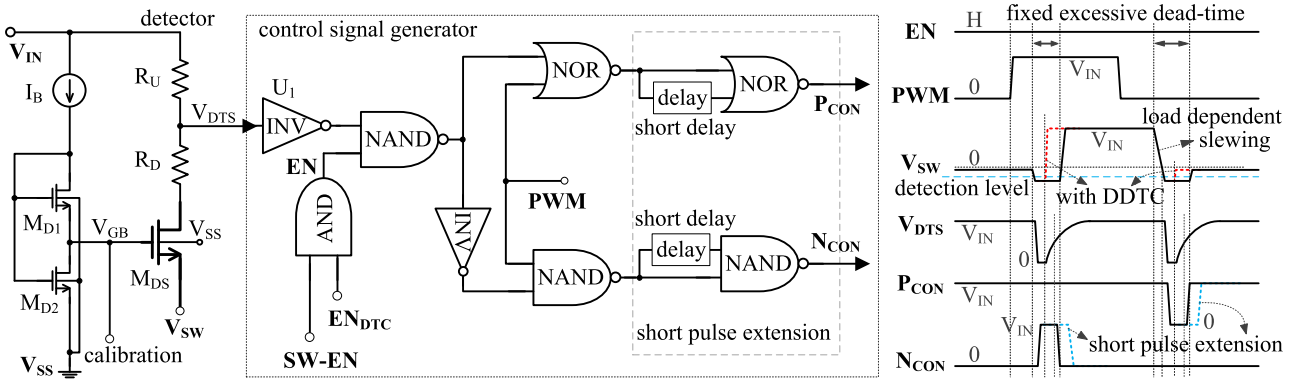

FIGURE 7. Proposed body-diode conduction sensor (BDCS) and the corresponding waveforms.

on M_4; hence, V_{HD} will be slowly discharged low via the slow path (M_4–M_2) to turn on M_{SP} when M_4 is turned on. During this on dead-time interval, the body diode conducts the inductor current and would be forward-conducted. Once the body-diode conduction is detected by the BDCS circuit, the signal N_{CON} is activated to quickly discharge the parasitic capacitor C_{p1} via the DDTC path (M_{4a}). Then, V_{HD} is pulled down quickly to turn on M_{SP} in order to prevent the body-diode conduction, as the dashed lines in Fig. 6.

Similar operations are performed at the off transition of V_{SW}. When VP becomes low, V_{HD} will be charged up to V_{IN} quickly via the fast path (M_1) to turn off M_{SP} immediately. After a short delay, VP1 becomes low to attempt to turn on M_3; hence, V_{LD} will be slowly charged high via the slow path (M_1–M_3) to turn on M_{SN} when M_3 is turned on. During this off dead-time interval, the body diode conducts the inductor current and would be forward-conducted. Once the body-diode conduction is detected by the BDCS circuit, the signal P_{CON} is activated to quickly charge the parasitic capacitor C_{p2} via the DDTC path (M_{3a}). Then, V_{LD} is pulled up quickly to turn on M_{SN} in order to prevent the body-diode conduction, as the dashed lines in Fig. 6.

By using the proposed design, the effective dead-time is dynamically optimized. Theoretically, with an appropriately designed BDCS circuit that predicts the excessive dead-time, the body diode cannot be turned on since M_{SP} (M_{SN}) will be turned on just before the body diode is forward-conducted. However, due to the propagation delay of the detector and driving chains, the body diode might be still forward-conducted for a short time. In this work, the body-diode conduction time is adjusted to be around 1 ns via the proposed BDCS circuit and additional DDTC path. Therefore, the body-diode-related power losses in (9) are reduced, particularly under medium and heavy load conditions.

C. BODY-DIODE CONDUCTION SENSOR (BDCS)

As illustrated in Fig. 7, the proposed BDCS circuit consists of a detector and a control signal generator. The detector detects the body-diode conduction via the V_{SW} signal, and activates the detection signal V_{DTS}. Then, the control signal generator differentiates the V_{DTS} signal into two control signals: N_{CON} and P_{CON} for the on and off transitions of V_{SW}, respectively, to control the additional DDTC path.

Instead of the complex undershoot detector and on-off circuit in [12], the detector is implemented by an NMOS transistor M_{DS} biased by a DC gate voltage V_{GB}. The V_{GB} determines the detection level of V_{SW} at the transition intervals. The value of V_{GB} is between V_{SS} and $(V_{THD} - V_{DS(on)})$, where V_{THD} is the threshold voltage of M_{DS}, and $V_{DS(on)}$ is the on drain-source voltage of the low-side switch. In this work, V_{THD} is about 610 mV, and V_{GB} is set to 200 mV; hence, when V_{SW} is less than –410 mV, M_{DS} will be turned on. The detection can be completed just before the body diode is forward-conducted where V_{SW} is about –750 mV. Therefore, the detector predicts the excessive dead-time.

In a standard CMOS process, the bulk of M_{DS} is directly connected to the substrate, which is different from the source. The threshold voltage of M_{DS} is slightly decreased due to the body effect since V_{SW} is always negative during the detection process, thereby leading to better detection.

Normally, M_{DS} is off since $(V_{GB} - V_{SW})$ is smaller than V_{THD}, and V_{DTS} is charged to V_{IN} via the resistor R_U. Once V_{SW} is pulled down to make $(V_{GB} - V_{SW})$ larger than V_{THD}, the M_{DS} is turned on, quickly decreasing V_{DTS} to even negative values. Thus, a resistor R_D is inserted between R_U and M_{DS} to prevent the latch-up issues that might be caused by a negative V_{DTS}. When M_{DS} is on, its resistance is negligible because of its wide size; hence, the V_{DTS} level can be calculated in the following manner:

$$V_{DTS} \approx \frac{R_D}{R_U + R_D}(V_{IN} - V_{SW}) + V_{SW}. \tag{15}$$

The V_{DTS} level can be well controlled by an appropriately selected R_U and R_D. In this work, R_U is set to 18 kΩ and R_D is set to 5 kΩ. Thus, V_{DTS} is quickly discharged when M_{DS} is on, and it is slowly charged when M_{DS} is off. In this manner, the detector achieves an ultra-fast detection, and the effective width of V_{DTS} is extended, as depicted in Fig. 7. Moreover, V_{DTS} is regulated by the inverter U_1, where U_1 is designed

with a large length to suppress the shoot-through current to less than 20 μA at the transition intervals. In addition, the effective width of the control signals P_{CON} and N_{CON} are further extended by a short delay to ensure the validity of controlling the additional DDTC path. The EN_{DTC} is an off-chip enable signal for testing purposes.

IV. EXPERIMENTAL RESULTS

The proposed four-phase synchronous buck converter is designed and fabricated using a 0.35-μm standard CMOS process. The buck converter is laid out in a 5.0 mm × 4.0 mm die for a quad flat package (QFP). The chip micrograph is presented in Fig. 8, which illustrates an active chip area of about 3.4 mm × 3.5 mm. The active area of each phase is about 1.35 mm × 1.75 mm, where the block of gate driver with DDTC consumes about 450 μm × 350 μm and the BDCS circuit occupies about 75 μm × 75 μm. The additional DDTC path occupies about 12% active area of the block of gate driver with DDTC, which introduces an increment of approximately 0.64% of the entire active chip area. The buck converter employs an inductor (L) of 1 μH in each phase and a shared output capacitor (C_{OUT}) consisting of four 22 μF ceramic capacitors to form the output LC filter.

The measured steady-state waveforms are depicted in Fig. 9, consisting of a DCM case and a CCM case. The measured duty cycle is slightly increased compared to the ideal value due to the parasitic component effects. The buck converter is able to support a wide range of output voltage from 1.0 V to 2.5 V, with the input supply voltage varying from 2.5 V to 3.3 V. With a 3.0 V input supply, a maximum load current of 6.0 A is obtained under a typical 1.2 V output voltage, whereas a maximum load current of 4.0 A is measured with a 1.8 V output voltage.

The measured on/off transition of the switching node voltage V_{SW} with DDTC in phase-I is illustrated in Fig. 10, at various load conditions. The negative peak voltage of V_{SW} is increased as the load current increases due to the higher power supply fluctuation [12] and parasitic ringing [13]. Without DDTC, a fixed dead-time of about 9.6 ns is generated and applied at both the on and off transitions; whereas with DDTC, the effective dead-time is dynamically optimized from the fixed value to a near-optimal value. The measured effective dead-time with DDTC at various load conditions is summarized in Table 1. Since the rising time t_{rh} of V_{SW} is with the slope $(I_{D,M_{SP}} - I_{L(avg)})/C_{SW}$ at the on transition [13], the effective dead-time is slightly increased as $I_{L(avg)}$ increases; whereas the falling time t_{fh} of V_{SW} is with the slope $-I_{L(avg)}/C_{SW}$ at the off transition, the effective dead-time is decreased as $I_{L(avg)}$ increases. The body-diode conduction time of about 1 ns is obtained with DDTC at both the on and off transitions.

The measured load transient response waveforms with a typical 1.2 V output voltage and a 3.0 V input supply are illustrated in Figs. 11 and 12. For load current steps from 0.1 mA to 1.0 A and vice versa, the output spike voltages are less than 38 mV and the load regulation is calculated as 12 mV/A. Due to the parasitic resistances of the bonding wires and PCB traces being more sensitive to heavy load conditions, the output spike voltage is increased and the load regulation is degraded to 33 mV/A for load current steps from 0.1 mA to 4.0 A and vice versa.

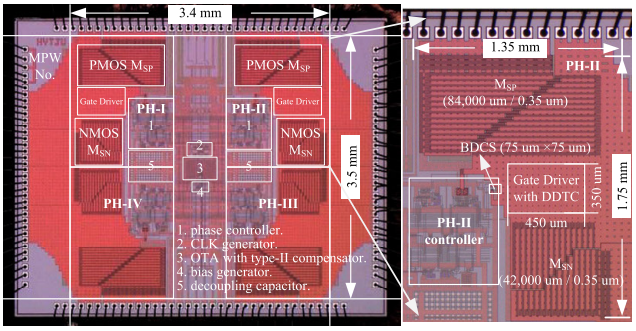

FIGURE 8. Chip micrograph of the proposed buck converter.

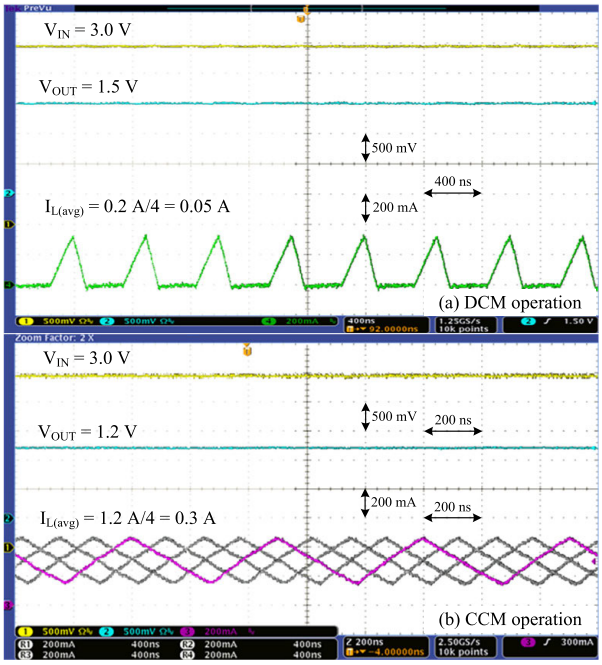

FIGURE 9. Measured steady-state waveforms of the proposed buck converter: (a) a DCM case and (b) a CCM case.

TABLE 1. Measured Effective Dead-Time at Various Load Conditions.

Load Conditions	effective dead-time with DDTC	
$I_{L(avg)} = I_{OUT}/4$	at on transition	at off transition
0.3 A	6.8 ns	8.8 ns
0.5 A	6.8 ns	8.4 ns
0.8 A	6.9 ns	7.8 ns
1.0 A	7.8 ns	6.6 ns
1.2 A	7.4 ns	5.6 ns
1.5 A	7.3 ns	5.2 ns

* dead-time without DDTC is about 9.6 ns at both on and off transitions.
** measured at V_{IN} = 3.0 V and V_{OUT} = 1.2 V.

TABLE 2. Performance Comparison with Reported Integrated Multiphase Buck Converters.

Parameters	[1]	[8]	[12]	[13]	[19]	[20]	[21]	This Work
Year	2014	2015	2007	2013	2015	2018	2019	2020
Technology	0.18-μm BCDMOS	0.13-μm BCDMOS	0.13-μm CMOS	0.35-μm CMOS	0.065-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	0.35-μm CMOS
Control Scheme	CM PWM/PFM	CM PWM	PWM	VM PWM	T-PID PWM	CCS	SAW Hysteretic	CM PWM
No. of Phases	4	4	1	1	4	4	4	4
F_S [MHz]	2.0	2.25	1.0	1.0	30 - 70	30	25	2.0
V_{IN} [V]	2.7 - 5.0	2.8 - 5.0	3.7	3.3	1.8	3.3	3.3	2.5 - 3.3
V_{OUT} [V]	0.8 - V_{IN}	0.68 - 1.92	1.8	1.5	0.6 - 1.5	0.7 - 3.0	0.3 - 2.6	1.0 - 2.5
$I_{OUT(max)}$ [A]	4.5	4.0	0.6	0.3	0.8	2.5	6.0	6.0*
L [μH]	0.47	0.47	N/A	N/A	0.09	0.22	0.2	1.0
C_{OUT} [μF]	2×22	88	N/A	N/A	0.47	0.62	2.47	4×22
Peak Efficiency [%] (V_{IN}/V_{OUT}) [V/V]	91.6 (2.7 / 1.8)	91.1 (2.8 / 1.0)	92.8** (3.7 / 1.8)	90*** (3.3 / 1.5)	87 (1.8 / 1.0)	88.1 (3.3 / 2.5)	88.1 (3.3 / 2.5)	92.8 (3.0 / 1.8)

* measured maximum $I_{OUT(max)}$: 6.0 A with 1.2 V output voltage and 4.0 A with 1.8 V output voltage from a 3.0 V input supply.
** simulation results. *** measured peak efficiency from the efficiency plots.

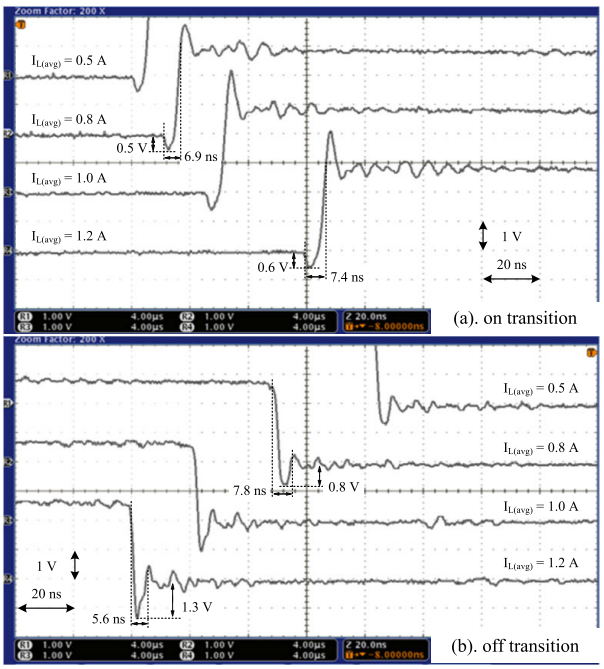

FIGURE 10. Measured on/off transition of the switching node voltage V_{SW} with DDTC in phase-I at various load conditions, with V_{IN} = 3.0 V.

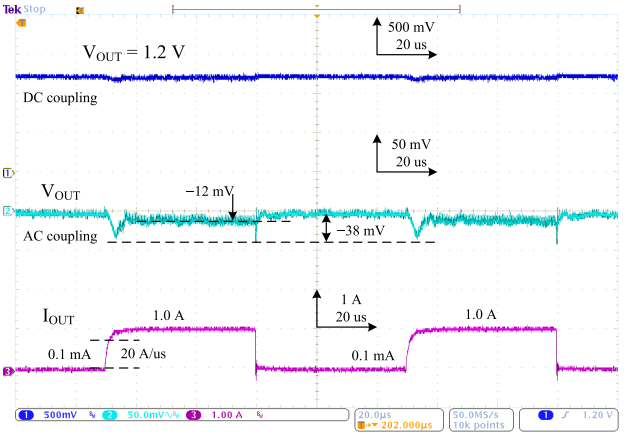

FIGURE 11. Measured load transient response of the proposed buck converter at V_{IN} = 3.0 V, V_{OUT} = 1.2 V, and I_{OUT} from 0.1 mA to 1.0 A.

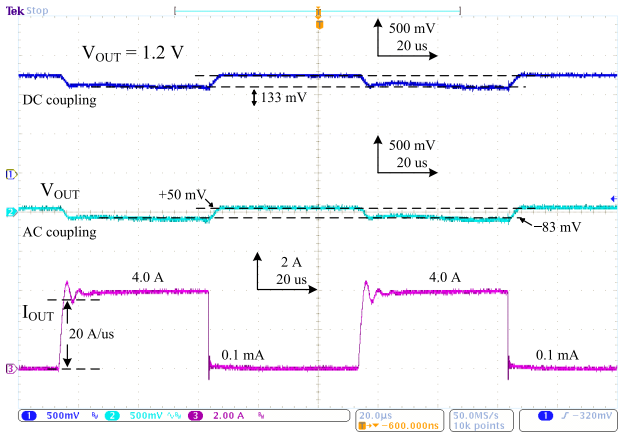

FIGURE 12. Measured load transient response of the proposed buck converter at V_{IN} = 3.0 V, V_{OUT} = 1.2 V, and I_{OUT} from 0.1 mA to 4.0 A.

The measured line transient response waveforms are presented in Fig. 13. When the 3.0 V input supply with a ±10% voltage variation is applied, the 1.2 V output voltage remains unchanged (within ±0.5%) at a 1.0 A load current.

The power efficiency plots are presented in Figs. 14 and 15, including the simulation results and measurement results. As I_{OUT} increases, the I_{OUT} related power losses in (6), (7), (9), (11), and (14) also increase; hence, the power efficiency decreases as the load current increases. A simulated peak efficiency of 96.1% (94.2%) is obtained at a 1.8 V (1.2 V) output voltage, whereas the measured peak efficiency is decreased to 92.8% (91.8%). This is because of the inherent parasitic component effects of the bonding wires and PCB traces, particularly under low-voltage high-current conditions; for

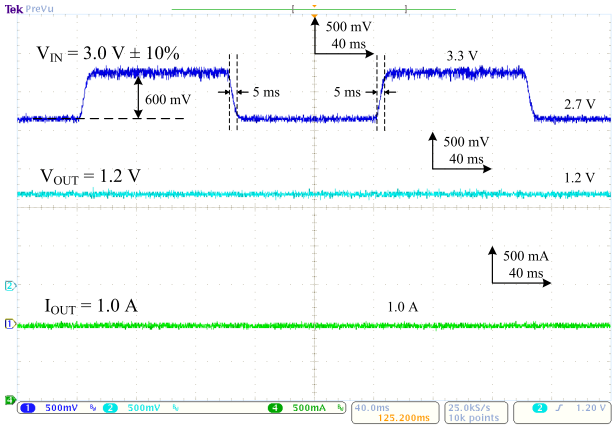

FIGURE 13. Measured line transient response of the proposed buck converter at V_{OUT} = 1.2 V, I_{OUT} = 1.0 A, and V_{IN} from 2.7 V to 3.3 V.

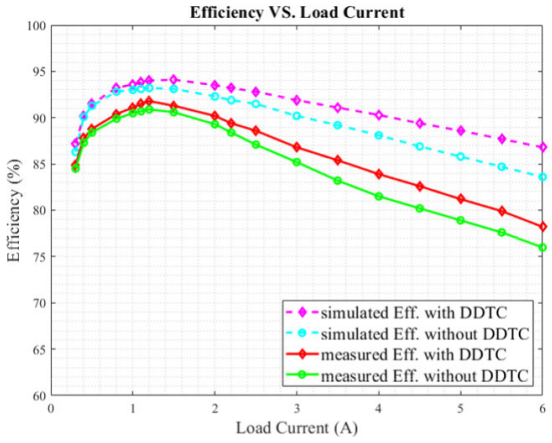

FIGURE 14. Efficiency versus load current plots of the proposed four-phase buck converter at V_{IN} = 3.0 V and V_{OUT} = 1.2 V.

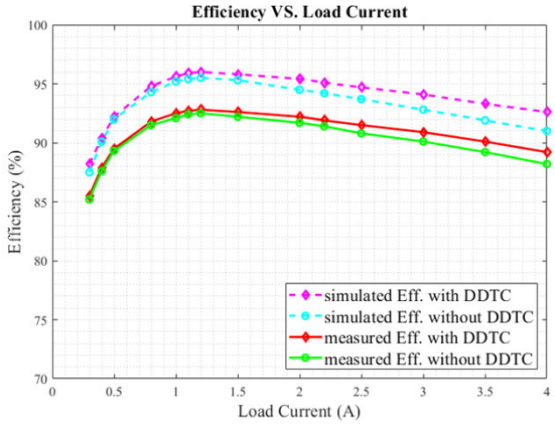

FIGURE 15. Efficiency versus load current plots of the proposed four-phase buck converter at V_{IN} = 3.0 V and V_{OUT} = 1.8 V.

example, the load resistance R_L is about 300 mΩ at 4.0 A load current with 1.2 V output voltage, whereas R_{trace} can be as much as 20 mΩ [16], which indicates about 6.7% power loss, as in (14). Since the optimized dead-time is obtained

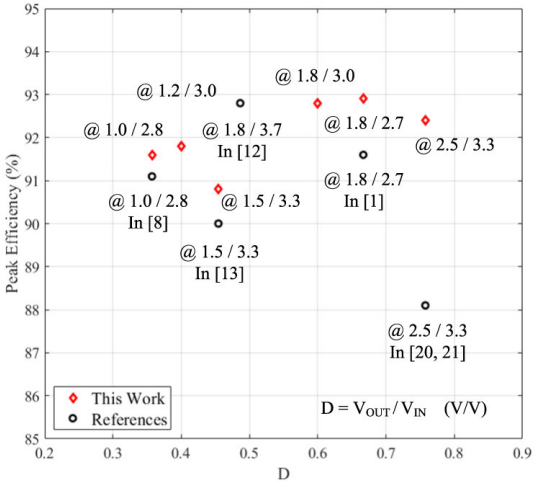

FIGURE 16. Peak efficiency of the proposed four-phase buck converter at various V_{OUT}/V_{IN} conditions.

with DDTC, the power efficiency is improved compared to the one without DDTC, particularly under medium and heavy load conditions. Under light load conditions, the DDTC path nearly cannot be activated because the initial fixed dead-time of about 10 ns is applied in this work; hence, there is little difference between the power efficiency plots with or without DDTC. However, under medium and heavy load conditions, the measured efficiency is improved by over 1.0% when the load current is over 2.0 A, and an efficiency improvement of about 2.4% is obtained at a load current of 4.0 A with a typical 1.2 V output voltage.

A brief performance comparison with previously reported works is summarized in Table 2. The multiphase topology is used for high-current delivery capability and low output voltage ripples. Moreover, high switching frequencies are usually applied for output filter size reduction and a fast transient response. However, as analyzed in Section II, there are certain trade-offs between the power efficiency, switching frequency (F_S), and transition performance, because the power losses in (7)–(10) are proportional to F_S. In this work, a moderate F_S of 2.0 MHz for each phase is applied to meet the transient response requirements and to obtain a high power efficiency, simultaneously. A measured maximum load current of 6.0 A (4.0 A) is obtained with an output voltage of 1.2 V (1.8 V) and input supply of 3.0 V, respectively. In addition, the peak efficiencies at various V_{OUT}/V_{IN} conditions are presented in Fig. 16, which indicates a better peak power efficiency.

V. CONCLUSION

A high-efficiency current-mode four-phase synchronous buck converter is presented in this work. A brief analysis of the power losses in the synchronous buck converter is reviewed to provide design guidelines. In spite of the design trade-offs between the power losses, switching frequency, size of power switches, and output filter, the dead-time can be optimized to improve the power efficiency in the synchronous

buck converters. Thus, a dynamic dead-time control (DDTC) method is proposed to reduce the power losses caused by the body diode, which can be easily inserted into a conventional fixed dead-time gate driver. A near-optimal dead-time adjustment is achieved via the DDTC method in every switching cycle, which not only prevents the shoot-through current but also minimizes the power losses caused by the body diode. A peak power efficiency of 92.8% is achieved at a 1.2 A load current of the proposed buck converter with a 1.8 V output voltage from a 3.0 V input supply. The power efficiency is improved for the moderate and heavy load conditions by over 1.0% when the load current is over 2.0 A, and an efficiency improvement of about 2.4% is achieved at a 4.0 A load current with a typical 1.2 V output voltage.

ACKNOWLEDGMENT

The chip fabrication and EDA Tools were supported by the IC Design Education Center (IDEC).

REFERENCES

[1] Y. Ahn, I. Jeon, and J. Roh, "A multiphase buck converter with a rotating phase-shedding scheme for efficient light-load control," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2673–2683, Nov. 2014.

[2] J.-T. Su and C.-W. Liu, "A novel phase-shedding control scheme for improved light load efficiency of multiphase interleaved DC–DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4742–4752, Oct. 2013.

[3] T. Reiter, D. Polenov, H. Pröbstle, and H.-G. Herzog, "PWM dead time optimization method for automotive multiphase DC/DC-converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1604–1614, Jun. 2010.

[4] P. Cheng, M. Vasic, O. Garcia, J. A. Oliver, P. Alou, and J. A. Cobos, "Minimum time control for multiphase buck converter: Analysis and application," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 958–967, Feb. 2014.

[5] W. Qiu, S. Mercer, Z. Liang, and G. Miller, "Driver deadtime control and its impact on system stability of synchronous buck voltage regulator," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 163–171, Jan. 2008.

[6] G. Eirea and S. R. Sanders, "Phase current unbalance estimation in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 137–143, Jan. 2008.

[7] R. F. Foley, R. C. Kavanagh, and M. G. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, Jun. 2012.

[8] Y.-S. Roh, Y.-J. Moon, J. Park, M.-G. Jeong, and C. Yoo, "A multiphase synchronous buck converter with a fully integrated current balancing scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5159–5169, Sep. 2015.

[9] Efficiency of Buck Converter. (Dec. 2016). *Rohm Semiconductor, Application Note*. [Online]. Available: https://fscdn.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/buck_converter_efficiency_app-e.pdf

[10] Y. Ahn, H. Nam, and J. Roh, "A 50-MHz fully integrated low-swing buck converter using packaging inductors," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4347–4356, Oct. 2012.

[11] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead times in DC–DC converters with synchronous rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 994–1002, Jul. 2006.

[12] F. Lima, M. Santos, J. Barata, and J. Aguiar, "Dead-time control system for a synchronous buck DC–DC converter," in *Proc. IEEE Conf. Power Eng., Energy Electr. Drives*, Nov. 2007, pp. 423–428.

[13] S. Lee, S. Jung, C. Park, C.-T. Rim, and G.-H. Cho, "Accurate dead-time control for synchronous buck converter with fast error sensing circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 3080–3089, Nov. 2013.

[14] W. Yan, C. Pi, W. Li, and R. Liu, "Dynamic dead-time controller for synchronous buck DC–DC converters," *Electron. Lett.*, vol. 46, no. 2, p. 164, 2010.

[15] C.-L. Kok, X. Li, L. Siek, D. Zhu, and J. J. Kong, "A switched capacitor deadtime controller for DC-DC buck converter," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 217–220.

[16] C. Wu, W. L. Goh, C. L. Kok, L. Siek, Y. H. Lam, X. Zhu, and R. P. Singh, "Asymmetrical dead-time control driver for buck regulator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 12, pp. 3543–3547, Dec. 2016.

[17] X. Zhou, P. Xu, and F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1153–1162, Nov. 2000.

[18] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, Dec. 2013.

[19] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-phase 30–70 MHz switching frequency buck converter using a time-based compensator," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2814–2824, Dec. 2015.

[20] Y.-W. Huang, T.-H. Kuo, S.-Y. Huang, and K.-Y. Fang, "A four-phase buck converter with capacitor-current-sensor calibration for load-transient-response optimization that reduces undershoot/overshoot and shortens settling time to near their theoretical limits," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 552–568, Feb. 2018.

[21] B. Lee, M. K. Song, A. Maity, and D. B. Ma, "A 25-MHz four-phase SAW hysteretic control DC–DC converter with 1-cycle active phase count," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1755–1763, Jun. 2019.

[22] S. Lee, "Demystifying type II and type III compensators using Op-amp and OTA for DC/DC converters," *TI, Appl. Rep.*, Jul. 2014, Art. no. SLVA662. [Online]. Available: https://www.ti.com/lit/an/slva662/slva662.pdf

[23] C.-J. Chen, Z.-Y. Zeng, C.-H. Cheng, and F.-T. Lin, "Comprehensive analysis and design of current-balance loop in constant on-time controlled multi-phase buck converter," *IEEE Access*, vol. 8, pp. 184752–184764, Oct. 2020.

[24] V. Svikovic, J. J. Cortes, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Multiphase current-controlled buck converter with energy recycling output impedance correction circuit (OICC)," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5207–5222, Sep. 2015.

[25] J. Gordillo and C. Aguilar, "A simple sensorless current sharing technique for multiphase DC–DC buck converters," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3480–3489, May 2017.

[26] H. Liu, D. Zhang, and D. Wang, "Design considerations for output capacitance under inductance mismatches in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5004–5015, Jul. 2017.

[27] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

[28] P. Azer and A. Emadi, "Generalized state space average model for multi-phase interleaved buck, boost and buck-boost DC–DC converters: Transient, steady-state and switching dynamics," *IEEE Access*, vol. 8, pp. 77735–77745, Apr. 2020.

JUN TANG received the B.S. degree in electronics and communications engineering from the Wuhan University of Science and Technology, Wuhan, China, in 2013. He is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, Hanyang University, Ansan, South Korea. His research interests include power management circuits and mixed-signal integrated circuits.

TIAN GUO received the B.S. and M.S. degrees in electrical and electronic engineering from the Tianjin University of Technology, Tianjin, China, in 2014 and 2017, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, Hanyang University, Ansan, South Korea. His research interests include power management circuits and mixed-signal integrated circuits.

JUNG SIK KIM received the B.S. degree in semiconductor science and technology from Junbuk University, Junju, South Korea, in 2017. He is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, Hanyang University, Ansan, South Korea. His research interests include power management circuits and mixed-signal integrated circuits.

JEONGJIN ROH (Senior Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from The University of Texas at Austin, in 2001. From 1990 to 1996, he was a Senior Circuit Designer for several mixed-signal products with the Samsung Electronics, Giheung, South Korea. From 2000 to 2001, he was a Senior Analog Designer for delta-sigma data converters with Intel Corporation, Austin, TX, USA. In 2001, he joined the faculty of the Hanyang University, Ansan, South Korea. His research interests include over sampled delta-sigma converters and power management circuits.