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Seven Level T-Type Switched Capacitor Inverter Topology for PV Applications

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ABSTRACT The conventional neutral point clamped (NPC) multilevel inverter topology needs voltage balancing circuits to balance the dc-link capacitor, the number of component count is high and output voltage is half of the input voltage which increase the size of the source side dc/dc converter in PV applications. In this paper, a new topology of seven level neutral point clamped inverter is developed. The proposed inverter has a self-voltage boosting capability using a floating capacitor to boost the output voltage one and half of the input voltage. In this proposed topology, no additional sensors are required for the floating capacitor voltage stability, which results in minimizing the complexity of designing the inverter. The direct link between the neutral point and the mid-point of the dc-link capacitors significantly reduces the leakage current and common mode voltage in this inverter. A thorough comparison between the developed topology and recent suggested topologies is carried out which set the benchmark for the proposed one due to its lower switch count and higher voltage gain. The proposed topology is verified in simulation and prototype hardware model and results are discussed with dynamic load variations. The efficiency of the inverter is 97.1% @200W and low as 88.1 % @ inductive load. The voltage THD is 17.01% for simulation and 19.3% I for experimental is results.

INDEX TERMS Switched capacitor circuits, seven level inverter, ANPC type, voltage boosting, self-voltage balancing.

I. INTRODUCTION

With the huge dependency for the energy requirement, the cost of the fossil fuels are increasing rapidly with a significant reduction in their quaintly along with the environmental concerns have leads to an investment and research in the other possible resources of energy. The renewable energy resources like photovoltaic (PV) or solar cells, wind energy ect., have given good alternative to the conventional fossil fuel, which have been used from centuries. These renewable energy resources are now used in almost every filed of applications and replacing the conventional resources of energy. Power electronic converters plays an integral part to the system consisting of renewable energy resources. Various categories of power electronic converters have been designed for the efficient and reliable power conversion which is necessitated due to the requirement of different applications. As the output of the most of the renewable resources are dc, the inverters are integrated in between renewable energy resources and load requires the ac voltage [1]–[4].

The use of multilevel inverters is increased significantly in last few decades due to their advantages like high quality output voltage waveforms and low voltage stresses. These attractive features have received more attention from the researcher to further improve the topology structure, reduction of component, etc. Among several multilevel inverter topologies, the NPC, and FC topologies utilize single dc source with several dc-link capacitors [5]–[7]. NPC topology suffers from the higher number of clamping diodes, balancing of dc-link capacitors (>3L) and non-uniform power distribution of the

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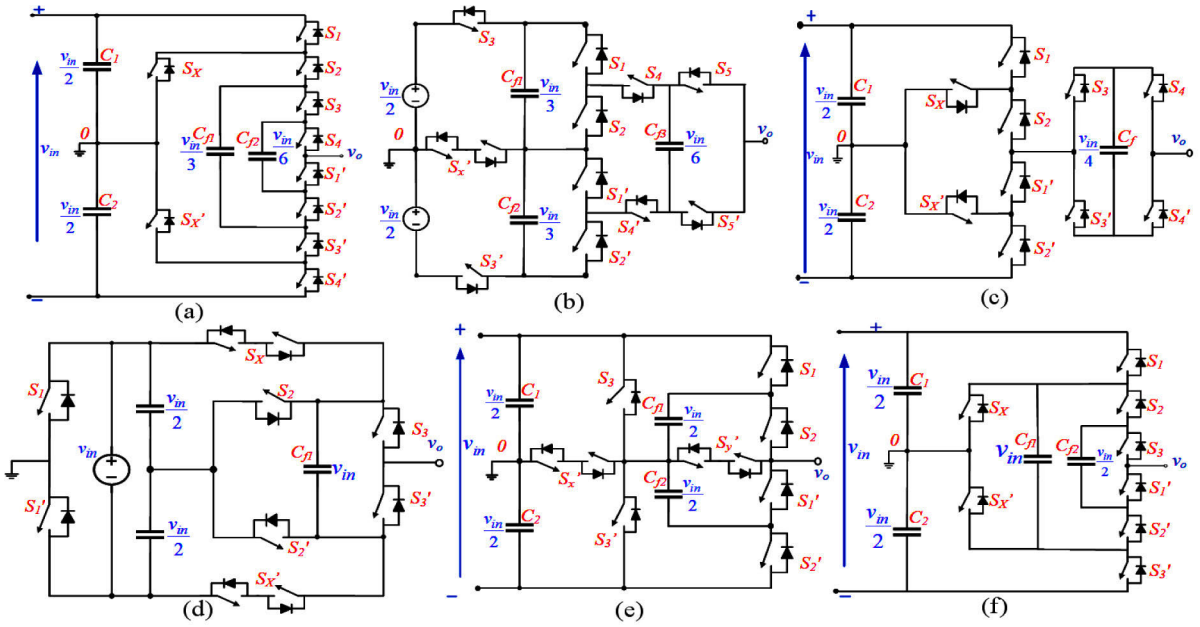

FIGURE 1. Multilevel inverter topologies (a) Topology 7L-ANPC [13], (b)Hybrid 7L-ANPC [14] (c) Hybrid 7L-ANPC-III [15], (d) 7L-SCMLI [16], (e) Topology DTT-7L-BANPC [17] and (f) 7L-Boost-ANPC [18].

switches. In order to resolve the drawback of NPC topology and to utilize the advantage of it, new ANPC topologies are developed. The floating capacitor of ANPC topology is balanced with or without sensors. The ANPC topology provide uniform power loss distribution and more precision control of the load [8] but the ANPC output voltage is half of the input voltage (v_{in}) and it exhibits the same characteristics of NPC. To increase the output voltage without adversely affecting the natural phenomena of ANPC, new topologies for switched capacitor multilevel inverter are proposed in [9]–[16]. A generalized structure of the switched capacitor multilevel inverter with self-voltage balancing is presented in [9]. In this a single dc source is used to provide the boosted output voltage based on number of switched capacitor cells. However, this topology needs more number of power components and the voltage stress on the switches are high, which in turn limits the medium and high voltage applications. Novel switched capacitor multilevel inverter structure is recommended in [10] and in order to generate high number of output voltage levels an extended topology is also presented. Further, this topology is configured in both symmetrical and asymmetrical mode, by extending the switched capacitor cell. The number of components are minimized but the voltage stress on switch is increased. Another topology with self-balancing and boosting capability is proposed in [11]. The topology uses eight switches and two diodes with a voltage boosting of 1:3. Since, the diode is presented in the main current path, the topology is not suitable for high inductive load applications. To overcome the stress on full bridge inverter switches, a cascaded topology is recommended, but the use of number of dc sources and other components are increased. These topologies are extendable to "m" number units and the voltage stress the on switch is also proportionally increasing. The output voltage is boosted to 1.5 times of v_{in} and it is presented in [12]. Voltage and current sensors are used to measure the change of voltage in floating capacitor and direction of load current. Further, logic form equation methods are implemented to select the appropriate levels based on the sensor output. This increases the complexity of the controller and reduces the reliability of the inverter because the whole operation depends on the sensors output. In order to resolve the above problems seven level topology with compact components and voltage stress on switches are presented in [13]–[24] and the recent innovated topologies are shown in Fig. 1(a)-(f).

In Fig. 1(a)-(c), the topologies are hybrid of the ANPC and FC structure. The structure uses two different voltage ratings of dc-link capacitors and the capacitor voltages are regulated by additional sensors. The output voltage of the inverter is always half of the input voltage (v_{in}). The boost converter topologies are shown in Fig. 1(d)-(f), where the output of these topologies is equal or higher than the input voltage. However, these topologies are suffering from high voltage stress and more number of power components. For less components, low voltage stress in a new boost active neutral point clamped T-Type 7-Level inverter (BANPC T-7L) topology is proposed in this paper.

II. PROPOSED BANPC T-7L INVERTER TOPOLOGY

Fig. 2 comprises of two dc-link capacitors (C_1 & C_2), one floating capacitor (FC) and nine switches ($S_1 - S_3$, $S_1' - S_3'$, B_x & S_x) with two diodes. The combination of a T-type and switched capacitor cell form the proposed 7L inverter topology. In the T-type inverter, the neutral point is taken at the mid-point of the series connected dc-link capacitors. The voltage across the dc-link capacitors C_1 & C_2 is $v_{in}/2$ and the voltage across the floating capacitor FC is equal to the input

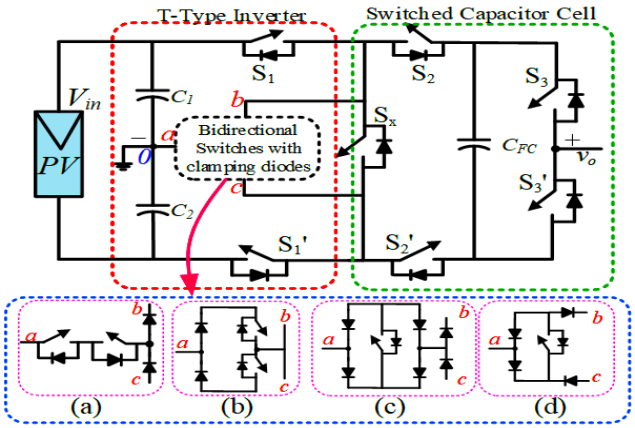

FIGURE 2. Proposed boost active neutral point clamped T-Type 7L switched capacitor inverter (BANPC T-7LSCI), (a)–(c) various bidirectional switch (Bx) and (d) proposed bidirectional switch (Bx).

TABLE 1. Switching sequence and corresponding states for BANPC T-7LSCI.

States	ON State Switches	ΔV_{FC}	V_o
STATE A	B_X, S_X,D,D',S_2,S_3	-	0 v_{in}
STATE A'	B_X, S_X,D,D',S_2',S_3'	-	
STATE B	S_1, S_2, S_1', S_2', S_3	▲	$+v_{in}/2$
STATE C	B_X, S_X,D,S_2',S_3	▼	$+v_{in}$
STATE D	S_1, S_X, S_2', S_3	▼	$+3v_{in}/2$
STATE E	S_1, S_2, S_1', S_2', S_3'	▲	$-v_{in}/2$
STATE F	B_X, S_X,D',S_2',S_3	▼	$-v_{in}$
STATE G	S_1', S_X, S_2, S_3'	▼	$-3v_{in}/2$

▲ - Charging of FC, ▲ - Discharging of FC

voltage (v_{in}). The upper capacitor C_1 is supplying the power in the first half cycle and C_2 in the second half cycle.

The proposed BANPC T-7L inverter topology has the following advantages:

i) Less power components
ii) Self-voltage balancing of floating capacitor (FC)
iii) Output voltage (v_o) is 1.5 times higher than v_{in}.
iv) The floating capacitor do not depend on the load power factor
v) Less leakage current since the neutral point is linked to the mid-point of dc-link capacitor.
vi) No additional circuits or sensors are needed for capacitors stability.
vii) Appropriate choice for transformerless grid connected PV system.

The switching sequence and corresponding output voltage is listed in Table 1. In that proposed topology Fig. 2(d) bidirectional switch is used which further reduce the two diodes. The various output voltage levels along with the current paths are shown in Fig. 3(a)-(h).

Mode ($0v_{in}$): Fig. 3(a) & (b) show the state A and A' and it provides the continuous current path in the zero voltage level. The switches *Bx* and *Sx* are conducting through the diode *D* and *D'* with S_2 & S_3 as given in Table 1.

TABLE 2. Voltage stress of switches.

V_o	S_1	S_1'	S_2	S_2'	S_3	S_3'	B_x	S_x
$3v_{in}/2$	0	$v_{in}/2$	v_{in}	0	0	v_{in}	$v_{in}/2$	0
v_{in}	$v_{in}/2$	$v_{in}/2$	v_{in}	0	0	v_{in}	0	0
$v_{in}/2$	0	0	0	0	0	v_{in}	$v_{in}/2$	v_{in}
Zero	$v_{in}/2$	$v_{in}/2$	0	v_{in}	0	v_{in}	0	0
$-v_{in}/2$	0	0	0	0	v_{in}	0	$v_{in}/2$	v_{in}
$-v_{in}$	$v_{in}/2$	$v_{in}/2$	0	v_{in}	v_{in}	0	0	0
$-3v_{in}/2$	0	$v_{in}/2$	0	v_{in}	v_{in}	v_{in}	$v_{in}/2$	0

TABLE 3. Current stress of switches.

v_o	S_1	S_1'	S_2	S_2'	S_3	S_3'	B_x	S_x
$3V_{in}/2$	I_o	0	0	I_o	I_o	0	0	I_o
V_{in}	0	0	0	I_o	I_o	0	I_o	I_o
$V_{in}/2$	I_o+I_c	I_o+I_c	I_o+I_c	I_o+I_c	I_o+I_c	0	0	0
Zero	0	0	I_o	0	I_o	0	I_o	I_o
$-V_{in}/2$	I_o+I_c	I_o+I_c	I_o+I_c	I_o+I_c	0	I_o+I_c	0	0
$-V_{in}$	0	0	I_o	0	0	I_o	I_o	I_o
$-3V_{in}/2$	I_o	0	I_o	0	0	0	0	I_o

I_o = Load current, and I_c = charging current

Mode ($+v_{in}/2$): The output voltage $v_{in}/2$, i.e both dc-link capacitors charge the floating capacitor through switches S_1, S_2, S_1' & S_2' and half of the input voltage $v_{in}/2$ is tapped to the load through S_3 as shown in Fig. 3(c) and State B given in Table. 1.

Mode ($+v_{in}$): In State C, the output voltage is equal to the input voltage and FC is discharged through the switches *Bx, Sx,* S_2' & S_3 as shown in Fig. 3(d).

Mode ($+3v_{in}/2$): The output voltage v_o is 1.5 times higher than v_{in}. It is obtained by adding the voltages of the upper capacitor (V_{C1}) and floating capacitor (V_{FC}). The corresponding switches S_1, *Sx*, S_2' & S_3 are turned ON as shown in Fig. 3(e). Similarly, in the negative half cycle the FC is charged and discharged as shown in Fig. 3(f)-(h). However, the maximum number conducting switches is five, which reduces the switching and conduction losses compare to topologies presented in [13]–[18].

The voltage and current stress of the proposed BANPC topology are given in Table 2 and 3 respectively. The switches S_1, S_1', and B_x need to block a voltage equal to half of the input voltage, i.e. $v_{in}/2$. The voltage blocking of the other switches needs to be equal to input voltage i.e., v_{in}.

III. CAPACITOR VOLTAGE ANALYSIS

The voltage of the capacitors are affected by several factors like output power magnitude with power factor, output voltage frequency, modulation technique, etc. In the literature, several modulation techniques have been discussed for the SC- based topologies, among which the phase disposition PWM (PD-PWM) technique has been extensively used. For the proposed topology, PD-PWM has been used and is shown

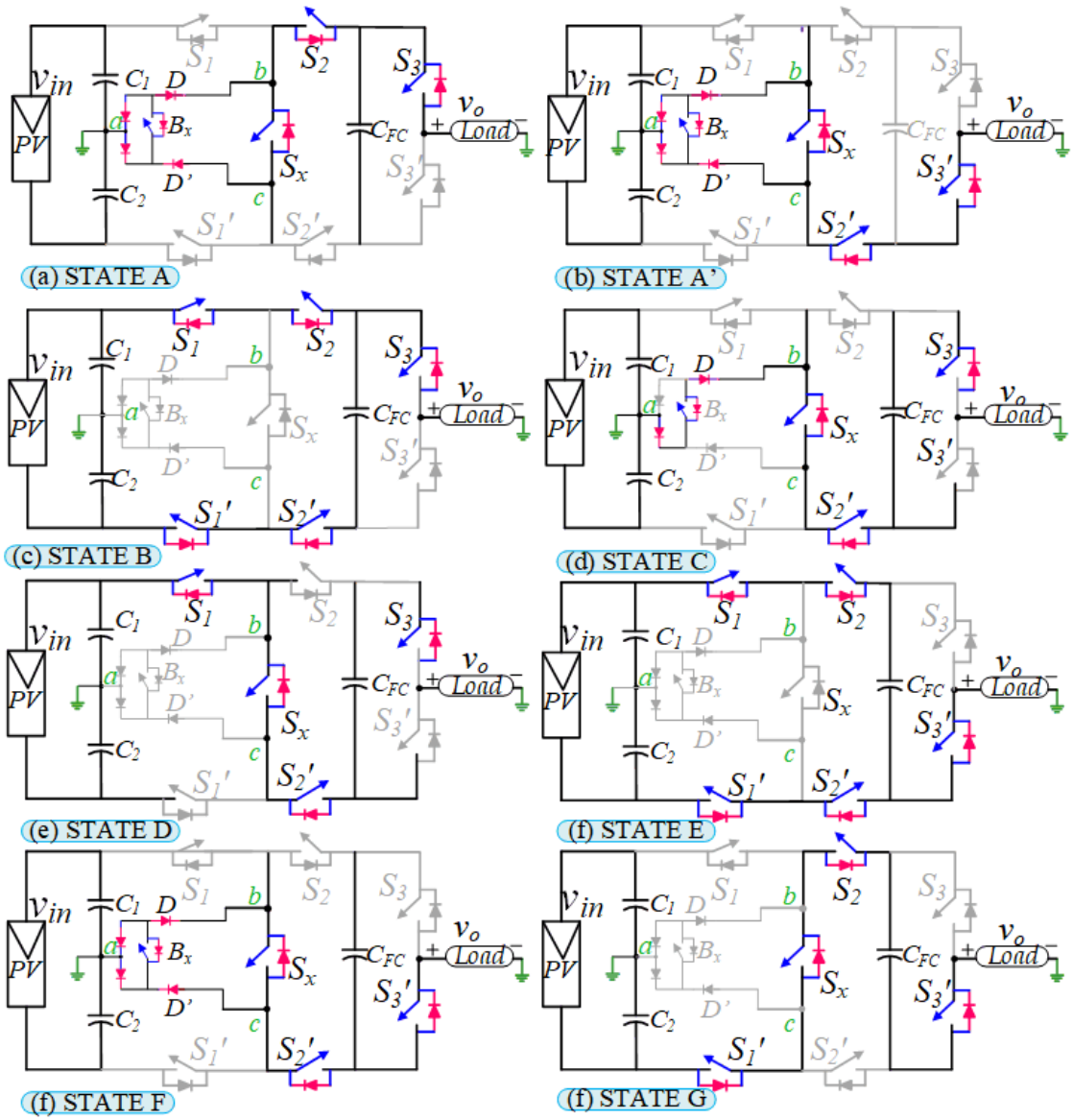

FIGURE 3. Operation modes of BANPC (a)-(h) different current path of each voltage level.

in Fig. 4 for a half cycle of the output voltage. To do the capacitor voltage analysis in the worst condition, the carrier signals can be replaced with some dc lines of magnitude equal to half of the carrier magnitude as shown in Fig. 4.

With worst condition, the output voltage is shown in Fig. 4 along with the floating capacitor voltage V_{FC}. Fig. 5 depicts the equivalent circuit with the capacitor connection for the proposed 7L topology with positive output voltage levels. The different equations for the output voltage are given as:

$$\left.\begin{aligned} V_o &= 0 \\ V_o &= \frac{V_{dc}}{2} e^{\frac{t_2-t_1}{R_L C_1}} \\ V_o &= V_{dc} e^{\frac{t_3-t_2}{R_L C_{FC}}} \\ V_o &= \frac{3V_{dc}}{2} e^{\frac{t_3'-t_3}{R_L (C_1+C_{FC})}} \end{aligned}\right\} \quad (1)$$

where R_L = resistive load, $C_1 = C_2$ = capacitance value of dc link capacitors and C_{FC} = capacitance value of FC.

The determination of capacitance is based on the discharging duration. Here, in second level (v_{in}) the floating capacitor continuous discharging and this duration is called as longest discharging duration (LDD) as shown in Fig. 6. This LDD is taken in to consideration while choosing the value of the floating capacitors. The maximum discharging and optimal capacitance for the developed inverter is expressed by

$$Q_{FC} = 2 \times \int_{t2}^{T/4} i_o(t)dt \quad (2)$$

where i_o is load current

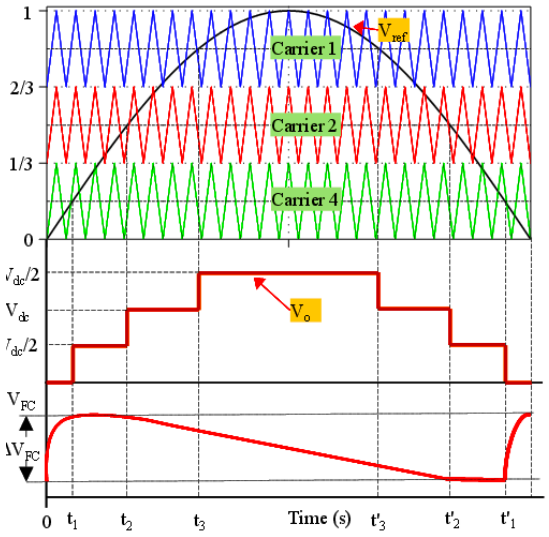

FIGURE 4. PD-PWM, output voltage and floating capacitor voltage variation of FC.

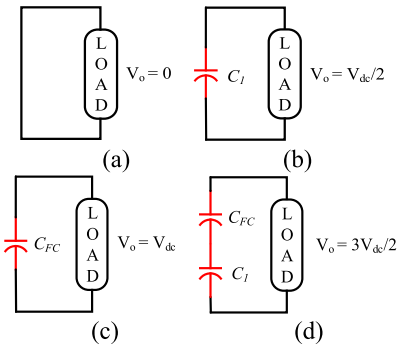

FIGURE 5. Equivalent voltage states with (a) $V_o = 0$, (b) $V_o = V_{dc}/2$, (c) $V_o = V_{dc}$ (d) $V_o = 3V_{dc}/2$.

A. FOR RESISTIVE LOAD (RL)

The load current during the level 2 and level 3 w.r.t to time period is expressed in (3)

$$i_o(t) = \begin{cases} \frac{v_{in}}{R_L} & t_2 \le t \le t_3 \\ \frac{3v_{in}}{2 \times R_L} & t_3 \le t \le \frac{T}{4} \end{cases} \tag{3}$$

where t_3 and t_2 equal $3T/16$ and $T/8$, respectively. The optimal capacitance for the FC with the highest acceptable voltage ripple is

$$Optimum_{Cap} \ge \frac{Q_{FC}}{k \times v_{in}} \tag{4}$$

where "k" is the FC ripple factor which lies between 0 to 1. Considering (2), (3), and (4) yields the optimal FC value as

$$Optimum_{Cap}, FC \ge \frac{5\pi}{8R_L \times k \times \omega \times v_{in}} \tag{5}$$

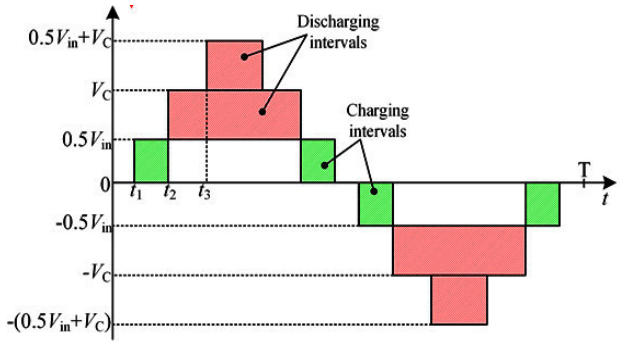

FIGURE 6. A typical seven level output voltage waveform of fundamental switching scheme.

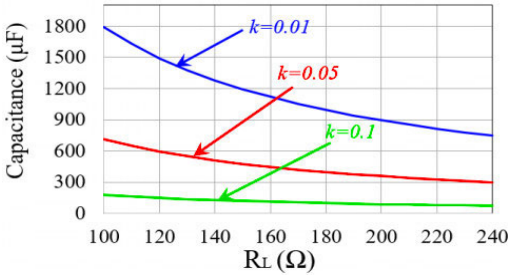

FIGURE 7. Optimum capacitance Value for various resistive load.

B. FOR RESISTIVE-INDUCTIVE LOAD

Considering the inductive loading condition, the load current is expressed as

$$i_o(t) = I_m Sin(\omega t - \varphi) \tag{6}$$

where I_m is maximum load current, φ-is phase angle between voltage and current. Therefore, by applying (2), (3) & (6) in to (4), the optimum capacitance is obtained from (7)

$$Optimum_{Cap}, FC \ge \frac{2I_m}{k \times \omega \times v_{in}} \left[cos\left(\frac{\pi}{4} - \varphi\right) - sin(\varphi) \right] \tag{7}$$

From the above equations (4) and (6) it can be seen that the optimum capacitance value is inversely proportional to the voltage ripple factor (k) and frequency ($\omega = 2\pi f$). In Fig. 7, the optimum capacitance value for various resistive load is shown for constant load current.

C. POWER LOSS ANALYSIS

With the association of power semiconductor devices to a converter topology, two types of losses occur with them, i.e., conduction losses and switching losses. The overall power loss of the power semiconductor device is given as

$$P_{loss} = P_c + P_{sw} \tag{8}$$

where Ploss represents the total power loss of the device, Pc amounts the conduction losses and Psw shares the switching loss of the Ploss.

TABLE 4. Comparison with other recent SCMLI topologies [9]–[18].

Topologies	N_{Switch}	N_{Diode}	N_{FC}	N_{ON-Sw}	MV_{FC}	MBV	H=MBV/v_o	G=v_o/v_{in}	Family of NPC	Remarks
[9]	7	4	2	4	v_{in}	3 v_{in}	1.0	1:3	No	The MBV is high.
[10]	9	1	2	5	v_{in}	3 v_{in}	1.0	1:3		
[11]	8	2	2	4	v_{in}	3 v_{in}	1.0	1:3		
[12]	9	-	1	5	$v_{in}/2$	v_{in}	0.66	1:1.5		Need sensors to balance the FC voltage
[13]	10	-	2	5	$v_{in}/2$	$v_{in}/2$	1.0	1:0.5	Yes	Number of switches are high and v_o<v_{in}.
[14]	12	-	3	5	$v_{in}/3$	$v_{in}/2$	1.0	1:0.5		Number of switches are high and v_o<v_{in}.
[15]	10	-	3	5	$v_{in}/4$	$v_{in}/2$	1.0	1:0.5		Number of switches and FCs are high and v_o<v_{in}.
[16]	10	-	3	6	v_{in}	v_{in}	0.66	1:1.5	No	Number of switches are high
[17]	10	-	2	5	v_{in}	2 v_{in}	1.33	1:1.5	No	High MBV and Switch Count also high
[18]	8	-	2	7	v_{in}	v_{in}	1.0	1:1	Yes	v_o=v_{in}, voltage gain is 1.
[19]	12	-	2	8	v_{in}	2 v_{in}	0.66	1:3	No	Switch Count is high
[24]	8	1	2	4	2 v_{in}	3 v_{in}	1.0	1:3	No	High MBV and Switch Count also high
Proposed	8	4	1	4	v_{in}	v_{in}	0.66	1:1.5	Yes	MBV equal to v_{in}, number of switches are less and 1.5v_o>v_{in}

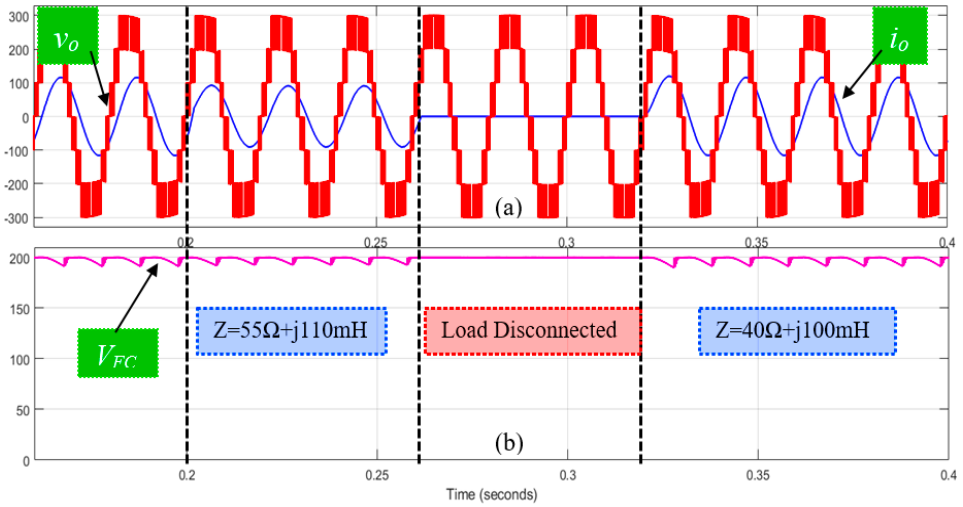

FIGURE 8. Simulation results during the dynamic load variations (a) Load voltage and current (b) the FC voltage.

The conductor losses within a device occur due to the power loss of the internal resistance. The conduction losses can be calculated as

$$P_c = \sum_{allswitches} I_{o,switch}^2 R_{on} \tag{9}$$

where $I_{o,switch}$ gives the current flow through each device and R_{on} is their internal resistance during the ON state of the device.

The other major losses are the switching losses. Switching losses take place in a power semiconductor device due to the intrinsic switching delays. Due to this, the voltage and current has a certain value and they overlap each other, results in the switching loss of the device which is given as

$$P_{sw} = \left[\sum_{allswitches} \sum_{within\ 1/f_o} \frac{V_{on} I_{on} T_{on}}{6} + \frac{V_{off} I_{off} T_{off}}{6} \right] \times f_o \tag{10}$$

where Von, Ion, and Ton are the *on*-state quantities of voltage, current and time over the on-transition period respectively. Voff, Ioff, and Toff are the off-state quantities of voltage, current and time over the off-transition period respectively. f_o represents the frequency of the output voltage waveform.

D. COMPARISON WITH OTHER RECENT ANPC TOPOLOGIES

In Table 4, the proposed 7L topology is compared with recent multilevel inverters using switched capacitor. A comparison for number of switches, (N_{Switch}), number of diodes (N_{Diode}), number of floating capacitors (N_{FC}), maximum voltage rating of floating capacitor (MV_{FC}) and maximum blocking voltage (MB V) on the switch is presented. Further, the maximum voltage on switches in terms of output voltage (H) and output voltage gain (G) is presented. The topologies [9]–[11] uses full bridge inverter circuit at the output having a voltage stress which is 3 times higher than the input voltage. In [12],

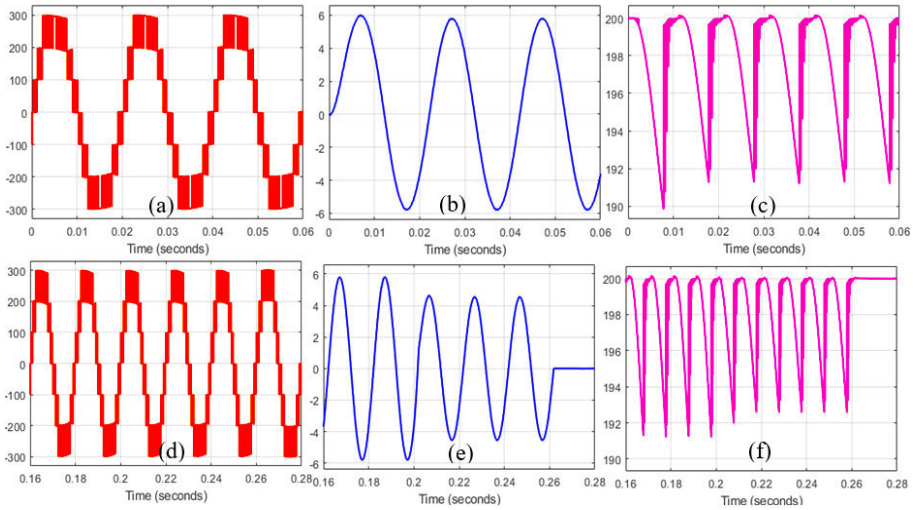

FIGURE 9. Zoomed view of simulation results during the steady state and dynamic load variations (a) for steady state Load voltage (b) for steady state load current (c) for steady state FC voltage (d) dynamic load variations load voltage (e) dynamic load variations load current and (f) dynamic load variations FC voltage.

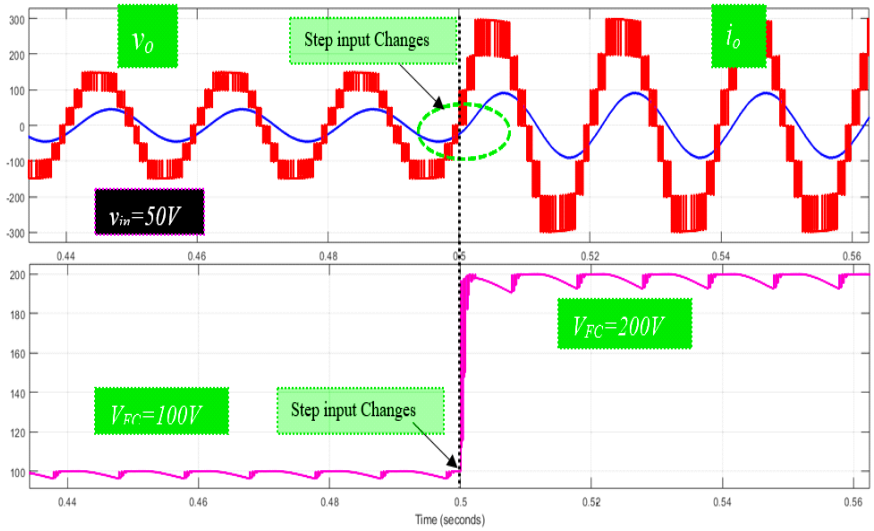

FIGURE 10. Simulation results during the v_{in} variations (a) v_{in} = 100V to v_{in} = 200V (b) the corresponding FC voltage.

the topology uses single dc source and no neutral mid-point. The topology needs voltage and current sensors to balance the floating capacitor and it decreases the reliability and increases the complexity of system. The output voltage is half of the input voltage but the uneven loss distribution is resolved in [13]. The topology with three floating capacitors and different voltage ratings are used [14] and sensors are required to balance the floating capacitors. In [15], the topology is developed for 7L output voltage waveform. The floating capacitor voltage is lower than the input voltage and the output voltage is half of the input voltage. The floating capacitor voltage and number of switch count are high in [16] and the voltage stress is also high. Other topologies [17], [18] are suitable for transformerless inverter operation due to the neutral point is directly connected to mid-point of the dc-link capacitors.

IV. RESULTS AND DISCUSSION

A. SIMULATION RESULTS OF THE PROPOSED 7L BOOST TOPOLOGY

The simulation of the proposed 7L BANPC has been conducted using MATALB/Simulink software and have been discussed in the section. The different parameters used for the simulation has been listed in the Table 5.

The simulation results for sudden load changing waveforms are given in Fig 8(a)-(b). In Fig. 8(a) load changing sequence of R = 40 Ω & L = 100 mH to R = 55 Ω & L = 110 mH to No-load to R = 40 Ω & L = 100 mH. When the load is Z = 40 Ω+ j100 mH the peak output current is ∼5.8A with current RMS of ∼4.1A as shown in Fig. 8(a) and after load changes occur the load current is reduced to 4.6A with current RMS 3.2 A for the power factor of (pf) 0.85.

TABLE 5. Simulation parameters.

Component		Rating/Value
Input Voltage (v_{in})		200V
Output voltage (v_o)		300V
Capacitors (C_{FC})		2700 µF
Switching & Fundamental Frequency		2.5 kHz & 50 Hz
Resistive, Inductive	Load 1	40 Ω, 100 mH,
	Load 2	55 Ω ,110mH

TABLE 6. Experimental parameters.

Description	Model Number	Ratings
Input voltage (v_{in})	-	200 V
Output voltage (v_o)	-	300V
Load	R-L Load Bank	2.0k W
Switches (MOSFET)	IRF640	600V/18A
Driver Circuits	TLP 250A	10-35 V/5 mA
Maximum Power @ load (P_{max})	-	~0.9 kW

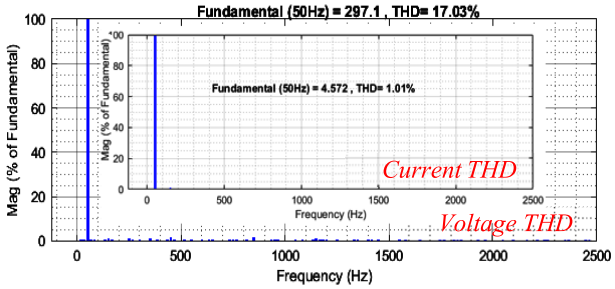

FIGURE 11. Voltage and current THD for Z = 55Ω+j110 mH.

In no-load condition, the output current is zero. However, during the load change the output voltage and the FC voltage is not affected and it is evident that the proposed topology is adoptable to load variation. In Fig. 8(b), the FC voltage ripple is little bit varying due to increasing of load current and maintaining constant at no-load condition. The zoomed view of the output voltage and current during the steady state and dynamic state is shown in Fig. 9. In this the FC ripple voltage is approximately varying to maximum of 10% which is allowable range. In normal the ripple voltage is allowable from 5% to 10%. When the v_{in} is varying the inverter circuit should maintain the output voltage level. In order to confirm the performance of proposed inverter during the v_{in} variations is shown in Fig. 10. In this the v_{in} changed from 100V to 200V (i.e $V_{C1} = V_{C2} = 50$V) and the output voltage level is maintained to 9L without any oscillation as shown in Fig. 10(a). During the v_{in} changing time the FC voltage also raised from 100V to 200V as shown in Fig. 10(b). The THD value of output voltage is 17.03% and current THD is 1.01% for the load impedance of Z = 55Ω+j110 mH as shown in Fig. 11.

B. EXPERIMENTAL RESULT

The experimental results of the proposed 7L output voltage and current are shown in Fig. 12(a)-(d). The experimental parameters are given in Table. 6.

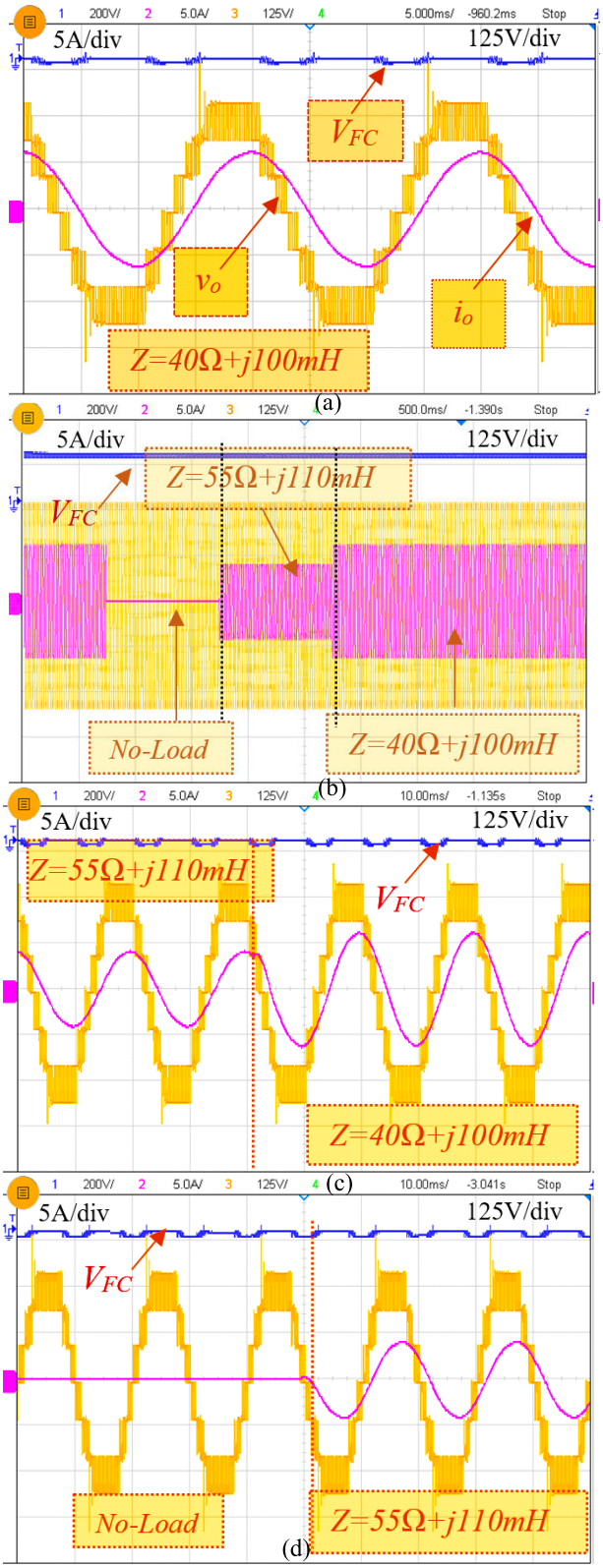

FIGURE 12. Experimental results (a) Output voltage and current (c)-(d) different load variations.

In the experiment, the input voltage (v_{in}) is 200 V, the dc-link capacitors C_1& C_2 are rated for 100V/470 μF and the rating of floating capacitor is 200V/2.7 mF. The output

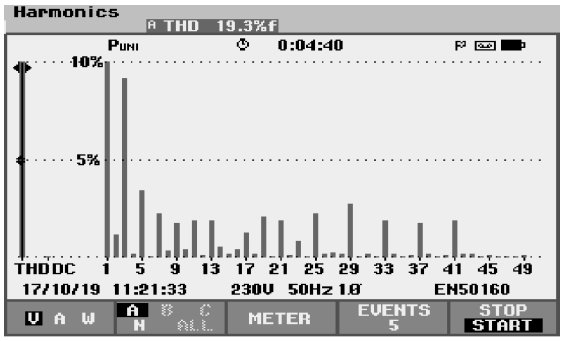

FIGURE 13. Experimental voltage FFT spectrum.

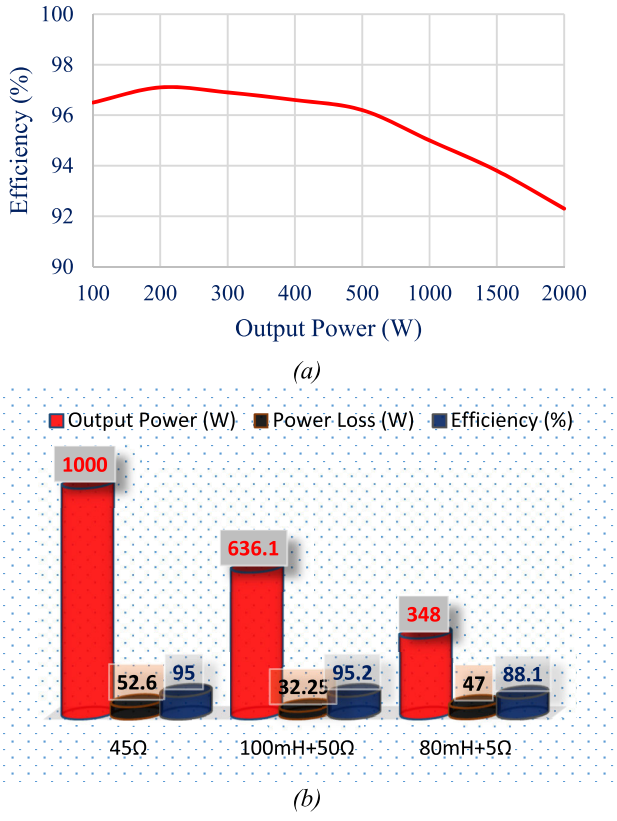

FIGURE 14. (a) Efficiency vs output power curve and (b) output power, power loss and efficiency with different loading condition.

voltage is 300 V (v_o), which is 1.5 times higher than v_{in}. The conventional SPWM switching method is used to generate the switching pulses. The resistive and inductive loads values are 40 Ω & 100 mH, respectively. When the load is low the output current is 5.7 A (i_o) with a lagging power factor of 0.79 due to high inductive load. Sudden load change is applied from Z = 40 Ω+j 100 mH to Z = 55 Ω +j 110 mH to no-load the corresponding waveforms are shown in Fig. 12(b). When the load change from low to high the output current is reduced from high to low (P_{max} = 0.7kW) as shown in Fig. 11(b). Further the clear view of each load change is shown in Fig. 12(c)-(d).

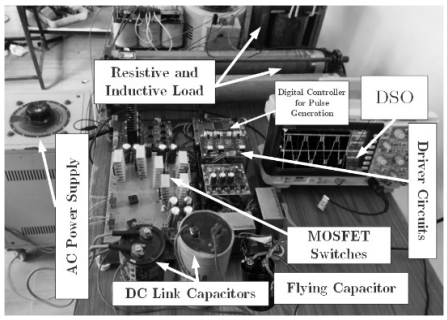

FIGURE 15. Photo of experimental setup.

TABLE 7. Power loss distribution of the proposed topology with Z = 50 Ω+j100mH.

Power Loss of	P_{sw} (W)	P_c (W)	P_{loss} (W)
Switch S_1	0.1981	3.7901	3.9882
Switch S_1'	0.1923	3.7895	3.9818
Switch S_2	0.0705	4.4808	4.5513
Switch S_2'	0.1018	4.2647	4.3665
Switch S_3	0.0173	1.4601	1.4774
Switch S_3'	0.0158	1.2377	1.2535
Switch B_x	0.0749	1.0216	1.0965
Switch S_x	0.011	2.1105	2.1215
Total switch losses	0.6817	22.155	22.8367
Didoes			2.2023
Capacitors			7.2123

The proposed topology is tested in switching frequency of 2.5 kHz. However, during the load changes the output voltage is not affected and the floating capacitor (V_{FC}) is able to supply the energy as required by the load without any disturbance. Since at the input side two capacitors are used, which is balancing automatically with a small ripple voltage as shown in Fig. 11(b). The THD FFT spectrum for output voltage is shown in Fig. 13. In simulation the THD value is 19.3%.

The power loss of the proposed topology has also been estimated. Fig. 14(a) depicts the efficiency curve of the proposed topology. The maximum efficiency of the proposed topology comes out to be 97.1% with the output power of 200W. In addition, the proposed topology has significantly higher efficiency at higher output power as shown in Fig. 14(a). Fig. 14(b) illustrates the effect of loading on the efficiency at different loading conditions. With purely resistive load of 45Ω, the output power is 1000W with the efficiency of 95%. As the load is changed to a combination of resistive-inductive load (Z = 100mH + 50Ω), the efficiency becomes 95.2% with output power of 636.1W. Similarly, with a highly inductive load (Z = 80mH + 1Ω), the efficiency drops to 88.1% due to higher demand of reactive power. The experimental setup photo is shown in Fig. 15.

The power loss breakdown of different components of the proposed topology has been given in Table 7. The switch pair

(S_1, S_1') and (S_2, S_2') have the higher power losses as both switches are involve in the charging of the FC along with the generation of different voltage levels.

V. CONCLUSION

New topology of seven level switched capacitor inverter with self-voltage balancing and boosting has been presented in this paper. The proposed topology requires a lower number of power components with a maximum voltage of v_{in}. The sizing of capacitance is analyzed by selecting the longest discharging time duration. The comparison was carried out in this study which proved that the proposed topology overcomes the other recent SCMLI topologies presented in the literature. Further, in simulation, sudden load changes are applied and results are shown. The results show that the proposed topology is suitable for dynamic load varying applications and also due to the direct connection of the neutral to mid-point, this topology is more suitable for transformerless grid connected PV applications.

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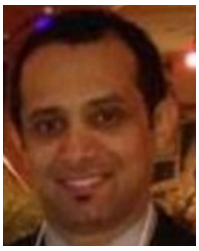

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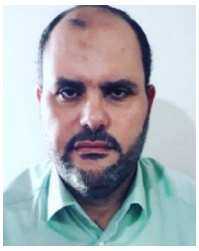

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