IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 6, 2021, accepted May 16, 2021, date of publication May 26, 2021, date of current version June 8, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3083721

A Comprehensive Review of Fault Diagnosis and Tolerant Control in DC-DC Converters for DC Microgrids

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This work was supported in part by the Research Development fund of XJTLU under Grant RDF-16-01-10 and Grant RDF-17-01-28; in part by the Research Enhancement fund of XJTLU under Grant REF-17-01-02; in part by the Suzhou Prospective Application programme under Grant SYG202016; and in part by the XJTLU Key Programme Special Fund under Grant KSF-A-08 Grant KSF-E-13, and Grant KSF-T-04.

ABSTRACT As the power interface between the energy storage devices (ESD) and the dc link of DC Microgrids, dc-dc converters, which have been regarded as the heart of many critical applications such as electrical vehicles, data center, and aerospace power systems, have gained more and more attentions recently. The fault diagnosis and tolerant control in dc-dc converters become essential to ensure a reliable and robust power system especially for critical applicants, where a sudden stoppage, loss of functionality, or degradation of performance might result in a catastrophe. This paper focuses on different types of faults in dc-dc converters by analyzing main failure spots and mechanism, covering catastrophic fault and parametric fault from component to system. A comprehensive review of the up-to-date fault mode analysis, fault diagnosis signals and algorithms, and fault tolerant control in various dc-dc topologies has been presented. This research will provide a useful design guideline for the reliability improvement in all forms of dc-dc converters.

INDEX TERMS DC-DC converters, fault detection, fault diagnosis, fault tolerance, reliability.

I. INTRODUCTION

Reliance on fossil fuel also known as dirty fuel for energy generation and transportation is not only contributing to climate change, but also causing health issues by releasing toxins in our environment. In an attempt slow down the climate change, a call for transition to nonpolluting alternate energy resources has been made. Renewable energy sources such as photovoltaic, geothermal and wind have been foreseen to replace the fossil fuel and huge effort is underway to make these resources cost-competitive. However, renewable energy resources are intermittent by nature and some times too small for traditional grid usage. To utilize these renewable energy resources, DC microgrids are introduced which acts as a power cluster of distributed energy generation units, energy storage devices and load accumulated together in vicinity to each other. DC microgrids have become the focus of interest due to its higher efficiency, flexibility, reduced capital cost, simpler control and its natural interface with the energy storage systems, electronic loads and renewable energy resources. DC-DC converters have been regarded as the heart of these DC microgrids and many other critical applications such as electric vehicles, data centers, and aerospace power systems etc. Figure 1 shows the system structure of DC microgrids, where DC-DC converters are acting as the power interface between the solar panels, fuel cells, super capacitors and the dc link of DC microgrids. As one of the oldest and vital branches of power electronics, a lot of research has been carried out to develop more efficient and low loss DC-DC converters. Several isolated and non-isolated topologies have been introduced along with more efficient control schemes. In terms of usage, there is no ultimate converter that is suited perfectly to all possible applications. These days, high performance converters are employed which have the advantage of wide input output range, high gain and low cost. Unfortunately these advantages come at the price of added stresses on the capacitors, semiconductor switches and diodes which make these components more prone to failure.

The associate editor coordinating the review of this manuscript and approving it for publication was Cristian Zambelli.

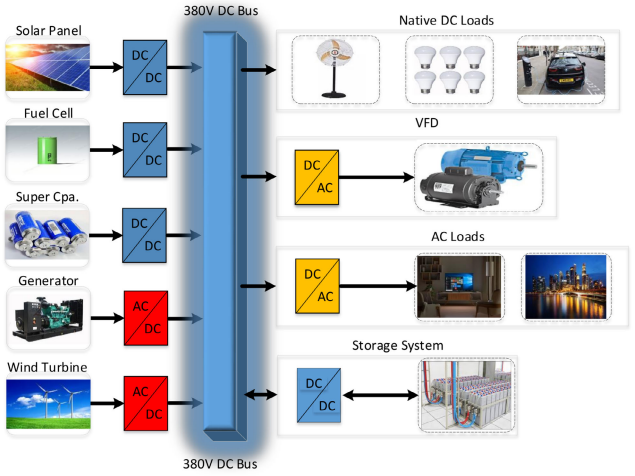

FIGURE 1. System structure of DC microgrids.

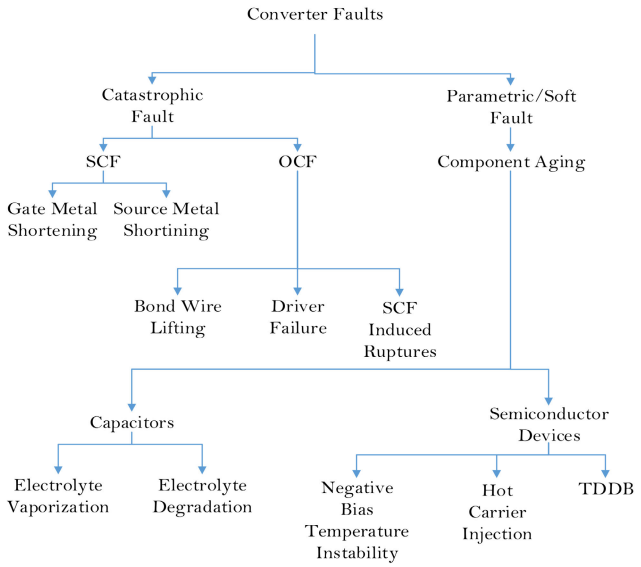

FIGURE 2. Classification of typical faults in DC-DC converters.

For mission critical applications such as medical equipment, nuclear power plants, full electric vehicles and aircraft control, the reliability of these converters is of the highest importance. In designing these converters, voltage and current stresses on the components are kept at a minimum. However, during their interaction with other converters/loads/sources, it is inevitable that these devices will experience high voltage and current transients. Moreover, external conditions such as power surges and temperature variations that affect these components cannot be ideally controlled. Since the research on perfecting the reliability of semiconductor devices has long way to go, the natural solution to improving the reliability of DC-DC converters was sought in incorporating fault diagnostics (FD) and fault tolerant (FT) strategies. FD is a wider term covering (1) fault detection which is related to the study of identifying the presence of a fault in the first place, and (2) fault identification (FI) which is related to the study of identifying the specific location of the fault for further processing. Fault tolerance, on the other hand, is employed in order to ensure converter reliability and continuity of service. These days, with the introduction of more efficient and complex converter topologies for wide ranging applications, novel FD and FT techniques are introduced. With a broad range of these techniques, an updated compilation of recent methodologies has always been welcomed. Up till now, a number of review articles have been presented [1]–[5] but with a constant increase in the number of articles on FD and FT techniques, a fresh review of the most recent research work is almost always overdue. The existing literature contains several reviews of important and latest technologies on FD and FT schemes. In contrast to the previous work, this paper provides a comprehensive, up to date overview and comparison of available technologies on FD and FT in tabular form with more converter parameter for an in-depth analysis. Moreover, for the first time more detailed classification of FD techniques is carried out and examples specific to these techniques are discussed, tabulated and categorized in a coherent manner. Additionally, systematic guidelines for selection of proper FD technique based on converter topology, and fault type has been prepared. It provides a general guideline on how to make a proper selection of FD technique for different topologies. Moreover, future trends and prominent research directions for FD techniques has been also presented. Additionally, a guidelines for selection of proper FT technique based on converter topology has also been added. Due emphasis on the previously neglected techniques has been made to give the readers a better idea of current trends. This research will provide a useful design guideline for the reliability improvement in all forms of dc-dc converters.

II. FAULTS CLASSIFICATION

In order to help better understand the implementation of FD and FT techniques, a classification of typical faults in DC-DC converters and their causes becomes necessary. DC-DC converter faults are mainly classified as (1) catastrophic fault causing a sudden loss of functionality and (2) parametric failures also known as soft faults, gradually degrading the performance due to device aging. Figure 2 gives the converter fault classification in the converter components. Catastrophic faults for DC-DC converters are mainly observed in semiconductor devices as Short Circuit Faults (SCF) and Open Circuit Faults (OCF). [6], [7] has discussed the specific causes of SCF, OCF and component degradation. A SCF usually results from gate oxide shorting due to electric field stress, gate metal and source metal shortening. During SCF, the switch latches on permanently regardless of the gate control signal, resulting in very high over currents. SCF can be easily detected in a converter circuit because it results in sudden large inrush current. Due to this reason, a fast FD technique is usually required to deal with a SCF. Almost all electronic systems are equipped with the SCF protection either in passive form such as quick blow fuses or active form such as SCF diagnostic

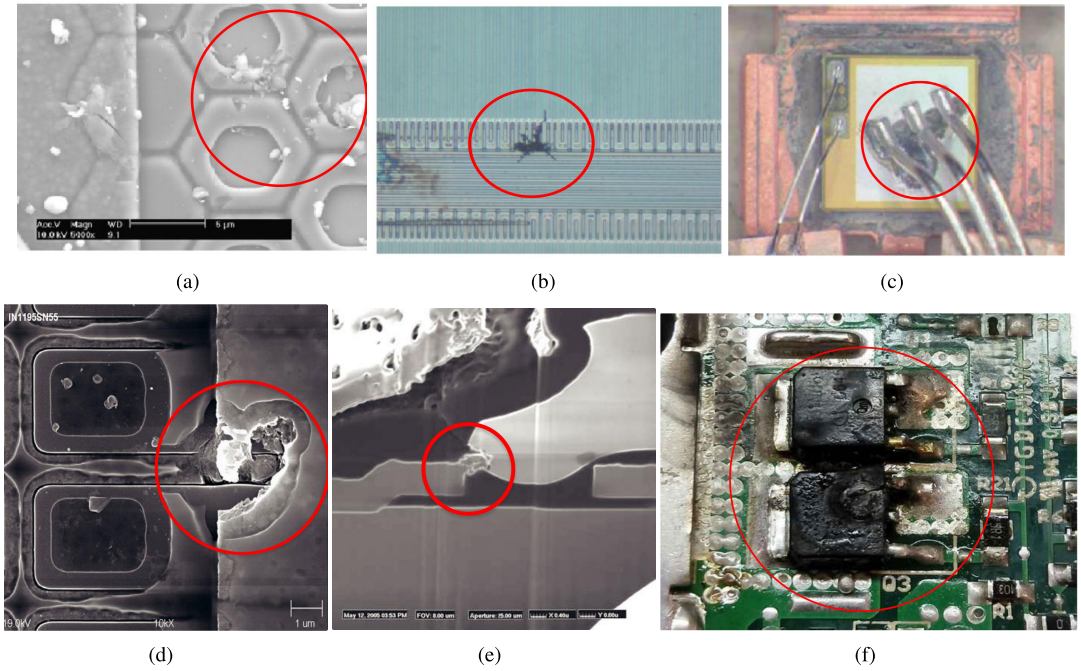

FIGURE 3. Typical component damages: (a) Fail site is gate oxide of edge cell in BUK9508-55A [6] (b) Fail site is gate oxide of edge cell in BUK7Y3R0-40H [6] (c) Burns located in center of die adjacent to wirebonds in BUK7L06-34ARC [6] (d) Source Metal to Gate Poly Short [7] (e) Gate Metal to Drain Poly Short [7] (f) Driver IC and Mosfet Damage.

modules in an effort to prevent the fault penetration to rest of the system. OCF on the other hand result from lifting of bond wire during thermal cycling, driver failure and SCF induced rupture. Despite the fact that OCF do not cause any surge current flow, they still cause power loss in a system. Contrary to SCF, detection of OCF can be difficult and may require more complicated diagnostic schemes. Nevertheless, timely detection of OCF is as critical as SCF since a delay in detection can result in fault penetration to other components of the converter. Figure 3 shows the pictures for several typical component damages. Parametric faults also known as soft failures are commonly caused due to aging of the converter components. These faults are commonly observed in electrolytic capacitors but they can also be experienced in semiconductor switches due to Time Dependent Dielectric Breakdown (TDDB), Negative Bias Temperature Instability (NBTI), and Hot Carrier Injection (HCI). Aging of aluminum electrolytic capacitor is the leading cause for DC-DC converter failure. Two basic reasons that results in the capacitor aging are the vaporization and degradation of liquid electrolyte [8]. These reasons for the degradation come from one of the strengths of aluminum electrolytic capacitor which is its self healing property. During this self healing mechanism, the capacitor restores any damage that occur to the dielectric membrane. High temperature thermal shocks and over voltage stresses are some of the common factors for the dielectric membrane damage which initiate the self healing process resulting in combination of oxygen from electrolyte with the aluminum of foils to form AL_2O_3 thus restoring any defects in the dielectric membrane. As a result of this process, hydrogen gas is released [9]. With aging, the dielectric defects increases the self healing mechanism and with that the oxygen saturation in electrolyte decreases. This ultimately results in the vaporization and degradation of electrolyte in the capacitor. Under normal conditions, the hydrogen gas generated because of the self healing is extremely small and the aging process is rather slow, but with a sudden change in the capacitor operating conditions such as increase in the ambient temperature, current ripple, over voltage stresses or reverse voltages, damage to the dielectric film is considerable. As a result, the self repairing mechanism increases resulting in production of more hydrogen gas and further vaporization of electrolyte. This causes an increase in the internal pressure of the capacitor which ultimately causes the pressure relief vent to open resulting in capacitor dry out and leading to a catastrophic failure in the form of open circuit.

III. REVIEW OF FAULT DIAGNOSTIC TECHNIQUES

FD is the mechanism of detecting and identifying the presence, location, type and severity of the faults, and it is the first step in fault handling. Depending upon the methodology, it can be broadly classified into three main types: hardware based, model based, and historic data based [10]. Each technique has its own advantages and drawbacks. Hardware based FD has proven to be fast and effective but expensive due to the requirement of extra sensors for fault signature measurement. Model based FD has been gaining a lot interest recently because of its sensor-less fault measurement methodology. To improve the robustness and accuracy of diagnosis, these techniques demand accurate mathematical models of the system and significant computational resources which happens

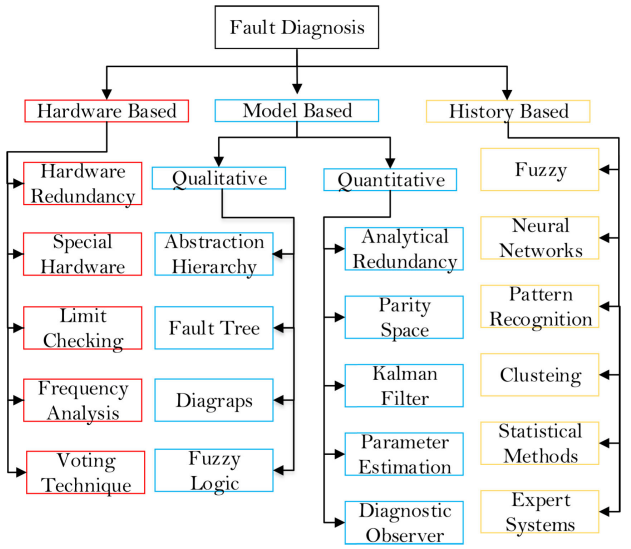

FIGURE 4. Classification of fault diagnosis techniques.

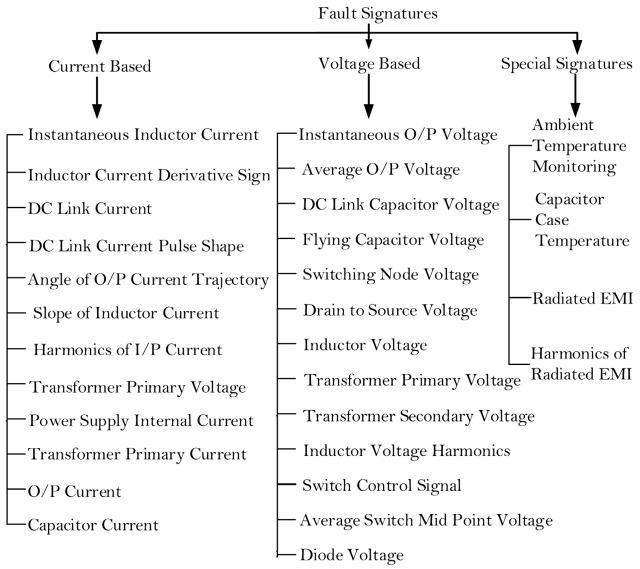

FIGURE 5. Lists of fault signatures.

to be one of the down side of this approach. With the induction of low cost, efficient computational resources and availability of input out process data, history based FD has proven to be a promising approach to model complex non-linear time invariant systems. Although they eliminate the need for development of complex mathematical models by treating the converter as a black box, still they require large training data which happens to be a weakness of this approach. These classifications can be further divided into subgroups depending upon specific implementation technique. Figure 4 gives the classification of these FD techniques. Almost all types of FD techniques lie within these categories.

A. HARDWARE-BASED FAULT DIAGNOSIS

Hardware based FD is one of the most widely used techniques for fault detection and isolation in DC-DC converters. It either uses sensors or the converter input and output information to detect abnormalities. Hardware based technique can be classified into hardware redundancy, special hardware, limit checking, voting and frequency analysis. Although a clear classification of these techniques have been achieved, a number of researchers have used combination of multiple techniques in a single fault diagnostic strategy. One of the reason for combining these techniques is to augment its effectiveness by adding multiple diagnostic schemes in a single FD strategy. Converter signals that are effected due to presence of faults are used to detect and isolate these faults and are called fault signatures. Figure 5 lists some of the popular and effective fault signatures that once measured are used to extract the desired information by further processing them with Pulse Width Modulated (PWM) or Gate Drive Signals (GDS). For better FD and isolation in more complex converters, more information is extracted from these signatures by calculating the mean, slope, root mean square, derivative or their integrals. Normally a threshold is calculated which defines the limit of these fault signatures and once these limits are crossed, a fault alarm is triggered.

1) HARDWARE REDUNDANCY

Hardware redundancy method is the most popular and basic type of hardware based fault detection in DC-DC converters. This method employs various types of hardware sensors to measure specific variables of interest or fault indicating signatures which includes inductor current i_L, switch and diode voltages, slope of the inductor current, DC link capacitor voltage etc. This technique has proven to be simple, fast and effective since these sensors are fast and give a prompt response in case any anomaly is detected in converter functionality. Usually, extra sensors are added to the system in order to measure the required signatures but some techniques have used sensors already installed to measure the control signals in the converter for normal operation. Once these signatures are measured, they are either fed to a simple logic circuit or a digital controller such as an Field Programmable Gate Array (FPGA) or Digital Signal Processor (DSP), which compares these signatures with the already calculated threshold values and flags a fault alarm. Main drawback of this approach is that, with incorporation of extra sensor, overall cost of the system is increased. Another shortcoming of this approach is that addition of sensors introduces extra hardware in the converter which ultimately requires additional space and increases overall weight. Under normal situation this increase in size and weight might be acceptable but for portable electronics devices where the real-estate on a PCB is a hot commodity, extra space requirement for these sensors could prove to be costly and impractical. Inductor current and voltage holds the fist-hand information regarding the functioning of DC-DC converters. An auxiliary winding can be installed on the inductor to obtain the magnetic component voltage v_L which can be used along with the GDS for FD

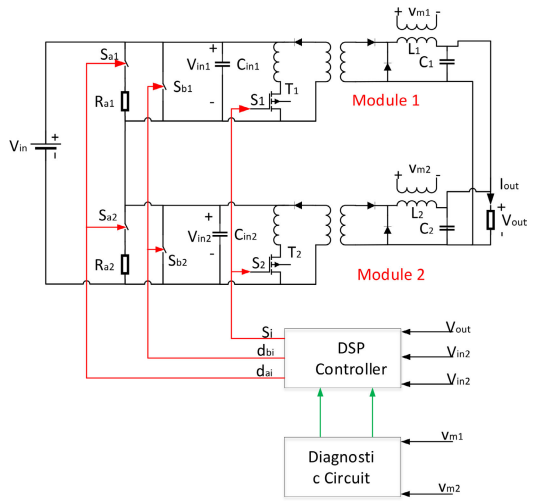

FIGURE 6. ISOP cascaded forward converter.

in Boost converter [11], single and dual switch DC-DC converters [12] and the modular forward converter [13]. By sampling the inductor voltage v_L with respect to GDS, switch OCF and SCF in the Boost converter working in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) can be detected within 2 switching cycles. Using simple logic circuit, FD can be implemented in all kind of single switch (Buck, Boost, Buck-Boost, SEPIC) and dual switch (push pull and half bridge) DC-DC converters. Using magnetic component voltage v_L as a fault detection signature along with GDS, switch OCF and SCF can be identified in input series output parallel cascaded forward converter with two stages and one redundant stage in less than one switching cycle with the help of a simple logic circuit. With additional hardware of two switches and one resistance per module, faulty module is bypassed. Figure 6 shows a 2 level input series output parallel cascaded forward converter discussed in [13]. Applicable for multiple types of converters and with fast detection response, the major drawback of this approach is the use of additional sensor to measure inductor voltage. The effectiveness of hardware based FD technique for more complicated and high performance converters has been demonstrated in [14]. Quadratic Boost Converters (QBC) illustrated in Figure 7 are one of these high performance converters which have the advantages of wide input output range, high gain and low cost. However, these advantages come with the price of added stresses on switches and diodes making them more prone to failure. Using an auxiliary winding installed across the inductor to measure v_L and the GDS, converter switch OCF/SCF and diode OCF/SCF can detected and identified in a very short duration with the help of logic gates. Although the implementation for QBC by using this approach has been reported, it can be extended for all types of quadratic single switch converters operating in CCM and is also robust to any changes in the duty cycle when operating in closed loop control. However, no information about its effectiveness in DCM has been shared. Figure 8 gives the complete flow chart for the fault detection and identification

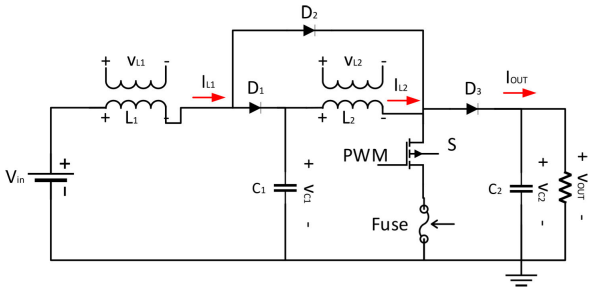

FIGURE 7. Quadratic boost converter.

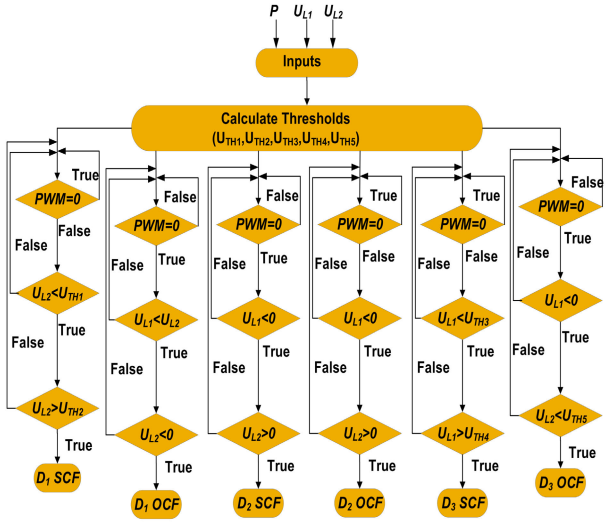

FIGURE 8. Inductor voltage polar signature based diode fault diagnostic technique.

in [14] for the quadratic boost converter. Diode voltage V_D holds important information regarding the switch/diode OCF and SCF faults in Buck, Boost and Buck-Boost converter. In [15], the authors have shown that using V_D along with information from the GDS, switch/diode OCF and SCF faults can be detected and isolated in less than one switching period. With the robustness to input, output and duty cycle variations and fast fault detection, the major drawback of this approach is the use of additional voltage sensor, which increases the price tag for this technique. Due to features of bidirectional power transfer, soft switching, galvanic isolation and high power density, Dual Active Bridge (DAB) converters have gained a lot of interest in recent years for its use in applications like electric vehicles, battery storage systems and solid state transformers. Owing to this fact, [16] has used polarity of DC component of transformer phase and magnetization current to identify switch OCF in Dual Active Bridge Isolated Bi-directional DC-DC Converter (DAB-IBDC). In a three pronged approach, the faulty bridge is identified by comparing the polarity of DC component of phase current to the polarity of DC component of the magnetization current of same phase. In the next step a faulty phase is identified if the polarity of the phase current DC component of two phases is opposite. After identifying the faulty bridge and phase,

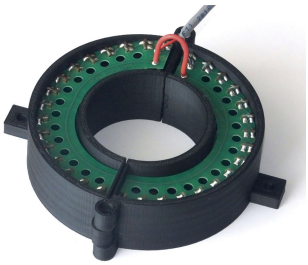

FIGURE 9. Mountable Rogowski coil sensor.

fault localization at component level is achieved by observing the polarity of phase current DC component. By adding extra current sensor per phase, the authors have shown the effectiveness of their technique via simulation by identifying and isolating switch OCF in all bridges but did not share hardware results to augment the proficiency of there proposed technique.

2) SPECIAL HARDWARE METHOD

This type of method is used for dynamic detection of various faults in DC-DC converters. Special hardware based method is different form the hardware redundancy on the basis of sensors used. These are special sensors to measure temperature, pressure, sound and vibrations etc. The outputs of these sensors are converted to electrical signals and then are compared to known thresholds. In an extension to [15], the authors were able to calculate switch and capacitor aging and inductor inter-turn fault by adding special hardware in the from of temperature sensors in [17]. Using 2 additional temperature sensor for ambient temperature monitoring T_A and capacitor case temperature monitoring T_B, a thermal model for capacitors is developed, which is used to predict the variation of capacitor Equivalent Series Resistance (ESR) with temperature. This model is then used to calculate the ESR values of new capacitors for temperatures where no data is available in the data sheet. A Rogowksi Coil Sensor (RCS) Figure 9 can be installed on an inductor of already built converter with low implementation cost and is used to measure inductor voltage v_L. RCS has a linear response for a wide range of frequencies making it a suitable sensor for high frequency switching converters. In conjunction with the information of GDS represented as s(t), inductor voltage v_{RCS} and diode voltage v_D can be used for FD and identification of the switch and diode in Buck converter using simple logic circuit. With the ability to detect the switch OCF/SCF, diode OCF/SCF and inductor inter-turn fault in less than one switching period, this method can also detect capacitor and switch aging with the help of 4 extra sensors which happens to be the low point of this research. Figure 10 gives the complete flow chart for the fault detection and in [17].

3) LIMIT CHECKING METHOD

This technique uses measurements from FD signatures and compares it with a predefined limits already established.

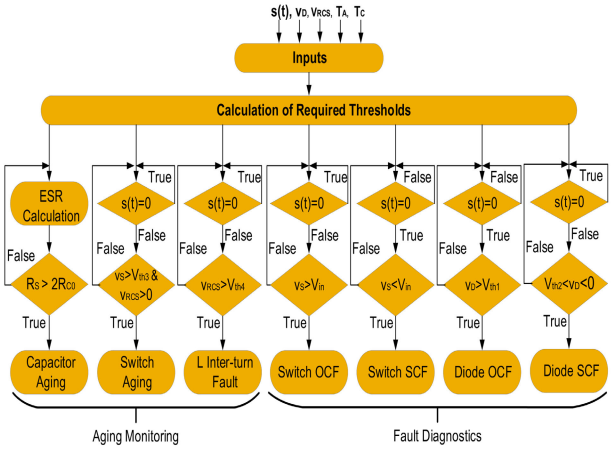

FIGURE 10. RCS based technique flow chart.

These limits specify a range for the normal operation of DC-DC converters. Once the values of fault indicating signatures cross these specified limits, a fault alarm is triggered. Obviously, the first step in developing the limit checking method would be to establish thresholds and then comparing them with the measured value. DC-DC converters normally use sensors for control signal measurements such as i_L. The behavior of i_L as a fault indicating signature happens to be same for all non-isolated single ended DC-DC converters. Switch OCF and SCF can be detected for all non-isolated single ended DC-DC converters using signed inductor current derivative for CCM [18], [19]. Two subsystems, using two different algorithms work in parallel to detect SCF and OCF faults by monitoring shape of the inductor current with respect to switching cycles. The primary algorithm is fast but less robust especially in detecting OCF for small duty cycle values and SCF for large duty cycle or high switching frequency. A secondary algorithm which is slow but more robust to these conditions is also used to detect the OCF and SCF. The fastest response from the two algorithms is propagated to the output for fault signaling. In case of cascaded non-isolated converters, parallel and unified FD algorithms are employed for each cascaded stage. Using shape of inductor current form all the stages along with their GDS, the unified approach is able to detect the switch OCF and SCF. However, due to inherent redundancy features of cascaded converters, fault localization has not been achieved in this work. The use of average inductor current instead of signed inductor current derivative as a fault measurement signature presents the benefits of improved and reliable FD in class E^2 resonant converters [20]. Hybrid Dickson Switched Capacitor (SC) converter offers the best switch utilization and are very popular among the automotive application where the presence of 48V high voltage rail necessitates the requirement of high density power converters for low voltage applications. Switch node voltage holds important information regarding the functionality of this converter. Sampled during different state intervals, the switch node voltage (V_{SW}) is used to detect the OCF and SCF occurrence in semiconductor switch and flying

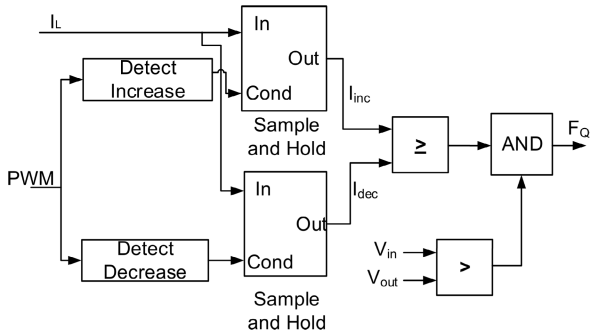

FIGURE 11. Fault diagnostics in unidirectional DC-DC converter.

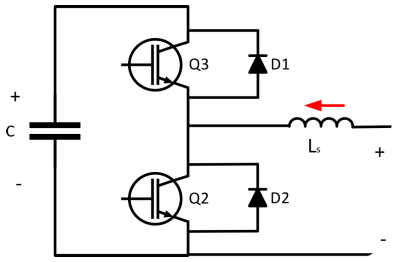

FIGURE 12. Fault diagnostics in bidirectional half-bridge converter.

capacitor [21], [22]. By comparing the sampled V_{SW} to a predefined threshold, FD for semiconductor switches is achieved using two different algorithms which is robust to all kinds of input and output transients. A FT approach is also employed which enables continuous power delivery to the load regardless of fault in any phase, while providing balanced current sharing and acceptable voltage regulation. Penalty in terms of cost increase and efficiency degradation due to inclusion of FT capability in this converter has also been calculated and is further used as a guideline for designing a FT power stage. In comparison with CCM, DCM ensures reduction of switching loss and inductor size. However, the effectiveness of most FD schemes has been studied under CCM due to ease of implementation. Without using extra sensor, the authors have used I_L, output voltage V_{OUT} and input voltage V_{IN} to detect switch OCF regardless of the operating mode for all types of unidirectional non isolated DC-DC converters [23] and bidirectional half-bridge DC-DC converters [24]. A block diagram of the FD method in [23] for Buck converter is given in Figure 11. Upon sampling i_L during GDS rising edge I_{inc} and falling edge I_{dec} and comparing the condition Vin > Vout for a Buck converter, OCF in the switch has been diagnosed. On the down side, the authors were unable to show the effectiveness of this technique for switch SCF and diode OCF/SCF. Figure 12 gives a diagram for the Bidirectional half-bridge converter mentioned in [24]. A delayed version of GDS can be used with the I_L slope to detect OCF and SCF in single ended DC-DC converters [25] and can also be applied on a system with several parallel DC-DC converters connected to a common dc bus [26]. Using the proposed FD algorithm, value of the counter is observed. Once the counter reaches the maximum threshold a fault alarm is triggered and a reconfiguration process is initiated depending upon the

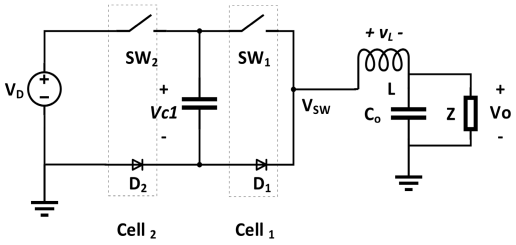

FIGURE 13. Flying capacitor Buck converter.

type of fault to ensure service continuity. By comparing the average values of midpoint i.e. Avg(V_A), Avg(V_B), Avg(V_C), Avg(V_D) with standard average value $V_1/2$ and $V_2/2$ in a DAB converter, switch OCF in every bridge can be detected and identified [27]. A threshold voltage V_{th} is calculated using experiments to adjust the sensitivity of detection and to avoid any false operation and malfunction. Calculation of average mean value of voltage on midpoints of converter legs is a slow procedure which results in slow switch OCF detection in this approach. One approach that uses duty cycle values along with PV array voltage and current to detect the switch OCF and SCF in the Boost converter is presented in [28]. In case of switch OCF, the PV array voltage increases and consequently value of the duty cycle increases to maximum value i.e. 1 from which the faulty condition has been identified in 5.7msec. In case of switch SCF, the PV array current decreases and correspondingly the duty cycle reduces to cater for this increase in PV current. The duty cycle value ultimately reduces to 0, which is used to detect the switch SCF in 4ms. Large detection delay is one of the short-coming of this approach when intended to be used with a FT scheme.

4) FREQUENCY ANALYSIS

Frequency analysis of the status variables of any converter can be effectively used for fault detection. These status variables have a specific frequency response under normal conditions and a fault will force this response to change. In order to pinpoint the exact fault location and type, frequency spectrum can be studied and associated to certain types of faults. N-level Flying Capacitor Buck Converter (FCBC) has smaller current ripple, lower voltage stress and low harmonic distortion. Figure 13 shows a 3 level FCBC consisting of two switches, diodes and corresponding switch voltage V_{SW}. Employing separate sensor for switches and diodes in each level will incur extra cost and produce a slack in the calculation of control variables thus resulting in slow diagnostics. Frequency spectrum based fault analysis which nullifies the need to install extra sensors for each level proves to be ideal for FD and identification in these types of converters [29]. v_L from the auxiliary winding installed on the inductor is analyzed using Discrete Fourier Transform (DFT) and every failure condition is correlated to a specific frequency spectrum allowing to pinpoint the fault. This technique effectively detected switch OCF and SCF within 2 switching cycles using extra auxiliary winding which is a downside regarding

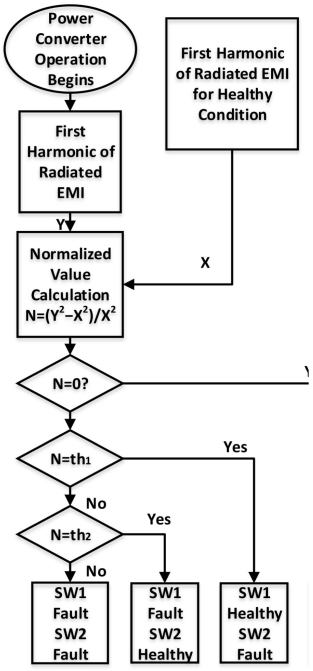

FIGURE 14. Flow chart for the radiated EMI based fault diagnostic technique.

cost adequacy. Power converters operating at frequencies of 200KHz or less can create conducted and radiated Electromagnetic Interference (EMI) within tolerable range. Frequency spectrum of the radiated EMI can be used to detect fault in a power converter [30]. In SR Boost converter, due to a periodic current flow between the two switches, its frequency spectrum consists of a component at DC value, at switching frequency and its harmonics. Converter switch is considered healthy if its radiated EMI pattern is consistent with the PWM pattern and is considered faulty if these patterns do not match. This research shows that normalized EMI values tend to increase with the presence of a faulty condition. For example, in a complete healthy converter, the normalized value of the first harmonic of the radiated EMI is equal to 0 and as the number of faulty switches increase so does the normalized value. This criterion is used to set threshold value of th_1 and th_2 for classifying and localizing switch faults. However, requirement of spectrum analyzer and DSP controller make this procedure an expensive choice for FD. A flow chart, representing this FD technique is given in Figure 14. Another approach which uses switching frequency based harmonic components for FD and localization in interleaved DC-DC power converters is presented in [31]. This approach enables post-fault restoration to ensure equal current sharing among the remaining healthy modules. Diagnosis of switch OCF in the interleaved boost converter is carried out through the analysis of magnitude and phase angle of switching frequency based harmonic components of the input current I_{fs}. During normal operation, the input current has a DC component and harmonics at three times the switching frequency. During switch OCF in any phase, i_L of the other 2 phases change

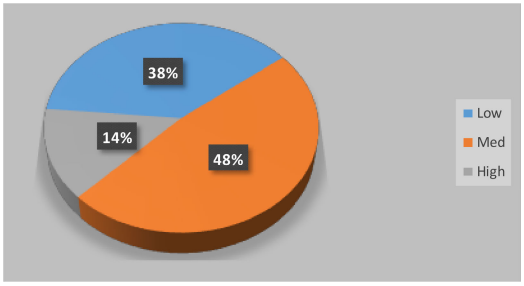

FIGURE 15. Percentage of hardware based techniques based FD techniques based on cost range.

and I_{fs} increases from the predefined threshold identifying the faulty phase. Phase shift of the remaining healthy phases is altered by maintaining the carrier of healthy phases at 180° resulting in equal distribution of phase current and minimum ripple in capacitors and output voltage. Table 1 gives a detailed comparison of hardware based FD techniques. Critical information is compiled in this table for quick reference. The second column in the table not only specifies the topology for which the experimental or simulation studies are carried out in that specific research but also includes the additional topologies for which the technique is applicable as claimed by the author. Third column specifies the type of component for which the FD technique is implemented. Here SW represents the switch device which can be a Mosfet, IGBT, Transistor or a Thyristor. D represents a diode, L denotes an inductor and Cap a capacitor. This table also present extra information regarding the applicability of FD technique in CCM and DCM mode. Moreover, this table not only identifies the fault indicator signature used to measure converter faults, but also states the number and type of extra sensors used for fault detection. It is necessary to point out that in this table, sensors already installed in the converter circuit for measuring control signals are not included although they may be used for capturing information about the fault signature. Since these sensors do not impose any financial burden when used in FD technique, therefore they are not included in the list of extra sensors. Data compiled form the table shows that for hardware based FD techniques, the cost range varies from low to high depending upon the number of sensors used. Figure 15 is a pie diagram which shows the percentage of hardware based FD techniques that lies in the high,medium and low cost FD techniques. According to this review, 47% of research studies used the already installed sensor for control signal measurement to measuring these fault signatures and 53% research installed extra sensors for fault signature measurement thus increasing the price tag for that technique. Inductor voltage and inductor current along with the GDS has been the major focus of researchers for fault detection and its type. Hardware based fault detection is considered a fast detection techniques and this review shows that almost 57% of total research studied carries out FD in less than 2 switching cycles and detection speed of rest of the FD techniques lies in μsec range with some exception of ms range. Major fault types covered by this techniques are

TABLE 1. Comparison table for hardware based fault diagnostic techniques.

Ref.	Topology	Fault Comp.	Fault Type	Isolation Type	FD Time	FI Sig.	Sensor Info.	Control	Fs	CCM/DCM	Cost
[11]	Boost Converter	SW	OCF/SCF	Non-Iso	$< 2T_S$	V_L, GDS	1, Voltage Sen.	DSP	25KHz	CCM DCM	Med
[12]	Single Switch Con. Dual Switch Con.	SW	OCF/SCF	Iso/Non-Iso	$< T_S$	Magnetic Component Voltage GDS	1, Aux. Win	Logic Gates	48KHz	CCM	Med
[13]	ISOP Cascaded Forward Con.	SW	OCF/SCF	Iso	$< T_S$	Magnetic Component Voltage GDS	1, Aux. Win	Logic Gates	50KHz	CCM	Med
[14]	Quadratic Boost Converter	SW, D	OCF/SCF	Non-Iso	SW OCF/SCF$<T_S$ D OCF/SCF$<2T_S$	V_L, GDS	1, Aux. Win	Logic Gates	50KHz	CCM	Med
[15]	Buck,Boost, Buck-Boost	SW, D	OCF/SCF	Non-Iso	$< T_S$	V_D, GDS.	1, Elec. sensor	Logic Gates	50KHz	N/A	Med
[16]	3φ DAB-IBDC	SW	OCF	Iso	NA	Sign of I_P, I_M	3, Current Sen.	Sim	NA	NA	High
[17]	Buck,Boost, Buck-Boost	SW, D Cap, L	OCF/SCF, SW & Cap. Aging, L Fault	Non-Iso	SW OCF/SCF$<T_S$ D OCF/SCF$<T_S$ L Fault$<T_S$	V_D, V_L,GDS Amb. Temp. Cap. Case Temp.	Elect. Sensor 2 Temp. Sensor 2	Logic Gates	50KHz	CCM	High
[18]	Single Ended DC-DC Con.	SW	OCF/SCF	Non-Iso	$<2T_S$ or 20µs	I_L, GDS	0	FPGA	15KHz	CCM	Low
[19]	Cascaded Single Ended DC-DC Con.	SW	OCF/SCF	Non-Iso	OCF$<2T_S$ SCF$<$200µs + $2T_S$	I_{L1}, I_{L2} GDS	0	SIM.	20KHz	CCM	Low
[20]	E^2 Resonant Con.	SW	OCF/SCF	Iso	$< 4T_S$	Avg I_L, GDS	0	NA	100KHz	NA	Low
[21]	4-1 Hybrid SW Cap. Dickson Con.	SW, Cap	OCF/SCF	Non-Iso	SW SCF 1.8µs OCF 69.4µs Cap SCF 5.8µs OCF 20.4µs	Switching Node Voltage	1, Voltage Sen.	FPGA	250KHz	NA	Med
[22]	4-1 Hybrid SW Cap. Dickson Con.	SW, Cap	OCF/SCF	Non-Iso	SW SCF 1.8µs SW OCF 69.4µs	Switching Node Voltage	1, Voltage Sen.	FPGA	250KHz	NA	Med
[23]	Single Ended DC-DC Con.	SW	OCF	Non-Iso	CCM SW OCF 0.5ms DCM SW OCF 0.4ms	I_L, V_{IN} V_{OUT}	0	NA	NA	CCM DCM	Low
[24]	Bidirectional Half Bridge DC-DC Con.	SW	OCF	Non-Iso	$<$ 2ms	I_L, V_{IN} V_{OUT}	0	Sim	NA	CCM DCM	Low
[25]	Boost Con.	SW	OCF/SCF	Non-Iso	$< T_S$	I_L, GDS	0	FPGA	15KHz	CCM	Low
[26]	Boost Con.	SW	OCF/SCF	Non-Iso	$< T_S$	I_L, GDS	0	FPGA	15KHz	CCM	Low
[27]	DAB with EPS	SW,D	OCF	Iso	3µs-10µs	Avg V_{MID}	0	DSP	20KHz	NA	Low
[28]	Boost	SW	OCF/SCF	Non-Iso	OCF=5.7ms SCF=4ms	V_{PV}, I_{PV}, GDS	0	Sim	62.5KHz	CCM	Low
[29]	3 level FCBC	SW	OCF/SCF	Non-Iso	$< 2T_S$	V_{HOR}	1, Aux. Win	FPGA	100KHz	CCM DCM	Med
[30]	SR Boost Con.	SW	OCF/SCF	Non-Iso	NA	Ist Hormonic of Fs	1, Monopole Antenna	DSP	19.8KHz	CCM DCM	High
[31]	Inter leaved Boost Con.	SW	OCF	Non-Iso	$< T_S$	Hormanic Component of I/P Current	0	DSP	10KHz	NA	Low

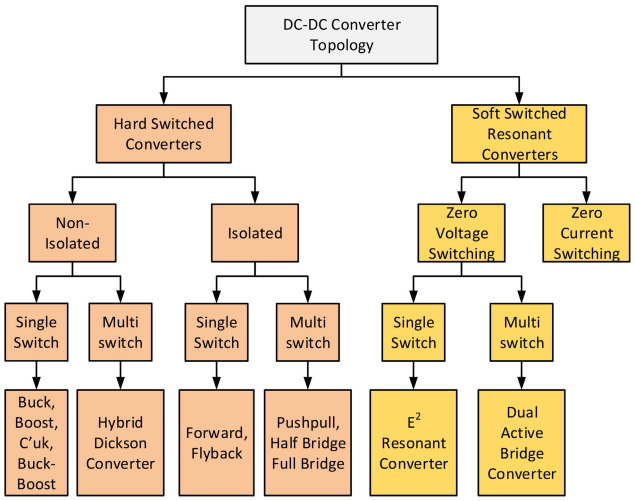

FIGURE 16. Converter classification.

catastrophic faults mainly SCF and OCF for switches and diodes and they prove to be equally effective for isolated and non-isolated converter types.

B. GUIDELINES FOR SELECTION OF HARDWARE BASED FD TECHNIQUES FOR DC-DC CONVERTERS

Several isolated and non-isolated topologies have been introduced along with more efficient control schemes. Figure 16 displays various types of switching converter topologies that are discussed in this literature. In terms of usage, there is no ultimate converter that is suited perfectly to all possible applications. Similarly, selection of proper FD strategy for specific converter can be difficult and this section aims to address this issue. In this literature, a large number of hardware based FD have been presented, where each of these methods have its own strengths and shortcomings. In order to help identify a proper FD scheme for the desired converter, a guideline for selection of proper FD technique based on the converter and fault type has been prepared. This section provides a general guideline on how to make a proper selection of hardware based FD technique in DC-DC converters as presented in Figure 17. As seen in the Figure 17, the first step in selection of hardware based FD technique is the identification of the converter topology since this technique is specific to both fault type and converter structure. Although broadly classified into three major types, i.e. linear, hard switched and soft switched, FD methods for hard switched and soft switched converters are discussed in this review. Hard switched converter can be further classified into non-isolated and isolated converters. This classification helps identify appropriate groups of fault diagnostic signatures that can be used for fault identification. However, acquisition of large number of signatures for FD can result in installation of extra sensors and processing all this information could impose heavy burden on the processor. Moreover, redundant information from various sensors will not add any useful information on FD. Due to this reason further classification into single switch and multi switch converter has been made in order to narrow down the selection of proper fault indicating signatures. After that, the final FD technique selection is based on the type of fault or group of faults that occurs within a DC-DC converter. These faults are classified into 3 major types based on the likelihood of their occurrence i.e. (1) open circuit faults (OCF), (2) open and short circuit faults (OCF/SCF) and (3) parametric faults. A short description of each FD scheme is presented here with different color coding for each type of converter topology. This description states the article number, faulty component, fault signature used, number of sensors used, and FD time in this order. Once classified, proper FD technique presented in Table 1 can be selected with detailed information available for further implementation.

C. MODEL BASED FAULT DIAGNOSTICS

The classical approach of hardware based FD techniques make use of multiple sensors and actuators to measure fault detecting signatures which are compared to fixed thresholds. However, for small and portable electronic devices, added cost and weight due to these sensors prove to be a hindrance in their application to these modules. Therefore, inclination to analytical redundancy was natural in which a mathematical relationship between the measured or estimated variables is utilized for anomaly detection. A mathematical model is developed based on the deep understanding of physical properties of the process. Figure 18 shows the control structure of the model based FD system. Model based FD is achieved in two stages. Initially, it compares the real output to predicted output of the model to produce a signal called the residual. Residuals should remain small as long as there is no fault, and become sufficiently large to be noticeable whenever faults occur. These residuals can be scalar quantities carrying information about a single fault or a vector quantity detailing multiple faults in a process and they depend upon the type of modeling procedure adopted. Once acquired, these residuals are fed to the decision making units which are responsible for FD and its isolation. This unit can simply use thresholds or a number of sophisticated statistical approach. Model based FD have gained a lot of attention because of its independence from extra sensors and is used in wide ranging applications covering electronics, nuclear, aeronautics, and chemicals etc. Extensive research is underway to develop more accurate models of high performance converters with complex control and modulation schemes which gives a precise representation of a real converter [32]–[37]. Accurate mathematical modeling is the key to proper fault diagnostics in these converter systems. Poor mathematical modeling may lead to false alarm due to inconsistency in the signal generated by the mathematical model and the actual system, under the normal operation. On the other hand, increasing accuracy and complexity of a model introduces burden on computational resources of the system. A generalized model based FD system is presented in Figure 18.

Model based FD can be broadly classified into qualitative or quantitative methods. Qualitative method utilizes a model

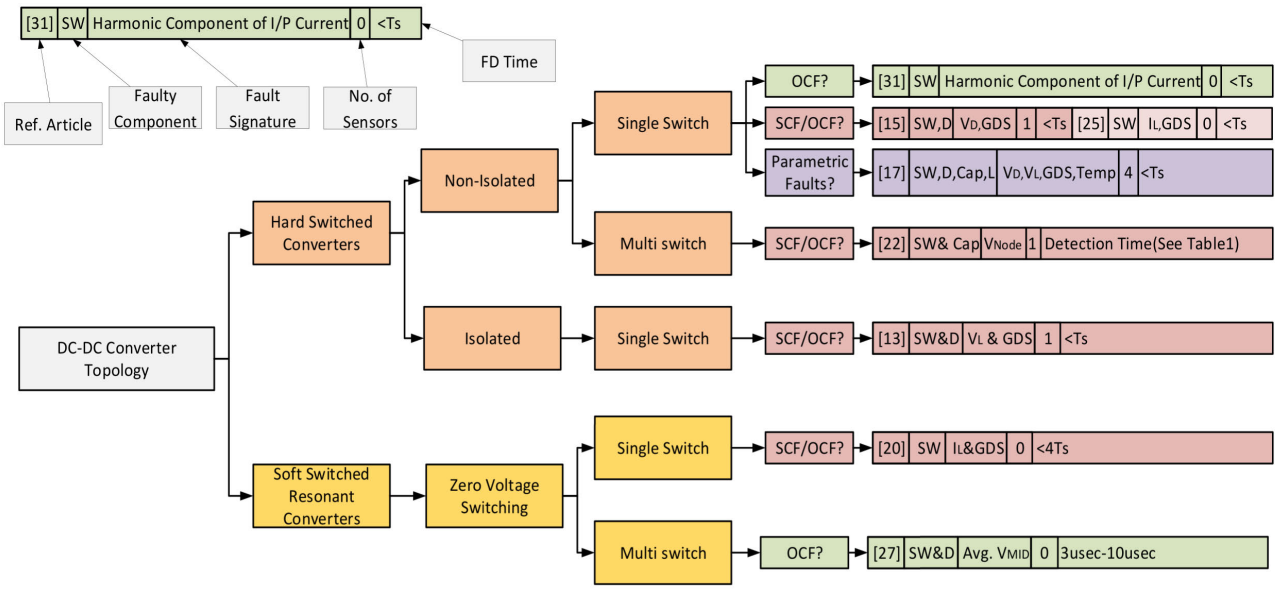

FIGURE 17. Converter fault FD selection.

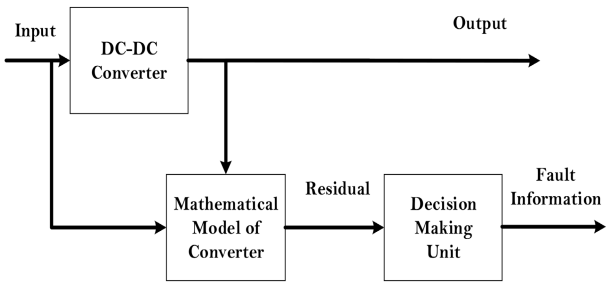

FIGURE 18. Model based fault detection technique.

in which the input output relationship of the converter is expressed in terms of qualitative functions based on different parts of the converter whereas quantitative model-based fault diagnosis methods utilize a model where the input–output relationship of the system is expressed in terms of mathematical functions. Quantitative model based FD technique can be further subdivided into analytical redundancy, parity space, Kalman Filters(KF), parameter estimation and diagnostic observers. Analytical redundancy make use of a mathematical model of the converter. Measurement signals are obtained from the actual system and are compared with the estimated signals generated from the mathematical model. Difference between the signal produced by the model and dynamic signals obtained from the actual converters, termed as the residual, is fed to a diagnostic unit which can be a logic circuit or a controller such as FPGA or DSP board which asses this residual. Based on this assessment, alarm signal is triggered to indicate a fault in the interleaved boost converter [38] and single switch DC-DC converter [39]. In this exploration, the authors developed a mathematical model for predicting the inductor current i_L on every sampling cycle $i_{L(n)}$. $i_{L(n)}$ is based on the measurement of i_L from the last switching cycle $i_{L(n-1)}$. The sampling frequency is 5 times the switching frequency. When the SR boost converter is under faulty condition, the inductor current i_L measured at that time is different from the inductor current when the converter is operating in normal state which is provided by the inductor current emulator. A fault detection alarm is triggered whenever the difference between predicted and measured inductor current becomes greater than a predefined threshold. Figure 19 gives a flowchart of this scheme stating out different error checking steps. In the FD literature, different types of diagnostic observers such as Eigenstructure assignment observer, unknown input observer and fault detection filters are used for residual generation. The basic principle of observer based FD is that by combining a measured feedback signal with knowledge of the converter components, the behavior of converter can be known with greater precision than by using the feedback signal alone. A sliding mode observer can be built for an Modular Multilevel Converter (MMC) representing its mathematical model and can be used to estimate its internal states. Driven by converter arm currents and the cell capacitor voltages which act as inputs and are already available as control system measurement signals, the sliding mode observer can be used for OCF detection [40], [41]. The authors were able to demonstrate the effectiveness of this scheme when they detected and located an OCF in a power semiconductor device under parameter uncertainties, measurement error, and other bounded disturbances. The Luenberger observer perhaps belongs to the one of the most practical observer form. It combines the sensor output, power converter output, an estimated model of the converter, model of the sensor and a proportional integral (PI) or proportional integral and derivative (PID) compensator. Figure 20 shows the implementation of Luenberger observer for residual generation. They have commonly been used to detect and isolate OCF

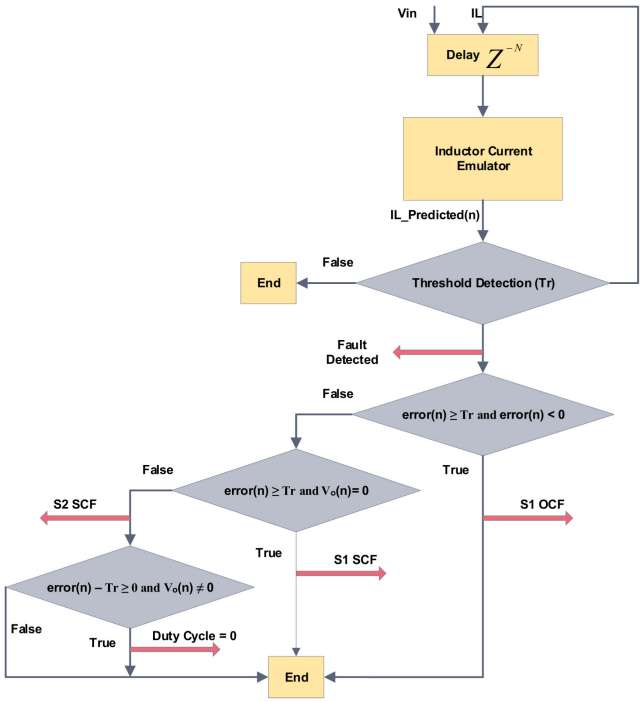

FIGURE 19. Inductor current emulator fault diagnostic technique flowchart.

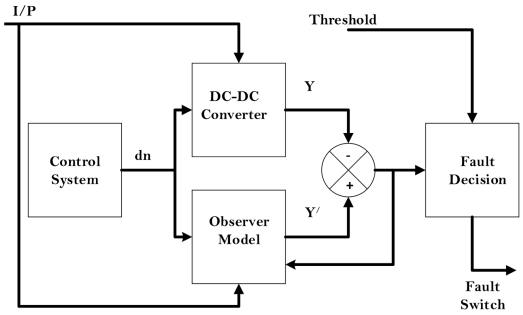

FIGURE 20. Proposed fault diagnostic technique based on [42].

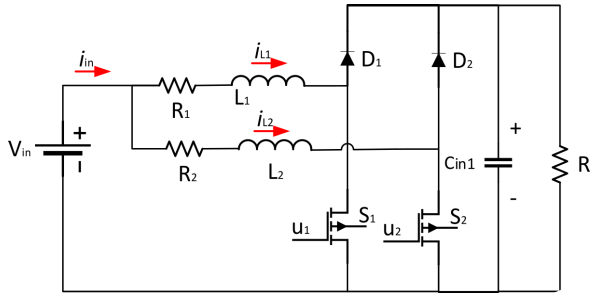

FIGURE 21. 2ϕ interleaved boost converter.

types in converter circuits [42], [43]. Interleaved Boost Converter (IBC) depicted in Figure 21, was chosen to prove the effectiveness of this technique. With state space equations, converter model was prepared and residual was calculated using difference between the estimated an measured output and was multiplied with a gain matrix. By adopting a linear observer, and using values of the residual and gain matrix, state of the converter system was estimated. Residual of the

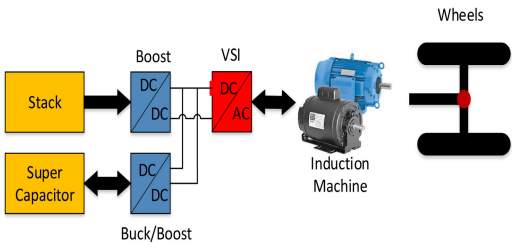

FIGURE 22. Hybrid energy management system proposed in [44].

faulty phase diverged from its original value once there was a switch OCF in a phase. Whereas residual from healthy phase remained same. These residuals were then compared with the already calculated threshold to flag an OCF signal in the corresponding phase [42]. Alternatively 3ϕ inductor current in Voltage Source Inverter (VSI) was used to develop a current observer from which, an average residual current for one complete switching period was calculated. This ensured the robustness and reliability by dealing with all types of modeling inaccuracies and noises. The authors have proven the capability of this approach by using the simulation and experimental results in which the switch OCF was detected and localized without false alarms [43]. In a hybrid energy management system for electric vehicles traction drive as shown in Figure 22, DC bus voltage is controlled and stabilized using by 2 DC-DC converters, a boost and buck-boost converter. By creating and combining the state space equation of these two converters, a global system model was proposed [44]. Using i_L, V_{BUS} and V_{CAP}, transition between different modes has been achieved and was used for comparison with the threshold value. Fault detection and isolation was achieved using banks of state observers. Due to its anti-interference and filtering characteristics, Extended State Observer (ESO) has been used to track the circulating current in MMC [45]. This resulted in production of observed full arm voltage of MMC as shown in Figure 23, which along with theoretical full arm voltage was fed to a Tracking Differential algorithm to filter higher order harmonics. Filtered values of observed v_{XOT} and theoretical v_{XDT} full arm voltage as well as their differentials v_{XOD} and v_{XDD} respectively were used to calculate difference differential between the theoretical and observed full arm voltage i.e. ($v_{XOD} - v_{XDD}$). When ($v_{XDD} - v_{XOD}$) was higher than the positive threshold value in a time range of T_{th}, Q_1 fault was identified. If the difference differential happened to be smaller than the negative threshold value in a time range of T_{th}, Q_2 fault was identified. Using simulation and experimental results, the authors were able to identify and localize the switch OCF however information regarding the SCF of switches or other components has not been provided. The basic idea of parity space approach is to provide a proper check of the parity (consistency) of the input output measurements of the system under consideration. In theory, under steady-state operating conditions, the residual generated by the parity space method is zero. However, these residuals are non-zero due to input output measurement and process noise,

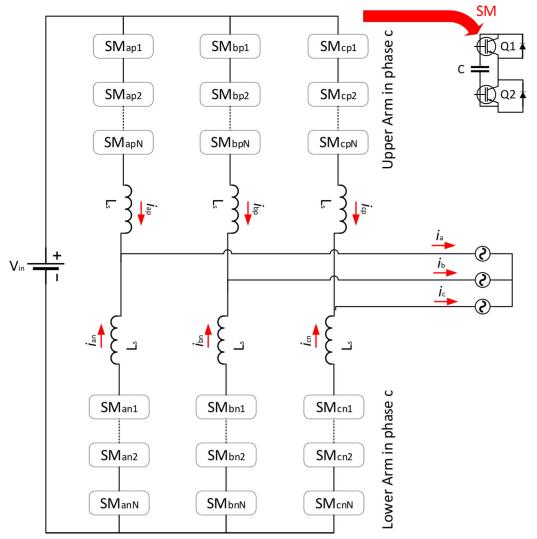

FIGURE 23. 3ϕ MMC with SM [45].

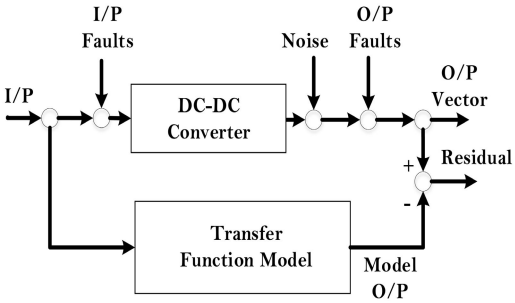

FIGURE 24. Residual generation with parity equation.

modeling errors and faults in the system. Based on the generated residual obtained using parity equations, fault detection procedure is developed which generates the fault flag and is able to isolate these faults in Buck and Boost converter [46]. Figure 24 illustrates the control diagram and architecture of the proposed residual generation with parity equation. In first instance, the residual is processed to detect if the system behavior lies within the specified threshold. To avoid false alarm, a debounce filter is incorporated in the scheme to limit variations in high frequency and avoid false alarm trigger. Parametric fault detection for capacitor and inductor have been reported but information regarding catastrophic faults in switch and diode has not been provided. Fault prognosis is the process of detecting anomalies and early signs of failure and helps predict the Remaining Useful Life (RUL) Figure 25. The main challenge in fault prognosis is the calculation of slow dynamics to measure the slow deterioration process. KF and its variants such as Adoptive Joint Extended Kalmen Filters (AJEKF) and Adoptive Dual Kalmen Filters (ADKF) are used to estimate the state of a dynamic system parameters with noisy measurements. One research that use the AJEKF and ADKF to estimate the degradation process in an bidirectional Boost converter is presented in [47]. Using a dynamic state space model, capacitor degradation is represented as dynamic process with time varying parameters.

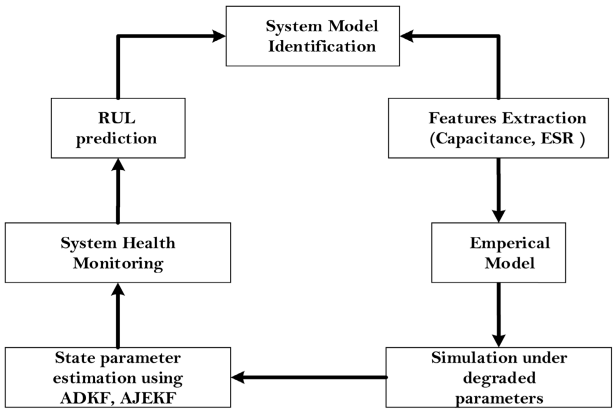

FIGURE 25. Model-based prognostics architecture.

In the next step, slow dynamics of the model are calculated. Using AJEKF and ADKF, estimation of the degraded parameters by handling the slow deterioration process is carried out. An end of life threshold is set as a failure point of the degraded parameters and this threshold is used to measure the RUL by computing the difference between point of measurement and the failure point. The authors however failed to present any information regarding the catastrophic faults in switch and diode. Joint Extended Kalman Filters (JEKF) shows high tracking and estimation accuracy of the empirical results and degradation of ON resistance in the Mosfet switches [48]. Mosfet degradation drops the output voltage of converter and KF are used to estimate this parameter variation. Change in system parameter may cause fault in the converter and parameter estimation proves to be an effective qualitative model based FD technique. In [49], the authors used small signal average modeling with neglected perturbation to develop a Linear Parameter Varying (LPV) model of the DC-DC Buck converter. An interval predictor is applied to the converter model which generates an interval residual that is used to for fault detection. Since noise can also produce inconsistency in the residual generation resulting in false alarm, a threshold level τ was computed to nullify the effects of noise. Once the residual becomes greater than the calculated τ, a fault signal is generated and corresponding fault isolation is achieved.

D. GUIDELINES FOR SELECTION OF MODEL BASED FD TECHNIQUES FOR DC-DC CONVERTERS

Model based FD techniques are based on the principle of analytical redundancy as compared to hardware or physical redundancy which make use of signal from sensors for FD. Model based FD system uses signals generated by the mathematical model of the converter under test. These measurements are compared with the actual measurement obtained from the converter. A residual which basically is difference between the actual signal and signal generated by the mathematical model is used for FD and identification. Residual generation is the most important step in model based FD and it can be achieved using various approaches. In order to choose a proper model based FD approach, this section gives

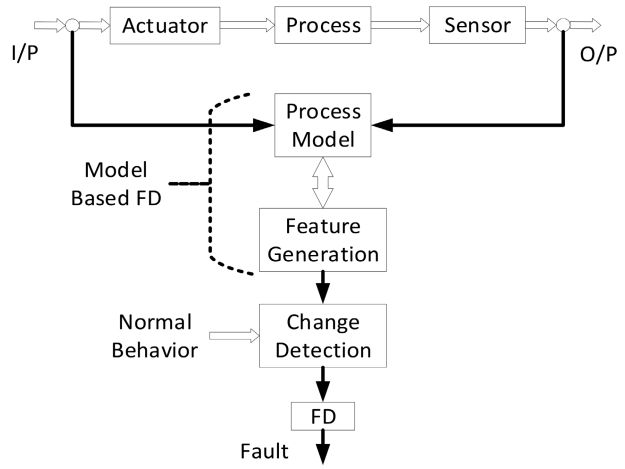

FIGURE 26. Model based FD system.

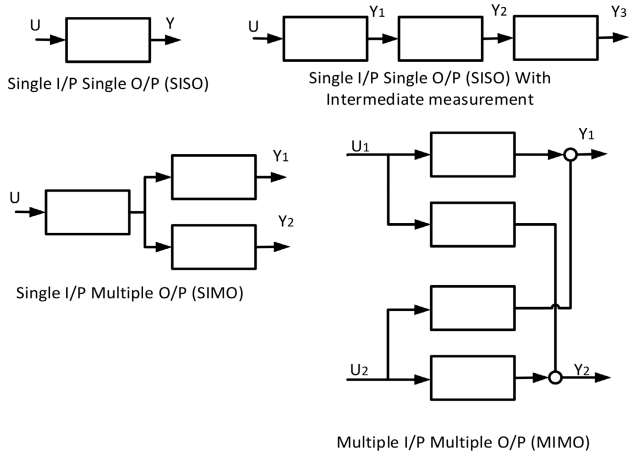

FIGURE 27. Process configuration model based.

a guideline for this selection depending upon the conditions and data available. Figure 26 gives a general scheme for model based FD and diagnosis. The first step in development of model based FD is production of an accurate process model [50]. These process models express the dependencies between different measurable signals. Based on input and output signals, the detection method generates parameter estimates, state estimates and residuals, which are called features. Changes in these features are detected by comparing with normal features. Another important step in process model development is the definition of process configuration. Figure 27 distinguishes various process configuration for model based FD techniques. In order to select the proper model for FD, further classification of system is carried out to depending upon the quantity of information required. The development can be static or dynamic. More information about the system can be obtained with dynamic process model which allows the detection of more and/or smaller faults instead of static models. After that, the fault detection method selection is carried out which is based on different types of faults that likely occur in the DC-DC converters. The fault is classified into three different groups: (1) intermittent faults, (2) abrupt faults and (3) incipient and slow drift faults. Intermittent fault is a state between a healthy and a faulty condition which may arise due to converter malfunctions such as faults in the PWM input signal due wiring faults or EMI etc. Abrupt faults are sudden faults that immediately changes the process features resulting in a fault alarm. Most common DC-DC converter abrupt faults are the semiconductor switch and diode OCF and SCF. Incipient and slow drift faults result in slow degradation and operating conditions respectively. Also known as parametric faults or soft failures, they are commonly caused due to aging of the converter components or change in converter operating conditions. These faults are most commonly observed in electrolytic capacitors but they can also be experienced in semiconductor switches due to TDDB, NBTI, and HCI. Due to different nature of the faults, methods which are a suitable for detection of slow drift faults may not be optimal for other types of faults such as abrupt or intermittent faults. Therefore several methods may be used in parallel to build up a reliable fault detection system. It can be observed form Figure 28 that the selection of model based technique is independent from the type of converter used or sensors installed. A model based FD algorithm can basically be implemented on the process controller, often without additional hardware requirements. Moreover, the measurements necessary to control the process are sufficient for the FD algorithm so that no additional sensors have to be installed. Under these circumstances, only additional storage capacity and greater computer power is needed for the implementation of a model based FD algorithm. The FD algorithm only requires input output data processing for implementation. Once a process model is developed feature generation has been carried out, Figure 28 can be used for the selection of proper analytical model. With reference to process model, process features, and fault types, Figure 28 gives brief information on the selection of proper analytical fault model with additional information of the reference article and faulty component. Table 2 gives a detailed comparison of model based FD techniques. It can be observed by looking at the table that cost range for model based FD fall in range of low cost techniques because of its independence from extra sensors. However these techniques could easily fall in medium to high price range if a complex mathematical model for the converter requires huge computational resources. These techniques have the added advantage of its effectiveness for converter working in CCM and DCM. Studies carried out in this review paper show that 50% of research based on model based FD techniques carried out their studies on converters operating in CCM as well as DCM. Simulation studies have been the preferred mode for the proof of concept in model based FD techniques with 50% research results based on it. Occasionally FPGAs and DSPs have been used to develop the mathematical models for these converters and carry out fault diagnostics. Perhaps the most noticeable advantage of using model based FD is independence from extra sensors. It can be seen from the model based FD comparison table that no extra sensor is used to measure the fault detection signatures.

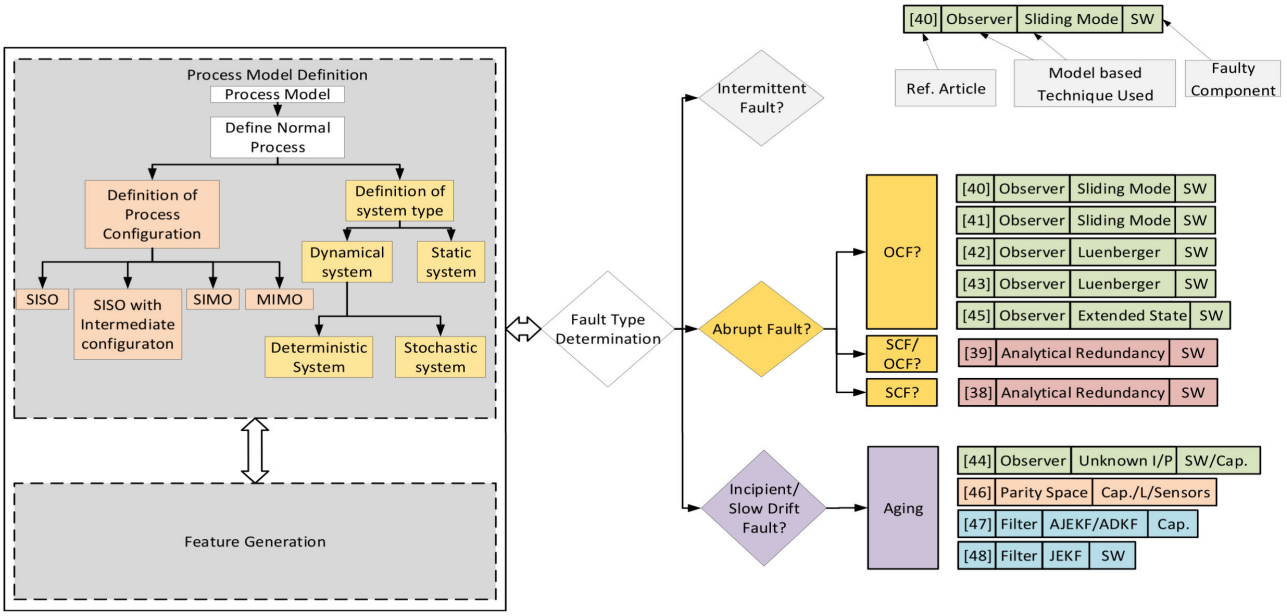

FIGURE 28. Model based FD system selection.

Inductor voltage and current along with the input voltage, output voltage and GDS has been the popular fault diagnostic signature for fault detection and its type. With almost 34% switch OCF and SCF detected in less than 2 switching cycles, parametric faults including switch and capacitor aging, were also addressed.

E. HISTORY BASED FAULT DIAGNOSTICS

Unlike the model based FD, history based or data driven fault detection techniques do not deploy a mathematical model, instead it derives a model from known and measured input/output process data. This technique is preferred for fault identification and diagnosis of non-linear dynamic systems. It develops a mapping between an input and output space thus creating an associated memory which can generate a legitimate output when presented with an unseen input. History based fault diagnostics method includes Fuzzy Logic (FL), Neural Networks (NN), Clustering, Self Organizing Maps, Statistical Methods, Expert System and Pattern Recognition. History based FD is gaining a lot of interest because of its ability to model complex and non-linear time invariant system with out going into details of converter models. With the introduction of more efficient and low cost processing resources, this technique is proving to be a promising alternative to other FD technique. FL techniques come in handy for situations where the system is not properly modeled or cannot be represented mathematically and a fuzzy model is created based on the knowledge of system behavior or experimental information. FL can be used in conjunction with average current Parks vector technique for 3ϕ Cascaded Multilevel Inverter (CMLI) used in a Permanent Magnet Synchronous Motor (PMSM) drive to identify intermittent single and multiple power switch OCF [51]. Intermittent faults are the conditions between a healthy and faulty condition which may arise due to faults in the PWM input signal, wiring faults or EMI. Using variable calculated from 3ϕ CMLI phase current such as error value of normalized absolute average currents, OCF detection for all switches is carried out. Techniques which diagnose OCF in the DAB converter employing Extended Phase Shift (EPS) uses mean voltage values with the preset limit [27]. Means calculation requires averaging of switch node voltage making it a FD signature in this technique. NN based Just In Time Learning (JITL) method can be effectively used to detect switch OCF in a DAB converter under EPS control [52]. These converters generate a lot of complex data, including i_L, v_L, primary switch voltage V_{AB}, secondary switch voltages V_{CD} and output power, which are not linearly coupled with different time periods and do not obey a Gaussian Distribution. This makes modeling of the system very difficult and error prone. JITL has been used to model the input and output data of complex non-linear system online in an adoptive process without interrupting the converter operation. Variables used as input to the JITL model are i_L, v_L, V_{AB}, V_{CD}, I_{IN}, I_{pri} and I_{sec} which makes an original database for comparison. If the sample measured in real time x_R is similar to sample in the database x_D, then x_R is replaced with x_D, otherwise the sample is discarded. After computing similarity s_i, local model parameters are computed by establishing a minimum and maximum threshold. To ascertain the deviation between actual and measure data, an error value is calculated. Based on minimum error values, an optimal value is obtained. Using the l_{opt}, a local model is prepared from the real time data and an Euclidean distance

between this model and the original data model is computed. Finally, thresholds are selected by using the Euclidean distance M_{th} to identify the fault in a DAB converter as this value is the largest distance of DAB converter without fault. NN and statistical decision making can also be put to effective use for diagnosing faults in the entire energy conversion system [53]. Using NN, inputs and outputs of the system are processed to develop a dynamic model which is further trained using first order gradient algorithms. This NN model is the representation of fault free energy conversion system. A residual sequence is extracted using the difference between output measurements of a real system and estimated output provided by the NN model which further undergoes statistical processing of developing a stochastic variable which follows the X^2 distribution. A fault threshold defining the upper and lower bound of a confidence interval of X^2 distribution was developed. As long as the stochastic variable is within this bound, the system is said to be fault free, but if this variable crosses the bound, system is said to be faulty. Furthermore, by repeatedly applying the corresponding statistical test into sub spaces of the system state-space model, these faults can further be isolated and it could be established weather the failure is in its mechanical part or electrical DC-DC converter part. Deep Feed-Forward Network (DFN) need fewer training samples, short training time and has one of the highest training accuracy among other NN algorithms. One approach that developed a FD classifier based on DFN and wavelet compression to identify and locate switch OCF in a phase sifted full bridge DC-DC converter was presented in [54]. Transient features are used to train these FD classifiers as the magnitude change of these fault related components is large and easily distinguishable than in the steady state analysis. Equally important for converter health, parametric faults need to be early diagnosed like catastrophic failures for system prognosis. Support Vector Machine (SVM) classifiers has been put to use to identify parametric and incipient faults in a single faulty component or group of components in a Buck converter [55]. A simulation software was used to generate number of time domain simulations of the converter circuit which were then used for testability evaluation and generation of data set to train the SVM classifier and Fault Indicating Neural Network (FINN) by randomly varying the values of components in given range. Another software was used to determine the testability and ambiguity groups of DC-DC converter. The procedure in this technique either identified the faulty component or in case of ambiguity it highlighted the family of components where the fault lied. Once the error was detected and identified, the estimation of degradation in the faulty component was carried out using FINN. Solar radiation and temperature measurement can be put to effective use with Artificial Neural Network (ANN) to detect and isolate the switch OCF in PV systems [56]. Using these parameters, ANN is trained to predict the output voltage and currents which is compared with the converter actual output to generate the required residual. Thresholds are calculated to define limits for the residuals and fault indication. Various statistical methods are used to develop a relationship between the input and output of the system for fault detection and isolation in DC-DC converters. One such research work which used a hybrid approach to detect system parametric faults was presented in [57]. Two types of classifiers namely, Deep NN based classifier and Naïve Bayes classifier were used. Initially, model based estimation of critical system parameters was carried out and instead of using these parameters as concrete ground truth, they are treated as statistical quantities with uncertainty. A second statistical classification stage was applied which made use of these statistical quantities to classify various converter conditions in terms of healthy or faulty. With characteristics of fast learning speed and ease of implementation, Extreme Learning Machine (ELM) has been employed for the parametric fault prognosis of a closed loop SEPIC converters [58]. Since practical converter circuits operate with a closed loop control structure and open loop response of the converter is different form the closed loop, the authors have built a relationship between the variable quantities of system level parameters with degradation response and operating conditions as well. Relationship in the form of a relational function was obtained using multivariate least square regression based on experimental data. A Fault Characteristic Parameter (FCP) was developed which exactly reflected the fault level of the closed loop SEPIC converter and was not effected by the variable operating conditions. FCP only reflected the degradation of circuit due to the parametric faults such as capacitor and inductor degradation as well as switch and diode aging due to increase in the on resistance. In the next step, system level parameter such as ripple ratio of output voltage delta and ripple resistance were calculated. This sample data was used to train the ELM model for fault prognostics of the closed loop SEPIC with good accuracy. An anomaly detection method by statistical feature estimation using Gaussian Process Regression (GPR) and Genetic Algorithm (GA) was proposed in [59]. Initially, GPR was used to estimate the normal output range, and building the GPR model required only normal samples obtained from actual circuits as the training data. This output range was taken as the key criterion to detect the anomaly. After that, seven statistical features of the output signal namely mean, standard deviation, skewness, kurtosis, entropy and centroid were calculated by a GA, and the extreme values of features were saved as detection indexes. With X_{max} and X_{min} as the maximum and minimum value, a normal detection was implemented by comparing the seven statistical features of the actual output with those saved detection indexes. When one of the features deviated from these indexes, it provided an indication that the working state of the DC-DC converter has become abnormal. This research has only been implemented to realize the anomaly detection of DC-DC converter but it cannot identify the degradation parameters and determine the fault location. Table 3 gives a detailed comparison of history based FD techniques. As compared to hardware and model based fault detection, history based fault detection studies are primarily focused on parametric fault detection

TABLE 2. Comparison table for model based fault diagnostic techniques.

Ref.	Topology	Faulty Component	Fault Type	Isolation Type	Fault Detection Time	Fault indicating Sig.	Sensor Info.	Control	Fs	CCM/DCM	Cost
[38]	Interleaved Boost Con.	SW	SCF	Non-Iso	$< T_S$	I_L, V_{IN}, GDS	0	DSP	10KHz	CCM	Low
[39]	Single Ended DC-DC Con.	SW	OCF/SCF	Non-Iso	$< T_S$	I_L, V_{OUT}, V_{IN}	0	DSP	20KHz	CCM DCM	Low
[40]	MMC using Half & Full bridge Con.	SW	OCF	Non-Iso	$<$ 100ms	Converter arm current, Cell capacitor voltage	0	Sim	NA	NA	Low
[41]	1φ MMC	SW	OCF	Non-Iso	$<$ 50ms	Converter arm current, Cell capacitor voltage	0	FPGA	NA	NA	Low
[42]	Interleaved Boost Con.	SW	OCF	Non-Iso	$< 2T_S$	I_L	0	FPGA	25KHz	CCM DCM	Low
[43]	VSI	SW	OCF	Non-Iso	$4\%ofT_S < FD < 16.7\%ofT_S$	3φ Current	0	dSPACE	10KHz	NA	Low
[44]	Hybrid Boost & Buck-Boost Con.	Cap.	Aging	Non-Iso	NA	I_L, V_{BUS} V_{CAP}	0	Sim	NA	CCM DCM	Low
[45]	MCC	SW	OCF	Non-Iso	FD=10ms FI=30ms	Full arm voltage $dV_{Cap}/d(t)$	0	NA	2KHz	NA	Low
[46]	Boost, Buck	Cap, Inductor Sensors	Parametric Fault	Non-Iso	NA	I_L, V_{OUT}	0	Sim	20KHz	CCM	Low
[47]	Boost Con.	Cap	Aging	Non-Iso	NA	Cap. V_{IN} Cap. V_{OUT}	0	Sim	15KHz	CCM DCM	Low
[48]	Bi-Dir Buck-Boost Con.	SW	Aging	Non-Iso	NA	V_{IN}, V_{OUT} to cal. $R_{DS(ON)}$	0	Sim.	15KHz	CCM DCM	Low
[49]	Buck Converter	SW, Diode	OCF	Non-Iso	SW 37.5μs Diode 20μs	I_L, V_{IN}	0	Sim	NA	CCM DCM	Low

TABLE 3. Comparison table for history based fault diagnostic techniques.

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[38]	Interleaved Boost Con.	SW	SCF	Non-Iso	$< T_S$	I_L, V_{IN}, GDS	0	DSP	10KHz	CCM	Low
[39]	Single Ended DC-DC Con.	SW	OCF/SCF	Non-Iso	$< T_S$	I_L, V_{OUT}, V_{IN}	0	DSP	20KHz	CCM DCM	Low
[40]	MMC using Half & Full bridge Con.	SW	OCF	Non-Iso	$<$ 100ms	Converter arm current, Cell capacitor voltage	0	Sim	NA	NA	Low
[41]	1φ MMC	SW	OCF	Non-Iso	$<$ 50ms	Converter arm current, Cell capacitor voltage	0	FPGA	NA	NA	Low
[42]	Interleaved Boost Con.	SW	OCF	Non-Iso	$< 2T_S$	I_L	0	FPGA	25KHz	CCM DCM	Low
[43]	VSI	SW	OCF	Non-Iso	$4\%ofT_S < FD < 16.7\%ofT_S$	3φ Current	0	dSPACE	10KHz	NA	Low
[44]	Hybrid Boost & Buck-Boost Con.	Cap.	Aging	Non-Iso	NA	I_L, V_{BUS} V_{CAP}	0	Sim	NA	CCM DCM	Low
[45]	MCC	SW	OCF	Non-Iso	FD=10ms FI=30ms	Full arm voltage $dV_{Cap}/d(t)$	0	NA	2KHz	NA	Low
[46]	Boost, Buck	Cap, Inductor Sensors	Parametric Fault	Non-Iso	NA	I_L, V_{OUT}	0	Sim	20KHz	CCM	Low
[47]	Boost Con.	Cap	Aging	Non-Iso	NA	Cap. V_{IN} Cap. V_{OUT}	0	Sim	15KHz	CCM DCM	Low
[48]	Bi-Dir Buck-Boost Con.	SW	Aging	Non-Iso	NA	V_{IN}, V_{OUT} to cal. $R_{DS(ON)}$	0	Sim.	15KHz	CCM DCM	Low
[49]	Buck Converter	SW, Diode	OCF	Non-Iso	SW 37.5μs Diode 20μs	I_L, V_{IN}	0	Sim	NA	CCM DCM	Low

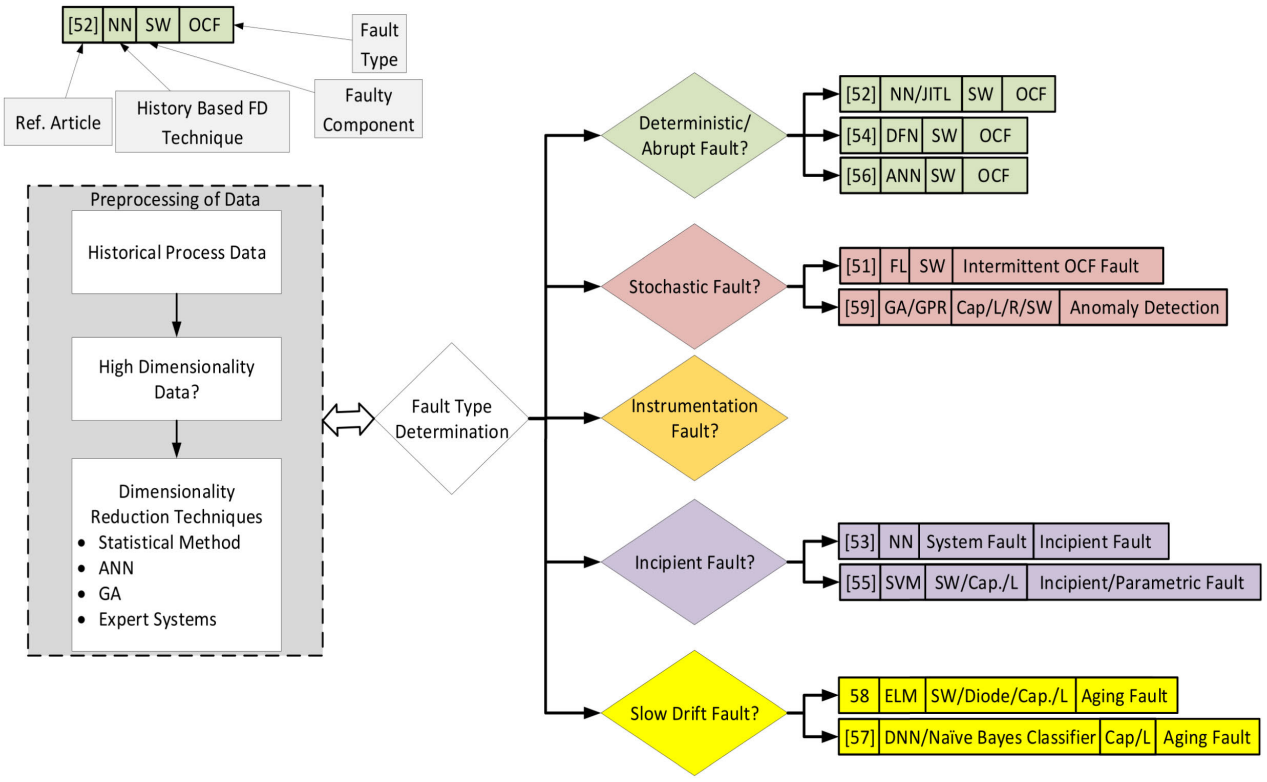

FIGURE 29. History based FD system selection.

for capacitors, switches and diodes with 66% studies related to component aging. A model based FD technique is suitable where the converter structure is known and a mathematical relationship between outputs and the degradation parameter is accurately established. However, history based FD relies on training using large data set obtained from input and output of the converter. With the availability of huge data set and powerful computational resources, simulation studies were carried out in more than half of the articles under history based FD techniques. They also prove to be equally effective for isolated and non-isolated converter types in CCM and DCM.

F. GUIDELINES FOR SELECTION OF HISTORY BASED FD TECHNIQUES FOR DC-DC CONVERTERS

History based FD is getting a lot of attention by the researchers due to its ability to model complex nonlinear behavior of the high performance DC-DC converters. Various methods have been considered for implementation of FD, and each of these methods has its own strength, limitation, and formulation towards different kinds of process data characteristics. Due to availability of a number of techniques, selection of a suitable FD method for the these converter system is getting more and more challenging. In order to choose a proper historic data based FD approach, this section gives a guideline which takes into consideration the fault types and data available. Figure 29 gives a general scheme for history based FD and diagnosis. The first problem is the presence of a high dimensional feature vector [60]. High performance DC-DC converters consist of various components or, parts and each of these parts may have significant numbers of measured variables resulting in a large number of high dimensional data samples. Handling these high dimensional process data is a challenge for the historic data based driven approaches. This problem is addressed by filtering out the irrelevant and redundant information hidden in the feature values with the help of feature selection or feature extraction. After that, the FD method selection is based on different types of faults that likely occur in the process systems. The fault is classified into five different groups: deterministic faults, stochastic faults, slow drift, instrumental faults, and incipient faults. Deterministic faults are the result of a sudden change in the process variable. In case of DC-DC converters, switches and diode OCF and SCF produces this step change which can be easily detected and diagnosed. Machine learning approaches such as ANN, Deep Feed Neural Network, JITL and multivariate statistical analysis methods are suggested to be applied for this particular scenario. Stochastic faults appears as random faults and are triggered with the random variation in the process operating conditions. GA and GPR with anomaly detection capabilities can be used for these stochastic fault detection. Fuzzy Logic has also been put to effective use for intermittent or in other words stochastic fault detection. Converter operation usually experiences

slow drift from normal operation which causes false alarm if not adapted to normal models. Slow varying processes are characterized by multiple operating points and applying traditional statistical methods will ultimately cause a fault alarm even if the converter is operating normally because these methods assume that the process has one stable operating region. Therefore problems will arise when traditional statistical approach are applied to slow varying process. This study shows that ELM, DNN and Naive Bayesian Classifiers can be effectively put to use for slow drift fault measurement. Incipient faults are characterized by the wear and tear due to aging of the converter elements. Aluminum Electrolyte Capacitor are the most common converter components to age and cause incipient faults. These are relatively difficult to handle due to its slow developing nature. Most of the machine learning methods, such as NN and SVM have been applied for the cases of incipient faults studied in this article, with the fault diagnosis being successfully achieved.

G. FUTURE TRENDS AND CONCLUSIONS ON FAULT DIAGNOSTIC TECHNIQUES

The main purpose of fault detection in DC-DC converters is to avoid all types of faults from turning into critical situations where human lives and critical equipment's are at risk. Thus, the detection and diagnosis of faults is an important and challenging research topic. In this paper, FD techniques were classified into three main categories depending upon the generation of error signal or residual and its processing to generate a fault alarm. (1) hardware based (2) model based and (3) historic data based. In hardware based FD, analogue or digital circuits are used to measure a particular variable of interest and in response a fault indicator circuit generate a fault signal based on the location and type of faulty component. These group of techniques are popular among the researcher due to its fast response which is important for incorporating fault isolation and FT, ensuring service continuity. However these techniques are specific to fault types and converter structure inhibiting their reusability. Furthermore, sensors and diagnostic hardware circuits are also prone to failure. They impose extra cost and weight which could prove to be impractical for portable low power electronic devices. Fault detection without relying on extra hardware has the obvious advantage of cost and size effectiveness and offers considerable implementation flexibility. With this in mind, researchers deviated their attention to model based and data driven FD techniques. Based on the model which is developed by gaining complete understanding of the converter, model based FD technique uses analytical approach to decide whether a fault has occurred. With exponential increase in computational power and raw data availability, machine learning approach is getting more popular with in the research community. It has been used to obtain knowledge from a large amount of empirical data at the cost of intensive computation. Without any need for converter explicit model, this approach can detect and diagnose faults from process data base. ANN, SVM, GA, Statistical methods, DFN, Bayesian

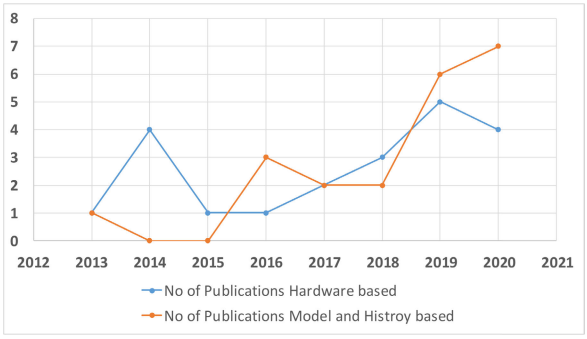

FIGURE 30. Comparison of FD techniques time line.

Networks, FL, ELM are some of the history data based approaches that have been mentioned in this review paper. Figure 30 illustrates the trend among various types of FD techniques based on the articles reviewed in this paper. As both model based and history based techniques are more inclined towards computer processing and lesser hardware dependence these techniques are combined and treated as one to give a better comparative analysis. By looking at the graph, it can be observed that within the last couple of years, more research articles were published based on model and history based FD techniques and this trend is getting more steep. Although still in its infancy, historic data based FD techniques have a lot of potential due to its ability to model high performance modern nonlinear DC-DC converters whereas it is very hard to establish fault mathematical models of these converter topologies. With the exponential increase in information and computer technology, collecting large amounts of data is no longer a problem, and history based methods have attracted more and more attention. It is now well established that there is no single FD procedure that could satisfy all the requirements of a perfect FD system. Moreover, future process monitoring and FD systems need to incorporate reliability, handle uncertainty and be able to use large amount of data. The solution to these problems have been sought in hybrid FD frameworks. One such approach has already been discussed in [57]. In this research, two types of classifiers namely, Deep NN based classifier and Naïve Bayes classifier were used. Initially, model based estimation of critical system parameters was carried out and instead of using these parameters as concrete ground truth, they are treated as statistical quantities with uncertainty. A second statistical classification stage was applied which made use of these statistical quantities to classify various converter conditions in terms of healthy or faulty. The hybrid approach can also be established between model based and history based FD technique. Model based FD methods establish the relationships between the outputs and the degradation parameters, and they are mainly applied to the DC-DC converters with the known circuit structure.However, in practical applications, the circuit structures of DC-DC converters are usually unknown. Therefore, history based data driven methods are applied to detect and diagnose the anomalous states. The relationship between the parameters to be estimated and the available signals is

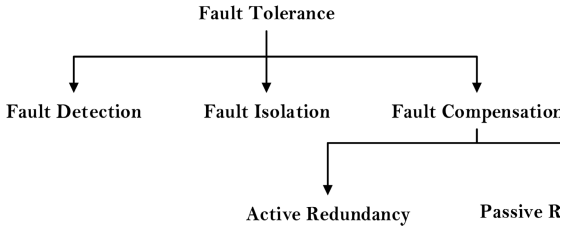

FIGURE 31. Fault tolerant scheme classification.

established through training data, which are obtained from the output of the DC-DC converter.

IV. REVIEW OF FAULT TOLERANT SCHEMES

The key goal of FT scheme is to intercept the propagation of fault to the rest of converter modules to prevent a cascaded failures. FT strategy is usually composed of three main attributes i.e. redundancy, reconfiguration and modularity. Steps involved in any FT procedure are fault detection, isolation and fault compensation. Due to its benefits, FT schemes are employed at the design stage of the converter to improve its resilience against all types of failures. In critical systems where continuity of service is important, FD and Fault Isolation (FI) is not adequate and a FT scheme must be applied which is composed of fault detection, isolation, and Fault Compensation (FC). Fault Detection is the first step for all types of FT schemes which detect the occurrence of a fault. This step is designed to be very fast to ensure FI and prevent its penetration to other parts of the converter. Most FT schemes carry fault detection in less one switching cycle. FI and containment confines the failure within a faulty subsystem. Some techniques use safety device such as quick blow fuses in a converter which increases the cost or degrades the form-factor and potentially sacrifice efficiency, neither of which is acceptable in high performance converters. Furthermore, using a fuse is not an effective method to prevent propagation of the fault in modern semiconductors due to its slow response time (in the ms range), while the short circuit immunity of silicon power devices is in the μsec range. Adoption of a multi-phase configuration is necessary for FC as it maintains continuous power delivery to downstream subsystems in case of a malfunction in one of the phases. FC can mask the effects of failure on system output and ensure recovery through redundancy. There are two basic types of redundancies: active, in which the redundant subsystems are operating and automatically overtake load for the failed unit and standby redundancy, in which the redundant subsystems are inactive and replace the failed unit upon a fault. However, redundancy is not the only requirement for FC and further precautions from control standpoint are necessary to provide a seamless post-fault operation. Figure 31 gives the information on FT schemes and its classes. A FT scheme for a Modular Multilevel Converter (MCC) was presented in [61]. MMC on its Low Voltage (LV) side, utilizes bridge based isolated DC-DC converter to realize Maximum Power Point Tracking (MPPT). This converter along with a PV panel

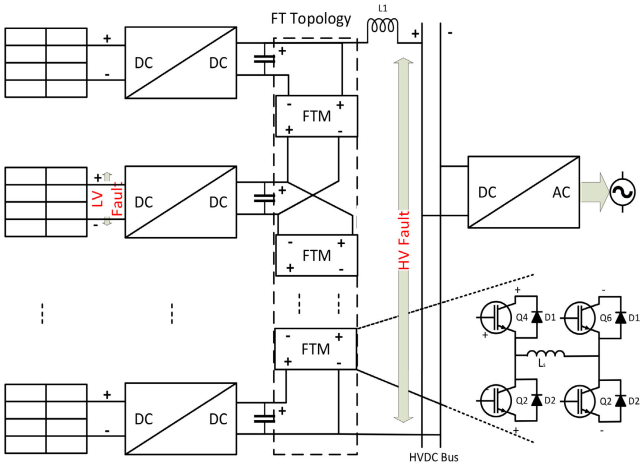

FIGURE 32. FT scheme for MCC.

make a Photovoltaic Sub-Module (PVSM) Figure 32. Using 4 switches with anti parallel diodes and an inductor in a FT Modules (FTM), this technique ensured the continuity of service in case of SCF in LV ports by keeping the output capacitor voltage of all the Sub Modules (SM) in balance and was able to shut down quickly and safely by guiding the SCF current into the SM's capacitors. Using N-1 extra SMs for N number of PVSM, FTM balanced the voltages of adjacent modules by working as a bidirectional Buck-Boost converter and capacitor of the faulted SM was charged by the remaining healthy SMs. In case of high voltage fault the connection between DC bus and the converter was cut off to save system form complete failure. PV stations are effected by partial shading, short circuiting and grounding faults which reduces power generation by reducing the series current of these modules. Partial shading results from shadows due to high rise buildings or trees whereas short circuit and grounding faults result from damaged insulation of cables and loosening lines respectively. On such research that addresses these issues for PV stations is presented in [62]. This approach made use of a Buck-Boost converter to regulate the output voltage and current during partial shading thus ensuring that all PV modules work at Maximum Power Point (MPP). For SCF in one of the SM, duty cycle was reduced to 0 in order to separate the faulty module form rest of the PV system and the controller duty cycles was regulated to step up the voltage to compensate for the dropped voltage due to faulty module. This ensured maximum power generation and stable operation. Grounding faults degrade the 3ϕ capacitor and destabilize the PV module system. This approach used a zero axis proportional resonant controller which suppressed the DC bias and the third harmonic components which eventually increased the system stability. In [63], a FT tapping scheme injected power from remote renewable energy resources to a High Voltage Direct Current (HVDC) line. Using a Modular Resonant DC-DC Converter consisting of Voltage Source Converter (VSC), power was drawn from the remote resources and fed to the SM in second stage to step up voltage to the desired HVDC level. By using a

charging and discharging cycle, this multi modular converter was able to inject power from the renewable energy resources to the HVDC line. During pole to pole fault, a substantial increase in the DC current or decrease in the DC voltage line is detected. Upon withdrawing the input pulses to all the switches in SM, the capacitors were inhibited from discharging into the shorted HVDC line thus protecting the load. Once line fault was over, the switches were again activated to transfer power from these resources. In conventional Battery Electric Storage Systems (BESS), combining different batteries with varying health and usage pattern can reduce system lifetime, capacity and reliability as overall performance of the system is defined by the weakest cell of the battery module. [64] introduced a re-configurable system which actively controlled the power flow in accordance with the battery condition, and resulted in improved utilization of the available cells in a battery modules. A modular re-configurable battery management system was developed utilizing the Cascaded DC-DC (CDCDC) converter. CDCDC was selected for this research after a comparison was made between the various configurable and conventional topologies in terms of scalability, capacity utilization and fault tolerance. A control scheme was presented in which when a fault in one SM occurred, the cell error signal was activated and the corresponding SM was bypassed by disconnecting it softly. However, the system still lacks a complete emergency shut-down procedure of battery system to make it fully functional for the practical applications. Interleaved DC–DC converters inherently have FT capabilities because of its redundant architecture and can be used to provide uninterrupted power [65]. Every control scheme for interleaved DC-DC power converter strives to improves the output voltage regulation as well as the current sharing of SMs. However under faulty conditions, they lose the equal sharing among the healthy SMs. The authors have proposed a method to diagnose faulty module and generate FD and identification signals that identify and isolate faulty switch. The fault diagnosis signals was used to adaptively tune the reference currents and current controller gain in the converter to achieve a desired output voltage generation and equal current sharing among the remaining healthy modules under the fault condition. FT strategy can also employ additional inverter leg with 4 bypass TRIACs in electric vehicle propulsion system consisting of a DC-DC boost converter and 3ϕ inverter [66]. Using I_L for switch OCF detection in Boost converter and angle of the output current trajectory for inverter switch OCF detection, the authors in this technique identified faulty component and performed the FT operation in less that 200ms. Upon Boost converter switch OCF, a bypass triac was used to connect the additional leg to the corresponding faulty module and correspondingly the gate signal of the faulty switch is bypassed to FT switch. For inverter side switch OCF, additional triac was used to connect the FT inverter leg to bypass the faulty switch and correspondingly the gate signal is bypassed to FT switch as illustrated in Figure 33. With the aim to avoid the use of extra SM, research presented in [67] used two separate schemes in

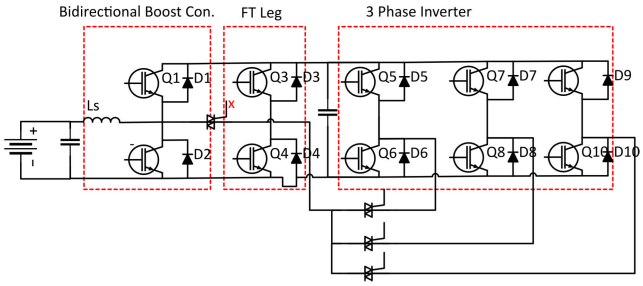

FIGURE 33. Bidirectional Boost converter with 3ϕ inverter and FT leg.

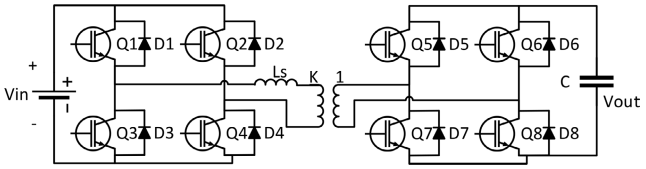

FIGURE 34. DAB converter utilized in [67].

order to provide FT in primary and secondary side of a DAB converter Figure 34. For secondary side it used Secondary Side Bypass Arm technique to incorporate fault tolerance by blocking the gate pulses of the faulty arm. In case of OCF in the primary side, Primary Side Lower Power technique is employed to lower the OCF current by decreasing the converter power. This power reduction is achieved through limiting the phase shifting ratio between the primary and secondary. Operating with 3/4 of the normal power, overall efficiency of the system did not suffer. By computing the difference between i_L in all the legs and comparing to a pre-specified criterion, OCF in the corresponding phase of a 6ϕ Mirror Interleaved Boost Converter can be diagnosed [68]. A FT strategy was developed which used this information to initiate two kinds of FT control techniques. One was symmetric reconfiguration in which symmetry between the two buses was maintained by deactivating the healthy phase symmetrical to the faulty phase. The authors showed that the system with overall 4 phases had high average phase currents and voltages which caused extra stress on the power switches. Second technique was asymmetrical reconfiguration in which the faulty phase was eliminated and the rest of converter phases kept working. With 5 phases, the system reconfiguration resulted in seamless transition during FT stage with unbalanced currents in 2 buses. The first stage a full DC-AC grid connected PV system is a distributed DC-DC Boost converter and the second stage is a 3 level Neutral Point Clamped (NPC) inverter and [69] presented a FT method for both stages. Mean Time to Failure (MTTF) was estimated for the first stage DC-DC converter and optimized using this approach. Converter FT operation was carried out by disconnecting the corresponding leg in case of the module fault and output phase of the faulty leg was connected to the NPC inverter neutral point. FT strategies are very critical for continuous operation of large rated generation units. A shared leg FT operation for 5 channel 3 Level NPC back to back power converter operating a 250MW Doubly Fed Induction

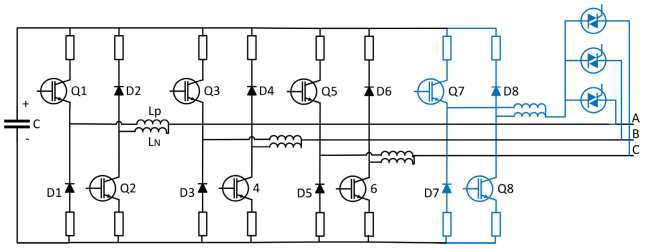

FIGURE 35. FT 3ϕ Dual Buck VSI topology using a single standby redundant half bridge with coupled inductor.

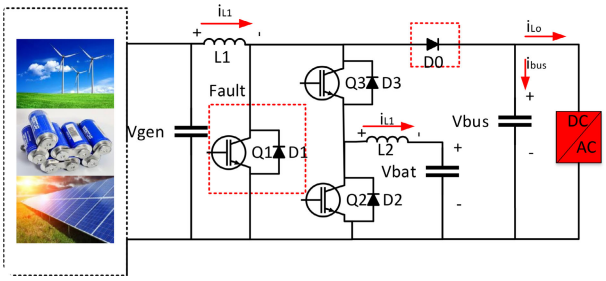

FIGURE 36. Modified power conversion system.

Machine was given in [70]. Switch OCF was diagnosed with the help of normalized phase current based average method by calculating a faulty phase error diagnostic variable ξ which was zero under normal conditions. Under fault, ξ for a particular phase reached a certain threshold and the corresponding phase was diagnosed to be faulty which was disabled in all the multichannel power converters by seizing its switching pulses. The fault phase was connected with the common leg with the help of shared leg reconfiguration switches and the common leg was shared between the rotor side converter and grid side converter. Under the FT operation, the total power delivery reduced to 50% of the original power. It was shown that in case full power delivery was needed, additional reactive power was to be absorbed from the grid and shared leg components rating had to be increased. 3ϕ VSI is used in various critical DC-AC power conversion applications such as variable speed drives, renewable energy resources and uninterrupted power supplies. In [71], after FD standby redundant dual Buck half bridge was activated in place of the faulty main half bridge. If switch OCF occurred in any phase, the healthy switch in that phase was turned off and the redundant dual Buck half bridge was used to provide positive and negative output. In case of SCF, the faulty phase was isolated by blowing up the fuse. After that, the standby redundant dual-buck half bridge was used to replace faulty main half bridge of the inverter Figure. Second proposal used three standby redundant dual-buck half bridge without coupled inductors. Third configuration was quite similar to the second type but it composed of three standby redundant classical branches with IGBTs plus free-wheeling diodes. In time detection of catastrophic failures and application of FT strategy to provide uninterrupted seamless reconfiguration has been embedded in the latest DC-DC converter. One such research where the FT technique detects a timely SCF and takes remedial actions in less than one switching cycle by employing only one additional switch to a conventional synchronous buck converter was presented in [72]. In case a SCF occurred, fuse protection was activated to inhibit inrush current. The SCF in switch was detected by comparing the GDS and the drain to source voltage V_{DS}. One of the powerful feature of this techniques was its application of affine parameterization based advance control technique to tune the feedback controller. Using this approach, the FT topology was able to increase the speed of post fault reconfiguration and minimize overshoots and undershoots providing efficient reconfiguration and smooth transition between a healthy and reconfigured state. By measuring the change in i_L with respect to GDS a fast FD and FT control scheme has been presented in [73]. Any change in the inductor current due to the fault was used as an event which was further detected by an event counter. By setting the target count threshold 1, the counter returned the fault signal in response to the fault. Due to fast FD and reconfiguration procedure, a seamless transition was achieved between a normal and fault tolerant converter which did not effect continuity and performance of a system essential for safety critical electronics applications. Wind energy resources are intermittent and produce power surges which may result in converter faults resulting in whole system shut down. Ultimately, more power will be demanded from rest of the wind turbines as total load will be divided with in the remaining power generation units. Authors in [74] introduced a FT scheme using modified two stage boost (Boost + bidirectional DC-DC converter) structure with energy storage capability Figure 36. In this scheme, a fault detection index Fd_{idx}, which is the ratio between i_L and sum of the measured i_L and load current was calculated. In case of switch fault, a sudden decrease in the measured i_L and output voltage resulted in abnormal increase in control current which ultimately increased Fd_{idx}. This value was compared with the pre-established threshold for the indication of faulty switch. In [75], the authors have implemented a FT scheme for two stage DC-DC conversion and storage system. The first stage consisted of a Buck converter operating in DCM to steps down the high PV output voltage to battery potential and the second stage consisted of a Buck-Boost converter operating in a CCM to provide power to variable load. Both stages were separated by battery as a storage system. Switches in both converters were separately and asynchronously controlled in healthy condition. When OCF occurred in any of the main switches, both switches were disabled by the controller and a synchronous switch equivalent circuit was activated to ensure service continuity at full power. In [25] and [26], FT operation was initiated upon detection of SCF and OCF. In case of SCF detection the reconfiguration process was initiated by isolating the switch using fast fuse in series with the main switch Figure 40. System reconfiguration was performed immediately using redundant switch in case of OCF. SCF reconfiguration had to wait for the fuse action. FT converter was able to continue to operate, after reconfiguration, in the same condition as in

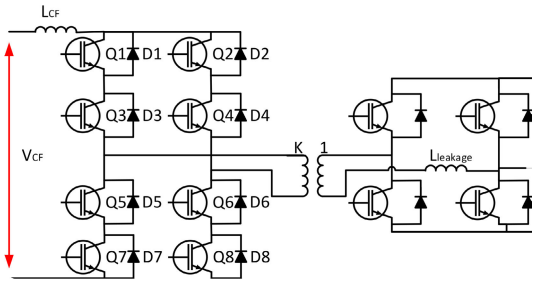

FIGURE 37. Current fed full bridge secondary modulated DC-DC converter.

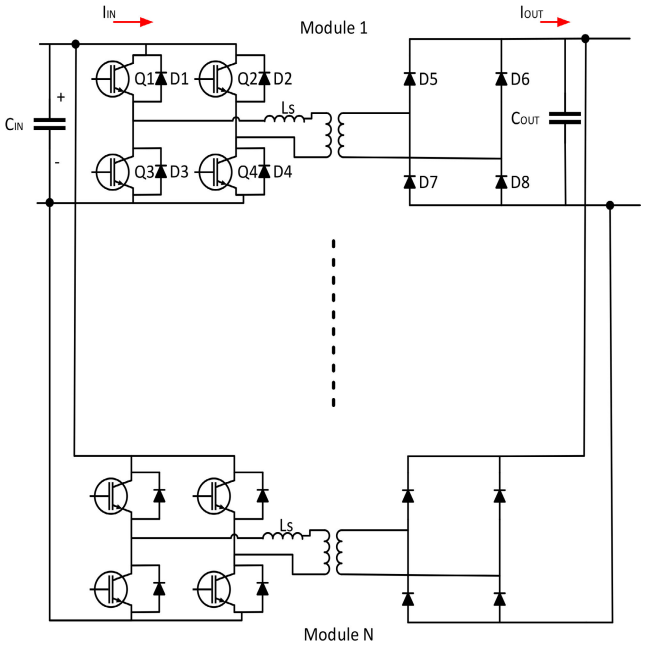

FIGURE 38. An N-parallel-connected SAB DC-DC converter.

healthy converter. FT scheme for the primary side switches of the Full Bridge Secondary Modulated Converter was presented in [76] as they are 5 times more prone to failure then the secondary side switches [77]. Figure 37 shows the Current Fed Full Bridge Secondary Modulated DC-DC Converter presented on [76].

After FD and FI, the authors took advantage of the high number of switches in the primary side and readjusted the modulation sequence to reconfigure the faulty converter as Flyback Secondary Modualted Converter. Output voltage on the secondary side doubled which was adjusted by turning on four quadrant switch on the secondary side forcing the output rectifier to operate in full bridge mode rather than the voltage doubler mode. Using single current sensor at output, type and location of switch fault in N level parallel connected single active bridge converters Figure 38 was identified with in 2 switching cycles [78]. Output current was sampled in the pre-established stage and used to point out the faulty phase. With improved input and output current quality by shifting the phase angles of healthy modules, a FT strategy allowed the operation of converter in full power for type1 fault and with limited power for type 2 fault. Buck converter and multi-mode single leg converter is used in conjunction in

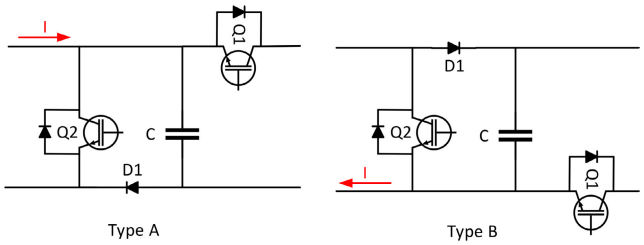

FIGURE 39. SM used in [63] for FT tapping to HVDC line.

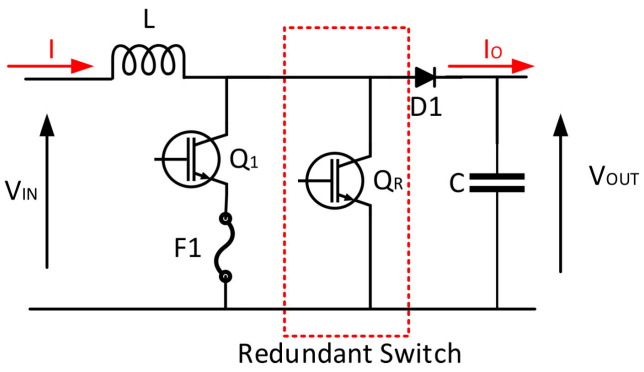

FIGURE 40. Use of redundant switch demonstrated in [25] in single ended converter.

a hybrid electric vehicle application. By modifying PWM pattern of switches in multi-mode single leg converter, switch failure in Boost converter can be compensated [79]. With out using additional sensors, i_L slope was compared with GDS to detect Boost converter switch OCF. After this activity, the multi-mode single leg converter was reconfigured as an auxiliary Boost converter to continue the service availability. By increasing the number of voltage levels in primary and secondary side of transformer in T type converter, voltage quality and ultimately efficiency can be improved. [80] presented a FT strategy for Modified 5 Level T-Type Dual Active DC-DC converter with Phase Disposition Pulse Width Modulation. After OCF, FT operation was carried out by modifying the reference voltage waveform to change the modulation scheme. 5 level T converter was modified to 3 level in order to provide fault tolerant capability and continue the service availability.

V. GUIDELINES FOR SELECTION OF FAULT TOLERANT TECHNIQUES FOR DC-DC CONVERTERS

Reliability of DC-DC converters is very importance in mission critical applications such as medical equipment, electric vehicles, and aerospace devices etc. It is therefore very critical to incorporate fault tolerant techniques at the design stage which eventually improves system resilience against unpredictable failures. A FT scheme is used to intercept the propagation of a fault and to ensure service continuity by preventing cascaded failures. FT strategy is composed of three main attributes i.e. redundancy, reconfiguration and modularity. The steps involved in a FT procedure are (1) fault detection and identification, also known as fault diagnosis, (2) isolation and (3) fault compensation or the remedial action.

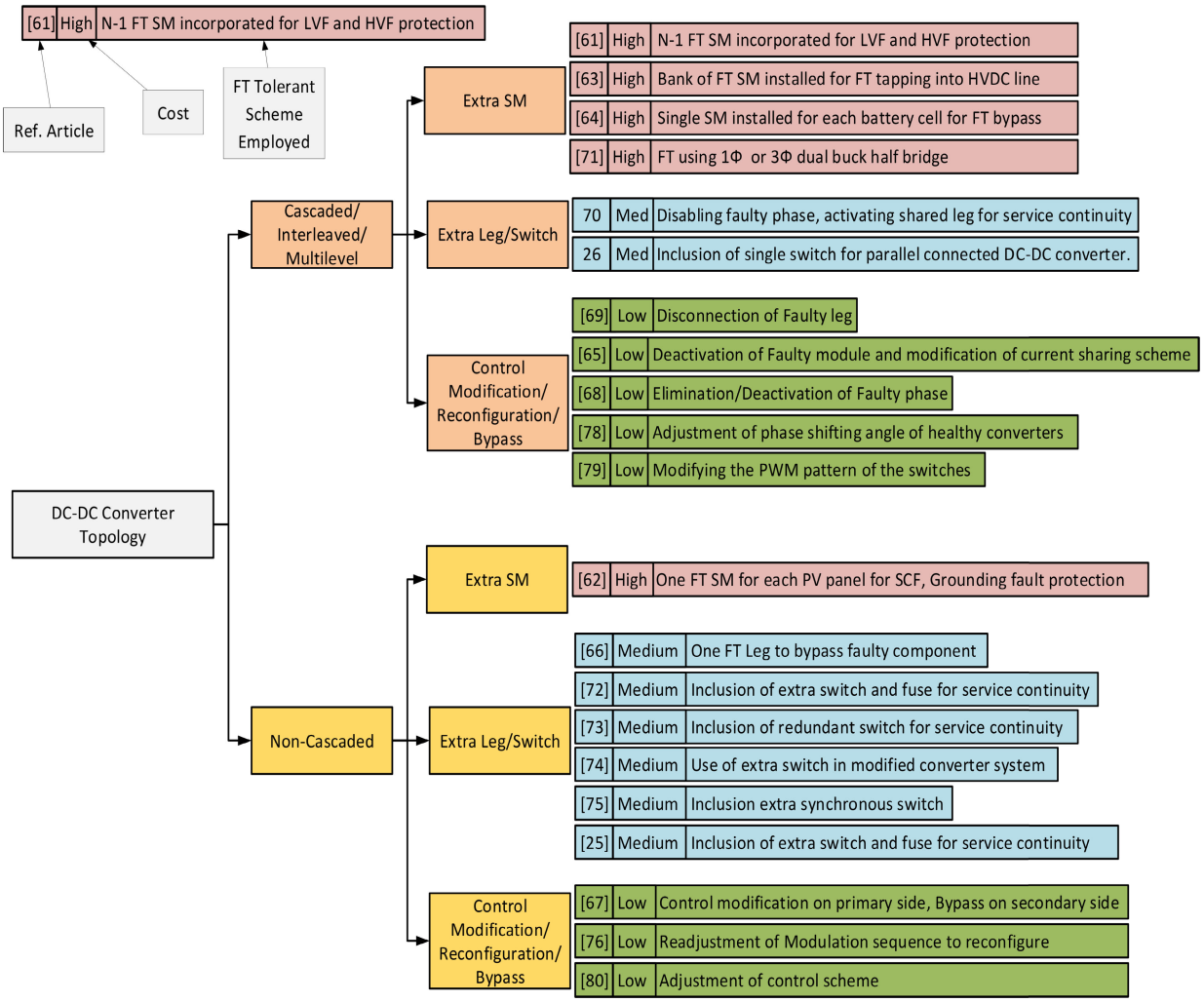

FIGURE 41. FT scheme selection guide.

The remedial actions first electrically isolate the faulty component, and then, reconfigure the converter by using a suitable fault tolerant control strategy. Several efficient converter topologies have been introduced along with more efficient control schemes. In some cases, service continuity is ensured by providing redundancy in which some components are duplicated or added in the basic converter structure. Whereas, in some cases reconfiguration of converter hardware is carried by changing the control sequence. However, these strategies cannot be blindly incorporated to any converter. Careful selection of a FT scheme must be carried out depending upon the converter topology. Some of the consequence of implementing a FT in DC-DC converters is higher conduction and switch loses, reduced power output and high ripples in the output. In this review, several cascaded and non-cascaded topologies have been introduced along with their control schemes. Based on the Table 4, appropriate FT schemes can be identified for specific converters. In this table, a large number of FT schemes have been presented, where each of these methods have its own strengths and shortcomings. In order to help identify a proper FT scheme for the desired converter, a guideline for selection of proper FT technique based on the converter type and budget limitations has been prepared. This section provides a general guideline on how to make a proper selection of FT technique in DC-DC converters as presented in Figure 41. The first step in the selection of FT technique is to identify the converter type. Since redundancy is a critical factor in any FT scheme, initial converter classification is carried out in term of cascaded and non-cascaded converter. The motivation behind this classification is that cascaded, parallel or interleaved topologies lend themselves effectively to a FT scheme as they already have components to be utilized as redundant components. Cascaded converter uses its modularity advantageously by introducing the idea of redundancy of a complete module. Therefore it is highly probable that modular cascaded converters are more fault tolerant and ensure service continuity as compared to non cascaded converters. Further classification of FT technique is made on the bases of cost expenditure. There are three major techniques used for incorporating FT mechanism namely (1) Introduction of extra sub-module(SM), (2) Introduction of extra leg/phase or switch, and (3) Modification of control

TABLE 4. Comparison table for fault tolerant techniques.

Ref.	Topology	Fault Type	Fault Detection Time	Fault indicating Signatures	Fault Tolerant Scheme	Service Continuity	Cost
[61]	Cascaded DC-DC Con.	SCF	$< 120\mu$sec	I_{PV}	Extra SM	LVF Partial, HVF No	High
[62]	PV Mod. with Buck-Boost Con.	SCF, Partial shading	NA	V_{PV}	Extra SM	Yes	High
[63]	Modular Resonant DC-DC Converter with VSC	SCF	NA	HVDC line current increase, HVDC line voltage drop	Extra SM	No	High
[64]	CDCDC	SW SCF	FD=5ms FT=12ms	NA	Extra SM for each Bat. Cell	Yes	High
[65]	Interleaved boost Con.	OCF/SCF	$< T_S$	I_L, I_{OUT}	Adj. of Control Scheme	Yes	Low
[66]	Bidirectional Boost converter with 3φ inverter	OCF	200ms	NA	Extra leg	Yes	Med
[67]	DAB with CPS Control	OCF	FT in ms Range	NA	Cont. adj. Pri. side Arm bypass Sec. side	Primary side 3/4 Power Secondary side 7/9 Power	Low
[68]	6φ IBC	OCF	$< T_S$	I_L	Bypass of Faulty Leg	Yes	Low
[69]	Reconfigurable Boost with NPC Con.	OCF/SCF	NA	NA	Disconnection of Faulty Leg	Yes	Low
[70]	5 Channel 3L-NPC	OCF	FT in ms Range	Normalized Phase Current Average Value	Extra Shared Leg	50% of Power	Med
[71]	3φ Dual Buck VSI	OCF/SCF	0.5ms	NA	Redundant Dual Buck Half Bridge with couple Inductor	Yes	High
[72]	Buck,Boost Buck-Boost	SCF	FD 2.5μs FT 10ms	V_{GS}, V_{DS}, GDS	Extra Switch	Yes	Med
[73]	Buck,Boost Buck-Boost	OCF	3μsec – 130μsec	I_L, GDS	Extra Switch	Yes	Med
[74]	Modified Boost Con.	OCF	FT in ms Range	Fault Detection Index	Extra Switch	80% of Power	Med
[75]	Two Stage Buck Buck-Boost Con.	OCF	10μsec	NA	Extra Switch	Yes	Med
[25]	Single ended DC-DC Con.	OCF/SCF	$< T_S$	I_L	Extra Switch	Yes	Med
[26]	Parallel connected DC-DC Con.	OCF/SCF	$< T_S$	I_L	Extra Switch	Yes	Med
[76]	FB-SMC	OCF/SCF	NA	NA	SW Reconfiguration	8% Less Efficient	Low
[78]	PCSAB	OCF	< 2Ts	I_{OUT}	Phase Adjustment of Healthy Module	Yes 100%Power for Type1fualt	Low
[79]	Buck with Multimode single leg Con.	OCF	$< 1.5T_S$	Slope of I_L, GDS	PWM Reconfiguration Relocation of Diodes	Yes	Low
[80]	M5LT DAB Con. with PDPWM	OCF/SCF	0.5ms	NA	Adj. of Cntrl Scheme	Yes with Reduced V Quality	Low

strategy. FT SM is a collection of components that is used to detect, bypass, and protect the converter form fault and allow continuation of operation. Figure 39 is the representation of two types of SM discussed in [63] for a FT tapping scheme. Remote renewable energy resources are connected to HVDC line using DC-DC converter and these SM. Type A and Type B are used on the positive and negative side of the converter respectively. An alternate method to express the redundancies of FT converters is in the form $N + M$, $2N$ and $3N$ redundant converter. In this form N represent the minimum number of working converter modules that are either in parallel or cascaded form and M represent the minimum number of backup devices associated with each module. Use of extra leg or a redundant switch is also a well proven technique to incorporate FT in converter systems. Here again, the specific use of redundant leg or switch is based on the type of converter. Under most of the cases, single ended converter topologies utilized redundant switch technique where a parallel switch is added to converter and upon primary switch fault, the redundant switch comes into action. Figure 40 show the use of redundant switch in [25] where FT operation was initiated upon detection of SCF and OCF. In case of SCF detection the reconfiguration process was initiated by isolating the switch using fast fuse in series with the main switch and activating the redundant switch. Similarly Figure 33 demonstrates the use extra leg for FT operation in [66]. The most cost effective FT strategy is the reconfiguration or adjustment of control scheme where by a careful adjustment of control pulses to the gate of the remaining healthy switches, service continuity can be ensured albeit with low or degraded performance. Along with that, a bypass mechanism is ensured to isolate the faulty module from rest of the converter. As evident, FT schemes that utilize extra SM will implicate more financial burden as compared to other FT techniques due to larger number of extra components used whereas FT based of control reconfiguration provides a more cost effective solution.

VI. CONCLUSION

This paper gives a comprehensive review of the up-to-date fault mode analysis, fault diagnosis signals, algorithms, and fault tolerant control in various DC-DC Converter topologies. Firstly, by the illustration of various component damages, typical faults in dc-dc converters have been classified into catastrophic faults and parametric or soft faults. Then, three main types of fault diagnosis techniques, including hardware based, model based, and historic data based methods have been discussed with the analysis of key characteristics. Main fault signatures, such as current, voltage, and other special signatures, including the ambient temperature, capacitor case temperature, radiated EMI, and its harmonics have been reviewed. For hardware based fault diagnostic techniques, latest researches have been systematically reviewed for the first time from different perspectives, including topology, faulty configuration, fault type, isolation type, fault detection time, fault indicating signature, sensors, control platform, fault detection time, operation mode of converters, and cost. Similarly, a comprehensive comparison of main model based fault diagnosis techniques has been presented. After that, main fault tolerant schemes have been discussed from the aspects of fault detection, fault isolation, and fault compensation. Main fault tolerant techniques have been reviewed in terms of the converter topology, fault type, fault detection time, fault indicating signature, fault tolerant scheme, service continuity, and cost. This article covers important and latest technologies on fault diagnosis and fault tolerant schemes, which can provide a comprehensive, up to date overview and comparison of available technologies on fault diagnosis and fault tolerance in tabular form with more converter parameter for an in-depth analysis. Moreover, for the first time more detailed classification of fault diagnosis techniques is carried out and examples specific to these techniques are discussed, tabulated and categorized in a coherent manner.

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