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2-D Design of Double Gate Schottky Tunnel MOSFET for High-Performance Use in Analog/RF Applications

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ABSTRACT In this work, a new structure of Schottky tunneling MOSFET has been designed and simulated. The proposed device structure uses floating gates and dual material main gates to counter short channel effects and to improve RF/Analog figures of merit for low power design applications. The use of floating gates modulates the Schottky barrier width, hence improves the ON state and RF/Analog figures of merit performance of the proposed device in comparison to a conventional device. A significantly high I_{ON} (1.231×10^{-4}A/μm) and I_{ON}/I_{OFF} ratio (2.52×10^{5}) is achieved in the proposed ST-MOSFET in comparison to conventional ST-MOSFET having I_{ON} (1×10^{-7}A/μm) and I_{ON}/I_{OFF} ratio (1×10^{2}). It has been observed that there is more than 100 times improvement in cutoff frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP), gain transconductance frequency product (GTFP), gain bandwidth product (GBP) and max oscillation frequency (f_{max}) in comparison to conventional ST-MOSFET. In addition, there are reductions of 98% and 33.33% in switching ON and OFF delays respectively in the proposed device-based inverter circuit in comparison to conventional ST-MOSFET based inverter circuit. Furthermore, the proposed ST-MOSFET device does not require any highly doped regions, hence does not have any doping related issues.

INDEX TERMS 2D devices, multiple gate devices, RF applications, Schottky MOSFET, tunnel FET.

I. INTRODUCTION

The performance characteristics of MOSFET are directly related to the device dimensions. The down scaling in MOS device dimensions has shown a significant improvement in speed, packaging density, power dissipation and cost [1], [2].However, the scaling of such devices below 32/22nm technology node becomes difficult due to gate oxide tunneling, parasitic and short channel effects (SCE) [3]. Various solutions have been put forward to overcome such difficulties [4], [5]. Planar structure with an ultra-thin body SOI MOSFET, tri-gate structures etc. have suppressed short channel effects [6]; however it has significantly increased the source drain (S/D) series resistance and fabrication complexity. The metal S/D has provided a solution to series resistance problem [7]–[11] and has reduced off leakage current [9], [10] but degrades the ON state performance. However, the ON state performance can be improved by using dopant segregated layer (DSL) [12], [13] but incorporating a thin doped layer results in the complexity in device fabrication process and increases the thermal budget. The SB-MOSFET [14], [15] has been considered as an alternative solution, but controlling such a device below 32nm technology node to have high performance is very difficult. Hence, an alternative solution is needed.

In this paper, we propose and simulate a new structure of double gate with dual material gates and floating gate ST-MOSFET to address above-mentioned issues. The main objective of this study is to improve the ON current, ON-OFF ratio and sub-threshold slope by incorporating the floating gates, dual material gates and HfO_2 as the dielectric. The floating gates of length 3 nm have been incorporated above

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and below the channel adjacent to the source contact; the top and bottom gates consist of dual material. The use of floating gates with metal work function engineering [16]–[20] induces the charge carrier concentration below the floating gates in the silicon film. This increase in charge carrier concentration modulates the barrier width and enhances the performance of the proposed device. The incorporation of floating gates and dual material main gates not only makes it immune to short channel and parasitic effects, but it also improves the other device parameters such as transconductance, cut-off frequency and other analog/RF Figures of merit of the proposed device. The high dielectric constant oxide (HfO_2) is responsible for high gate capacitance which in turn leads to higher I_{ON}/I_{OFF} in the proposed device. Using high-k oxide gives the flexibility of using thicker oxide layer for the same value of capacitance which reduces gate leakage current caused due to direct tunneling of electrons through the oxide. This also reduces the power dissipation. Besides, the sub-threshold slope is improved with the increase in dielectric constant. The performance of the proposed device named as "Double Gate Material Floating Gate Schottky Tunnelling MOSFET (DGM-FG-ST-MOSFET)" and conventional ST-MOSFET has been analyzed by using Atlas device simulator [21] at a gate length of 20nm. All the performance characteristics of both the devices have been compared and it has been observed that the proposed DGM-FG-ST-MOSFET outperforms the conventional ST-MOSFET in all performance measuring parameters. The ON current (I_{ON}) and I_{ON}/I_{OFF} of the proposed DGM-FG-ST-MOSFET have both increased by $\sim 10^3$ times to that of the conventional device. Moreover, the cut-off frequency (f_T) has been obtained by doing the ac analysis of both the devices and it has been observed that f_T of the proposed device has increased by 5×10^2 times as compared to the conventional device. A dopant segregation layer (DSL) has been realized by using a low metal work function floating gates in the proposed device. Therefore, since no conventional doping technique has been used to realize DSL, it is thus expected that proposed device is free from random doping fluctuations (RDF) and doping control issues and most importantly, it can be processed at low temperature.

This paper is organized as follows. Section II introduces physical structure used in the simulation. Section III provides comparative results and analysis. The paper is concluded in Section IV.

II. MODELS AND METHODS

The proposed device structure consists of dual gate material and a floating gate with appropriate work functions. The ATLAS device simulator [21] has been used to carry out simulations of conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET. The different models used in the simulations are drift diffusion, conmob, fldmob, srh, fermi, consrh and ust. The drift diffusion model mainly governs transport of carriers in the channel. The tunneling across the metal semiconductor junction is captured by Universal

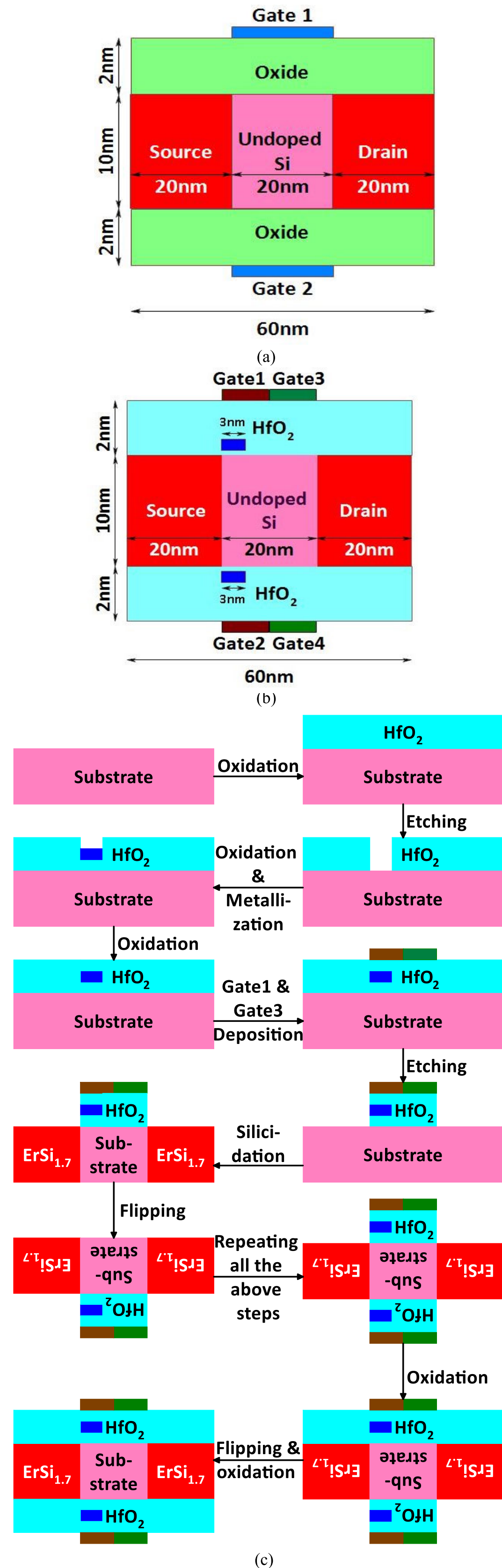


FIGURE 1. Schematic diagrams of (a) Conventional ST-MOSFET (b) Proposed DGM-FG-ST-MOSFET (c) Process flow of proposed DGM-FG-ST-MOSFET.

Schottky tunneling model, fldmob and conmob mobility models have been used to capture the field and concentration dependent mobilities.

The schematics of DGM-FG-ST-MOSFET and conventional ST-MOSFET studied in this work are shown in Fig. 1. In DGM-FG-ST-MOSFET structure, the floating gates of length (L_{FG} = 3nm) and low metal work function are incorporated under gate 1 and below gate 2 inside the oxide at distance 0.1 nm away from silicon material adjacent to the source. The main gate has been split into two gates with two different metal work functions of 4.9 eV and 4.65 eV. Moreover, the oxide used in the proposed device is Hafnium oxide of 2nm thickness. The simulation parameters used in the study are listed in the Table 1.

TABLE 1. Simulation parameters of conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET.

Parameters	Conventional ST-MOSFET	Proposed DGM-FG-ST-MOSFET
Gate length (nm)	20	20
Length of channel (nm)	20	20
Substrate thickness (nm)	8	8
Oxide thickness (nm)	2	2
Length of floating gate (nm)	NA	3
Oxide thickness under floating gates (nm)	NA	0.2
Oxide	SiO_2	HfO_2
Dielectric constant of oxide	3.9	22
Band gap of oxide (eV)	9	5.8
Doping concentration of channel (cm^{-3})	1×10^{16}	1×10^{16}
Work function of Source/Drain(eV)	4.5	4.5
Gate1 & Gate2 work function (eV)	4.72 (Rhodium)	4.9 (Platinum)
Gate3 & Gate4 work function (eV)	NA	4.65 (Copper)
Floating gate work function (eV)	NA	2.5(Barium)

Fig.1(c) shows the process flow for the fabrication of proposed DGM-FG-ST-MOSFET. The process flow starts with the deposition of Hafnium oxide (HfO_2) on the Si wafer. HfO_2 thin films are deposited on Si substrates by remote plasma Atomic Layer Deposition (RP-ALD) followed by a rapid thermal annealing [22]. This step is followed by etching the oxide layer for the deposition of floating gate. The oxidation is again done in the pit upto 0.1 nm followed by the floating gate implantation in the area above the oxide layer and then the oxidation is done on the floating gate. After that, gate 1 and gate 2 deposition is done followed by the etching of oxide and silicidation using $ErSi_{1.7}$ [23]. $ErSi_{1.7}$ thin films are grown on Si substrate in <100> orientation [24]. $ErSi_{1.7}$ is used as source and drain because of its low Schottky barrier height. In the next step, the device is flipped and all the above steps are repeated. At last, the oxidation is done and the oxide is etched out from the gates.

III. RESULTS AND ANALYSIS

The energy band diagrams of conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET in OFF and ON-states are shown in Figs. 2(a) and 2(b) respectively. The improvement in performance characteristics of the proposed DGM-FG-ST-MOSFET can be understood from the energy band diagram of both the devices. By using floating gates of work function 2.5eV in the proposed device, high electric field is created which is responsible for the reduction of barrier height. Moreover, a significant increase in quantum band to band tunneling is evident from the energy band diagram of the proposed device. Due to these effects, a prominent increase in ON current and I_{ON}/I_{OFF} ratio of the proposed DGM-FG-ST-MOSFET is observed.

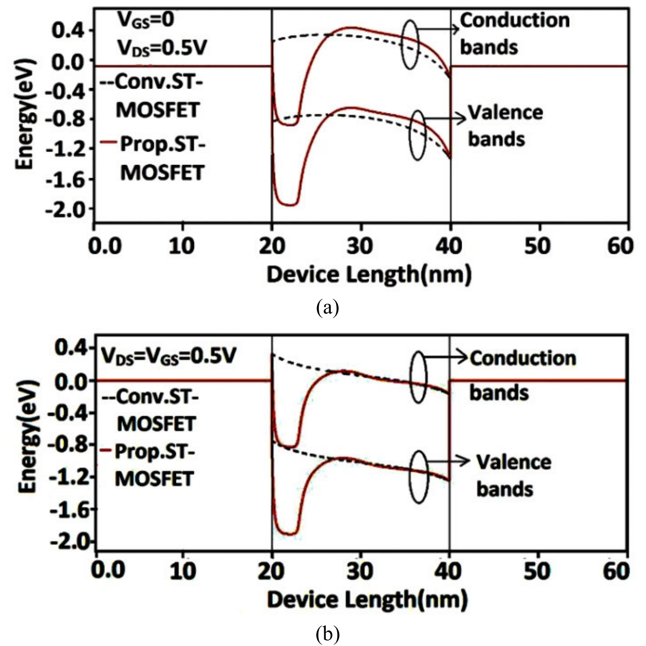


FIGURE 2. Energy band diagrams of: (a) conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET in OFF state, and (b) conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET in ON state.

The transfer characteristics of both conventional ST-MOSFET and proposed DGM-FG-ST-MOSFET are shown in Fig. 3. It is clear from the graph that there is significant improvement in I_{ON}, I_{ON}/I_{OFF} and Sub-threshold Swing (SS) of the proposed device. The I_{ON} (calculated at $V_{DS} = V_{GS} = 0.5V$) of the proposed device is 1.231×10^{-4}A/μm and that of the conventional device is 6.247×10^{-8}A/μm. Also, the I_{OFF} (calculated at $V_{DS} = 0.5V$, $V_{GS} = 0V$) of the proposed device is 4.88×10^{-10}A/μm and that of the conventional

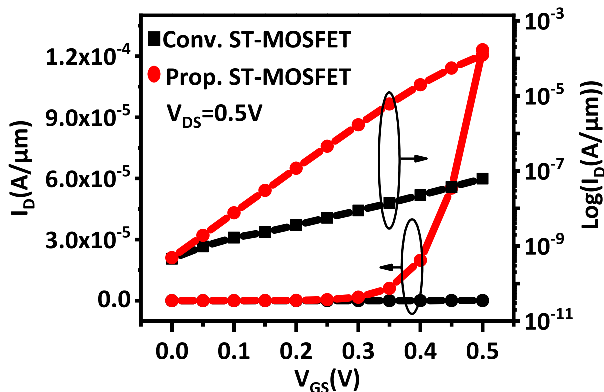
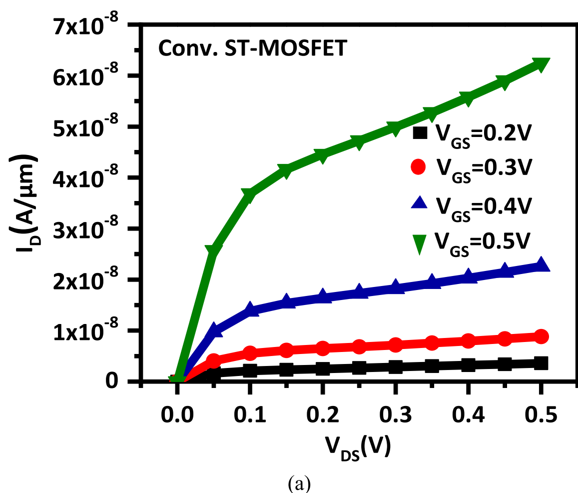
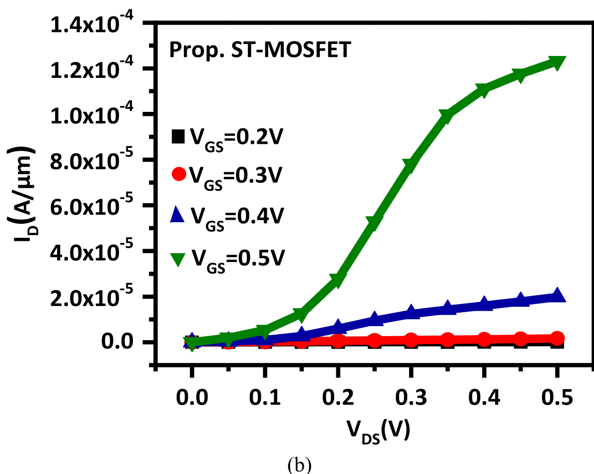


FIGURE 3. Transfer characteristics of the proposed DGM-FG-ST-MOSFET and conventional ST-MOSFET.



(a)



(b)

FIGURE 4. Output characteristics of (a) Conventional ST-MOSFET and (b) Proposed DGM-FG-ST-MOSFET.

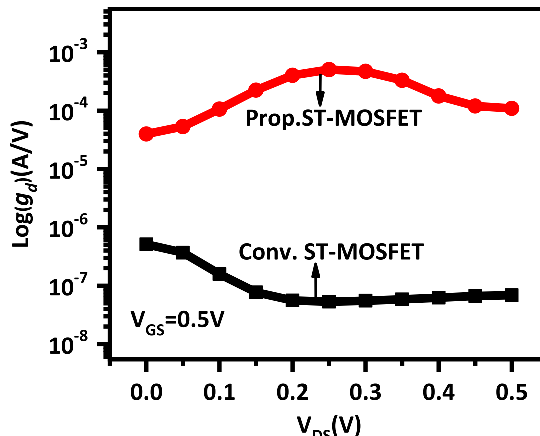


FIGURE 5. Logarithmic form of output conductance (g_D) of the proposed DGM-FG-ST-MOSFET and Conventional ST-MOSFET.

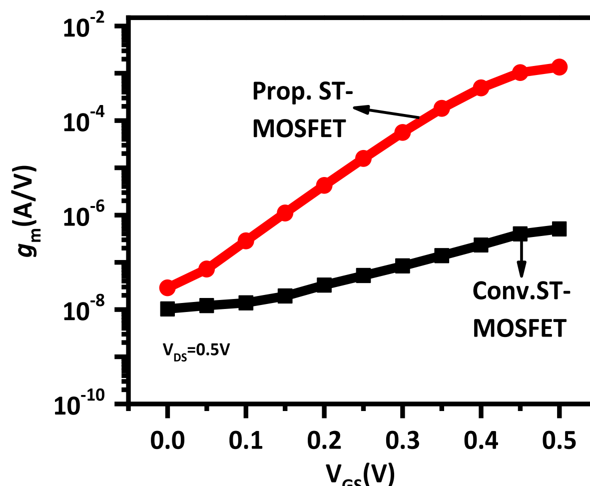


FIGURE 6. Transconductance (gm) of the proposed DGM-FG-ST-MOSFET and Conventional ST-MOSFET.

device is 4.559×10^{-10}A/μm. Hence, the I_{ON}/I_{OFF} ratio of the proposed and the conventional device is 2.52×10^5 and 1.37×10^2, respectively. The enhancement in I_{ON} and reduction in I_{OFF} in the proposed device can be attributed to low metal work function floating gates and dual-material main gates. The use of low metal work function floating gates modulates the barrier width at the source side and enhances the ON state performance, whereas the use of dual material main gate improves the OFF state performance of the proposed device as can be seen from Fig. 2(a). There is 45.5% decrease in SS of the proposed device (83.34mV/decade) to that of the conventional one (153mV/decade). The decrease in SS is because of the use of HfO_2 in the proposed device.

The output characteristics of the proposed and the conventional devices are shown in Fig. 4. In the output characteristics of the proposed DGM-FG-ST-MOSFET, the drain current shows some dependence on drain voltage because of the channel length modulation effect. Moreover, the output characteristics show offset for lower drain voltage due to the asymmetry in the proposed device.

The output conductance (g_d) of both the conventional ST-MOSFET and the proposed DGM-FG-ST-MOSFET is shown in Fig. 5. It is clear from the graph that the proposed DGM-FG-ST-MOSFET has higher output conductance than the conventional ST-MOSFET. The higher conductance is due to higher driving capability of the proposed device. The higher driving capability is because of the use of floating gates in the proposed device.

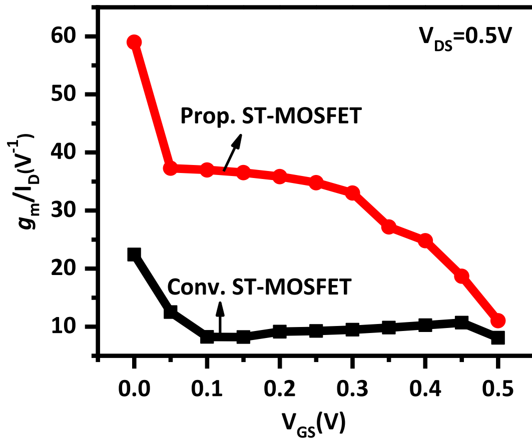
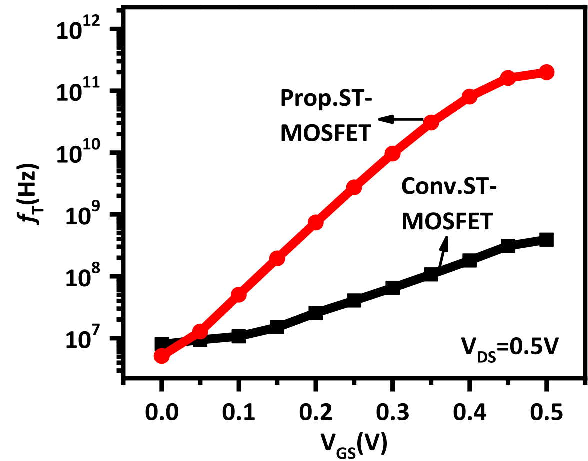


FIGURE 7. Transconductance generation factor (g_m/I_D) vs. V_{GS}.



(a)

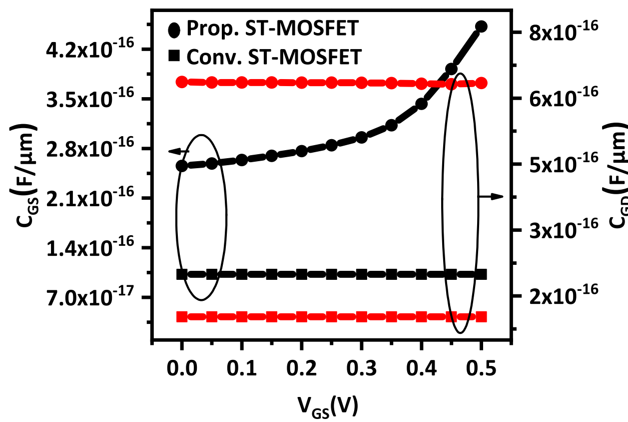
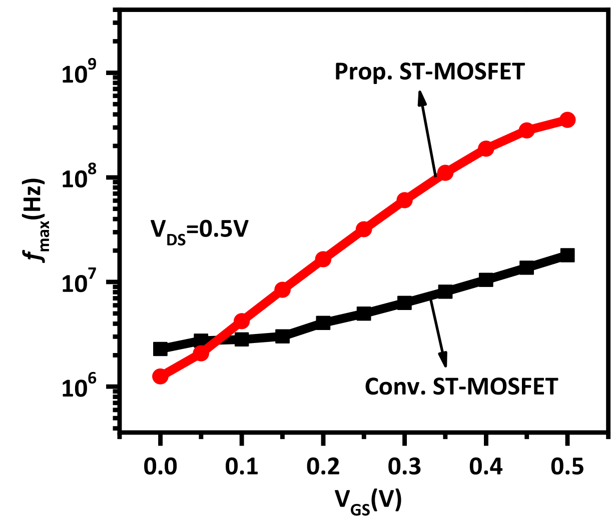


FIGURE 8. Variation of C_{GS} and C_{GD} with respect to V_{GS} of the proposed DGM-FG-ST-MOSFET and Conventional ST-MOSFET.



(b)

FIGURE 10. Variation of (a) Cut-off frequency (f_T), and (b) maximum oscillation frequency (f_{max}) of the proposed DGM-FG-ST-MOSFET and conventional ST-MOSFET w.r.t. V_{GS}.

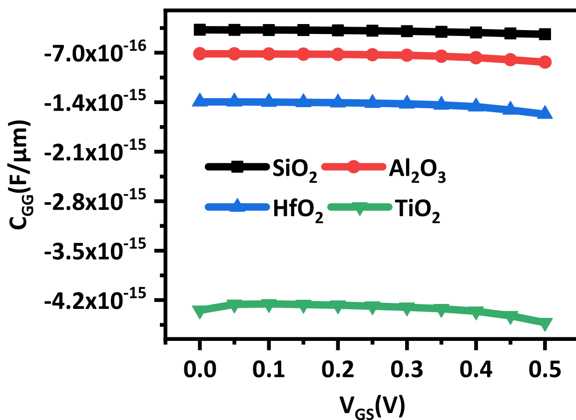


FIGURE 9. Variation of C_{GG} with respect to V_{GS} for different oxides of proposed DGM-FG-ST-MOSFET.

The variation of transconductance (g_m) with gate voltage (V_{GS}) is shown in Fig. 6. It is evident from Fig. 6 that higher g_m is achieved in the proposed DGM-FG-ST-MOSFET in comparison to the conventional ST-MOSFET. A significantly higher transconductance of the proposed device is attributed to the efficient modulation of the source channel barrier due to low work function of floating gates and higher oxide capacitance because of high dielectric constant oxide.

The transconductance generation factor (g_m/I_D) signifies how efficiently current (I_D) is used to obtain a particular value of transconductance (g_m). The benefit of high transconductance generation factor is to realize the circuits operating at low voltage. g_m/I_D is the change in transconductance with a change in drain current. It should be high so that higher ac power gain could be extracted from the input dc power [25]. Fig. 7 shows that the proposed ST-MOSFET has large transconductance generation factor (g_m/I_D) in comparison to the conventional ST-MOSFET. The efficient barrier modulation, because of using floating gates and HfO_2 as dielectric, results in the higher transconductance in the proposed device.

Fig. 8 shows the variation of gate source capacitance (C_{GS}) and gate drain capacitance (C_{GD}) with respect to gate voltage of both conventional and proposed ST-MOSFET. It has been observed that higher value of capacitance in the proposed device is due to the use of high dielectric constant material. The variation of $C_{GG}(= C_{GS} + C_{GD})$ with respect to gate

voltage for different oxides has been shown in Fig. 9. It can be seen that as the dielectric constant of oxide increases, the capacitance also increases.

The higher transconductance in the proposed ST-MOSFET leads to the improvement in cut-off frequency (f_T) in comparison to the conventional ST-MOSFET. Fig. 10(a) shows the cut-off frequency plot of the proposed DGM-FG-ST-MOSFET (1.988×10^{11}Hz) is $\sim 10^3$ times higher than the conventional ST-MOSFET (3.92×10^8Hz). The cut-off frequency has been calculated by using equation (1)

$$f_T = \frac{g_m}{2 * \pi * C_{gg}} \tag{1}$$

where C_{gg} is the total gate capacitance.

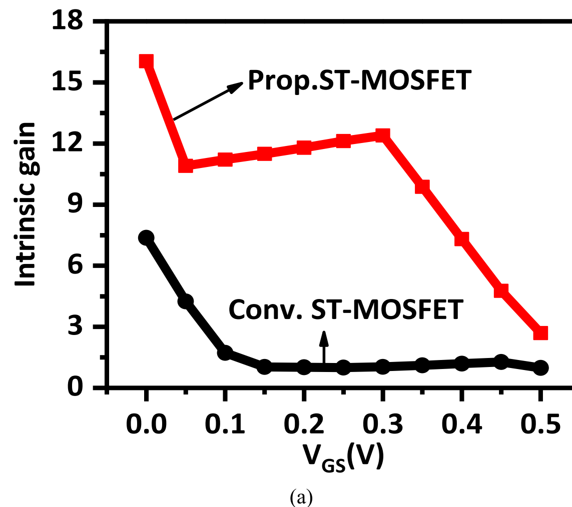
The maximum oscillation frequency of both the devices has been plotted as shown in Fig. 10(b) by using equation (2).

$$f_{max} = f_0 \times \sqrt{\frac{|y_{21} - y_{12}|^2}{4[(y_{11}y_{22}) - (y_{12}y_{21})]}} \tag{2}$$

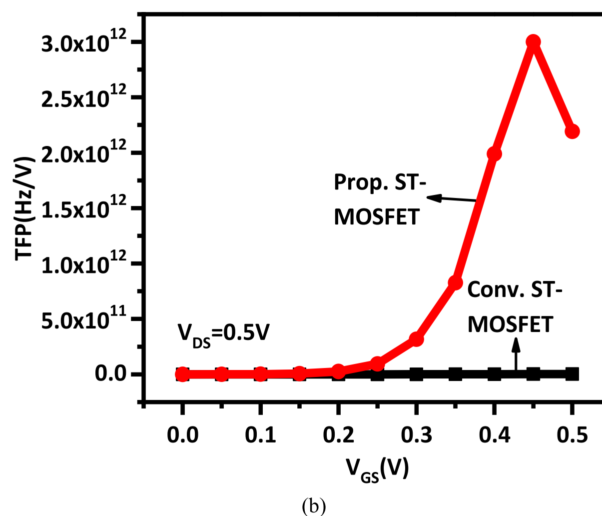
where f_0 is the small signal frequency used in the ac analyses of both the devices, which has been taken as 10^6Hz. f_{max} is the maximum frequency of oscillation calculated by using Y-matrix. The maximum oscillation frequencies of both the devices have been compared and it is evident from the Fig. 10(b) that f_{max} of the proposed DGM-FG-ST-MOSFET (3.5×10^8Hz) is 10 times higher than the conventional ST-MOSFET(1.8×10^7Hz).

To analyze the analog/RF performance for the proposed DGM-FG-MOSFET and conventional ST-MOSFET, it is necessary to have knowledge of intrinsic gain, transconductance frequency product (TFP), gain frequency product (GFP), gain transconductance frequency product (GTFP) and gain bandwidth product (GBP). These parameters are significantly higher in the proposed DGM-FG-ST-MOSFET as compared to conventional ST-MOSFET. All these parameters are plotted against gate voltage and shown in Figs. 11 and 12. The intrinsic gain is higher in the proposed DGM-FG-ST-MOSFET because of the higher value of transconductance in the proposed device. The TFP (product of g_m/I_d and f_T) represents a compromise between power and bandwidth and is used for moderate to high-speed designs. GTFP includes both the switching speed and gain of the device and is very useful for circuit design. The higher TFP and gain in the proposed device has resulted in higher GTFP. GFP is also plotted against gate voltage for both the devices and the proposed ST-MOSFET outperforms because of high gain and high cut off frequency. GBP is higher in the proposed ST-MOSFET as compared to the conventional ST-MOSFET because of the significant improvement in g_m of the proposed device.

The use of floating gates plays important role for obtaining higher performance from the proposed device. The transfer and the output characteristics of the proposed DGM-FG-ST-MOSFET with the variation of work function of floating gates is shown in Fig. 13. Besides this, the different performance measuring parameters such as I_{ON}, I_{ON}/I_{OFF}, f_T



(a)



(b)

FIGURE 11. Variation of (a) Intrinsic gain (b) TFP of the proposed DGM-FG-ST-MOSFET and conventional ST-MOSFET w.r.t. V_{GS}.

and SS show dependence on the metal work-function used on the floating gates. Fig. 13 shows all these parameters degrade with the increase in work function of floating gates.

To explain the role of floating gates in the performance of the proposed device, the following notations are made.

$$\varphi_s = \text{work function of channel(Si)}$$
$$\varphi_f = \text{work function of floating gate}$$
$$\Delta\varphi = \varphi_s - \varphi_f$$

The significant performance characteristics at minimum φ_f can be attributed to the maximum $\Delta\varphi$ which is responsible for the highest electric field. As electric field decreases with the decrease in $\Delta\varphi$, the concentration of charge carriers under floating gates decreases which in turn increases the Schottky barrier width, thereby degrading the performance characteristics of the proposed device.

The effect of change in the length of floating gates on the transfer characteristics, SS and threshold voltage has been shown in Fig. 14. It has been observed that the optimum results are obtained at the length of 3nm. The length of

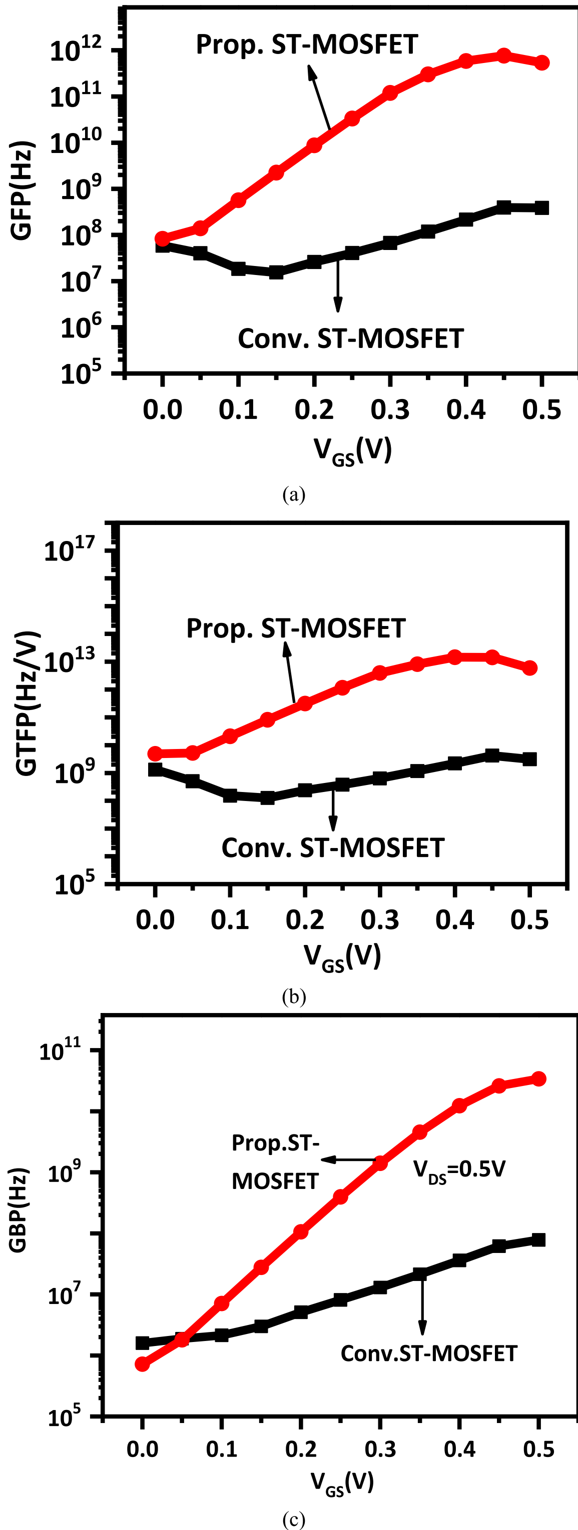


FIGURE 12. Variation of (a) GFP (b) GTFP (c) GBP, of the proposed DGM-FG-ST-MOSFET and conventional ST-MOSFET w.r.t. V_{GS}.

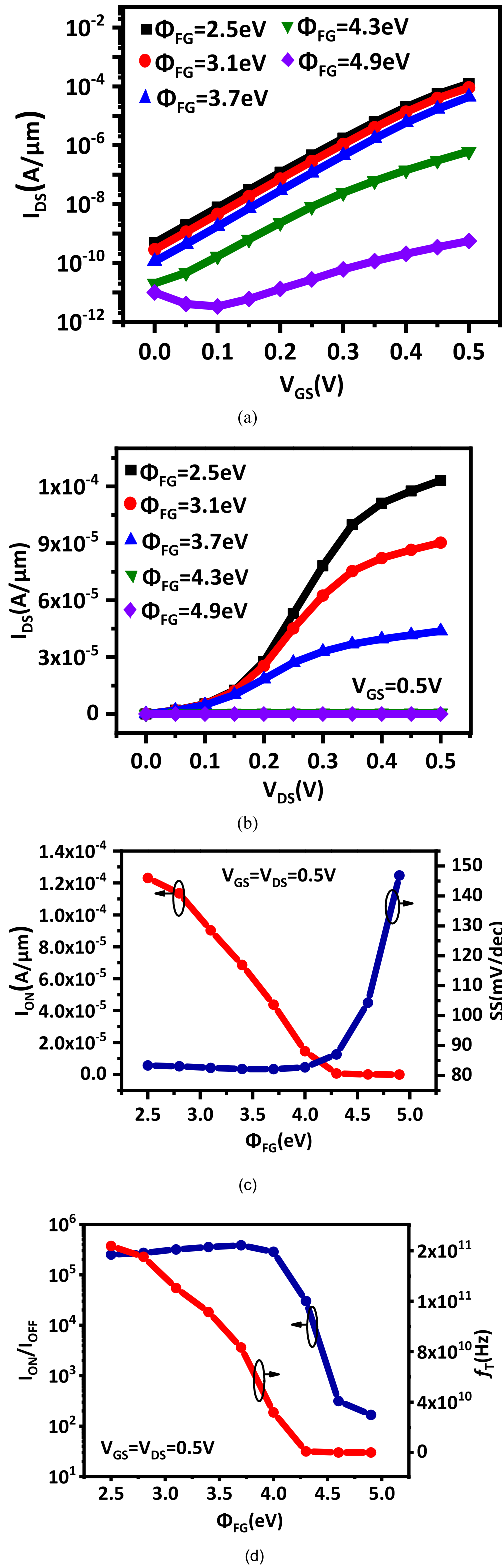


FIGURE 13. Effect of floating gate work function (Φ_{FG}) on (a) Transfer characteristics (b) Output characteristics (c) I_{ON} and SS (d) On-off current ratio and cut-off frequency of the proposed DGM-FG-ST-MOSFET.

floating gates makes a significant effect on the performance of the proposed device. As can be seen from the Fig. 14 (b) that with increase in length of floating gates, SS degrades and threshold voltage decreases. This is because the increase in length of floating gates leads to the increase of charge carriers in the un-doped silicon film and smaller length of Silicon film is left for the gate voltage to be inverted.

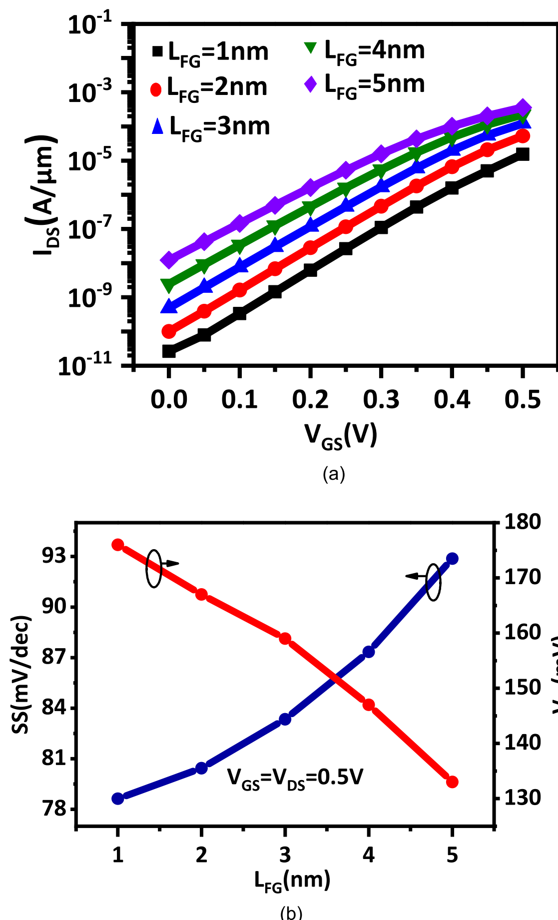


FIGURE 14. Effect of floating gate length on (a) Transfer characteristics (b) SS and threshold voltage(V_{th}) of the proposed DGM-FG-ST-MOSFET.

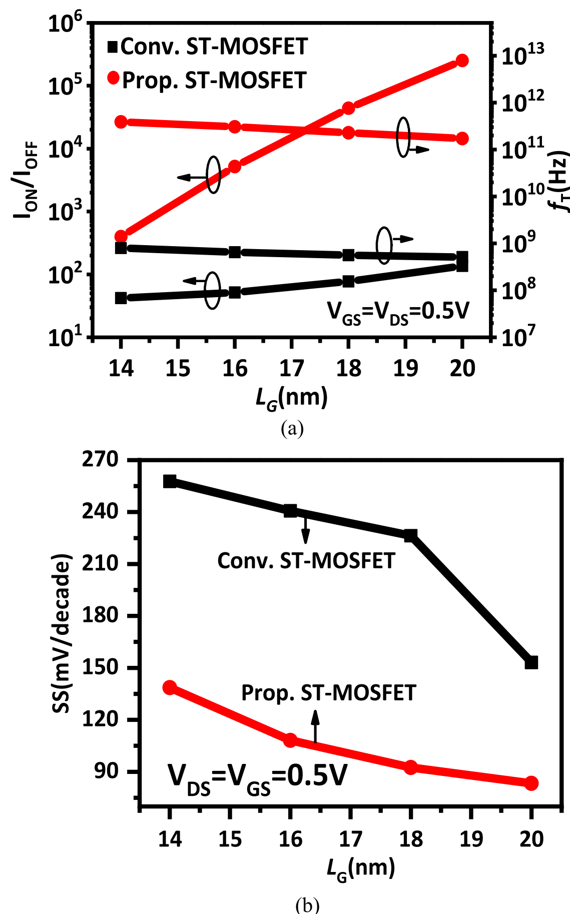


FIGURE 15. Effect of gate length on the (a) On-Off ratio and cut off frequency (b) SS of both the devices.

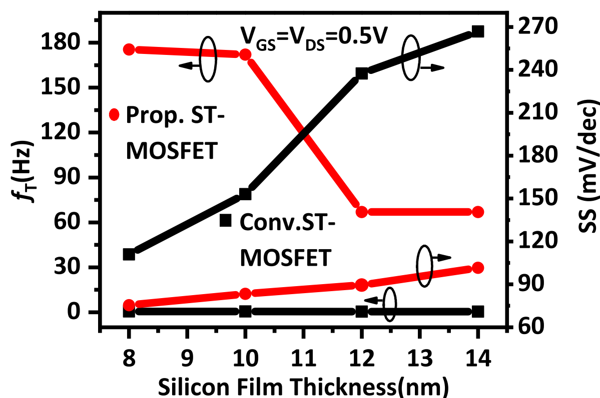


FIGURE 16. Effect of silicon film thickness on f_T and SS.

Fig. 15 shows the effect of channel length on the performance of the DGM-FG-ST-MOSFET and conventional ST-MOSFET. With decrease in channel length, I_{ON}/I_{OFF}, and SS degrades but these parameters are better in the proposed device than in conventional device at each gate length. Thus, the severity of the short channel effects is very less in the proposed device as compared to the conventional device due to the use of dual gate material, which keeps barrier height higher in the OFF state as seen from the Fig. 2(a).

Fig. 16 shows the effect of silicon film thickness on cut off frequency (f_T) and SS of both the devices. As can be seen from the graph that cut-off frequency of the proposed device decreases with increase in the thickness of silicon film and sub-threshold slope degrades (increases) with increase in silicon film thickness. However, in conventional ST-MOSFET, it is highly degraded. The increase in SS with the increase in silicon film thickness can be justified by equation (3) [26].

$$SS \approx \frac{KT}{q} \ln(10) \left(1 - e^{\frac{-d}{\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox}}}}\right) \tag{3}$$

Fig. 17 shows the variation of SS of both the devices with respect to the temperature. It is observed from the figure that with an increase in temperature, SS degrades (increases). SS increases linearly with the increase in temperature which can be justified by equation (3), however, the increase is seen less in the proposed device. For a good turn on characteristics of the device, SS should be as small as possible which can be obtained at lower operating temperatures.

Fig. 18 shows the variation of SS and On-Off current ratio of the proposed DGM-FG-ST-MOSFET with respect to the oxide. It is observed from the figure that with the increase in dielectric constant of the oxide, I_{ON}/I_{OFF} and SS improve.

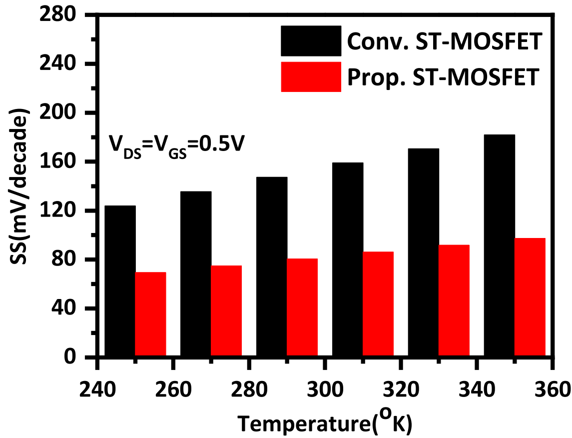


FIGURE 17. Variation of SS of both the devices with respect to temperature.

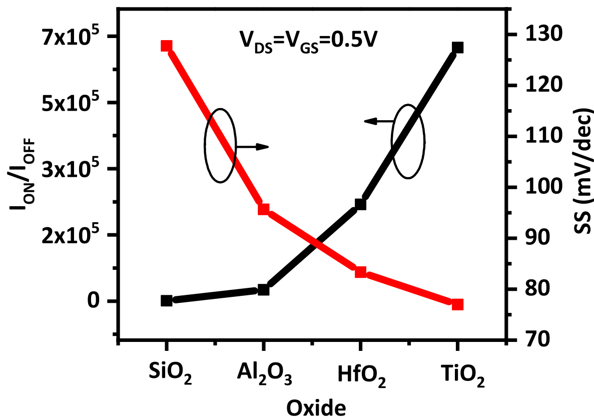


FIGURE 18. Variation of On-off current and SS of the proposed DGM-FG-ST-MOSFET with respect to oxide.

Higher I_{ON}/I_{OFF} can be attributed to high gate capacitance because of the high dielectric constant and the decrease in SS with the increase in dielectric constant can be governed by the equation (3). Also, it has been observed that with the increase in dielectric constant, there is negligible decrease in I_{ON} and f_T of the proposed device.

Fig. 19 shows the comparison of transfer characteristics of single material (SM) gates with oxide and dual material (DM) with HfO_2 of the proposed DGM-FG-ST-MOSFET. The result shows that there is a reduction of Off current with the combination of dual material gates and HfO_2. Fig. 20 (a) and (b) show the optimization of the work function of gates of the proposed DGM-FG-ST-MOSFET. It has been observed that the optimum results are obtained at gate1, gate2 work function ($\Phi_{G1} = \Phi_{G2}$) equal to 4.9eV and gate3, gate4 work function ($\Phi_{G3} = \Phi_{G4}$) equal to 4.65eV.

The performance of the proposed device was compared with the previously published works on SB-MOSFET and is summarized in Table 2. From the table, it can be seen that the proposed device presents comparatively a very good performance considering the employed gate length and supply voltages. The references [12], [14] and [15] use the same supply voltage but higher gate length (50 nm); nevertheless,

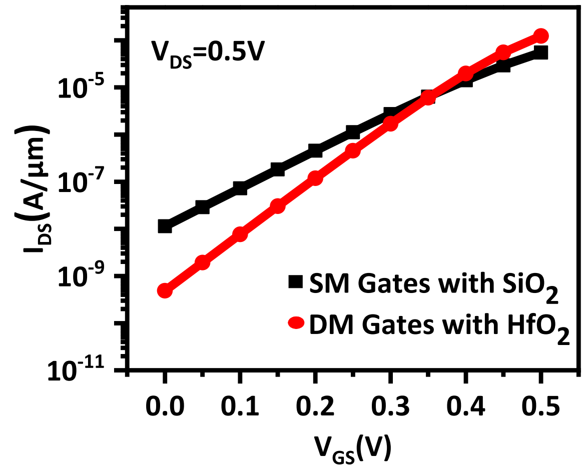
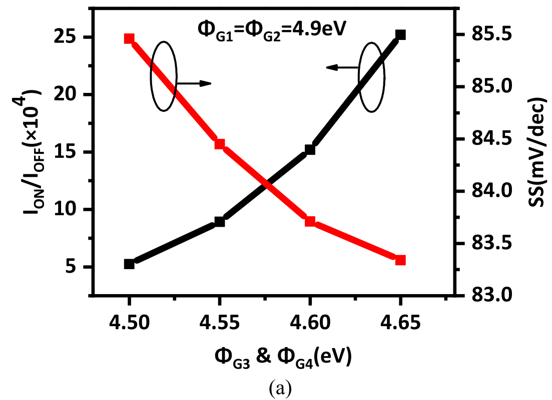


FIGURE 19. Comparison of transfer characteristics of Single material(SM) gates with SiO_2 and Dual material(DM) gates with HfO_2 of the Proposed DGM-FG-ST-MOSFET.



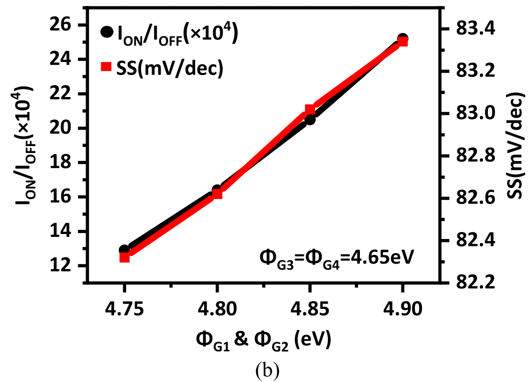


FIGURE 20. Optimization of the work function of gates of the proposed DGM-FG-ST-MOSFET.

the proposed device still has a comparable performance even after employing the gate length of only 20nm. The work in [27]–[29] use higher gate length and supply voltages, but still the performance of the proposed device is better. The work in [30] uses same gate length and higher supply voltages, but still the performance of the device is comparable. Even the SS performance of the proposed device is better. The work in [31] seems to offer better performance but the authors have carefully chosen the supply voltages to achieve this performance. If the same scheme is applied to the

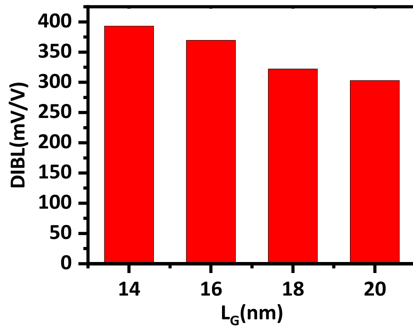


FIGURE 21. Analysis of DIBL of the proposed DGM-FG-ST-MOSFET.

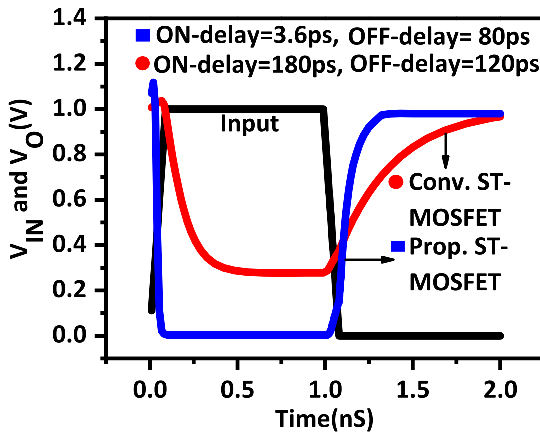
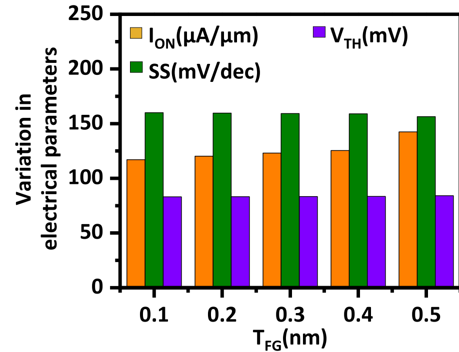


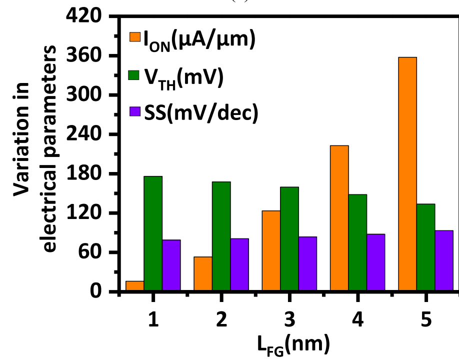
FIGURE 22. Transient analysis of the proposed and conventional ST-MOSFET.

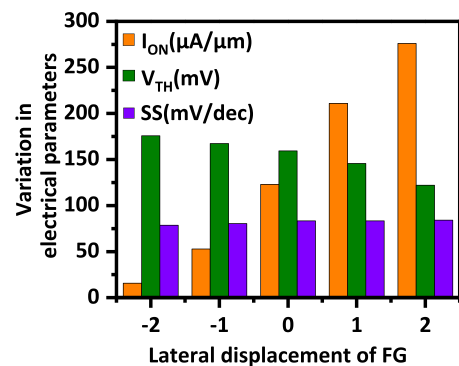
proposed device, the device shall offer much better performance than [31].

As the proposed device works on the lower technology node, one of the SCEs such as DIBL has been calculated and is shown in Fig. 21. It is clear from the Fig. 21 that as the node technology lowers, DIBL becomes prominent. The performance of DGM-FG-ST-MOSFET and conventional ST-MOSFET based inverter has been analyzed using mixed mode feature of ATLAS device simulator. Fig. 22 shows the transient analysis of both the device-based inverters. The delay is calculated and it has been observed that there is a reduction of 98% and 33.33% in switching ON and OFF delays respectively in the proposed device based inverter circuit in comparison to the conventional ST-MOSFET based inverter circuit. The smaller delay observed in the inverter designed using the proposed DGM-FG-ST-MOSFET as compared to the one designed using the conventional ST-MOSFET is because of the high driving capability of the proposed ST-MOSFET.

The process-induced variations in the proposed DGM-FG-ST-MOSFET after the introduction of floating gates is analysed by estimating the change in the electrical parameters such as ON current, Subthreshold Swing and threshold voltage by the change in the physical parameters of the floating gates. The variation has been calculated by changing one of the physical parameters of the floating gates, keeping all the other physical parameters of the device constant. It has been observed that there is slight variation in the electrical parameters of the proposed device with the change in the physical parameters of the floating gates as can be depicted from Fig. 23.







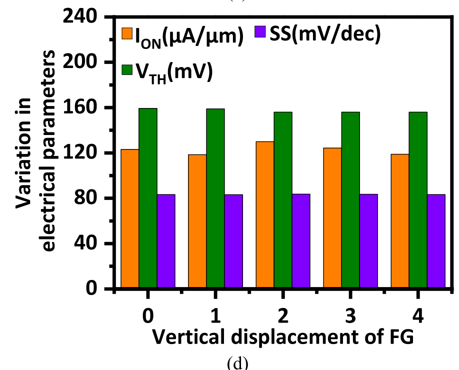


FIGURE 23. Variation in electrical parameters with change in physical parameters such as (a) Thickness (b) Length (c) Lateral displacement (d) Vertical displacement of floating gates(FG) of the proposed DGM-FG-ST-MOSFET.

TABLE 2. Comparison of our work with the previous published works.

Ref.	L_G (nm)	V_{DS}/V_{GS} (V/V)	I_{ON} ($\mu A/\mu m$)	I_{ON}/I_{OFF}	f_T (GHz)	SS(mV/dec)
[12]	50	0.5/0.5	*0.2*	9.3×10^4	230	74.5
[14]	50	0.5/0.5	*45*	2.6×10^5	200	72.53
[15]	50	0.5/0.5	*1200*	10^6	290	77.76
[27]	30	-1.1/-2.6	*314*	1870	280	117
[28]	50	1.0/2.0	*319*	3.19×10^6	-	125
[29]	500	1.2/5.0	*900*	10^5	-	180
[30] (WSE)	20	0.6/1.4	*2380*	1.85×10^6	-	96.5
[30] (WSDE)	20	0.6/1.4	*2040*	5.6×10^8	-	93.3
[31]	10	0.1/2.0	-	10^8	-	66
This work	**20**	**0.5/0.5**	**123.1**	$\mathbf{2.52\times10^5}$	**198.8**	**83.34**

IV. CONCLUSION

In this paper, a double gate structure of Schottky tunneling MOSFET has been designed and simulated. The proposed device structure uses gate engineering technique to enhance the performance of the proposed device. The use of floating gates modulates the Schottky barrier width, hence improves the ON state and RF/Analog figures of merit performance of the proposed device in comparison to the conventional device. The use of dual material main gates improves the short channel performance and the OFF-state behavior of the proposed device in comparison to conventional device. Further, there is a significant improvement in I_{ON}, I_{OFF}, SS, f_T, f_{max}, etc. in the proposed device. In addition to that, the doping related issues like random dopant fluctuations and doping control issues are absent in the proposed device, since a dopant segregation layer has been realized by using floating gates. In future, the proposed device can be analyzed for the detection of various biomolecules. In addition, as we have seen that the proposed device has good analog figures of merit and hence will be used in various RF applications.

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