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An Extended Multilayer Thermal Model for Multichip IGBT Modules Considering Thermal Aging

MOHSEN AKBARI[1], (Student Member, IEEE), MOHAMMAD TAVAKOLI BINA[1], (Senior Member, IEEE), AMIR SAJJAD BAHMAN[2], (Senior Member, IEEE), BAHMAN ESKANDARI[3], (Member, IEEE), EDRIS POURESMAEIL[3], (Senior Member, IEEE), AND FREDE BLAABJERG[2], (Fellow, IEEE)

[1]Faculty of Electrical Engineering, K. N. Toosi Univer sity of Technology, Tehran 16317-14191, Iran
[2]Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark
[3]Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland

Corresponding author: Edris Pouresmaeil (edris.pouresmaeil@aalto.fi)

ABSTRACT An accurate and real-time knowledge of temperatures in insulated-gate bipolar transistor modules is crucial for reliability analysis and thermal management of power electronic converters. For this purpose, this paper establishes an integrated thermal equivalent circuit model comprising self-heating thermal impedances and cross-heating thermal impedances to provide a temperature profile of the junction and solder joints during various operations and in the case of thermal aging. The thermal resistance and capacitance parameters of the thermal impedances are characterized in terms of different electro-thermal operating conditions and solder joints aging conditions with the help of three-dimensional finite element simulations. Also, the effect of the heatsink, which brings an uneven heat transfer coefficient distribution at the module baseplate, is investigated and modeled into the thermal impedances. The introduced thermal model can work even if the conditions change simultaneously. The accuracy of the model is verified by experiments and finite element simulations, all of which agree with negligible error unlike thermal models given in the datasheet and fixed-parameter thermal models.

INDEX TERMS Cross-heating effect, IGBTs, layers temperature, operating conditions, solder fatigue, thermal impedance model.

I. INTRODUCTION

Accurate knowledge of temperatures in insulated gate-bipolar transistor (IGBT) modules is of substantial importance to reduce thermal stress, prevent over-temperature [1], and estimate the remaining useful lifetime [2] that could be applicable to power electronic devices in a real-time basis. To reach the internal temperatures of insulated-gate bipolar transistor (IGBT) modules, numerical methods such as finite element (FE) [3] and finite difference (FD) [4] methods are known to be able to thermally analyze complex geometries with high accuracy, thanks to powerful computers. However, the numerical methods demand a huge amount of computational cost, especially when the complex geometries are exposed to long-term load profiles. To solve this problem, thermal impedance models or thermal equivalent circuits (TECs), which are time-efficient and easily integrated into various circuit simulators such as PLECS [5], are introduced. TECs are categorized into Foster and Cauer types based on a few lumps of thermal resistance (R_{th}) - thermal capacitances (C_{th}) cell. The Cauer model is constructed with the help of device structural information; whereas the Foster model is mathematically fitted to temperature responses obtained from experiments/numerical methods.

The accuracy of the TECs has been challenged in the literature and efforts have been made to improve it; for example, [6] proposed to subdivide thick layers into a few sublayers. However, the time-domain TECs have limits to correctly predict the device temperatures, especially when considering the cooling conditions outside the device. The main reason is due to an incorrect heat behavior flowing out of the device [7]. Generally, the Foster-type TEC has

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no filtering effect of the injected power loss (heat), and it results in a large error at the beginning of the transient temperatures, especially in fast-varying loading conditions [8]. In contrast, the Cauer-type TEC has an over-filtering effect on the injected power loss, and thereby the temperatures might have a larger error in steady-state [7].

Some frequency-domain approaches are proposed to overcome the limits in the existing time-domain TECs. For example, [9] represented the Fourier series of the time-domain power loss of the IGBT module and characterized the frequency-domain thermal impedance from the frequency response of the manufacturer based Foster-type TEC. [8] characterized the dynamical thermal behavior of an IGBT module by a linear time-invariant (LTI) system, whose frequency response is obtained by applying the fast Fourier transform to the data of the time derivative of transient thermal impedance. [7] proposed a thermal model established by characterizing the slope variation from the bode diagram of the Foster-type TEC of the IGBT module for the filtering of power loss. [10] directly measured the cross-heating effect caused among the devices using a discrete Fourier transform-based technique; then, to reduce the computational complexity, it fitted a digital infinite impedance response (IIR) filter to each cross-heating characteristic. However, the direct use of frequency-domain characteristics is computationally intensive, especially for a long power profile, since the calculation of forward and inverse Fourier transforms are required.

The above efforts achieve the highest accuracy only under specific operating conditions. In other words, by changing the operating conditions under which the thermal model parameters are extracted, the model accuracy decreases. The operating conditions are ambient temperature, power loss or heat, and cooling rate. In efforts to solve this weakness, [11] proposed the use of multiple TECs for multiple cooling rates, however, it has no high efficiency for unstudied cooling rates and also it does not investigate other types of operating conditions, e.g., ambient temperature and power dissipation. Also, [12] introduced a TEC-based Kalman filter obtained from thermo-sensitive electrical parameter (TSEP) measurements; however, TSEP evaluation methods are limited in practice by, e.g., complex and high-cost additional circuitry, the introduction of degradation in the power converter performance, and questioned measurement correlation with the maximum temperature of the chip [13]. In [14], the authors demonstrated that either power loss or heat transfer coefficient (*htc*) could affect the self-heating behavior of the closest layer to the exposed boundary. However, the model could lead to errors in the temperature estimates because of simplifying the cooling system effect to a uniform *htc* distribution and ignoring the temperature dependency of thermal properties of the direct bonded copper (DBC) ceramic. Although [15] introduced a new method for modeling the real heatsink effect, it still uses an equivalent uniform *htc*, which is not realistic in practice.

As another drawback of present TECs, a detailed investigation of the effect of the operating conditions on cross-heating thermal impedances has been neglected; whereas cross-heating effects exist in any multichip modules and their severity affects the temperature distribution within the modules.

The accuracy of TECs drastically reduces over time due to changing of lumped elements that originate from the thermal fatigue of solder joints. To cover this defect, [16] proposed to add a variable Rth in series with the TEC of the fresh module to compensate for the baseplate solder fatigue. Also, [17]–[20] all employed a temperature gradient of the baseplate ∇T_{bp} for monitoring of the health status of the baseplate solder. Then, once a change is detected in the gradient, the junction temperature T_j gets measured with TSEPs to recalculate total R_{th} from junction to baseplate [17], or to recalculate RC parameters of Foster model for the whole module [18], or to recalculate RC parameters of Cauer model for the baseplate solder and its two adjacent material layers [19]. Furthermore, [20] presented new mathematical relations to recalculate the Cauer model parameters only for the aged chip solder layer. However, the impact of fatigue caused in both chip and baseplate solder layers on the self-heating and cross-heating behaviors within all material layers still needs precise considerations.

Since the effect of 3-D heat dissipation within material layers is typically reflected in the Foster model (Fig. 1) in comparison to the 1-D heat dissipation assumed in the Cauer model, the Foster model has higher accuracy and has become more popular than the Cauer model among researchers and designers. Therefore, in this paper, a Foster-type model is established with the help of FE simulations.

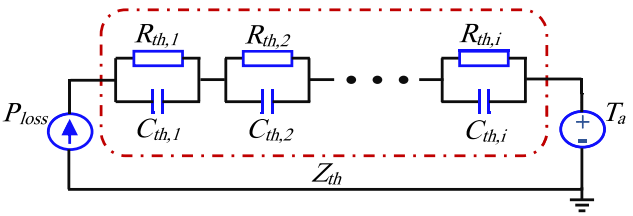


FIGURE 1. Typical Foster network for modeling of a power module and ambient.

To verify the performance of the introduced TEC, thermography measurements from a power cycling test setup are employed. The device under test is the IFS75B12N3E4_B31 [21], six-pack IGBT module, 1200 V, 75 A from Infineon.

This paper is organized as follows: The structure of the IGBT module and the FE simulation environment are described in Section II, together with a detailed analysis of the *htc* distribution due to the thermal gradient in the heatsink. In Section III, the effect of different electro-thermal operating conditions and solder joints aging conditions on self-heating thermal impedances (STIs) and cross-heating thermal impedances (CTIs) are investigated through FE

simulations. Then, Section IV introduces a generic Foster model where the dependency of RC parameters to each of the conditions is mathematically presented. Finally, the TEC is validated by experiments and FE simulations under various conditions.

II. FINITE ELEMENT MODELING OF THE STUDIED CASE

A. CASE STUDY

As cross-sectionally shown in Fig. 2(a), the case under study includes a module (with various material layers) mounted on a horizontal rectangular-fin heatsink. The module comprises six IGBT chips and six free-wheeling diode (FWD) chips distributed on three separate DBC substrates as shown in Fig. 2(b) where the shown chip numbering is used in the following. In this paper, bond wires are ignored for simplification because of the low impact on the temperature distribution within the underlying material layers.

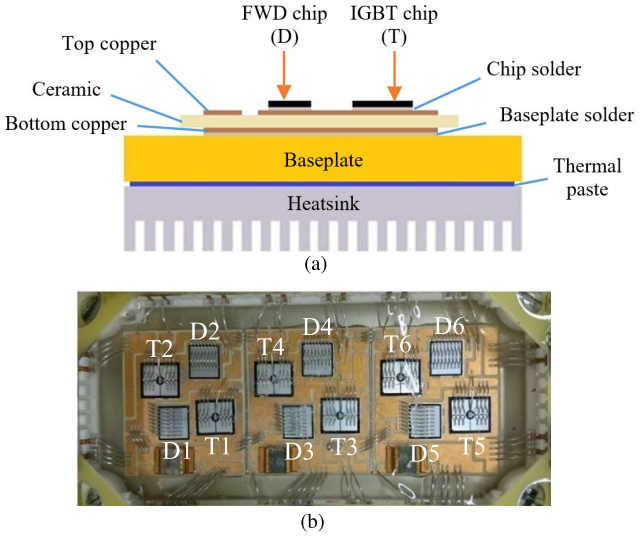


FIGURE 2. IGBT module under study: (a) cross-sectional view; (b) uncovered top view (IGBT and FWD chips are labeled as T and D, respectively).

It should be mentioned that because of the non-closure of detailed information by the IGBT module manufacturer, the material and thickness of the layers were determined by a scanning electron microscope (SEM) in the laboratory as given in Table 1. To make reliable results, SEM measurements were performed at five different locations of each layer, as shown in Fig. 3. Also, the thermal properties of the materials listed in Table 2 are found in [22]. It reveals that the thermal properties of Si and Al2O3 significantly change with temperature; whereas those of other materials are slightly affected.

The heatsink in this study has a length, width, and height of 35 cm, 30 cm, and 4.7 cm, respectively, with 30 parallel fins in total. To fill in air gaps between the heatsink and baseplate and as a result, to improve the heat transfer efficiency, some Deepcool thermal paste [23] is injected with an approximate thickness of 50 μm [24]. The thickness can be calculated according to [25].

TABLE 1. Determined physical characteristics of the components.

Component	Material	Density (kg/m^3)	Thickness (μm)
IGBT/FWD chip	Silicon (Si)	2329	120
Chip solder (s1)	SAC305	7800	100
Top copper	Copper (Cu)	8960	300
Ceramic	Alumina (Al_2O_3)	3965	380
Bottom copper	Copper (Cu)	8960	300
Baseplate solder (s2)	SAC305	7800	250
Baseplate	copper (Cu)	8960	3000
Thermal paste	-	5100	50
Heatsink	Aluminum 6063	2730	-

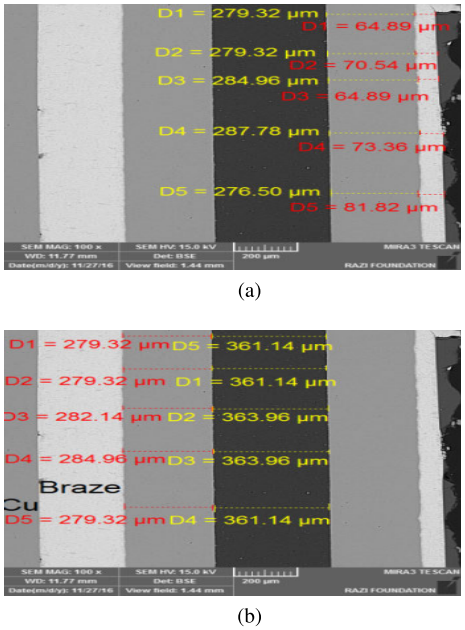


FIGURE 3. SEM images×100: (a) the thickness of chip solder (red color), and top copper (yellow color; (b) the thickness of Al2O3 ceramic (yellow color), and bottom copper (red color).

TABLE 2. Thermal properties of the system materials [22].

Material	Temperature (°C)	Conductivity (W/(m·K))	Specific capacity (J/(kg·K))
Si	25	148	705
	75	119	758
	125	99	788
	225	76	831
SAC305	all	57	220
Al2O3	25	37	785
	75	32	869
	125	27	942
	225	21	1077
Cu	all	401	385
Thermal paste	all	1.134	-
Al 6063	all	201	900

B. FINITE ELEMENT MODEL IMPLEMENTATION

To analyze thermal dynamics of the case study, a 3-D geometry as shown in Fig. 4 is established in COMSOL Multiphysics [26] where geometries are broken down into so-called

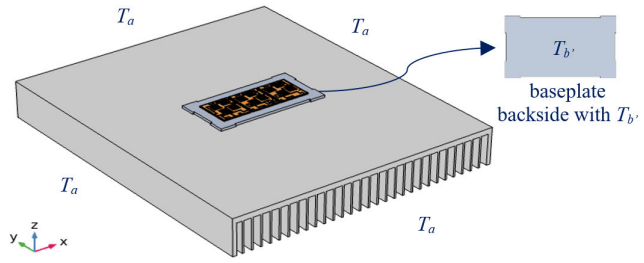


FIGURE 4. 3-D FE model for the whole system under study.

FE meshes. As the mesh is refined, the solution becomes accurate, however, the computational cost increases. Thus, an appropriate mesh density is chosen by making a trade-off between accuracy and simulation speed.

To simulate the cooling system in COMSOL, the heatsink is placed in a rectangular channel with insulated walls. The coolant flows into the heatsink at a constant inlet velocity and temperature. At the outlet, the normal stress is equal to the outlet pressure, and the tangential stress is canceled. The base surface of the heatsink receives heat flux from the IGBT module heat source, while the remaining exterior walls of the heat sink are considered adiabatic. The temperature field and heat flux are assumed continuous at the solid-fluid interface. The thermal conductivity, heat capacity, and density of the fluid are all temperature-dependent material properties. The fluid flow is modeled using the algebraic yPlus turbulence model [27], where the meshing and solver settings have been simplified, which also makes the model setup fast.

Mathematically, the *htc* value at different points of the baseplate can be evaluated by [28]

$$htc = \frac{q}{T_{b'} - T_a} \tag{1}$$

where q is the heat flux, $T_{b'}$ is the temperature at the baseplate backside, and T_a is the ambient temperature (see Fig. 4).

As an illustration, Fig. 5(a) presents the *htc* distribution at the baseplate when chip T2 is heated (single operation). It reveals that the *htc* distribution is severely non-uniform with a maximum value directly under the heated chip resulting from extra concentrated heat flux [14]. However, Fig. 5(b) shows that if multiple chips are in operation, the *htc* values under the heated chips would be smaller in comparison to a single operation. The reason can be explained by (1) where a higher temperature difference between ambient and baseplate is present, whereas the local heat flux is slightly changed. Moreover, it is found through FE simulations that for the given number and arrangement of on and off chips, the non-uniformity and values of *htc* distribution are independent of the coolant (or ambient) temperature and power loss; however, the *htc* values can be dependent on the flow rate and type of coolant. Once a chip is turned on (off), the *htc* distribution will change, and peak *htc* values will be decreased (increased).

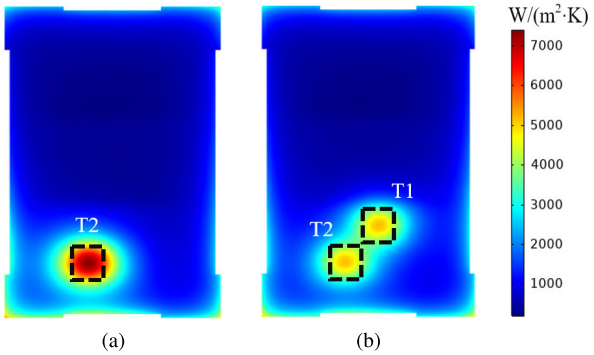


FIGURE 5. The *htc* distribution at the baseplate backside with P_{loss} = 100 W (per chip), T_a = 20 °C, and v_{air} = 6 m/s due to (a) heating of chip T2; (b) heating of chips T1 and T2.

C. SOLDER FATIGUE MODELING

Fatigue cracks are initiated and propagated at the corner of the solder joints and they develop local delamination, as shown in Fig. 6(a). If left untreated, the delamination can proceed towards the center as presented in Fig. 6(b) until the end-of-life of the IGBT module [29]. For the delaminated area of solder joints, the thermal conductivity, specific heat capacity, and density are defined as 1 W/(m·K), 820 J/(kg·K), and 2340 kg/m^3, respectively, as found in [30].

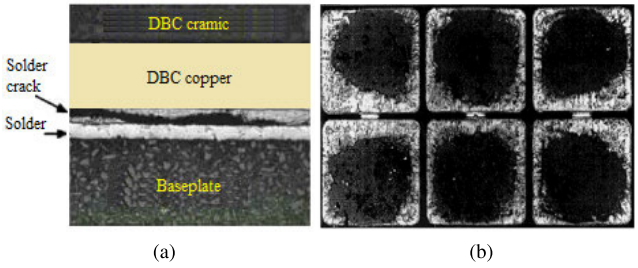


FIGURE 6. Cracking in baseplate solder joint: (a) cross-section of an IGBT module after 100 thermal cycles [31]; (b) delamination of the solder joint after 43,000 thermal cycles [32].

Generally, if the delamination initiates and/or progresses at the baseplate solder (del_{s2}), the degree of non-uniformity of temperature distribution on the baseplate will change [19]. However, based on FE simulations, any level of del_{s1} cannot do so. Therefore, a straightforward relationship between del_{s2} and the degree of non-uniformity of baseplate temperature is established to get the parameter k_{bp} as [19]

$$k_{bp} = \frac{R_{th,bp-chip}}{R_{th,bp-side}} = \frac{\frac{T_{bp-chip}-T_a}{P_{loss}}}{\frac{T_{bp-side}-T_a}{P_{loss}}} = \frac{T_{bp-chip}-T_a}{T_{bp-side}-T_a} \tag{2}$$

where $R_{th,bp-chip}$, and $R_{th,bp-side}$ are the equivalent thermal resistances obtained from two different locations on the baseplate to the ambient; one location is right beneath the chip center with $T_{bp-chip}$ and the other is right beneath the baseplate solder edge with $T_{bp-side}$.

It should be pointed out that k_{bp} is independent of electro-thermal operating conditions [19]. By running FE

simulations for various levels of del_{s2} and with the help of (2), a lookup table is predetermined to find del_{s2} according to k_{bp} in real-time applications, and then the obtained del_{s2} is applied to update the sensitive RC parameters of the TEC. This procedure does not require any T_j information. In the next step, V_{CE_ON} is measured to estimate $T_{j\_measurement}$ [33], and the TEC adapted to del_{s2} is employed to estimate T_{j_model}. The difference between these two temperatures indicates that the delamination of the chip solder (del_{s1}) has begun/progressed. In this case, del_{s1} is changed to set the sensitive RC parameters of the TEC so that T_{j_model} agrees exactly with $T_{j\_measurement}$. The accepted del_{s1} indicates the existing delamination level of the chip solder.

III. FACTORS AFFECTING THERMAL IMPEDANCES

Through transient FE simulations, thermal impedances at any desired location can be mathematically extracted by [34]

$$Z_{th}(t) = \frac{T_m(t) - T_{ref,m}(t)}{P_{loss}} \tag{3}$$

where t is the time, P_{loss} is the power loss, T_m is the temperature of the monitoring point m, and $T_{ref,m}$ is the reference temperature for the monitoring point m.

For multichip IGBT modules, it is assumed that the number of chips is k, we can extend (2) to [35]

$$\begin{vmatrix} T_1 \\ T_2 \\ \vdots \\ T_m \end{vmatrix} = \begin{vmatrix} Z_{ths}(1,1) & Z_{thc}(1,2) & \cdots & Z_{thc}(1,k) \\ Z_{thc}(2,1) & Z_{ths}(2,2) & \cdots & Z_{thc}(2,k) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{thc}(m,1) & Z_{thc}(m,2) & \cdots & Z_{thc}(m,k) \end{vmatrix} \begin{vmatrix} P_{loss,1} \\ P_{loss,2} \\ \vdots \\ P_{loss,k} \end{vmatrix} + \begin{vmatrix} T_{ref,1} \\ T_{ref,2} \\ \vdots \\ T_{ref,m} \end{vmatrix} \tag{4}$$

where, $Z_{ths}(m,k)$ and $Z_{thc}(m,k)$ are the STI and CTI between the point m and reference, respectively, when the chip k is heated.

In healthy IGBT modules, the highest temperature in layers (known as monitoring points) emerges under the center of a heated chip, although in the presence of the cross-heating effect it can be slightly moved. However, in the presence of solder delamination, those monitoring points are moved towards the delaminated area as shown for chip T2 in Fig. 7 where the baseplate solder under chip T2 is 70% delaminated. The nodes correspond to the critical locations, i.e., chip, chip solder, baseplate solder, and baseplate that are denoted by letters "j", "s1", "s2", and "bp" respectively, as shown in Fig. 7.

To extract STIs and CTIs, step responses obtained from the FE models are analyzed under conditions defined as follows. The ambient temperatures are considered as 20 °C (room condition), 75 °C (normal working condition), 125 °C (severe condition), and 150 °C (very critical condition). Very high ambient temperatures can be found in applications, such as tractions [36]. Also, the levels of del standing for "delamination" are defined as 0% (fresh solder), 20% (beginning of delamination), 50% (hard delamination), and 90% (end-of-life). Furthermore, the power losses of 10, 100, 200, and 300 W, and the coolant flow rates (v_c) of 1, 3, 6, and 10 m/s, as well as natural flow, are considered for the study. Thermal impedances under conditions other than the above can be estimated by a lookup table.

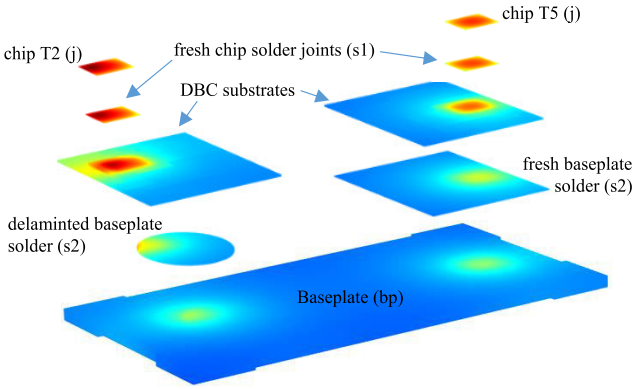


FIGURE 7. Typical temperature distribution inside the IGBT module due to the heating of chip T2 with the delaminated baseplate solder joint and due to the heating of chip T5 with the fresh baseplate solder joint.

With Intel i7 6700K and RAM 32GB desktop computer, each FE simulations take about 50 min to reach the equivalent *htc* in steady-state and about 20 min to derive only the desired transient thermal impedance curves under specific conditions. The post-processing to curve-fitting and finding the RC parameters of thermal impedances takes time depending on the skills of the researcher.

It is necessary to say that for chips placed on different DBC substrates, the temperature difference between the chips is marginal and the difference can be accepted by the industry in most of the applications [37]. Therefore, it is sufficient to derive the TEC only for a couple of IGBT/FWD chips and then to extend it to others.

The flowchart illustrated in Fig. 8 summarizes how to extract RC parameters of the TEC with the help of FE simulations and how to update them into different conditions.

A. FACTORS AFFECTING SELF-HEATING THERMAL IMPEDANCE

1) ELECTRO-THERMAL OPERATING CONDITIONS

Fig. 9 shows that the steay-sate STI between the baseplate and ambient $Z_{ths}(bp-a)$ decreases and reaches a steady-state soon with airflow rate, as expected. Furthermore, in [14], the impact of some electro-thermal operating conditions on the STI of the critical layers was studied. The authors concluded that any variation in power loss and/or fixed baseplate temperature could affect only the STI of the chip; whereas the STI of either baseplate or baseplate solder is influenced by only the equivalent *htc*. However, in the present research, we found that the STI of the baseplate solder is not influenced by the equivalent *htc* at all. Also, by considering the temperature-dependent thermal properties of the DBC

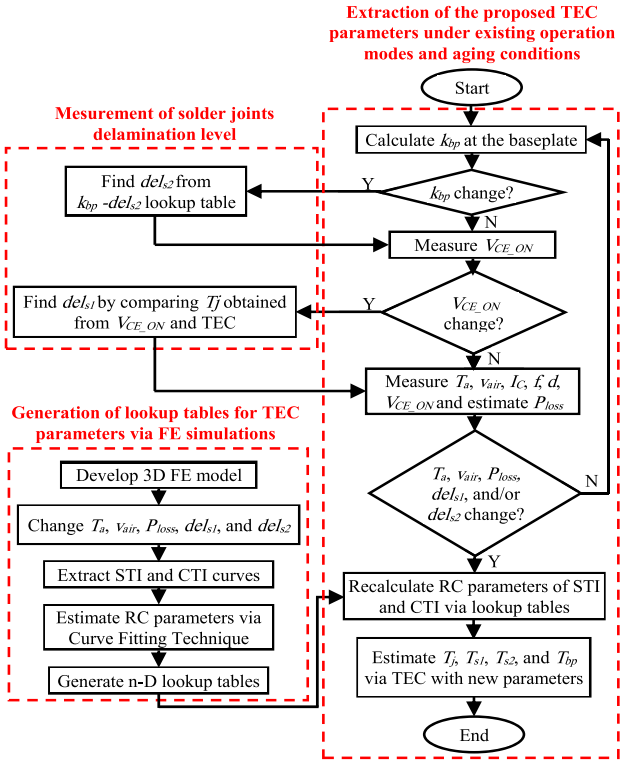


FIGURE 8. Flowchart of the proposed modeling method.

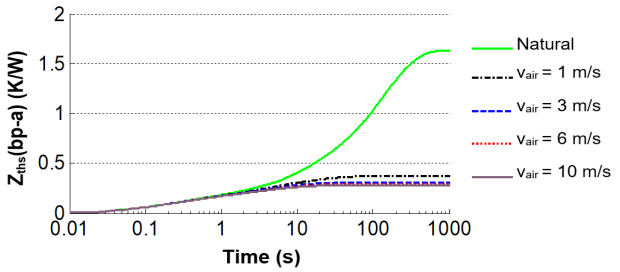


FIGURE 9. Calculated self-heating thermal impedance of $Z_{ths}(bp-a)$ at various flow rates of the air-cooled heatsink (v_{air} in m/s).

ceramic given in Table 2, we understood that the STI between chip solder and baseplate solder $Z_{ths}(s1-s2)$ dramatically increases with either power loss or ambient temperature (see Fig. 10 under airflow rate vair of 6 m/s, for example); whereas varying the coolant flow rate cannot affect $Z_{ths}(s1-s2)$ at all.

2) SOLDER FATIGUE

a: CHIP SOLDER DELAMINATION

Fig. 11(a) shows that if even a low level of del_{s1} is caused, the STI between junction and chip solder $Z_{ths}(j-s1)$ can grow dramatically. However, only large delamination levels (above 50%) can influence the STI of the underlying critical locations, i.e., the impedances $Z_{ths}(s1-s2)$ and $Z_{ths}(s2-bp)$ as shown in Figs. 11(b)-(c). Also, Fig. 11(d) shows that the impedance $Z_{ths}(bp-a)$ is not influenced by the del_{s1} level at all.

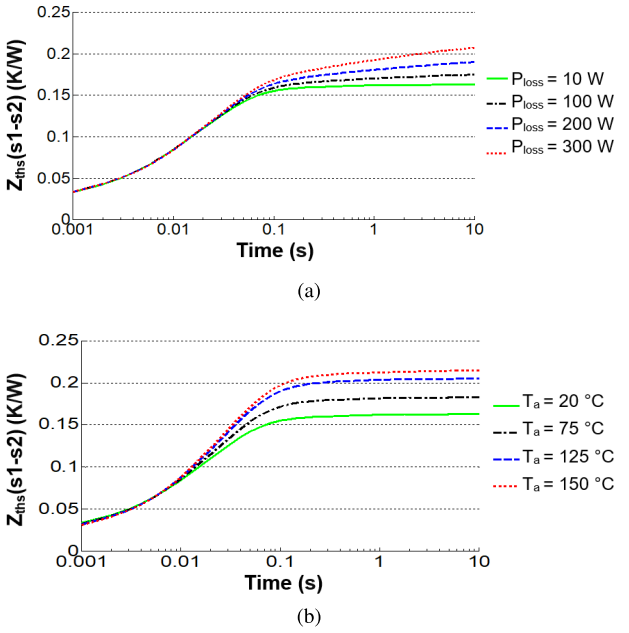


FIGURE 10. Calculated self-heating thermal impedance $Z_{ths}(s1-s2)$ under v_{air} = 6 m/s and del_{s1} = del_{s2} = 0%: (a) at various power losses with T_a = 20 °C; (b) at various ambient temperatures with P_{loss} = 10 W.

b: Baseplate solder delamination

Through FE simulations, we found that the impedance of any chip to its solder joint ($Z_{ths}(j-s1)$) remains almost unchanged in any level of the baseplate solder delamination (del_{s2}). The reason is likely due to the relatively long distance of the chip from the baseplate solder joint delaminated. Also, FE simulations revealed that any level of del_{s2} cannot influence the impedance $Z_{ths}(bp-a)$; because as shown before in Subsection II-C, under a single operation, the equivalent *htc* is not affected by the density of heat transferred towards the baseplate. However, Fig. 12 demonstrates that although small and medium levels of del_{s2} cannot affect the impedances $Z_{ths}(s1-s2)$ and $Z_{ths}(s2-bp)$, a large level of del_{s2} (over 50%) may do so because of the lengthening of the thermal path between chip solder and baseplate.

B. FACTORS AFFECTING CROSS-HEATING THERMAL IMPEDANCE

1) ELECTRO-THERMAL OPERATING CONDITIONS

Different FE simulations show that under any variation in either ambient temperature or power loss, CTI among chips and layers remains unchanged. Nevertheless, the CTI between either nearby or faraway chips reduces with coolant flow rate as shown in Fig. 13 for chips T2-D2 ($Z_{thc}(T2-D2)$) and chips T2-T5 ($Z_{thc}(T2-T5)$), for example. This is because of the weakening the horizontal heat dissipation within the material layers due to augmenting the equivalent *htc*.

Following Fig. 13, it can also be understood that even at high airflow rates, faraway chips continue to create a significant cross-heating effect. This is in contrast to the findings in [38] where the authors demonstrated that the chips with a distance of more than 10 mm are no longer thermally coupled

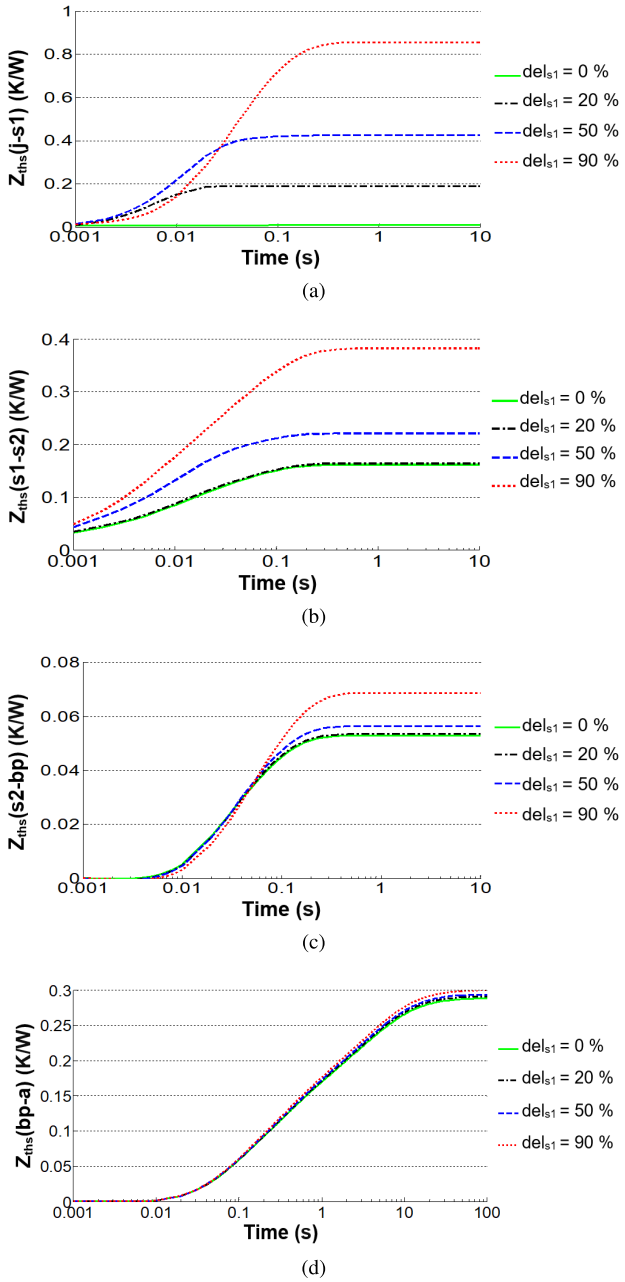


FIGURE 11. Calculated self-heating thermal impedance at various chip solder delamination levels (T_a = 20 °C, P_{loss} = 10 W, v_{air} = 6 m/s, and del_{s2} = 0%): (a) $Z_{ths}(j-s1)$; (b) $Z_{ths}(s1-s2)$; (c) $Z_{ths}(s2-bp)$; (d) $Z_{ths}(bp-a)$.

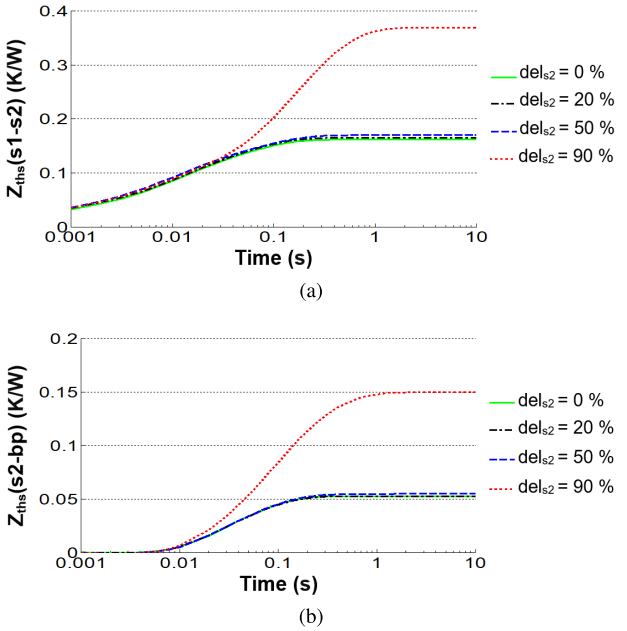


FIGURE 12. Calculated self-heating thermal impedance at various baseplate solder delamination levels (T_a = 20 °C, P_{loss} = 10 W, v_{air} = 6 m/s, and del_{s1} = 0%): (a) $Z_{ths}(s1-s2)$; (b) $Z_{ths}(s2-bp)$.

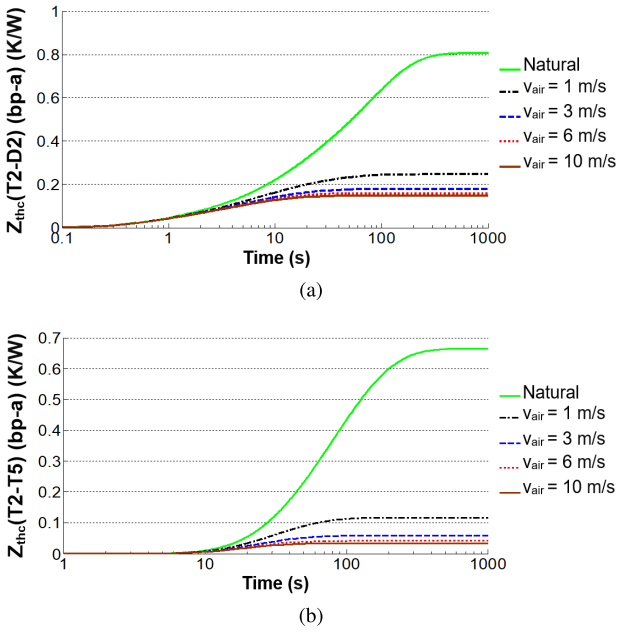


FIGURE 13. Calculated cross-heating thermal impedance at the baseplate at various airflow rates (T_a = 20 °C, P_{loss} = 10 W, and del_{s1} = del_{s2}=0%): (a) $Z_{thc}(T2-D2)$; (b) $Z_{thc}(T2-T5)$.

with any cooling system. As further research, Fig. 14 shows that if the equivalent *htc* is severely augmented, for example by using a forced-liquid heatsink, the cross-heating effect between faraway chips can be neglected. The liquid (water)–cooled heatsink is investigated here to just understand the effect of cooling systems with large values of equivalent *htc* on the cross-heating effect among chips.

2) SOLDER FATIGUE

FE simulations revealed that various levels of del_{s1} cannot change the CTIs throughout the IGBT module at all. This lack of effect is also revealed for the levels of baseplate solder delamination (del_{s2}) up to 50%. In other words, for $del_{s2} > 50\%$, the CTIs within layers lying above the delaminated baseplate solder would be influenced. For example, Fig. 15 demonstrates CTI between chips T2-D2 versus del_{s2} levels. Furthermore, FE simulations revealed that any delamination level at both solder joints has no effect on the CTI between chips/layers with different DBC substrates.

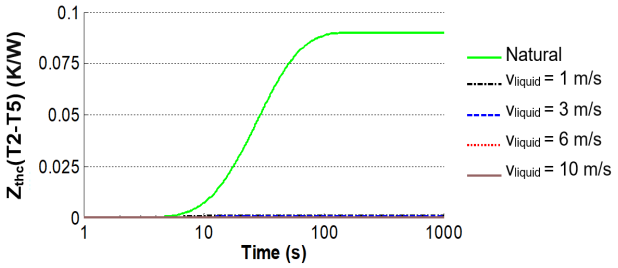


FIGURE 14. Calculated cross-heating thermal impedance $Z_{thc}(T2-T5)$ at various flow rates of liquid-cooled heatsink ($T_a = 20$ °C, $P_{loss} = 10$ W, and $dels1 = dels2 = 0$).

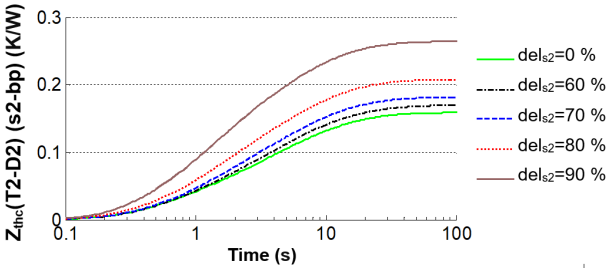


FIGURE 15. Calculated cross-heating thermal impedance $Z_{thc}(T2-D2)$ at the baseplate solder with various delamination levels ($T_a = 20$ °C, $P_{loss} = 10$ W, $v_{air} = 6$ m/s, and $del_{s1} = 0\%$).

By considering Fig. 1 and the use of the RC circuit concept, it can be concluded that in the limit of steady-state for a step response, the impedance equals the resistance. Therefore, the description given in this Section about the effect of electro-thermal and aging conditions on STIs and CTIs can also be generalized to relevant thermal resistances because above, we are analyzing the change of STIs and CTIs in the steady-state. Regarding how the thermal capacitances change, a technique to fit thermal impedance curves must be used that will be described in the following.

IV. IMPROVED THERMAL MODEL

Transient STI and CTI curves derived from FE simulations can be mathematically fitted to a Foster network based on the following finite series [39].

$$Z_{th}(t) = \sum_i R_{th,i}(1 - exp(-\frac{t}{R_{th,i} \cdot C_{th,i}})) \qquad (5)$$

where i^{th} exponential term corresponds to i^{th} RC cell of the Foster network for the thermal impedance under study.

To fit curves to data, the MatLab curve fitting toolbox (CFTool) is used in this work where the least square of the correlation coefficient (R^2) is set to 0.99 to keep the accuracy high for all fitted curves. Subject to this constraint, one RC cell is found enough for modeling of STIs and CTIs inside the IGBT module, whereas two RC cells are needed to fit the impedance $Z_{ths}(bp-a)$ curves with $R^2 \geq 0.99$.

By obtaining the equivalent RC parameters at various conditions, the curve of RC parameters versus the affecting conditions can be drawn. Fig. 16 shows RC curves to airflow rate beside the fitted mathematical relations for the impedance $Z_{thc}(T2-T5)$. It can be seen that the resistance component $R_{thc}(T2-T5)$ decreases but the capacitance component $C_{thc}(T2-T5)$ increases with the airflow rate. In the same way, all RC curves can be obtained in terms of the affecting conditions for different locations throughout the IGBT module; however, to save space, the curves are avoided in this paper and only the relations are given in Table 3. It is found that if the conditions change, a variation of the influenced RC parameters can often be approximated by an incremental or decremental exponential function added to a constant term. Also, changes in thermal capacitances inside the IGBT module can be ignored because they are small compared to that of the heatsink. A schematic of the proposed TEC is shown for a generic chip in Fig. 17.

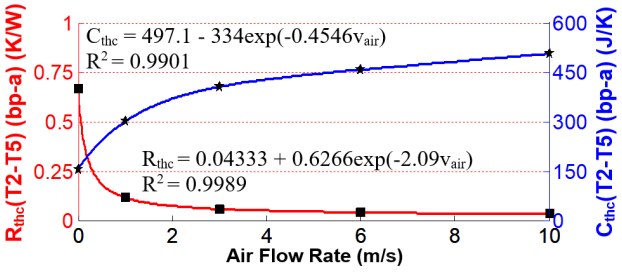


FIGURE 16. Curve fitted cross-heating thermal resistance $R_{thc}(T2-T5)$ and thermal capacitance $C_{thc}(T2-T5)$ at the baseplate with various airflow rates.

V. VERIFICATIONS

A. EXPERIMENTAL SETUP

To verify the introduced TEC, an experimental setup consisting of the same IGBT module and heatsink used in the simulation is built with a circuit topology and structure shown in Fig. 18. Here, the DC link is supplied through a rectifier; then it is connected to the inverter IGBT module supplying a resistive-inductive load.

During operation, the switching frequency is set to 1 kHz, and the fundamental output frequency is set to 1 Hz, which is often used in power cycling tests [40].

To realize thermal images via IR camera, a solvent from Dynaloy products [41] is used for the removal of the silica gel of the IGBT module. Then, a thin coating using the black paint is sprayed to the top surfaces of the decapsulated module, as shown in Fig. 19. The IR camera can display high-quality thermal images at 320 × 240 resolution, 60 Hz frame rate, and ±2% accuracy for a wide range from -20 to 650 °C. By considering the inaccessibility of the layers, which underlie the chips, in terms of thermography, FE simulations are used to verify the temperature of the underlyig layers. Also, two extra TECs are considered in this study to investigate and compare their performance with that of the proposed TEC: the manufacturer TEC and fixed-parameter TEC.

TABLE 3. Relations for RC parameters of Foster TEC model of system under study obtained by simulations.

Thermal impedance	Location	Independent variables	Relation	Parameters for T2 branch coupled with T5 and D2 under air cooling	R-square
STI	j-s1	$T_a, P_{loss}, del_{s1}, del_{s2}$	$R_{ths} = a + b \cdot T_a + c \cdot exp(d \cdot P_{loss}) + e \cdot del_{s1}$	$a = 0.3522, b = 0.00008, c = 0.0043, d = 0.00589, e = 0.0069$	0.9923
		-	$C_{ths} = a(Const.)$	$a = 0.024$	-
	s1-s2	$T_a, P_{loss}, del_{s1}, del_{s2}$	$R_{ths} = a + b \cdot Ta + c \cdot exp(d \cdot P_{loss}) + e \cdot exp(f \cdot del_{s1}) + g \cdot exp(h \cdot del_{s2}) \cdot bin^*$	$a = -9.305, b = 0.00044, c = 0.025, d = 0.00386, e = 9.532, f = 0.00029, g = 0.00031, h = 0.07686$	0.9914
		-	$C_{ths} = a(Const.)$	$a = 0.12234$	-
	s2-bp	del_{s1}, del_{s2}	$R_{ths} = a + b \cdot exp(c \cdot del_{s1}) + d \cdot exp(e \cdot del_{s2}) \cdot bin^*$	$a = 0.04898, b = 0.00329, c = 0.0213, d = 0.00121, e = 0.05089$	0.9972
		-	$C_{ths} = a(Const.)$	$a = 0.1023$	-
	bp-a (first RC cell)	v_c	$R_{ths} = a + b/exp(c \cdot v_c)$	$a = 0.1348, b = 1.178, c = 3.028$	0.9998
		v_c	$C_{ths} = a + b/exp(c \cdot v_c)$	$a = 35.19, b = 55.25, c = 1.324$	0.9949
	bp-a (second RC cell)	v_c	$R_{ths} = a + b/exp(c \cdot v_c)$	$a = 0.1508, b = 0.1614, c = 1.907$	0.9983
		v_c	$C_{ths} = a + b/exp(c \cdot v_c)$	$a = 1.678, b = 2.834, c = 2.753$	0.9997
CTI	All layers (mutual chips are on different DBCs)	v_c	$R_{ths} = a + b/exp(c \cdot vc)$	$a = 0.04333, b = 0.6213, c = 2.135$	0.9989
		v_c	$C_{ths} = a + b/exp(c \cdot v_c)$	$a = 497.1, b = -334, c = 0.4546$	0.9901
	All layers (mutual chips are on the same DBC)	v_c, del_{s2}	$R_{thc} = a + b/exp(c \cdot v_c) + d \cdot exp(e \cdot del_{s2}) bin^*$	$a = 0.1655, b = 0.6543, c = 2.04, d = 0.00004, e = 0.087$	0.9923
		v_c, del_{s2}	$C_{thc} = a + b/exp(c \cdot v_c) - d \cdot exp(e \cdot del_{s2}) \cdot bin^*$	$a = 30.57, b = 26.13, c = 1.867, d = -0.3145, e = 0.0447$	0.9907

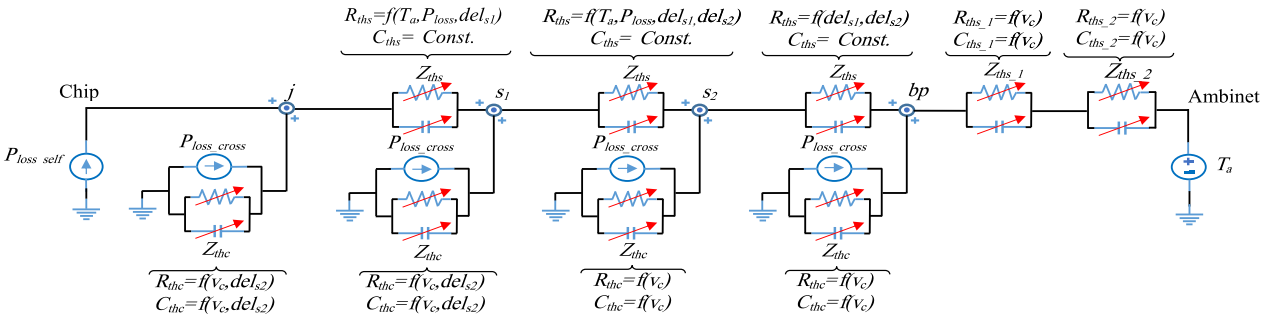
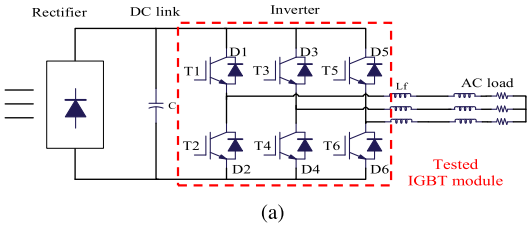


FIGURE 17. Schematic of the Foster-type TEC for a generic chip adaptive to electro-thermal operating and thermal aging conditions (P_{loss_self} is the power loss calculated in the chip itself, P_{loss_cross} is the power loss in a mutual chip, and v_c is the coolant flow rate through a heatsink).

The TEC provided by the manufacturer in the datasheet of the module under study lacks cross-heating branches, which is usually the case. However, the fixed-parameter TEC considered has the same structure as the proposed TEC for any chip, i.e., a self-heating branch combined with cross-heating branches but with RC parameters set at the standard conditions ($T_a = 20$ °C, $P_{loss} = 10$ W, $v_{air} = 6$ m/s, and $del_{s1} = del_{s2} = 0\%$). In addition, in order to focus on only thermal model of the module, the RC parameters of all three TECs for the components outside the module have been the same values in accordance with the existing operating conditions. In other words, what distinguishes these three TECs are the presence/absence of cross-heating branches and variability/invariability of RC parameters for thermal model of the module; whereas they have the same RC parameters for the components outside of the module including the cooling system and thermal paste.

B. MODEL VALIDATION

In this section, several scenarios are examined to evaluate the performance of the TECs compared to experiments and FE simulations with a focus on temperatures of the chip T2 branch. In the first experiment, 20 A (peak) electric current is fed to a single-phase load through chips T2 and T5 of healthy IGBT module. The module is operated with natural air heatsink at $T_a = 24$ °C. As it can be seen in Fig. 20, a slight temperature difference lower than 1 °C is present between maximum T_j of chip T2 obtained from the proposed TEC and IR camera, and also FE simulation. However, dramatic errors of about 26 and 29 °C are present in the maximum T_j obtained from the manufacturer TEC and fixed-parameter TEC. The reason for the large errors is explained by the cross-heating effects or CTIs. As can be seen in Fig. 13, the CTIs throughout the module are found to be sensitive to the flow rate of coolant in the heatsink.



(a)

(b)

FIGURE 18. Test setup: (a) circuit topology; (b) the whole system.

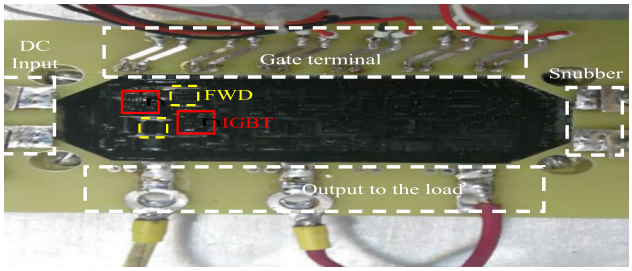
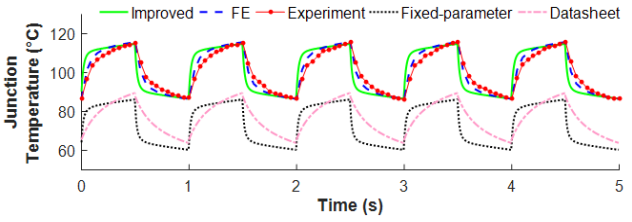
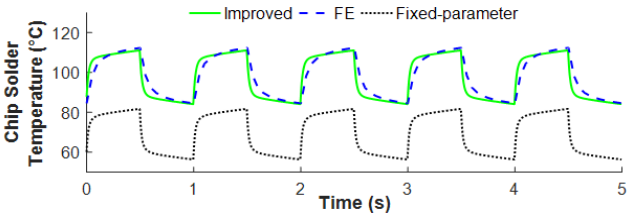


FIGURE 19. Decapsulated and black painted IGBT module.



(a)



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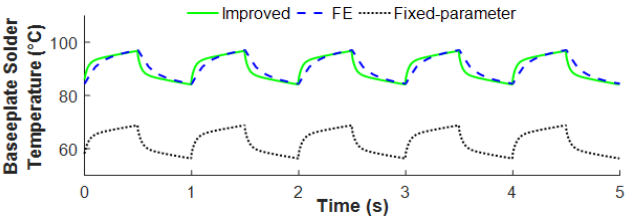

(c)

FIGURE 20. Performance comparison of the proposed, fixed-parameter, and manufacturer TECs with experiment and FE simulation in estimating the temperatures under chip T2 ($T_a = 24$ °C, $I_C = 20$ A (peak), natural air cooling, $del_{s1} = 0\%$, $del_{s2} = 0\%$): (a) T_j; (b) T_{s1}; (c) T_{s2}.

CTIs of the proposed TEC are set at the current coolant flow rate; whereas those of the fixed-parameter TEC are set at $v_{air} = 6$ m/s under which the CTIs would be much smaller than those of natural airflow. In addition, the manufacturer TEC model lacks the CTI branches that can make large temperature errors under natural air cooling, as found in Fig. 13. Furthermore, in Figs. 20(b)-20(c), the proposed TEC and FE simulation indicate a good agreement in the prediction of T_{s1} and T_{s2}, whereas a large temperature error of 28 °C is still observed at T_{s1} and/or T_{s2} predicted by the fixed-parameter model.

In conditions like in the previous scenario, but with the natural liquid heatsink, another experiment is performed. To implement the natural liquid cooling system, the heatsink is placed directly in a pan of water. As shown in Fig. 21, the proposed TEC provides maximum T_j very close to the experiment and FE simulation (about 1 °C difference), whereas the fixed-parameter TEC estimates maximum T_j to be 2 °C above that of the experiment. The reason is to be a smaller cross-heating effect in the presence of liquid cooling compared to the standard cooling condition under which the fixed-parameter model is set. Also, the manufacturer TEC estimates maximum T_j very close to the experiment because the cross-heating effects become insignificant under the liquid cooling system of the experiment. Figs. 21(b)-21(c) show that the estimated T_{s1} and T_{s2} using the proposed model and the fixed-parameter model are close to those obtained using FE simulation.

In the following, the effect of solder joints delamination on the performance of the TECs is investigated. In this research work, to induce 70% delamination in the baseplate solder joint, a thermal cycling process was performed within a chamber. The process has the least impact on the chip solder's health. In this condition, the IGBT module is put into operation to supply a single-phase load current of 10 A through chips T2 and T5. The IGBT module is operated at $T_a = 24$ °C and a 4 m/s air fan is attached to the heatsink. Fig. 22(a) indicates that the maximum T_j obtained from the proposed model agrees well with experiments and FE simulations (lower than 1 °C temperature difference). However, it can be seen that the manufacturer model and the fixed-parameter model are unable to predict maximum T_j close to the experiment (about 5 °C temperature difference). In Figs. 22(b)-22(c), T_{s1} and T_{s2} obtained from the proposed TEC and FE simulation are also in good agreement, whereas the fixed-parameter model has a noticeable error in the prediction of T_{s1} and T_{s2}.

Furthermore, the DC cycling approach was employed in the laboratory to induce delamination of 20% into the solder

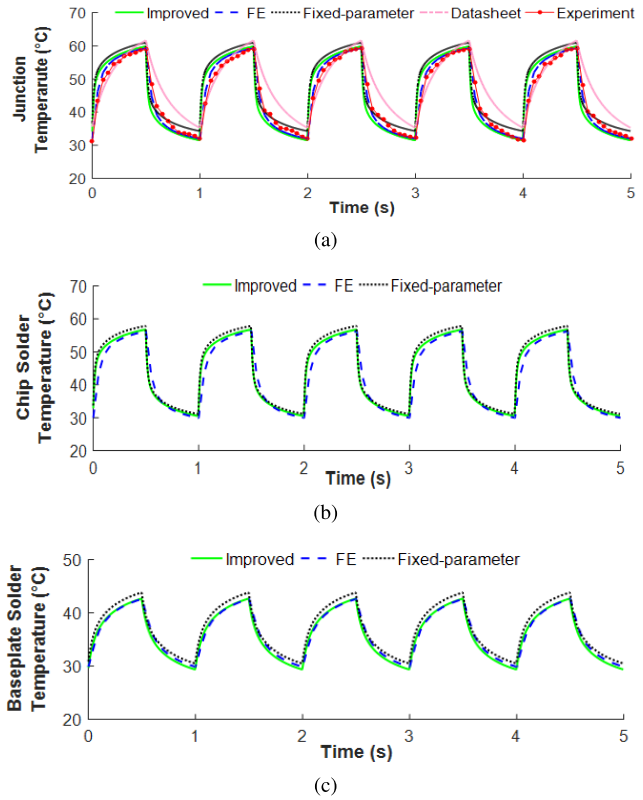

FIGURE 21. Performance comparison of the proposed, fixed-parameter, and manufacturer Foster TECs with experiment and FE simulation in estimating the temperatures under chip T2 ($T_a = 24$ °C, $I_C = 20$ A (peak), natural air cooling, $del_{s1} = 0\%$, $del_{s2} = 0\%$): (a) T_j; (b) T_{s1}; (c) T_{s2}.

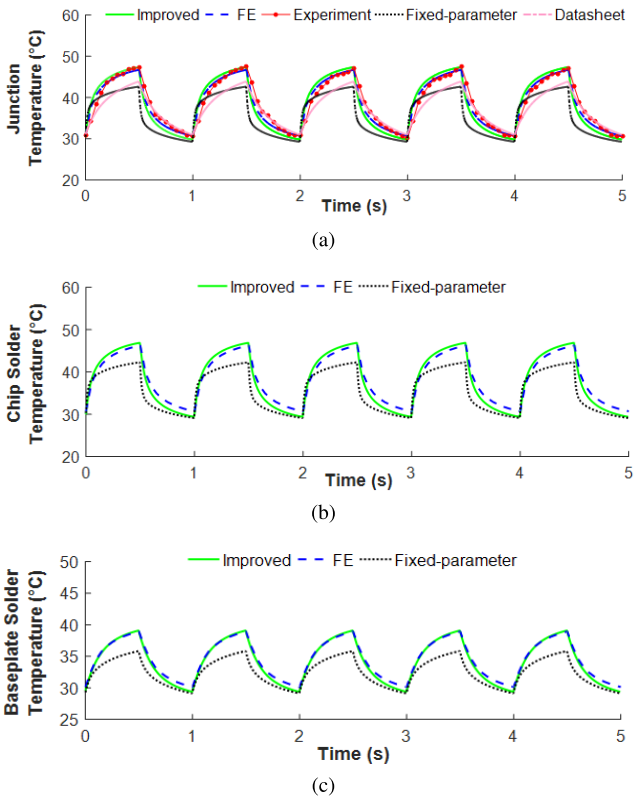

FIGURE 22. Performance comparison of the proposed, fixed-parameter, and manufacturer Foster TECs with experiment and FE simulation in estimating the temperatures under chip T2 ($T_a = 26$ °C, $I_C = 10$ A (peak), 4 m/s air cooling, $del_{s1} = 0\%$, $del_{s2} = 70\%$): (a) T_j; (b) T_{s1}; (c) T_{s2}.

of chip T2. It has the least impact on the baseplate solder health.

Under the condition of $T_a = 26$ °C, 6 m/s air cooling heatsink, and with $del_{s1} = 20\%$ and $del_{s2} = 70\%$ for chip T2, an electric current of 10 A is supplied by chips T2 and T5 for a single-phase load. Fig. 23(a) presents that the proposed TEC has high accuracy and it is very close to experiment and FE simulation (about 1.5 °C temperature difference). However, the manufacturer model and the fixed-parameter model make a significant error in the estimation of maximum T_j. Also, Figs. 23(b)-23(c) show a good performance in the estimation of T_{s1} and T_{s2} by using the proposed model compared to the fixed-parameter model.

C. LIFETIME ESTIMATION

To show the importance of the proposed TEC and to show how the TEC accuracy affects the calculations of lifetime models, a detailed study is performed. To this aim, the lifetime model presented in [42] has been used. This model gives the number of thermal cycles to failure as a function of various parameters, with emphasis on junction temperature cycling and its mean value as given by

$$N_f = A \cdot {\Delta_j}^{\beta_1} \cdot e^{\frac{\beta_2}{T_{j,m}+273}} \cdot {t_{on}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \qquad (6)$$

where N_f is the number of cycles to failure, $T_{j,m}$ is the mean junction temperature, t_{on} is the on-pulse duration, I is the current per wire, V is the chip blocking voltage and D is the bonding wire diameter. For the IGBT module under study, the constants β_1 to β_6 are obtained from [42] as $[\beta_1, \ldots, \beta_6] = [-4.416, 1.285 \times 10^3, -0.463, -0.716, -0.761, -0.5]$ the constants D=500 μm and V=1200 V are defined in [21] and since the module belongs to the 4^{th} generation of Trench Field Stop IGBT [21], the constant A should be 9.34×10^{14} according to [43].

TABLE 4. Number of cycles to failure using different TECs for scenarios defined in Subsection V-B.

Scenario	Datasheet TEC	Fixed- parameter TEC	Proposed TEC
1	7.4602×10^5	7.7505×10^5	3.9091×10^5
2	9.0364×10^5	8.7521×10^5	6.6603×10^5
3	4.0010×10^7	3.4894×10^7	1.1493×10^7
4	1.3972×10^7	3.8306×10^7	1.4956×10^5

By considering the scenarios introduced in previous Subsection, and by replacing temperatures $T_{j,min}$ and $T_{j,max}$ in (6) with the above values for the parameters, N_f would be calculated as given in Table 4. It is understood that the value

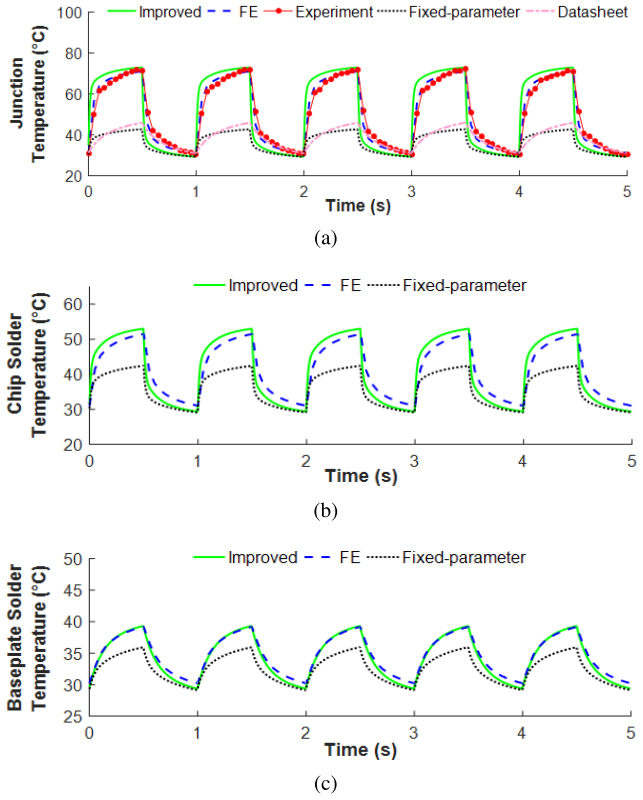

FIGURE 23. Performance comparison of the proposed, fixed-parameter, and manufacturer Foster TECs with experiment and FE simulation in estimating the temperatures under chip T2 ($T_a = 26$ °C, $I_C = 10$A (peak), 4m/s air cooling, $del_{s1} = 20\%$, $del_{s2} = 70\%$): (a) T_j; (b) T_{s1}; (c) T_{s2}.

of N_f obtained from the proposed TEC is much lower than that of the datasheet and/or fixed-parameter TECs, especially when the cooling system is very different from the system in which the TEC parameters are extracted and/or when the power module is aged. In other words, this comparison shows that the thermal model can be misleading if it is not properly adapted to different operation modes and/or aging conditions.

VI. CONCLUSION

This paper presents a TEC based on mathematical relations for accurate estimation of temperature profiles in critical locations of a multichip IGBT module mounted on a heatsink. The introduced model is appropriate to be merged into circuit simulators for long-term analysis. The TEC model gives clear and easy access to the evaluation of how a change in electro-thermal operating and/or solder joints aging conditions may change RC parameters of STIs and CTIs and as a result, the temperature profiles. It reveals that the TEC parameters are significantly influenced by any change in the cooling system with low to medium equivalent *htc*, e.g., in the conversion of natural to forced cooling or air to the liquid coolant. Moreover, the chip solder delamination, however small, can largely affect the temperatures; whereas only large levels of baseplate solder delamination (above 50%) can make significant changes to the temperatures. It also indicates that under a cooling system with low to medium equivalent *htc*, there exists a significant cross-heating effect among chips far away, and the cross-heating effect and equivalent *htc* distribution can interact. In addition, it can improve the accuracy in predicting the life of the devices with the help of models that use temperature profiles and it can cause the conditions to be properly chosen according to the desired electro-thermal requirements. The results obtained in this paper can also be used to compensate for the undesirable effect caused by altered operating and/or aging conditions on RC parameters with the help of other conditions.

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MOHSEN AKBARI (Student Member, IEEE) received the M.Sc. degree (Hons.) in electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2010, where he is currently pursuing the Ph.D. degree in electrical engineering. From 2017 to 2018, he was a visiting Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His publications are mainly in distributed energy resources, microgrids, and multiphase power systems. His current research interests include multiphysics modeling, thermal management, packaging, and reliability of power semiconductor devices.

MOHAMMAD TAVAKOLI BINA (Senior Member, IEEE) received the B.Sc. degree from the University of Tehran, in 1988, the M.Sc. degree from the University of Ferdowsi, Iran, in 1991, and the Ph.D. degree from the University of Surrey, Guildford, U.K., in 2001, all in power electronics and power system utility applications. From 1992 to 1997, he was a Lecturer with the K. N. Toosi University of Technology, Tehran, where he was involved in power systems. He joined the Faculty of Electrical and Computer Engineering, K. N. Toosi University of Technology, in 2001, where he is currently a Professor of electrical engineering and he is engaged in teaching and conducting research in the area of power electronics and utility applications. His research interests include power electronics, flexible power systems, and power quality.

AMIR SAJJAD BAHMAN (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Aalborg University, Denmark. He was a Visiting Scholar at the Mixed Signal Computer-Aided Design Research Laboratory (MSCAD), University of Arkansas, USA, in 2014, and a Thermal Design Intern at Danfoss Silicon Power, Germany, in 2014. He is currently an Associate Professor at the Center of Reliable Power Electronics (CORPE), Aalborg University. His current research interests include multiphysics modeling, packaging, thermal management, and reliability of power electronic components and systems. He is an Associate Editor of IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION and *Elsevier Microelectronics Reliability*.

BAHMAN ESKANDARI (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the K. N. Toosi University of Technology (KNTU), Tehran, Iran, in 2003, 2006, and 2013, respectively. He joined Malayer University, Hamedan, Iran, as an Assistant Professor. He had a long-term collaboration with the Advanced Power Electronics Laboratory (KNTU) in the field of flexible ac compensation in the power system as a Research Assistant, in 2014. He is currently a Postdoctoral Researcher with the Department of Electrical Engineering and Automation (EEA), Aalto University, Espoo, Finland. His research interests include design, implementing, control and modulation techniques for power electronic converters, and their application in a wide range of applications.

EDRIS POURESMAEIL (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Technical University of Catalonia (UPC-Barcelona Tech), Barcelona, Spain, in 2012. He joined the University of Waterloo, Waterloo, ON, Canada, as a Postdoctoral Research Fellow and then he joined the University of Southern Denmark (SDU), Odense, Denmark, as an Associate Professor. He is currently an Associate Professor with the Department of Electrical Engineering and Automation (EEA), Aalto University, Espoo, Finland. His main research interests include application of power electronics in power and energy sectors.

FREDE BLAABJERG (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995. He is currently pursuing the honoris causa degree with University Politehnica Timisoara, Timisoara, Romania, and the Tallinn University of Technology, Tallinn, Estonia. From 1987 to 1988, he was with ABB-Scandia, Randers, Denmark. He became an Assistant Professor, in 1992, an Associate Professor, in 1996, and a Full Professor of power electronics and drives, in 1998. Since 2017, he has been a Villum Investigator. He has authored or coauthored more than 600 journal articles in the field of power electronics and its applications. He is the coauthor of four monographs and an editor of ten books in power electronics and its applications. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives. He was a recipient of 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award, in 2009, the EPE-PEMC Council Award, in 2010, the IEEE William E. Newell Power Electronics Award, in 2014, the Villum Kann Rasmussen Research Award, in 2014, the Global Energy Prize, in 2019, and the IEEE Edison Medal, in 2020. From 2006 to 2012, he was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS. He was a Distinguished Lecturer for the IEEE Power Electronics Society, from 2005 to 2007, and for the IEEE Industry Applications Society, from 2010 to 2011, as well as, from 2017 to 2018. From 2019 to 2020, he was a President of the IEEE Power Electronics Society. He is a Vice-President of the Danish Academy of Technical Sciences. He was nominated in 2014–2019 by Thomson Reuters to be between the 250 most cited researchers in engineering in the world.