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Dynamic and Steady State Response Analysis of Selective Harmonic Elimination in High Power Inverters

JINGLING CHENG[1], TINGTING XU[1], DONGDONG CHEN[2], AND GUOZHU CHEN[1], (Member, IEEE)

[1]Department of Electrical Engineering, Zhejiang University, Hangzhou 310027, China
[2]School of Electronic and Electrical Engineering, Minnan University of Science and Technology, Quanzhou 362700, China

Corresponding author: Dongdong Chen (cdd1911@qq.com)

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ABSTRACT Selective harmonic elimination (SHE) technique has drawn tremendous interests for its superior harmonic performance, especially in high power devices where switching power loss and passive filter size are the main concerns. However, the drawbacks of slow dynamic response and difficulties in hardware implementation limit its engineering application. Based on a 3-level inverter, this paper analyzes the dynamic response of SHE. A system model is established and an improved method of updating the switching angles at sampling frequency is proposed. And a combination of notch filters and low-pass filter is designed to achieve a higher system bandwidth. The dynamic response and stability of the system are analyzed in detail. In addition, the influence of control errors on steady-state performance during hardware implementation is also discussed. A simple hardware structure of a DSP with a small-scale FPGA is adopted to realize the above method. Both dynamic response and steady-state response of the improved system are analyzed and compared with the regular SHE modulation and the widely used sinusoidal pulse width modulation (SPWM). Simulation and experimental results provided that the improved method proposed in this paper retains the excellent steady-state characteristics of the regular SHE modulation, and at the same time achieves as good dynamic performance as SPWM.

INDEX TERMS Dynamic response, high power inverter, selective harmonic elimination, steady-state response.

I. INTRODUCTION

With the development of the high-power semiconductors, the capacity of a single power electronic device has increased to the level of several megawatts [1]. Due to the advantages of lower dv/dt, reduced total harmonic distortion (THD), lower switching frequency and smaller electromagnetic interference, multi-level topologies such as neutral point clamped (NPC) converters, modular multilevel converters (MMC), and cascaded H-bridges (CHB) are playing an increasingly important role in the high-power industries [2]–[4]. In these devices, switching power loss, passive filter volume, system efficiency and harmonic performance are the main concerns. To meet these requirements, the choice of the modulation techniques is crucial in the system design process. Sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), nearest level modulation (NLM), and carrier phase shifted pulse width modulation (CPS-PWM) are the most commonly used modulation techniques [5]. However, no matter which modulation method is used, there is always a trade-off between harmonic performance and switching power loss [6], [7].

Selective harmonic elimination (SHE) was first proposed in the early 1960s, and quickly developed into the form of the current version [8], [9]. Since its proposal, SHE has been found to stand out among the modulation strategies because of the reduced number of commutations and tight control

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of low order harmonics [10]. The engineering application of SHE was limited at the beginning because of the huge difficulties of solving the nonlinear and transcendental equations [11]. Higher hardware overhead especially the memory consumption also brought a problem. In recent years, with the development of the digital processors, SHE has regained interests and has been studied a lot. Most of the research focuses on the following aspects, a) solution range extending, b) formulations in multilevel situations, c) optimization or mitigation based techniques, d) methods that facilitate online implementation, e) power balance or DC link voltage equalization [12]–[15]. These studies have greatly broadened the application areas of SHE, from variable frequency motor drives, high-power current source rectifiers to multi-level grid-connected voltage source inverters [16].

Nevertheless, it is still generally believed that SHE has two main drawbacks which prevent it from being more widely used, namely slow dynamic response and high memory consumption [17]. The former is because SHE is an optimization algorithm based on the fundamental period and needs to maintain the symmetry of its waveform throughout the fundamental period. The latter is due to the fact that the nonlinear and transcendental SHE equations cannot be solved online while ensuring convergence. The usual approach is to solve the equations numerically offline under all possible operating conditions and store the results as a look-up table (LUT) in memory of the digital processor [18]. A large amount of memory is then required to ensure high accuracy. Nowadays, as the development of the very large scale integrated circuits (VLSI), low cost digital signal processors (DSP) with enough memory has been widely used in control systems. Therefore, this paper focused on the dynamic response of SHE which is the most urgent issues encountered in high power inverters.

Several researches have been done to improve the dynamic response of SHE. In [19] and [20], a combination of model predictive control (MPC) and SHE are proposed. The MPC controller is to achieve a fast dynamic response in transient state while the SHE controller ensures high harmonic performance and slow switching frequency in steady state. Amirhossein M., etc. introduced a hybrid modulation of SHE and CPS-PWM in a CHB inverter [17]. Similarly, SHE is applied in steady state and CPS-PWM in dynamic process to simultaneously achieve a good dynamic and steady state performance. The idea of the above methods is straightforward, but it faces the problems of complicated control system and stability issues during the process of switching the modulation mode. In [21], the disturbance of the switching angle of SHE was controlled by an inner closed loop with an instantaneous observer. The steady state error is claimed to be zero but the transient process lasts about one fundamental period. In [22], a low-pass filter on the phase of the modulation index is added to avoid unwanted glitches during transient operation. But the dynamic response is not further discussed. Other recent implementations of SHE can be found in [23]–[31]. In these studies, dynamic response is not the main requirement of the system, or is not discussed in detail.

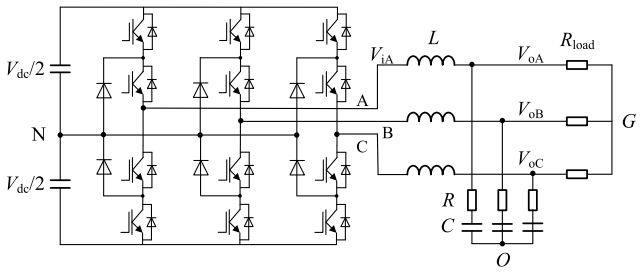

FIGURE 1. Topology of 3-level neutral point clamped voltage source inverter.

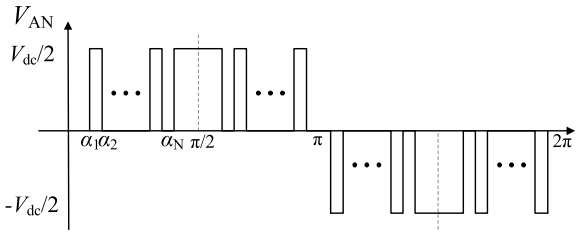

FIGURE 2. 3-level SHE waveform with quarter-wave even symmetry and half-wave odd symmetry.

Based on a 3-level NPC voltage source inverter, this paper establishes a system model including the modulation process and analyzes the reasons for the slow dynamics of SHE. Then, an improved method of updating the switching angles at sampling frequency is proposed. Both dynamic and steady-state response of the proposed method are analyzed and compared with the conventional SHE and SPWM. The proposed method slightly sacrifices the steady-state response, and obtains as good dynamic performance as SPWM. Simulation and experimental verification are provided. The remaining parts of this paper are organized as follows. Section II briefly introduces the principle and realization process of SHE. Section III analyzes the dynamic response of SHE based on system modeling. Considering the hardware control errors, the steady state performance is evaluated in section IV and the simulation and experimental verification is shown in section V. Finally, a conclusion is made in section VI.

II. PRINCIPLES OF SHE

Three level neutral point clamped (NPC) voltage source inverter (VSI) is one of the most popular multilevel topologies in high power applications for its proper harmonic performance and system complexity [32]. This paper utilizes a three phase NPC VSI topology with resistive load (as shown in Fig. 1) to illustrate the performance of SHE. It is noted that the results should not be limited to NPC topology or type of the loads.

The principle of SHE is based on calculating the Fourier decomposition of the output waveform of the inverter, as shown by v_{xN} $(x = A, B, C)$ in Fig. 1. The waveform varies according to the topology. For the case of 3-level NPC inverter, the most widely used SHE waveform maintains quarter-wave even symmetry and half-wave odd

symmetry [33], as shown in Fig. 2. The Fourier decomposition is shown in (1)–(2), in which n, ω, N, V_{dc}, α_i denote the harmonic order, the fundamental angular frequency, number of the switching angles, the DC link Voltage, the switching angles, respectively. It can be seen that the even harmonics are eliminated because of the symmetry. And the fundamental component and low order harmonics can be artificially controlled (b_n denotes the amplitude of the n^{th} harmonic component) by specially arranging the switching angles α_i.

$$v_{AN} = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{1}$$

where

$$\begin{cases} a_n = 0 \\ b_n = \dfrac{4}{n\pi} \dfrac{V_{dc}}{2} \displaystyle\sum_{i=1}^{N} (-1)^{i-1} \cos(n\alpha_i) & \text{if } n \text{ is odd.} \\ b_n = 0 & \text{if } n \text{ is even.} \end{cases} \tag{2}$$

A common practice is to get the switching angels α_i from (3)–(5) in which M, v_{1m}, $\mathbb{H}$ denote the modulation ratio, the amplitude of the fundamental voltage, and a set of harmonics that are eliminated. It is clear that the fundamental component in the output voltage v_{xN} is controlled by the modulation ratio M, and the harmonics in set $\mathbb{H}$ are eliminated if the switching angles α_i satisfy (3)–(5). Equation (3) is a group of nonlinear and transcendental equations which lead to great difficulty to get an analytical solution. Nevertheless, there are still many numerical solutions with sufficient accuracy to be used in engineering applications [34], [35]. In general, because the convergence of the numerical solution cannot be guaranteed, the SHE equations are usually solved offline with a certain step within the entire operation range [36], [37], e.g., from M=0.001–1. The results are stored in the memory of the digital controller as a look-up table (LUT) and are read in real time using M as the index. An example of the solution trajectories of (3)–(5) when N=9 are shown in Fig. 3 with M=0.001–1 and a step size of 0.001. Note that the control of low-order harmonics is arbitrary and does not have to be consistent with (3). For example, in grid connected applications, the total harmonic distortion (THD) could be minimized when selecting the switching angles, rather than setting low-order harmonics to zero.

$$\begin{cases} \displaystyle\sum_{i=1}^{N} (-1)^{i-1} \cos(\alpha_i) = \frac{\pi}{4} M \\ \displaystyle\sum_{i=1}^{N} (-1)^{i-1} \cos(n\alpha_i) = 0 \end{cases} \tag{3}$$

where

$$\begin{cases} M = 2v_{1m}/V_{dc} \\ n \in \mathbb{H} \end{cases} \tag{4}$$

and

$$\mathbb{H} = \{5, 7, 11, 13, \cdots, 3N - 2\} \tag{5}$$

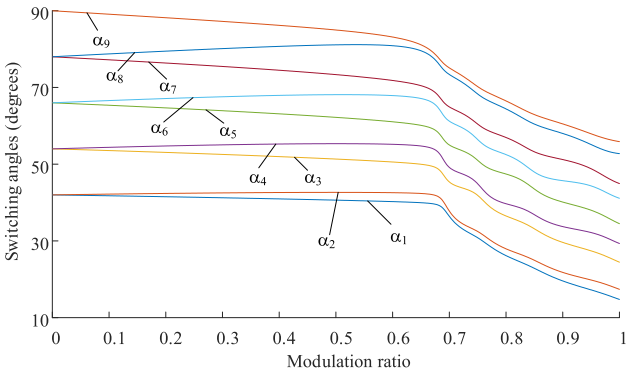

FIGURE 3. Switching angle trajectories when $N = 9$.

From the above principles of SHE, it can be seen that the harmonic performance is determined by the number of switching angles. Besides the fundamental voltage, there are $N-1$ control degrees of freedom. If (5) is adopted, the lowest characteristic harmonic in the output voltage is located at the $(3N+2)^{th}$. Taking $N = 9$ for example, the lowest characteristic harmonic is the 29^{th} (1450Hz in a fundamental frequency of 50Hz) with a switching frequency of $9 \times 50\text{Hz} = 450\text{Hz}$. As a comparison, in a 3-level SPWM modulation with the same switching frequency, the lowest characteristic harmonic is located at $2 \times 450\text{Hz} = 900\text{Hz}$. The superior harmonic performance of SHE brings advantages of low switching loss, smaller filter size, easier thermal management, etc. In the applications of high power converters that mainly focus on switching losses and device size, SHE has gained more and more attention.

However, as described above, in order to achieve the ideal performance of SHE, the output voltage waveform of the inverter should be symmetrical within a fundamental period. Therefore, the switching angle data obtained from the LUT of the controller must remain unchanged within a fundamental period. The feature that the control command is updated only once per fundamental cycle will result in a very slow dynamic response, which will be discussed in the following part. For convenience, the regular SHE is denoted as F-SHE (Fundamental Frequency Updated SHE) in this paper.

III. SYSTEM MODELING AND DYNAMIC RESPONSE

This section takes a 3-level NPC topology with resistive load (shown in Fig. 1) as an example to analyze the dynamic response of F-SHE modulation. The proportional integral (PI) controller in the dq coordinate system is employed, which is commonly used in a three phase three wire system. The control block diagram is shown in Fig. 4 and (6)∼(11), where M, θ, α_1–α_N, ωt, v_{ix}, v_{ox} $(x = d, q)$ denote modulation ratio, displacement angle, switching angles, instantaneous phase, bridge arm voltage, output voltage, respectively. The space vector is illustrated in Fig. 5 and G_{LPF} is a widely used second order low pass filter (LPF) used in feedback sampling. This paper focuses on the impact of modulation methods on dynamic response, hense, a single voltage control

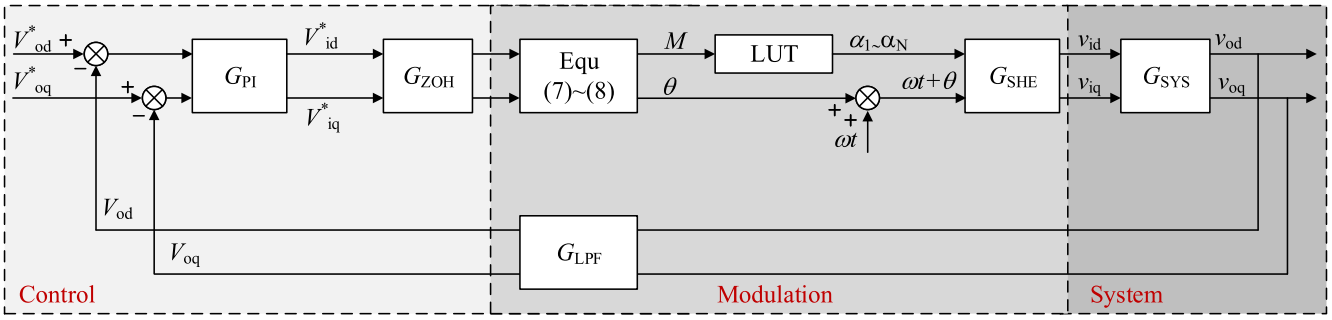

FIGURE 4. Control block diagram of the system.

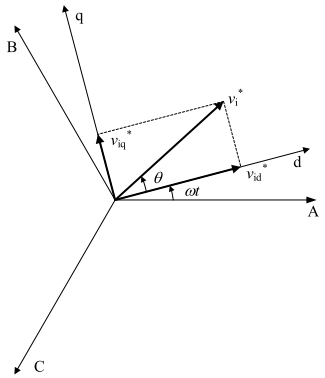

FIGURE 5. Space vector illustration in d-q axis.

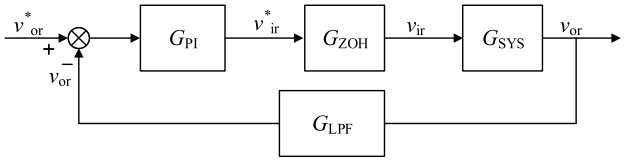

FIGURE 6. Simplified control block, $r = d, q$.

loop is employed and the cross-decoupling terms are omitted. Other techniques to improve the dynamic response from a control point of view [38]–[40], such as adding an inner inductor current loop, are beyond the scope of this paper.

$$G_{PI} = k_p + \frac{k_i}{s} \tag{6}$$

$$M = \frac{2}{V_{dc}}\sqrt{\left(v^*_{id}\right)^2 + \left(v^*_{iq}\right)^2} \tag{7}$$

$$\theta = \begin{cases} \tan^{-1}\left(\dfrac{v^*_{iq}}{v^*_{id}}\right) & \left(v^*_{id} > 0\right) \\ \tan^{-1}\left(\dfrac{v^*_{iq}}{v^*_{id}}\right) + \pi & \left(v^*_{id} > 0\right) \end{cases} \tag{8}$$

$$G_{ZOH} = \frac{1 - e^{-sT_0}}{s} \tag{9}$$

$$G_{SYS} = \frac{RCs + 1}{LCs^2 + RCs + 1} \tag{10}$$

$$G_{LPF} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{11}$$

As shown in Fig. 4, the system model can be divided into three parts, i.e., control, modulation, and system. In an digital controller, the control part is generally implemented with a high sampling frequency, which is 20kHz in this paper, to ensure high accuracy and speed. However, as explained in the last section, in the regular F-SHE algorithm, the switching angles are only updated once per fundamental period to maintain the waveform symmetry, which can be modeled as an inserted zero order hold (ZOH) G_{ZOH} as shown in Fig. 4 and (9), where T_0 denotes the fundamental period. G_{SHE} represent the SHE modulation process shown in (3) – (5). Since the low order harmonics in $\mathbb{H}$ are all eliminated and the fundamental component is controlled by the reference voltage v^*_{ir} $(r = d, q)$, the modulation part in Fig. 4 can be ideally approximated to 1, and the control diagram can be simplified to Fig. 6.

From Fig. 6, the open loop transfer function is derived in (12) and its Bode diagram is shown in Fig. 7. The model parameters are shown in Table 1, the control parameters are selected at which the phase margin is 60 degree under SPWM, and the sampling filter is selected with a cut-off frequency of 1000Hz to avoid samling the high order harmonics. The Bode diagram under SPWM modulation is also shown as a comparison where the system model G_{SYS} and the control parameter G_{PI} are the same but without the delay G_{ZOH}. It can be seen that the introduction of the delay time results in a significant drop of the open-loop bandwidth of the system which greatly reduced the dynamic response. And the increased phase delay will also affect system stability which is not reflected in the Bode diagram due to the non-linear delay link.

$$\begin{aligned} GH(s) &= G_{PI} \cdot G_{ZOH} \cdot G_{SYS} \cdot G_{LPF} \\ &= \frac{k_p \frac{R}{L}\omega_n^2 \left(s + \frac{k_i}{k_p}\right)\left(s + \frac{1}{RC}\right)\left(1 - e^{-sT_0}\right)}{s^2\left(s^2 + \frac{R}{L}s + \frac{1}{LC}\right)\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)} \end{aligned} \tag{12}$$

To illustrate the stability, the non-linear delay part e^{-sT_0} is linearized utilizing a 3^{th} order Pade approximation [41] as

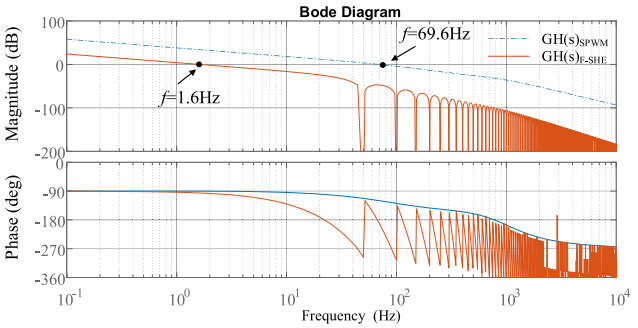

FIGURE 7. Bode diagram of SHE and SPWM with the same control parameters.

TABLE 1. Parameters for Bode diagram.

PI controller	$k_p = 0.1, k_i = 500$
Sampling	$\omega_n = 2\pi \times 1000$Hz, $\zeta = 0.707$
Delay time	$T_0 = 1/50$s
LC Filter	$R = 2\Omega$, $L = 3$mH, $C = 22\mu$F

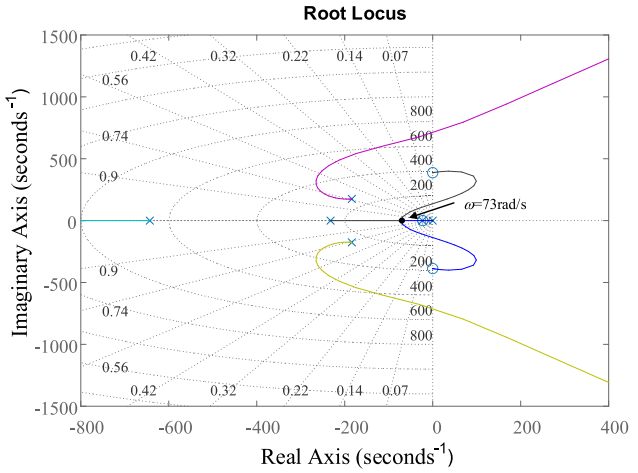

FIGURE 8. Root locus of the linearized open loop transfer function under F-SHE.

shown in (13). Combining (12) and (13), the root locus of the open loop transfer function is ploted as shown in Fig. 8 (There are a pair of conjugate poles and a zero far from the imaginary axis, which are omitted). Aagin, as a comparison, the root locus under SPWM modulation is ploted in Fig. 9. From Fig. 8 and Fig. 9 it can be seen that the system is dominated by a pair of conjugate poles closest to the imaginary axis, with the effect of the poles far away from the imaginary axis and the pole-zero pairs that are close to each other are ignored. The system behavior is similar to that of a second order system, and the system is stable when appropriate PI parameters are selected. Note that the further the closed-loop pole is from the imaginary axis, the faster the system dynamic response. At critical damping (closed-loop poles are located on the real axis), the dynamic process under F-SHE attenuates at a frequency of 73rad/s, while under SPWM it is 321 rad/s.

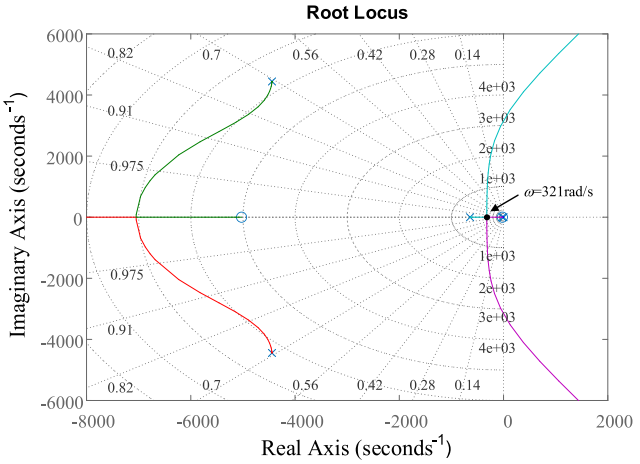

FIGURE 9. Root locus of the linearized open loop transfer function under SPWM.

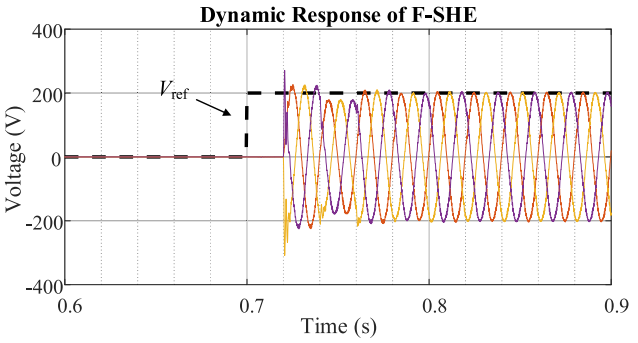

FIGURE 10. Dynamic response of SHE.

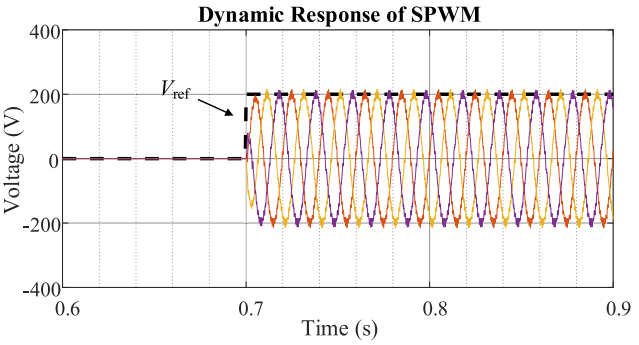

FIGURE 11. Dynamic response of SPWM.

The dynamic response of F-SHE is much slower.

$$e^{-sT_0} = \frac{-s^3 + 600s^2 - 1.5e5s + 1.5e7}{s^3 + 600s^2 + 1.5e5s + 1.5e7} \tag{13}$$

A simulation verification was carried out using the MATLAB Simulink Toolbox with the topology in Fig. 1 and the parameters in Table 1. A reference step from 0 $\sim$ 200V was employed to illustrate the dynamic response of F-SHE and the output voltage waveform is shown in Fig. 10. As a comparison, the output under SPWM is shown in Fig. 11.

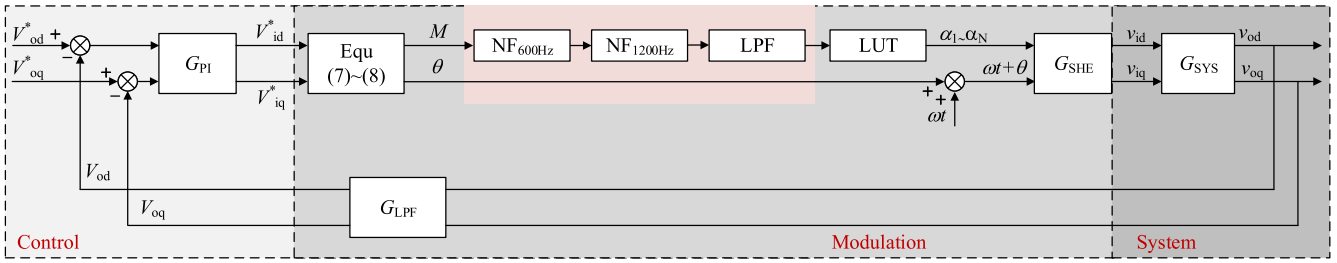

FIGURE 12. Control strategy proposed in this paper.

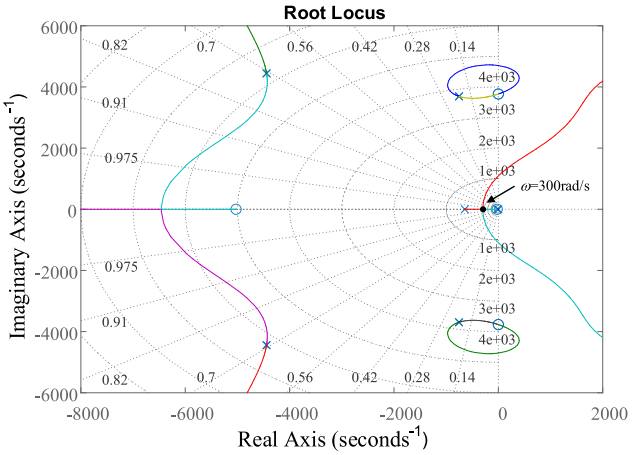

FIGURE 13. Root locus of the improved system under S-SHE.

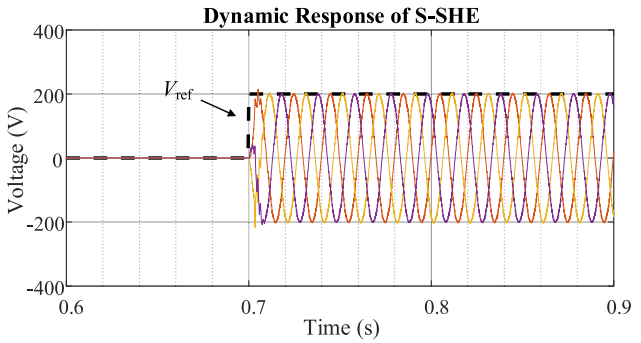

FIGURE 14. Dynamic response of improved S-SHE.

It can be seen that the dynamic of F-SHE is much slower under which it takes 3 fundamental period to track the changes in reference. While in the case of SPWM, less than 1/3 fundamental period is required.

A simple idea to solve the problem is to update the SHE angles per sampling period, just like in SPWM, and thereby cancel out ZOH link. This is the basic idea of this paper. However, it is claimed that the fluctuation in the modulation index M will lead to low order harmonics in the output voltage [42]. In [22] and [42], a low pass filter (LPF) with a cut-off frequency as low as 100Hz is used to deal with this problem. The disturbance of the modulation index is suppressed, but a considerable phase delay is still introduced, i.e., a slow dynamic response.

In a three wire system, the low order harmonics with the highest content coupled into the control loop are 5^{th}, 7^{th}, 11^{th}, and 13^{th}. In a dq coordinate rotating system, these harmonics are transformed to 6^{th} and 12^{th}. This paper proposes an improved S-SHE (Sampling Frequency Updated SHE) control algorithm in which the switching angles are updated at the sampling frequency and a group of filters consisting of two notch filters and a second order low pass filter are employed to stabilize the modulation index as shown in Fig. 12. The negative peaks of the notch filters are designed at 300Hz (6^{th}) and 600Hz (12^{th}), as in (14) ($\omega_{N1} = 2\pi \times 300$) and (15) ($\omega_{N1} = 2\pi \times 600$), respectively. The 2^{nd} order LPF are designed with the cut-off frequency 1000Hz to eliminate the high order harmonics that may be coupled into the control loop. The root locus of the improved system is shown in Fig. 13. It can be seen that the system behavior is still dominated by a pair of conjugate poles and remains stable with proper PI parameters. Further, the frequency of the closed-loop pole is 300rad/s at critical damping which means the dynamic response of the improved S-SHE is close to that of SPWM. The simulation verification is shown in Fig. 14.

$$G_{N1} = \frac{s^2 + \omega_{N1}^2}{s^2 + 2\zeta\omega_{N1}s + \omega_{N1}^2} \tag{14}$$

$$G_{N2} = \frac{s^2 + \omega_{N2}^2}{s^2 + 2\zeta\omega_{N2}s + \omega_{N2}^2} \tag{15}$$

IV. STEADY STATE RESPONSE

SHE modulation stands out for its steady state response. However, in engineering application, there are two main factors that reduce the harmonic performance of SHE, i.e. the step size of the modulation index in the LUT, and the accuracy of the instantaneous phase (ωt in Fig. 12). The former one has been studied a lot in literature [43], while the latter one is rarely discussed. In the hardware implementation of SHE, the PWM signal is generated by comparing the phase of the modulation voltage ($\omega t + \theta$) with the switching angles ($\alpha_0 \sim \alpha_N$) each control cycle. In the steady state, the displacement angle θ stays unchanged while the instantaneous angle ωt increase linearly. In a digital controller, ωt is discretized at a modulation frequency $f_m = 1/T_m$ as shown in

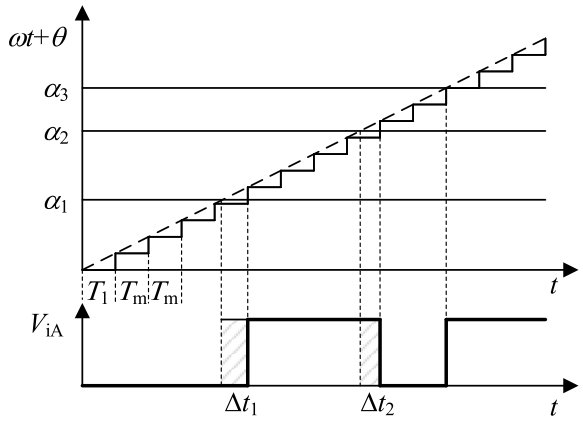

FIGURE 15. SHE modulation process.

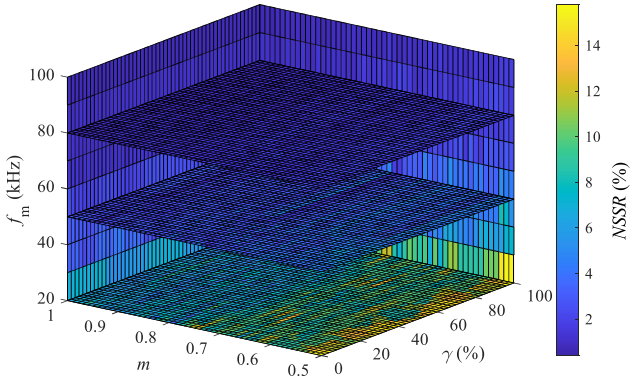

FIGURE 16. *NSSR* of different f_m, m, and γ.

Fig. 15. Due to the limited control speed, the switching instant will have a delay up to one control cycle. This can cause large control errors and reduce the steady-state performance of SHE.

The difference between the actual switching instant and the ideal switching instant will cause (3) no longer hold strictly, and lead to the introduction of low-order harmonics. To directly illustrate the effect of the delay, this paper utilized the normalized square root (NSSR) value defined in (16) as an evaluation indicator. Note that v_{1m} and v_{nm} denote the magnitude of the fundamental and n^{th} harmonic component of the SHE waveform, respectively. The *NSSR* represent the content of the low order harmonics that are supposed to be eliminated in an ideal SHE modulation process. Thus, the smaller the *NSSR* value is, the better the steady state performance is.

$$NSSR = \sqrt{\sum_{n\in\mathbb{H}} \frac{v_{nm}^2}{v_{1m}^2}} \tag{16}$$

As shown in Fig. 15, the delay of the switching time is related to the relative position of the discrete instantaneous phase and the switching angles which is described using three variables f_m, m, and γ. f_m denotes the modulation frequency ($T_m = 1/f_m$), m denots the modulation ratio which determines the specific distribution of the switching angles, and γ denotes the phase relationship between the discrete and ideal instantaneous phase, as defined in (17).

$$\gamma = \left(1 - \frac{T_1}{T_m}\right) \times 100\% \tag{17}$$

The *NSSR* at different f_m, m, and γ are calculated using the switching angles in Fig. 3, and ploted in Fig. 16.The following conclusions can be made:

1) Modulation frequency f_m has the greatest impact on *NSSR*. As f_m increases, *NSSR* decreases rapidly, and the influence of m and γ gradually decreases. It is because the steady-state performance of SHE modulation approaches ideal characteristics when the modulation frequency increases.
2) At lower f_m, the higher the modulation ratio is, the smaller the *NSSR* is, and the better the steady-state performance. This is consistent with the case under SPWM modulation. The bigger m is, the fundamental content is higher, and the proportion of harmonics is smaller.
3) At lower f_m, *NSSR* is nonlinearly affected by γ which is due to the nonlinear distribution of the switching angles (as shown in Fig. 3).

It can be seen from the above analysis that increasing the modulation frequency f_m can greatly improve the steady-state performance of SHE modulation. In particular, when the system has a large operating range (it is possible to run at low modulation ratio), increasing the modulation frequency has a more substantial improvement. However, higher modulation frequency will bring higher hardware costs. In this paper, a modulation frequency of 50kHz is selected because the *NSSR* is small enough, and the minor improvement brought by higher frequencies is not necessary as shown in Fig. 16.

V. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

In other researches, the implementation of SHE is generally achieved by a microcontroller unit (MCU) and a field programmable gate array (FPGA), where MCU is responsible for sampling and control procedures, and FPGA is responsible for SHE modulation [10], [42]. A large scale of FPGA is usually needed as the number of the switching angle increases because a large amount of switching angle data and control information need to be transmitted between MCU and FPGA. The communication also needs to be carefully designed to ensure transmission speed and the accuracy.

In this paper, a dual core DSP TMS320F28377D and a small scale FPGA is adopted to realize the SHE modulation as shown in Fig. 17. All the sampling, control, and modulation procedure are accomplished in the DSP. And the FPGA bears only the work of adding dead-zone to the SHE PWM signals which is omitted in Fig. 17. The dual

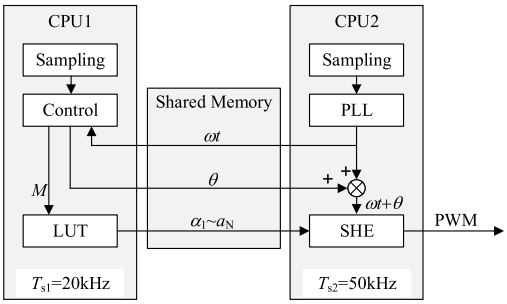

FIGURE 17. Hardware implementation.

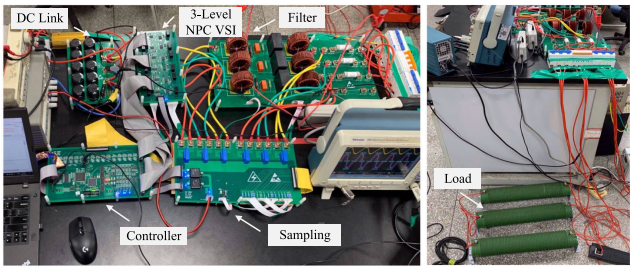

FIGURE 18. Experiment platform.

TABLE 2. Experiment Parameters.

Modulation	F-SHE	S-SHE	SPWM
Switching angle number /Carrier frequency	$N = 15$	$N = 15$	1500Hz
Switching frequency	750Hz	750Hz	750Hz
RLC filter	$R = 2\Omega$, $L = 3$mH, $C = 22\mu$F		
PI controller	$k_p = 0.1$ $k_i = 50$	$k_p = 0.1$ $k_i = 500$	$k_p = 0.1$ $k_i = 500$
Sampling frequency	20kHz	20kHz	20kHz
Modulation command update frequency	50Hz	20kHz	20kHz

cores (CPU1 and CPU2) run in parallel. CPU1 executes the sampling and control program in an interrupt service routine (ISR) at a frequency of 20kHZ, while CPU2 executes the SHE modulation program in 50kHz ISR in order to reduce the steady state error caused by the discretization as described in section V.

To verify the proposed method, a 6.6kVA experiment platform (shown in Fig. 18) which is composed of a three phase diode rectifier, DC link capacitors, a 3-level NPC inverter, and resistive loads was built. Three comparative experiments were implemented, including regular F-SHE modulation, improved S-SHE modulation, and SPWM modulation. Except for the modulation method, the hardware parameters and control strategies are all the same. Note that the PI parameters under F-SHE modulation are different from that under S-SHE modulation and SPWM modulation. It is because that the large phase dealy in the F-SHE algorithm reduces the system bandwidth and the PI parameters are limited for stability reasons. Detailed experiment parameters are shown in Table 2.

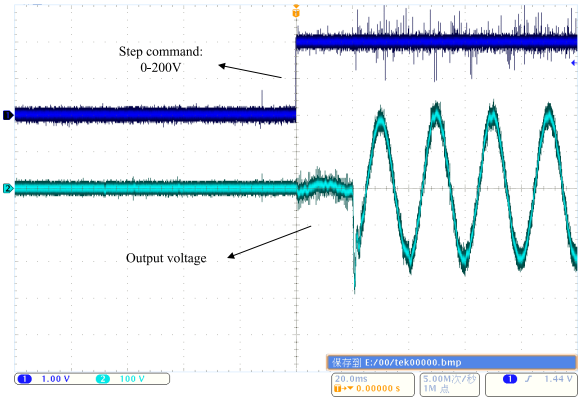

FIGURE 19. Dynamic response under F-SHE modulation.

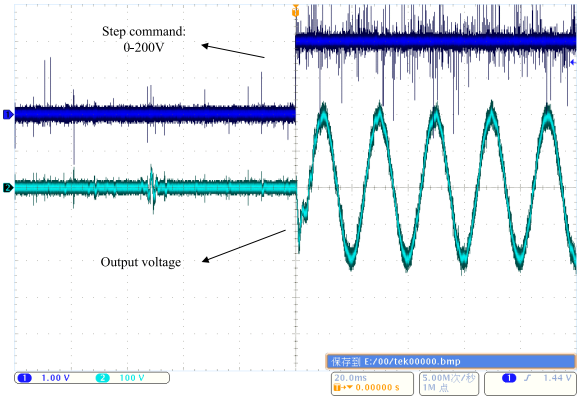

FIGURE 20. Dynamic response under S-SHE modulation.

A. DYNAMIC RESPONSE

Under a 0–200V step command of the output voltage, the dynamic responses of the F-SHE, S-SHE, and SPWM modulation are shown in Fig. 19, Fig. 20, and Fig. 21, respectively. It can be seen that the dynamic response of the F-SHE is much slower. It takes more than 2 fundamental period for the output voltage to track the step command. Furthermore, the overshoot in the dynamic process is very large. This is because the modulation command (switching angles data) is updated after a fundamental period, during which the output remains unchanged but the PI controller continuously integrates the feedback error (at the sampling frequency 20kHz), thereby increasing the step size acts on the inverter. This is the prime reason that bigger PI paramters will lead to instability under F-SHE modulation. Comparing Fig. 20 and Fig. 21, the dynamic response of S-SHE is almost as fast as SPWM. The output voltage quickly follows the step change of the command in both cases. And the overshoot is much slower than that in F-SHE which is because there is much smaller phase delay between control and modulation. In summary, the S-SHE modulation method proposed in this paper has greatly improved the dynamic response of the regular F-SHE method and performs as fast as the widely used SPWM.

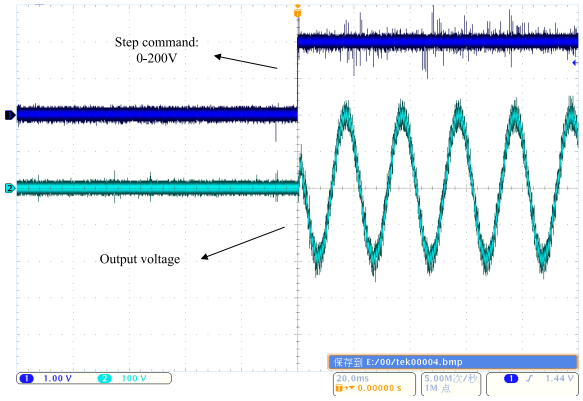

FIGURE 21. Dynamic response under SPWM modulation.

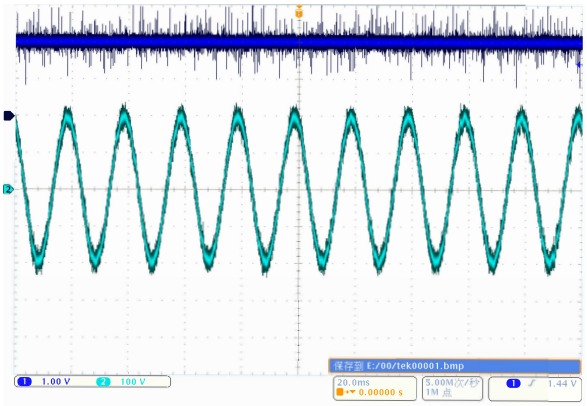

FIGURE 22. Steady state response under F-SHE modulation.

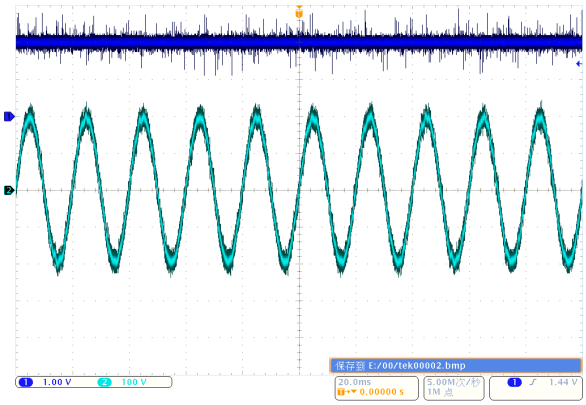

FIGURE 23. Steady state response under S-SHE modulation.

B. STEADY STATE RESPONSE

The steady state responses of the F-SHE, S-SHE and SPWM modulations are shown in Fig. 22, Fig. 23, and Fig. 24, respectively. And the corresponding FFT analysis is shown in Fig. 25, Fig. 26, and Fig. 27. It can be seen that the F-SHE algorithm has the best harmonic performance with the THD value as low as 2.83%. There exist a few low-order harmonics (below 2%) which are caused by the error of the discretized

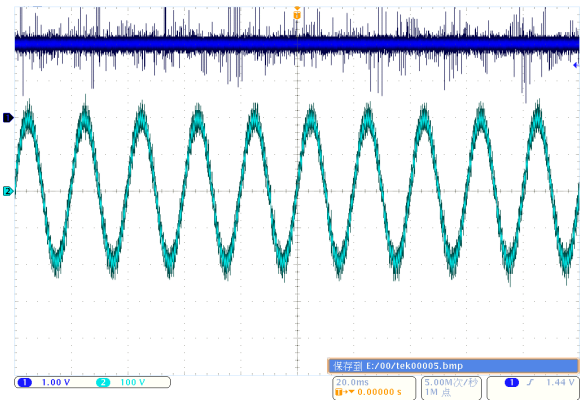

FIGURE 24. Steady state response under SPWM modulation.

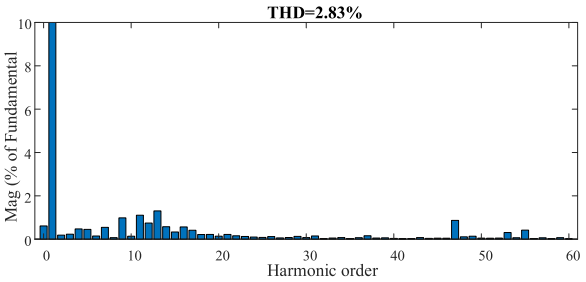

FIGURE 25. Steady state response under F-SHE modulation.

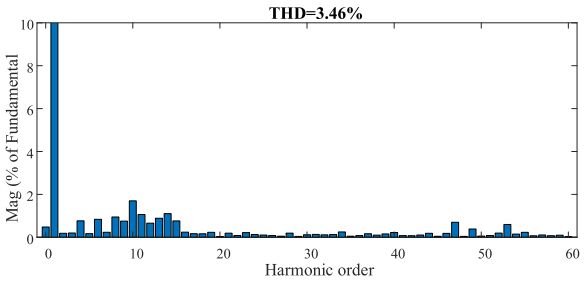

FIGURE 26. Steady state response under S-SHE modulation.

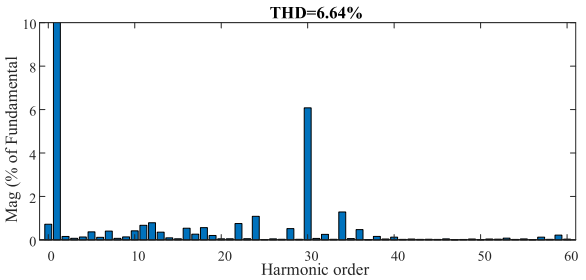

FIGURE 27. Steady state response under SPWM modulation.

control system. The lowest uneliminated harmonic (47^{th}) is attenuated to a sufficiently low level by the filter. The experimental results have proved the superiority of the regular F-SHE in the terms of harmonic performance. As shown in Fig. 23 and Fig. 26, the harmonic performance of S-SHE

proposed in this paper is slightly worse than that of F-SHE with the THD value increased from 2.83% to 3.46%. This is because there exists small disturbance in the switching angles which are updated at the sampling frequency. As a consequence, the SHE waveform is NOT strictly symmetrical and the content of the low-order harmonics slightly increases (still below 2%). Nevertheless, the harmonic performance of S-SHE is still far better than that of SPWM as shown in Fig. 27. In addition to a few low-order harmonics caused by control errors, there exist a large number of switching order harmonic (around 6%) at the case of SPWM. Under the condition of the same switching frequency, the lowest harmonic frequency of SPWM (switching frequency, 30^{th}) is much lower than that of SHE (47^{th}). To achieve the same harmonic performance as SHE, either the switching frequency of SPWM or the size of the passive filter must be increased. In summary, the steady state performance of S-SHE proposed in this paper is slightly worse than that of the regular F-SHE but still far better than SPWM.

VI. CONCLUSION

This paper proposed an improved S-SHE modulation technique where the switching angles are updated at sampling frequency. With the utilization of notch filters and low-pass filters, the system guarantees a high bandwidth. Both simulation and experimental results validate that the proposed S-SHE achieves as good dynamic as SPWM modulation, but at the expense of a small amount of steady-state response, which is slightly worse than the regular F-SHE, but still much better than SPWM. In addition, this paper analyzes the influence of control error on steady-state performance during hardware implementation, and gives a visualization method of modulation frequency selection. A simple DSP with a small scale FPGA hardware structure is introduced to realize the above method. Hardware platform is built and experimental results are provided.

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JINGLING CHENG received the B.S. degree in electrical and electronics engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering with the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His current research interests include high power grid connected converters, modulation techniques, and control strategies under low switching frequency.

TINGTING XU was born in Jiangsu, China. She received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2017. She is currently pursuing the M.S. degree in electrical engineering with Zhejiang University, Hangzhou, China.

Her research interests include offshore micro grids, and energy management systems.

DONGDONG CHEN received the B.S. degree in electronic information engineering from Zhejiang University, Hangzhou, China, in 2013, and the Ph.D. degree in electrical engineering from the College of Electrical Engineering, Zhejiang University, in 2018.

He is currently a Vice Professor with the Minnan University of Science and Technology. His research interests include power electronics system design, power converter digital control, and optimal design.

GUOZHU CHEN (Member, IEEE) received the B.S. degree in electronics from Zhejiang Gongshang University, Hangzhou, China, in 1988, and the M.S. and Ph.D. degrees in power electronics from Zhejiang University, Hangzhou, in 1992 and 2001, respectively.

In 1992, he joined the College of Electrical and Engineering, Zhejiang University, as a Faculty Member, where he was a Lecturer, from 1993 to 2000, an Associate Professor, from 2000 to 2005, and a Full Professor, since 2005. He has authored or coauthored one book, more than 130 journal articles, and more than 100 conference papers, and holds about 23 invention patents. His research interests include high-power electronics applications and their digital control; active power quality control, such as APF, UPQC, SVC, dSTATCOM, and dFACTS; grid connection of renewable energy/distributed power generation; large-capacity distributed energy storage systems (BESSs); power electronics system integration (PEBB) and high reliability (PSI, PI, and EMC) technology; and converters for smart grid and special power supplies. He has been the "New Century Excellent Talents in University" (2006, by the Chinese Ministry of Education), the Core Team Member of the "Zhejiang Key S&T Innovation Group Program of new energy and power electronics," in 2010, the "Elite Talent of Southern Taihu Science and Technology Plan," in 2012, and the "Thousand People Plan, Specially-Invited Expert, Zhejiang Province," in 2013. He was a recipient of ten scientific research awards, including the Second-Class S&T Progress Prize of the Chinese Ministry of Education, and the First-Class S&T Progress Award of Zhejiang Province, China.