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A Single Parameter Voltage Adjustable Immittance Topology for Integer- and Fractional-Order Design Using Modular Active CMOS Devices

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ABSTRACT A simple single parameter adjustable immittance concept designed with modular active devices, fabricated in I3T25 0.35 μm 3.3 V CMOS process of ON Semiconductor, is introduced. The proposed devices employ an integer-order capacitor and specifically designed fractional-order capacitors (sometimes called constant phase elements). The proposed active topology consists of two simple active elements, namely a linearly voltage adjustable operational transconductance amplifier and a voltage differencing unity gain voltage follower/buffer, and only two passive elements, i.e. redundancy is minimized. The designed topology offers generation of an adjustable immittance having both the capacitive and inductive character. The importance of the order as well as the value of the pseudo-capacitance for design and analyzes are shown, including all important parasitic features for estimation of expected operational bandwidth which have to be considered in the design. The operational bandwidth is determined by high values of approximants of fractional-order capacities (225, 56 and 8.8 μF/sec^1-α, where α represents the order equal to 0.25, 0.5 and 0.75, respectively). These parameters result into ranges between tens of Hz and units-tens of kHz. The adjustability of the transconductance from 70 to 700 μS by the driving voltage between 0.05 and 0.5 V offers approximately one decade change of equivalent capacitance and inductance. Laboratory-based experiments done with a fabricated prototype confirmed the theoretical presumptions.

INDEX TERMS Capacitance multiplier, CMOS, constant phase element, fractional-order, immittance generation, linear voltage adjustment, synthetic inductance.

I. INTRODUCTION

Various active elements and analog constructing parts [1], [2] allow a design of standard as well as special building parts of modern communication and signal processing systems. Circuits for impedance function synthesis of inductive, capacitive and other special characters (frequency dependent negative resistor, etc. [2]) represent very useful and popular blocks in the design of analog and mixed-signal systems. The basic topology of active circuitry for generation of various immittance functions using standard operational amplifiers (opamps) is referred to as the generalized immittance converter [3], [4]. A simple interchange of the positions of standard R and C passive elements offers a selection of a specific impedance character. Unfortunately, the lack of electronically adjustable parameters of opamps limits the allowed signal operations and does not allow direct electronic adjustment of applications. However, there are other active devices. They use mutual conversion between signal operations with voltage as well as current (or both simultaneously), having possibilities of adjustment of gains (transfers) and conversion constants between terminal features of these active device [1].

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Such devices improve the adjustability of the designed immittance functions when opamps are replaced by these devices, for instance by operational transconductance amplifiers (OTAs) [5]. Survey of solutions reported in recent literature will be discussed in Section II.

This work targets at the design of a very simple adjustable integer- as well as fractional-order immittance [5], [6] allowing single parameter electronic adjustment of equivalent values of two specific functions: capacitance multiplier (equivalent value – C_{eq}) and synthetic inductance simulator (equivalent value – L_{eq}). Aims of our design that are not available simultaneously in recent literature can be summarized as follows:

1) A simple circuitry (two active devices; electronic adjustment by tuning of internal parameters of single device – no necessity of matching of parameters, no additional redundancy),
2) No replacement of the resistor by electronically adjustable equivalent (MOSFET) in order to obtain a controllable parameter,
3) Comfortable and standardly required (available by digital-to-analog converters) linear driving of transconductance by a DC voltage (L_{eq} or C_{eq} value giving approximately one-decade readjustment – in both cases: integer-order and fractional-order approach) in order to simplify the control of applications (immittance value),
4) No necessity of a special additional circuitry for linearization of dependence of transconductance on driving force,
5) Scalable range (adjustable magnitude and range of L_{eq} or C_{eq} can be shifted by the value of the resistor the second passive element of the topology having a constant value during the adjustment procedure),
6) Both active devices in the topology were fabricated (CMOS 0.35 μm ON Semiconductor process) and integrated in a single IC package.

The rest of this paper is organized as follows. The state-of-the-art of single parameter electronically adjustable solutions of immittance converters is elaborated in Section II. The proposed solution is compared with the most important of similar concepts from literature in the area of integer- as well as fractional-order applications. Principles of active devices in the designed topology are introduced in Section III. The proposed circuitry and definition of its operation are presented in Section IV. Practical modeling including the most significant non-idealities, experimental setup for measurement and the obtained results for integer-order behavior are shown in Section V. Fractional-order behavior of the proposed circuitry is studied in Section VI. Concluding remarks are given in Section VII.

II. STATE-OF-THE-ART

The survey of single parameter electronically adjustable solutions of immittance converters, presented in this section, is divided into two parts. The first one is focused on integer-order solutions. Attention to the fractional-order solutions is given in the second part of this section. The difference between integer- and fractional-order solutions consists in frequency behavior of impedance magnitude and phase, as clear from these equations: $Z_{IN\_L}(s) = L_{eq} \cdot s^{\alpha}$; $Z_{IN\_C}(s) = 1/(C_{eq} \cdot s^{\alpha})$. Fractional-order solution performs "arbitrary" magnitude slope and constant phase equal to $\pm\alpha \cdot \pi/2$ (in limits of approximation validity) in frequency domain for $0 < |\alpha| < 1$. Integer-order devices have fixed $\alpha = 1$. Their phase response reaches "constant" value $\pm\pi/2$ ($\pm 90°$) for L_{eq}, C_{eq}.

A. INTEGER-ORDER SOLUTIONS

Devices based on integer-order solutions serve for intentional change of the value of capacity or inductance (including conversion from capacity [5], [6]) by an additional multiplicative parameter (called multiplication factor). This parameter is used for intentional increasing or decreasing of the value of capacity/inductance beyond the value of the original passive element (usually capacitor). These solutions are designed with the help of active elements with controllable parameters used for adjustability of the multiplication factor. In our work, we assume a single-parameter control. However, there are concepts where the multiplication factor depends on several parameters (see the list of references in [7]). However, our attention is focused on lossless solutions allowing C_{eq} and L_{eq} controllability by a single active parameter (transconductance in majority of cases) due to elimination of redundancies. The comparison of recent solutions employing various active elements with concept proposed in this paper is given in Table 1. These solutions can be found as useful also for the fractional-order design. Note that many works target on enlargement of adjustability by a combination of many active parameters influencing the multiplication factor. There are solutions focusing on the coincidence of transconductances (g_m) and resistances of the current input terminal (R_X) [8], coincidence of g_m and an externally adjustable replacement (by MOSFET transistor) of resistor [9], product and division of several g_m-s [10] or multiplication of several R_X parameters [11]. The matching (equality and simultaneous change) of parameters is useful and beneficial, but it requires a very accurate design. Moreover, these solutions either require more than two active devices [10] or they have a complex internal topology even when the active device is reported as a single device [11]. Unfortunately, many of such devices are not available on the market.

According to the survey presented in Table 1, the following conclusions were established:

a) Maximally two simple [14], [15] or one single active device composed from internal subparts [12], [13], [16]–[27], where some devices have more sophisticated internal complexity [19]–[22], are sufficient for construction of a capacitance multiplier,
b) Most of the proposed topologies offer only one type of the requested immittance character (C_{eq} or L_{eq}), both functions are available rarely [24]–[26],

TABLE 1. Survey of Single parameter (without matching conditions) electronically adjustable capacitance multipliers and lossless inductance simulators suitable for adjustment of fractional-order element approximants.

Reference	Number of passive; Active devices	Type of active device (total number of transistors), supply voltage	Simple active devices (minimal number of internal parts – where applicable)	Multiplication of parameter(s)	Connection of Z_1, Z_2	Approximate tested frequency range	Experimental fabrication and testing	Type of adjustment (controlled value of), where B stands for current gain	Type of driving force	Dependence of adjustable parameter on driving force	Dependence of C_{eq} parameter on driving force	Dependence of L_{eq} parameter on driving force	Operation without additional converter and linearization for driving by DC voltage	Fractional-order design/configuration tested	Another parameter (resistor) required for scalability	Experimental laboratory tests	Active devices fabricated in CMOS process as a single IC package	Power consumption [mW]
[12]	2; 1	VDBA (11), ±1.5 V	Yes	C_{eq}	f,g	100 Hz – 10 MHz	No	g_m	I_{SET}	linear	linear	N/A	No	No	Yes	No	No	0.89
[13]	2; 1	FB-VDBA (20), ±0.75 V	Yes	C_{eq}	f,f	1 kHz – 100 MHz	No	g_m	I_{SET}	nonlinear	nonlinear	N/A	No	No	Yes	No	No	7.4
[14]	2; 2	CCII, OTA (33), ±5 V	Yes	L_{eq}	f,g	0.01 Hz – 10 MHz	Yes+	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	Yes	No	N/A
[15]	2; 2	CFOA, OTA (N/A), ±5 V	Yes	C_{eq}	g,g	1 Hz – 1 GHz	Yes+	g_m	I_{SET}	linear	linear	N/A	No	No	Yes	No	No	N/A
[16]	2; 1	VDCC (22), ±0.9 V	Yes	L_{eq}	g,g	10 kHz – 100 MHz	No	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	No	No	0.87
[17]	2; 1	VDCC (22), ±0.9 V	Yes	L_{eq}	g,g	1 kHz – 10 MHz	No	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	No	No	N/A
[18]	2; 1	VDBA (N/A), ±5 V	Yes	L_{eq}	f,f	1 kHz – 100 MHz	Yes	g_m	N/A*	N/A	N/A	N/A	N/A	No	Yes	Yes	No	N/A
[19]	2; 1	VD-DIBA (>24), ±0.9 V	No	L_{eq}	g,g	1 kHz – 10 MHz	No	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	No	No	62.5
[20]	2; 1	VDDDA (N/A), ±5 V	No	L_{eq}	f,g	100 Hz – 10 MHz	Yes	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	Yes	No	N/A
[21]	2-3; 1	EXCCTA (40), ±0.9 V	No	L_{eq}	g,g	1 kHz – 100 MHz	Yes+	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	Yes	No	N/A
[22]	2; 1	VDCC (22), ±0.9 V	No	L_{eq}	g,g	1 kHz – 100 MHz	No	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	No	No	N/A
[23]	2; 1	VDBA (9), ±0.75 V	Yes	L_{eq}	f,f	1 kHz – 100 MHz	No	g_m	I_{SET}	nonlinear	N/A	nonlinear	No	No	Yes	No	No	0.35
[24]	2; 1	DXCCDITA (35), ±1.5 V	No	$C_{eq}L_{eq}$	f,g	100 Hz – 100 MHz	No	g_m	I_{SET}	nonlinear	nonlinear	nonlinear	No	No	Yes	No	No	N/A
[25]	2; 1	VDCC (21), N/A	Yes	$C_{eq}L_{eq}$	f,g	1 kHz – 100 MHz	No	g_m	I_{SET}	nonlinear	nonlinear	nonlinear	No	No	Yes	No	No	N/A
[26]	3; 1	VCA822 (N/A), ±5 V	No	$C_{eq}L_{eq}$	f,f	100 Hz – 20 MHz	No	B	V_{SET}	linear	linear	nonlinear	Yes	Yes	Yes	No	No	N/A
[27]	2; 1	VD-DIBA (22/44), ± 2 V	Yes	L_{eq}	f,g	1 Hz – 10 GHz	No	g_m	V_{bias}	nonlinear	N/A	N/A	No	No	Yes	No	No	N/A
This work																		
Fig. 3	2; 2	OTA, DVB (75), ± 0.9 V	Yes	$C_{eq}L_{eq}$	g,f	100 Hz – 1 MHz	Yes	g_m	V_{SET}	linear	linear	nonlinear	Yes	Yes	Yes	Yes	Yes	20

* Not Available (not tested); f – floating; g – grounded; + using CMOS elements for simulations but standard off the shelf active devices for experiment (different band and design specification than in CMOS simulations); VDBA – voltage differencing buffered amplifier; FB-VDBA - fully balanced-voltage differencing buffered amplifier; CCII – current conveyor of second generation; OTA – operational transconductance amplifier; CFOA – current feedback operational amplifer; VDCC - voltage differencing current conveyor; VD-DIBA - Voltage Differencing Differential Input Buffered Amplifier; VDDDA – voltage differencing differential difference amplifier; EXCCTA - extra X current conveyor transconductance amplifier; DXCCDITA – Dual X current conveyor differential input transconductance amplifier; DVB- differential voltage buffer

c) Most of the solutions use a driving current for the nonlinear adjustment of nonlinear transconductance (for large values of input voltage) in simple or basic OTA topologies [12]–[25],
d) In many cases, dependence of transconductance on the bias driving current (or directly on bias voltage) is nonlinear (CMOS concepts) [13], [14], [16], [17], [19]–[25], [27] (linear only for active devices with internal structures based on bipolar transistors [12], [15]) and the nonlinearity of parameter adjustment has also an impact on the character of tuning of C_{eq},
e) Additional conversion (and linearization) of the driving current to DC voltage is required in many cases for adjustability range extension, except of [26] (lack of straightforward linear adjustment by control voltage in almost all cases),
f) All solutions require also a passive parameter (except the controllable transconductance) for scalability of the adjustable range and,
g) Only several solutions were tested experimentally [14], [18], [20], [21] and for fractional-order design.

The circuit topologies introduced in [20] and [27] are the most similar to our proposal. However, in the case of [20], there are significant differences in the: a) dependence of g_m on the driving force (voltage vs current), b) topology (connection of the feedback passive element), c) availability of L_{eq} and, d) way of verification (commercially available devices in [20]).

In the case of [27] differences are in: a) nonlinear dependence of g_m on the driving bias voltage, b) tested availability of L_{eq} and c) way of verification using basic differential CMOS pairs (OTAs). In addition, many performances used in Table 1 are not available (verified) in [27].

It can be easily revealed that the power consumption is not among the monitored parameters (see Table 1). In general, the values of the power supply can be found between ±0.7 and ±5 V. The power consumption is expected maximally from tens of μW up to hundreds of mW (for bipolar solutions). In our case, it is below 20 mW at 3.3 V (±1.65 V) occupying an area of 0.23 mm^2. The frequency properties of each prototype differ and also depend on the value of the working capacitor (passive element) as well as on the capability of the active device (given technologically – design and fabrication process). The operational ranges are between kHz and tens of MHz. Therefore, a comparison of these features is not suitable or even available for an objective evaluation and judgement. Our design focuses on the frequency range of tens of Hz up to tens of kHz.

B. FRACTIONAL-ORDER SOLUTIONS

1) FRACTIONAL-ORDER IMMITTANCES AND THEIR APPROXIMATION

The fractional-order behavior of the real world was expected and proved several centuries ago. However, it started to be important especially in recent years [28], [29] (for researchers from electrical engineering and many other fields). The fractional-order design of synthetic elements is not a new phenomenon. First attempts started with simple opamps and Antoniou's generalized immittance converter [3], [4], where researchers have used fractional-order elements. Recent development indicated that these elements can be designed in

the form of solid-state devices based on various approaches, e.g. electrochemical materials [30], [31], electrolytes [32], polymer composites [33], [34], layers of resistive, dielectric and insulating materials [35]. However, these devices are not easily accessible, for instance in a form of standard passive elements series (R, C, L). Therefore, many methods of approximation of fractional-order devices by passive elements have been developed [36]–[38]. Such devices are also known as constant phase elements (CPEs) [37], [38]. These devices have a limited range of validity and accuracy of approximation in both magnitude and phase responses.

2) DISCUSSION OF RECENT DEVELOPMENT

Work [39] shows a typical basic concept of a fractional-order immittance converter using opamps and a solid-state based fractional-order device. It was tested in various topological positions of the Antoniou circuit. This concept was used also for various tested orders and C_{eq}, L_{eq} cases by Adhikary *et al.* [40]. However, these circuits have a lack of electronic adjustability and compared to concepts presented in Table 1, they are quite complex. Khattab *et al.* [41] have shown that the implementation of current feedback opamps offers significant simplification in comparison with standard opamps (fractional-order device was represented by CPE). Unfortunately, electronically adjustable properties are also not available in the concept [41]. Dimeas *et al.* [42] introduced different ways of approximation of a fractional-order device. The fractional-order behavior was obtained as a voltage-to-current conversion at the input terminal of the voltage-mode transfer response representing a high-order multi-loop filter with specific setting of the transfer response. It offers reconfiguration of the fractional-order device (order and character - C_{eq} or L_{eq}) as well as tunability of the multiplication factor. Unfortunately, these concepts are quite extensive and are using many active and passive devices. Similar fully electrically adjustable form using operational transconductance amplifiers was developed by Tsirimokou *et al.* [43] in a form of a fully integrated concept (on chip). Unfortunately, its complexity compared to passive approximants of CPE is very high. Herencsar [44] worked with fractional-order passive approximants (CPEs) together with special electronically adjustable current feedback amplifiers. His design introduced features similar to our proposal, but single-parameter electronic adjustability is not possible and L_{eq} expects matching of two small-signal resistances of a current input terminal (nonlinear driving by a DC current) that represents significant drawback. A solution allowing a configuration of the fractional-order active immittance functions electronically is shown in [45]. The concept in [45] uses operational transconductance amplifiers and a feedback loop also offering $C_{eq} \leftrightarrow L_{eq}$ interchange even without any voltage-to-current conversion as required in [43]. As it was in the case of [43], overall complexity of structure [45] for discrete construction is high. Dvorak *et al.* [46] simulated the fractional-order capacitor in a similar way, employing extensive topology with many advanced active devices. This active solution has benefits of reconfigurability of the order and C_{eq}, but the power consumption reflects necessity of numerous active devices as in previous cases [43], [45]. The circuit topology of the fractional-order inductance proposed by Jain *et al.* [47] uses two special active devices based on operational transconductance amplifiers and RC ladder topology of CPE. Electronic adjustability of L_{eq} is possible by two transconductances simultaneously. Unfortunately, the obtainment of C_{eq} is not discussed as well as details about adjustability and tunability. Kubanek *et al.* [48] analyzed the features of CPE usage in a standard loop of two transconductors-based gyrator including real properties of the active devices [5]. All consequences of parasitic properties of active devices are important for a correct selection of values of elements and precise results as well as a design guide [48]. Authors of [26] (included in comparison with integer-order solutions in Table 1) have shown a very simple topology utilizing a single commercially available active device including several integrated subparts (current conveyors, adjustable current amplifier, current feedback operational amplifier [1], [2]). The specific arrangement of subparts offers various interconnections that result in integer- or fractional-order (tested with CPE) electronically adjustable (current gain) capacitor, inductor, and frequency dependent negative resistor requiring three external passive elements (CPE is always taken into account as a single element without consideration of the RC ladder character). When compared to [26], the design presented in this paper offers several benefits, namely: simplicity, a simple interchange of $C_{eq} \leftrightarrow L_{eq}$ by interchange of CPEs, a fully integrated form of active elements (CMOS) and linear adjustment of transconductance by DC voltage.

Our circuit can be easily utilized in electronically tunable resonators [43], [49] as well as in oscillators with settable phase shift between generated waveforms (see [50] and references cited therein), as construction parts of fractional-order RLC filters (for example [47]), and in modeling of various behavior in electrical, and general engineering and natural sciences [28], [29].

From the above presented survey, it can be concluded that tens of solutions of integer-order immittance converters exist (non-tunable, electronically tunable, differential, using families of various active devices, etc.). However, only several topologies and concepts of fractional-order immittance converters have been studied. As it was shown in [51], this field still has many open challenges.

III. INTRODUCTION OF ACTIVE DEVICES

Simplicity and flexibility of the proposed application are among the most important aspects of any circuit design [1], [2], [26], [27], [52], [53]. Many special active devices offers very simple fulfilment of these requirements in comparison with standard opamps. Our paper [52] focused on the performances of specially designed active sub-blocks (cells) suitable for various electronically adjustable applications

including basic signal operations (sum, subtraction, integration, differentiation, amplification, multiplication) in frequency band approx. up to units of MHz [52], [53]. These active sub-blocks were fabricated in I3T25 0.35 μm 3.3 V CMOS process of ON Semiconductor company and they are available in a single IC package. Our following design requires only two of these devices.

The voltage multiplier (MLT) with current output terminal [53], [54] can be easily used as an OTA [1], [5] when one from two pairs of the input differential voltages serves for driving by DC voltage V_{SET_gm}, as it is shown in Fig. 1 a). Thereby, the device behaves as an OTA having linearly adjustable g_m (see Fig. 1 b)). The transconductance constant $k \cong 1.4 \cdot 10^{-3}$ mA/V^2 is given technologically and the transconductance can be expressed as $g_m \cong 1.4 \cdot 10^{-3} \cdot V_{SET\_gm}$.

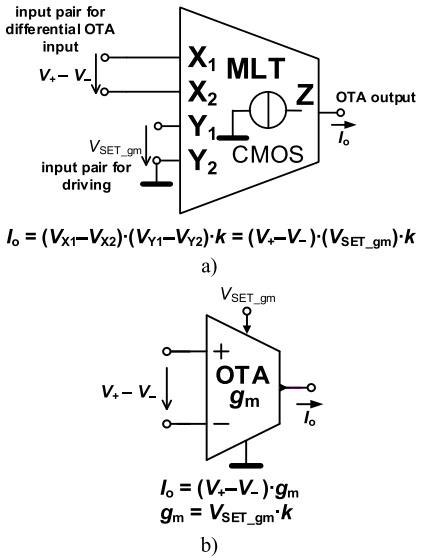

FIGURE 1. Electronically adjustable device (transconductance): a) principle of multiplier, b) schematic symbol of OTA created by MLT with inter-terminal relations.

The so-called voltage differencing differential buffer (VDDB) [53] provides useful linear signal operations. The basic idea is shown in Fig. 2 a). Our designed topology assumes subtraction of nodal voltages. Thereby, as it is depicted in Fig. 2 b), VDDB can be simplified into a simple differential voltage buffer (DVB) having unity gain. All details about parameters of these devices are available in [52] and [53]. Both devices occupy an area of 0.23 mm^2 with power dissipation below 20 mW.

IV. GENERAL VOLTAGE ADJUSTABLE IMMITANCE CONVERTER AND INVERTER

The proposed circuits based on one topology are shown in Fig. 3, where the active devices are actually implemented as single-package integrated circuit. The topology of our simple circuitry consists of a voltage adjustable OTA and a DVB complemented by two passive elements marked (in basic

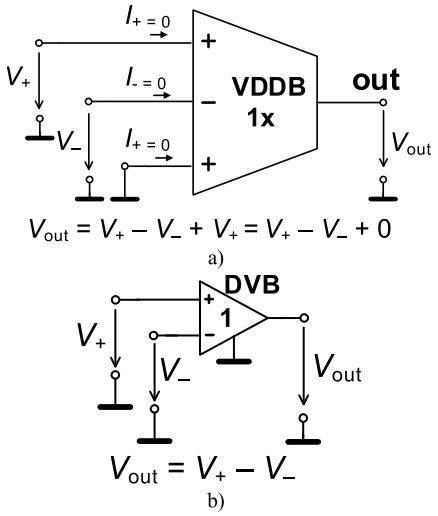

FIGURE 2. Device for simple signal operation of subtraction: a) principle of VDDB, b) schematic symbol of DVB created by VDDB with inter-terminal relations.

principle) as general impedances. The ideal form of the input impedance of the circuit can be calculated as:

$$Z_{IN}(s) = \frac{1}{g_m} \cdot \frac{Z_2(s)}{Z_1(s)} \cong \left(\frac{1}{1.4 \cdot 10^{-3} \cdot V_{SET\_gm}} \right) \cdot \frac{Z_2(s)}{Z_1(s)}. \quad (1)$$

Configuration of the character of the input impedance is possible by the selection of Z_1(s) and Z_2(s). The replacement of Z_1 and Z_2 by a resistor and a fractional-order capacitor changes the input impedance of the device (see Fig. 3b)) as follows:

$$Z_{IN\_C}(s) = \frac{1}{s^\alpha C_{eq}} = \frac{1}{s^\alpha C_\alpha R g_m} \cong \frac{1}{s^\alpha C_\alpha R} \left(\frac{1}{1.4 \cdot 10^{-3} \cdot V_{SET\_gm}} \right). \quad (2)$$

This configuration creates an adjustable fractional-order capacitance multiplier having the capacitance multiplication factor given by the product $R \cdot g_m$ (i.e., $R \cdot 1.4 \cdot 10^{-3} \cdot V_{SET\_gm}$). The equivalent capacity is expressed as $C_{eq} = C_\alpha \cdot R \cdot g_m$. Such a feature offers adjustability of equivalent capacity by a DC driving voltage influencing the g_m transconductance. Parameter α represents the order of the capacitor (fractional-order for $0 < \alpha < 1$). When $\alpha = 1$, an integer-order solution is obtained and Z_2(s) is actually represented by a standard capacitor.

Interchange of positions of both elements $Z_1(s) \leftrightarrow Z_2(s)$ in the circuit creates a fractional-order electronically adjustable synthetic inductance (see Fig. 3 c)) with the following input impedance:

$$Z_{IN\_L}(s) = s^\alpha L_{eq} = \frac{s^\alpha C_\alpha R}{g_m} \cong s^\alpha C_\alpha R \left(\frac{1}{1.4 \cdot 10^{-3} \cdot V_{SET\_gm}} \right). \quad (3)$$

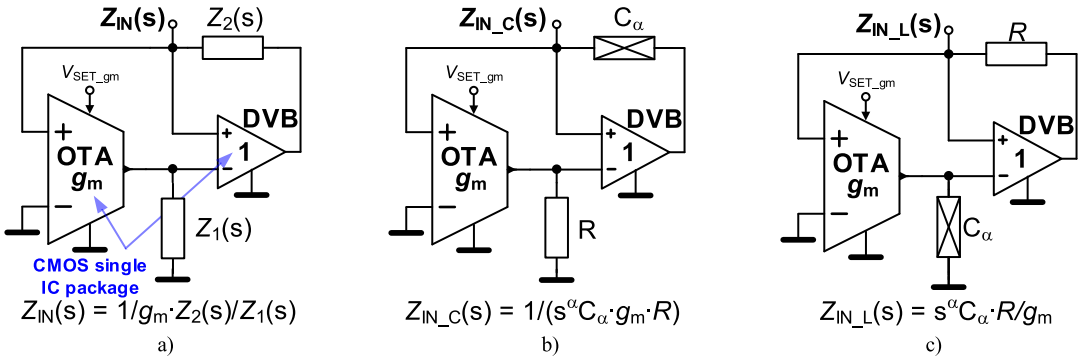

FIGURE 3. The proposed devices: a) general voltage adjustable immmittance converter and inverter, b) fractional-order capacitance multiplier, c) synthetic fractional-order inductance simulator.

The value of the equivalent inductance $L_{eq} = C_\alpha \cdot R/g_m$ has a similar meaning as the equivalent capacity (presented above). Again, an integer-order solution can be derived easily.

V. REAL CIRCUIT MODELS INCLUDING PARASITIC PROPERTIES

Considering the real features of the circuitry during its design even at very low frequencies is very important. Our experimental setup for impedance measurement (see Fig. 4) utilizes a converter based on a current feedback operational amplifier (CFOA) AD844 [54] and also creates a significant amount of real effects (parasitic features of behavior) on the analyzed active immittances. The impedance plots are obtained from the conversion of the transfer response (Bode plot) by multiplication of a known resistance value: $Z_{unknown}(s) = V_2(s)/V_1(s) \cdot R_{conv}$. The Keysight DSOX-3024T oscilloscope with the option of frequency response analysis can perform such an analysis. The results are valid up to 1 MHz. Also used input amplitude profile (property of the generator) settable between 20 mV and 2 V (RMS value) was suitable for this measurement setup.

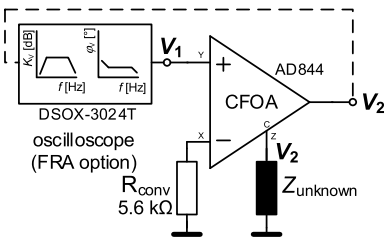

FIGURE 4. Experimental setup for measurement of unknown integer-and fractional-order impedance (immittance).

We will take as an example solution from Fig. 3 in the variant with integer-order capacitor (connected as Z_1 and Z_2) in order to explain real effects of parasitic features on the behavior of the circuit. Similar effects occur in the case when a fractional-order passive device (CPE) [37], [38] is used instead of a capacitor (in the bandwidth of valid approximation of course). From the viewpoint of the low-frequency operational bandwidth (limitation of active devices and the selected CPEs), the values of C and R in the circuit (see Fig. 5 a)) are 100 nF and 560 Ω, respectively. Such a setting allows fitting a suitable operation of applications between tens of Hz and units-tens of kHz. The behavior of the circuit was measured in the frequency domain from 10 Hz up to 1 MHz. The CFOA-based converter is a commercially available current conveyor of second generation (CCII) [1], [2] having the following inter-terminal relations: unity gain voltage follower between the Y and X terminal ($V_X = V_Y$, where $I_Y = 0$) and unity gain current follower between the X and Z terminal ($I_Z = I_X$). The unity gain voltage buffer ($V_Z = V_{out}$) accompanies the CCII in the same package. The value of the conversion resistor $R_{conv} = 5.6\,k\Omega$ was selected with consideration of sufficient gain, frequency response and minimization of the effects of the internal small-signal X terminal resistance (≅50 Ω). The frequency limits of this measurement setup should be significantly beyond the expected operational bandwidth of supposed tests (30-60 MHz at the used supply voltage of ±5 V for AD844 [54]). The maximum available gain of the voltage transfer has also an impact on the frequency bandwidth when the impedance magnitude is increasing above the known value of the terminal impedance of the input node ($Z_{IN}(s)$).

VI. ANALYSIS OF INTEGER-ORDER BEHAVIOR

A. REAL BEHAVIOR OF CAPACITANCE MULTIPLIER

The topology, shown in Fig. 5, represents a particular solution of the capacitance multiplier including the most important influences. Note that when the symbol C is replaced by C_α, integer-order or fractional-order is obtained, respectively.

All significant real parasitics (small-signal parameters) important for evaluation of the behavior in the expected low-frequency band are included.

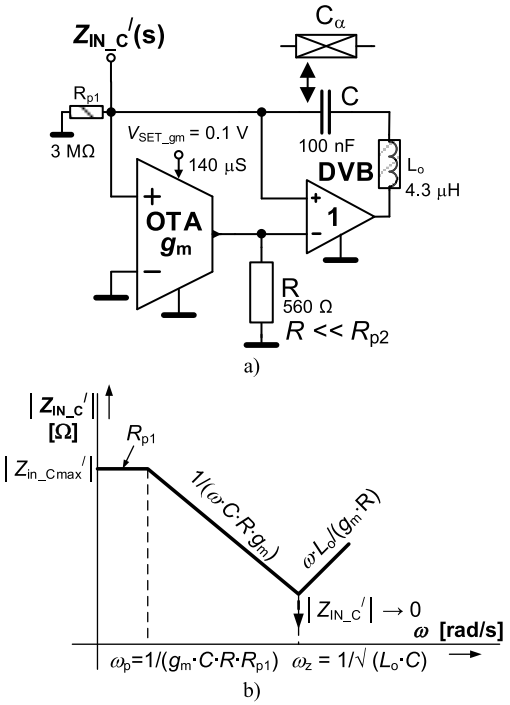

FIGURE 5. Model for small-signal parasitic analysis of real behavior of the capacitance multiplier: a) circuit, b) simplified diagram of expected impedance magnitude.

The transfer response of this circuit in the integer-order variant has the following approximate symbolical form:

$$K_V^{/}(s) = \frac{1}{R_{conv}} \cdot Z_{IN\_C}^{/}(s) \cong \frac{1}{R_{conv}} \cdot \left[R_{p1} \cdot \left(\frac{s^2 CL_o + 1}{sCRR_{p1}g_m + 1} \right) \right], \quad (4)$$

where the complex zero frequency can be found as $\omega_z \cong 1/\sqrt{(L_o \cdot C)}$ and the pole frequency as $\omega_p \cong 1/(C \cdot R \cdot R_{p1} \cdot g_m)$, respectively. The maximal low-frequency magnitude of the input impedance is defined by: $|Z_{in\_Cmax}^{/}| \cong R_{p1}$. Note that the output resistance of OTA (marked as R_{p2} in Fig. 5) has insignificant effect when $R \ll R_{p2}$. It is caused by the terminal impedance (resistive part) of AD844 transimpedance (Z terminal) because, according to [54], the input resistances of OTA and DVB are significantly higher (>10 MΩ). The pole frequency significantly depends on the value of the parallel combination of the output resistance of the z terminal of used CCII, input resistance of OTA and input resistance of DVB. The value of the pole frequency significantly depends on the parallel combination of the output resistance of the Z terminal (CCII) and on the input resistance of OTA and DVB. This pole cannot be identified on traces in many cases (also in many plots in our case) because of its very low value (lower than units of Hz) caused by the high value of R_{p1} and the start of all AC analyses from 10 Hz (common limitation of measuring devices). Comparison of theoretical expectations, model simulation with included parasitics (Fig. 5) and

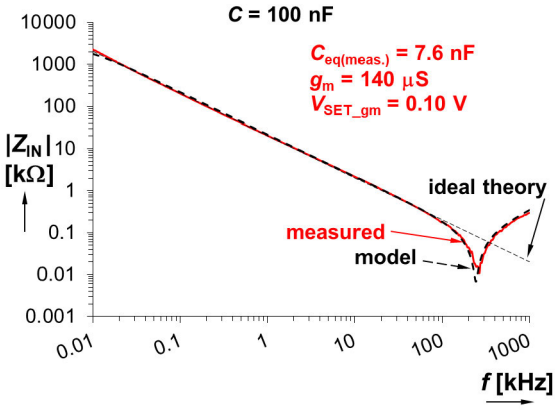

FIGURE 6. Comparison of experimental and expected behavior of the integer-order capacitance multiplier magnitude impedance plot (for parameters in Fig. 5).

experimental results for the integer-order capacitance multiplier in magnitude characteristics of impedance is shown in Fig. 6.

B. REAL BEHAVIOR OF SYNTHETIC INDUCTANCE

Configuration of this model (see Fig. 7) is very similar to the previous one (Fig. 5), but the consequences of small-signal real behavior are different. Again, a fractional-order solution is obtained by interchange of C and C_α as indicated in the figure.

Routine analysis of the integer-order circuit revealed the following simplified transfer response:

$$K_V^{//}(s) = \frac{1}{R_{conv}} \cdot Z_{IN\_L}^{/}(s) \cong \frac{1}{R_{conv}} \cdot \left[\frac{R}{R_{p2}} \cdot \left(\frac{sCR_{p2} + 1}{s^2 CC_{p1}R + g_m} \right) \right]. \quad (5)$$

The zero frequency can be expressed as: $\omega_z \cong 1/(C \cdot R_{p2})$ whereas the value of the complex pole frequency is: $\omega_p \cong \sqrt{(g_m/(C \cdot C_{p1} \cdot R))}$. The low-frequency magnitude limitation can be expected from $|Z_{in\_Lmin}^{/}| \cong R/(R_{p2} \cdot g_m)$. Now, the zero frequency is a very important and limiting factor due to R_{p2} (tens of kΩ) and it is depending on the value of C. The comparison of experimental results with simulation of the model (Fig. 7) and the theoretical ones is shown on Fig. 8.

Parasitic nodal capacitance of the terminal (package+bonding+IC leg/pin+copper area of pin on printed circuit board) can be even more than 15 pF. Measurements provided for the test-chip (DIL28) [52], [53], used also in these experiments (in the testing board), yield a terminal capacity around 15 pF. Therefore, we consider $C_{p1} \cong 30$ pF (that fits well with experimental results) and $R_{p1} \cong 3$ MΩ (based on datasheet). The value of L_o (~4.3 μH) was experimentally obtained in [54] as well as the value of R_{p2} (~60 kΩ).

The expected values of important parasitic properties of circuits shown in Figs. 5 and 7, as well as experimental

TABLE 2. Comparison of the Features of the Proposed Circuits and simplified model for selected value of equivalent capacity C_{eq} or inductance L_{eq} at 1 kHz.

Capacitance multiplier (see Fig. 5): C = 100 nF, R = 560 Ω, $R_{p1} \cong$ 3 MΩ, $L_o \cong$ 4.3 µH, g_m = 140 µS (V_{SET_gm} = 0.1 V)				
parameter	ideal theory	model	experiment	error
C_{eq} [nF] @ 1 kHz	7.8	7.8	7.6	–2.6 %
f_p [Hz]	N/A	0.5	N/A*	-
f_z [kHz]	N/A	243	244	0.4 %
$\lvert Z_{IN\_Cmax}' \rvert$ [MΩ]	∞	≈ 3	N/A*	-
Synthetic inductance (see Fig. 7): C = 100 nF, R = 560 Ω, $R_{p1} \cong$ 3 MΩ, $R_{p2} \cong$ 60 kΩ, $C_{p1} \cong$ 30 pF, g_m = 140 µS (V_{SET_gm} = 0.1 V)				
parameter	ideal theory	model	experiment	error
L_{eq} [H] @ 1 kHz	0.400	0.400	0.427	6.8 %
f_z [Hz]	N/A	27	30	11.1 %
f_p [kHz]	N/A	46.0	44.7	–2.8 %
$\lvert Z_{IN\_Lmin}' \rvert$ [Ω]	0	67	63	–6.0 %

* equipment limitation (below 10 Hz); error is calculated for both model and experiment

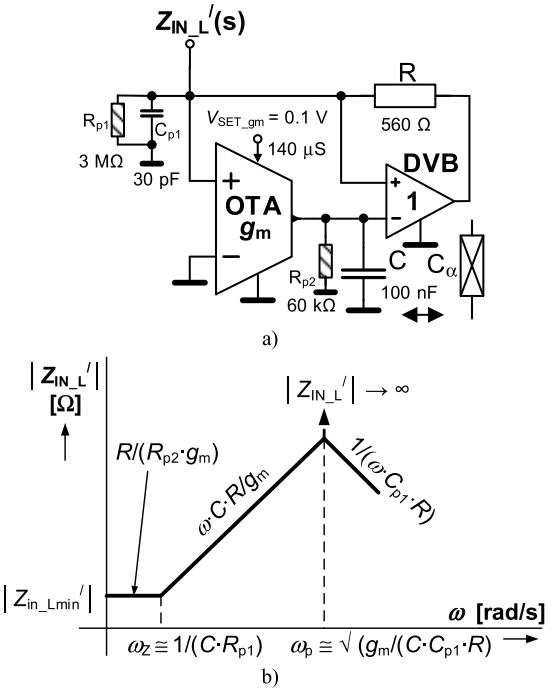

FIGURE 7. Model for small-signal parasitic analysis of real behavior of the integer-order synthetic inductance: a) circuit, b) simplified magnitude diagram of impedance magnitude.

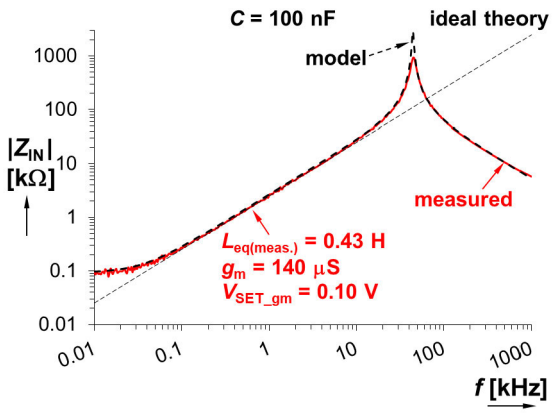

FIGURE 8. Comparison of experimental and expected behavior of the synthetic integer-order inductance magnitude impedance plot (for parameters in Fig. 7).

results, are summarized in Table 2. Note that there were some simplifications in the parasitic analysis. However, the obtained results are sufficient for estimation of real behavior as obvious from graphs.

The electronic adjustability of both integer-order impedances was verified and the measurement results in comparison with theory are shown in Figs. 9 and 10. The value of V_{SET_gm} was adjusted in both cases in five steps: 0.05, 0.1, 0.2, 0.3, and 0.5 V ($g_m \cong$ 70, 140, 280, 420, 700 μS). The magnitude and phase impedance plots for multiplication of capacitance are shown in Fig. 9, while multiplication of synthetic inductance in Fig. 10. These results are complemented by the comparison of theoretical (ideal) and experimental equivalent values (taken at 1 kHz) in dependence on driving voltage V_{SET_gm}.

The ideal range of C_{eq} yields 3.9 → 39 nF whereas the results from the experiment show 3.8 → 39 nF (the maximal error in the tunability range is lower than 3%). For L_{eq}, the ideal range is 0.8 → 0.08 H, while the experimental-based range is 0.82 → 0.083 H (maximal error around 7 %). The available range of the frequency bandwidth where the phase error is not larger than several degrees (±3°) reaches approximately 100 Hz up to 50 kHz for C_{eq} and only from 3 kHz up to 13 kHz for L_{eq}. This behavior is expectable for reasons shown in model (Fig. 7). Fortunately, the operational band of L_{eq} can be limited but suitable for many applications (oscillators for example [50]).

VII. ANALYSIS OF FRACTIONAL-ORDER BEHAVIOR

The main contribution of this work is represented by the fractional-order configuration of the designed immittance - using fractional-order elements (approximants) or constant phase elements. Three types of CPEs-based RC ladder were used, previously introduced in [50], with values C_α = 225 μF/sec$^{3/4}$ (α = 1/4), C_α = 56 μF/sec$^{1/2}$ (α = 1/2) and C_α = 8.8 μF/sec$^{1/4}$ (α = 3/4). Their practical validity of the approximation falls into the bandwidth between 10 Hz

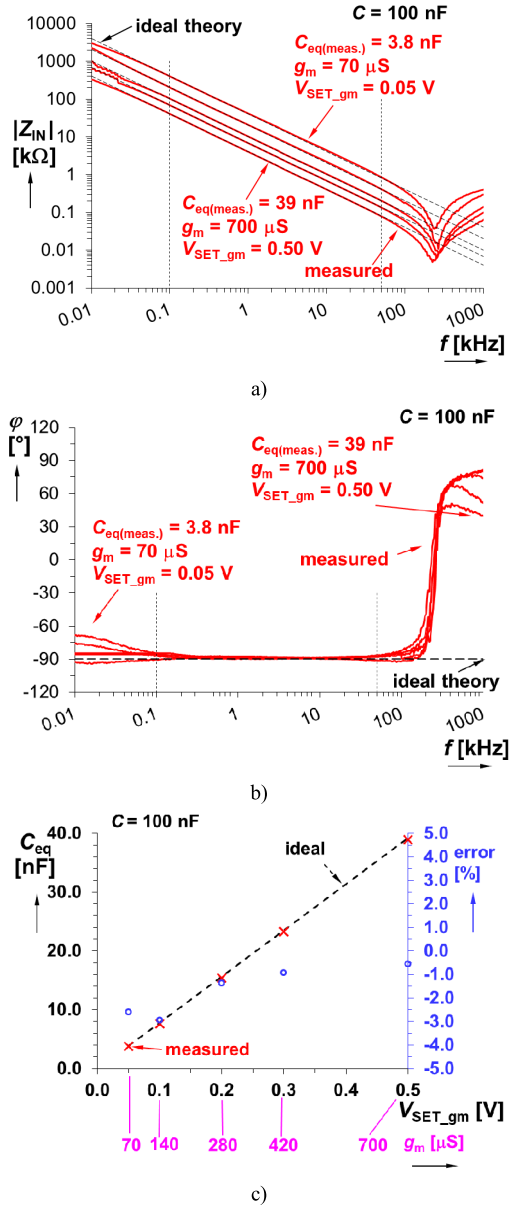

FIGURE 9. Control of equivalent capacitance value – comparison of measurement results and theory: a) magnitude responses, b) phase responses, c) comparison of ideal and measured C_{eq} dependence on V_{SET_gm}.

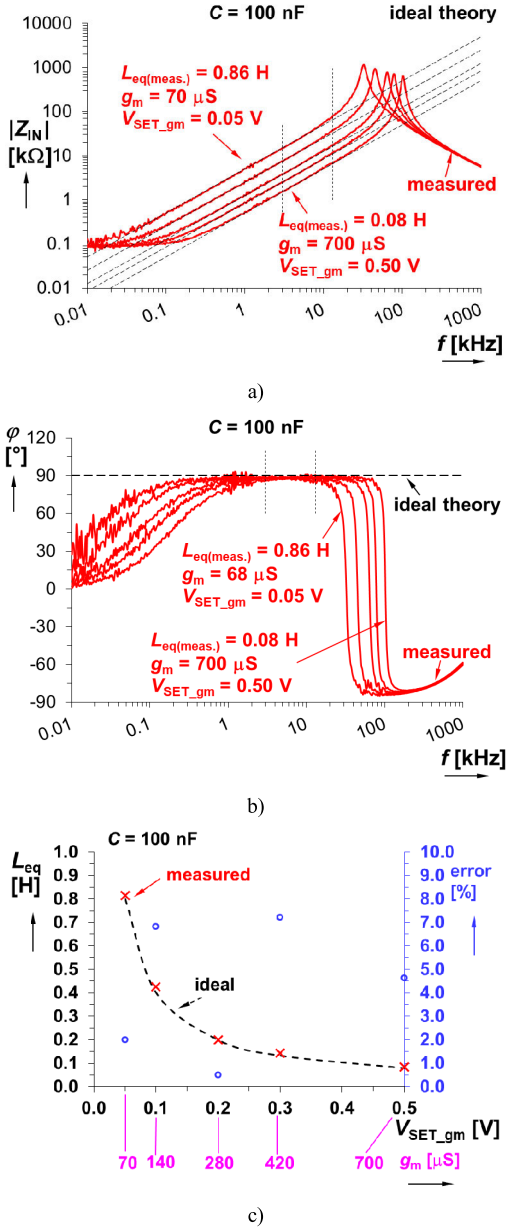

FIGURE 10. Experimental test of inductance multiplier: a) magnitude responses, b) phase responses, c) comparison of ideal and measured L_{eq} dependence on V_{SET_gm}.

and 1 MHz and the phase ripple is $\Delta\varphi = \pm 3°$ in the real case. Details about the behavior of these CPEs can be found in [50]. The following parts deal with sequential testing of all three CPEs in both the previously studied cases (capacitance multiplier and inductance simulator).

A. FRACTIONAL-ORDER CAPACITANCE MULTIPLIER

All the obtained results (magnitude and phase plots in dependence on frequency and dependence of C_{eq} on V_{SET_gm} and g_m) are shown in Fig. 11. The results for the capacitance multiplier, obtained for all tested cases and evaluated at 1 kHz, using $C_\alpha = 225\ \mu F/sec^{3/4}$ ($\alpha = 1/4$) indicate the ideal range of the equivalent capacity C_{eq} between 8.8 and 88 $\mu F/sec^{3/4}$ for V_{SET_gm} variation from 0.05 and 0.5 V (obtained by $g_m = 70 \rightarrow 700\ \mu S$).

The experiment-based evaluation shows the C_{eq} yields range $9.2 \rightarrow 85.1\ \mu F/sec^{3/4}$ and the maximal error below 5% (theory vs measurement). The operational bandwidth is between 18 Hz and 27.3 kHz in this arrangement (considering a band where the phase stays in $\pm 3°$ tolerance area).

The second CPE having $C_\alpha = 56\ \mu F/sec^{1/2}$ ($\alpha = 1/2$) brings the following results: the ideal range of C_{eq} adjustment

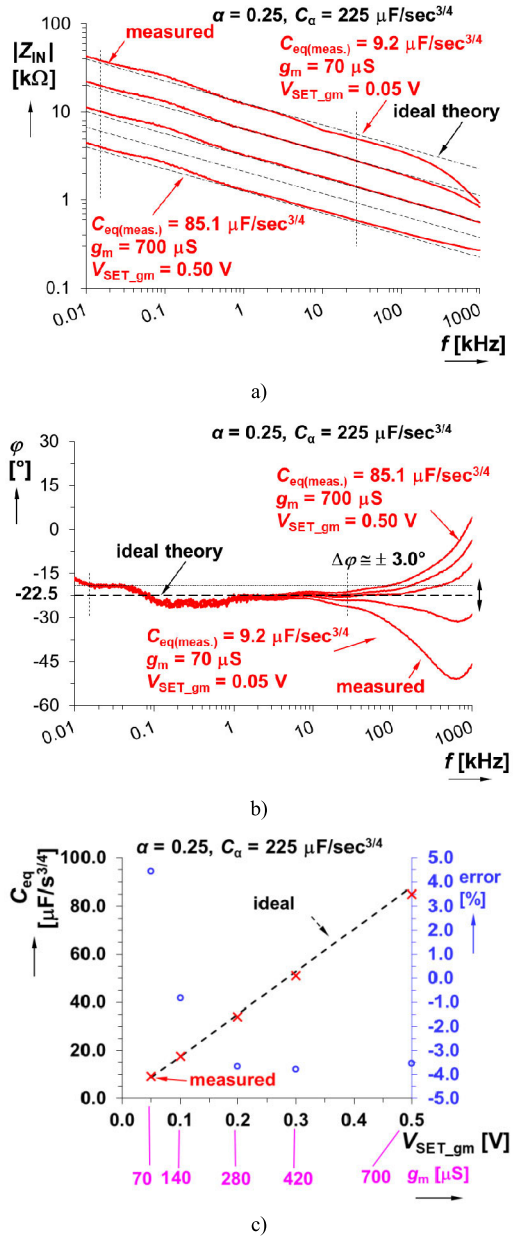

FIGURE 11. Experimental test of the fractional-order capacitance multiplier using $C_\alpha = 225\ \mu F/sec^{3/4}$ ($\alpha = 1/4$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured C_{eq} dependence on V_{SET_gm}.

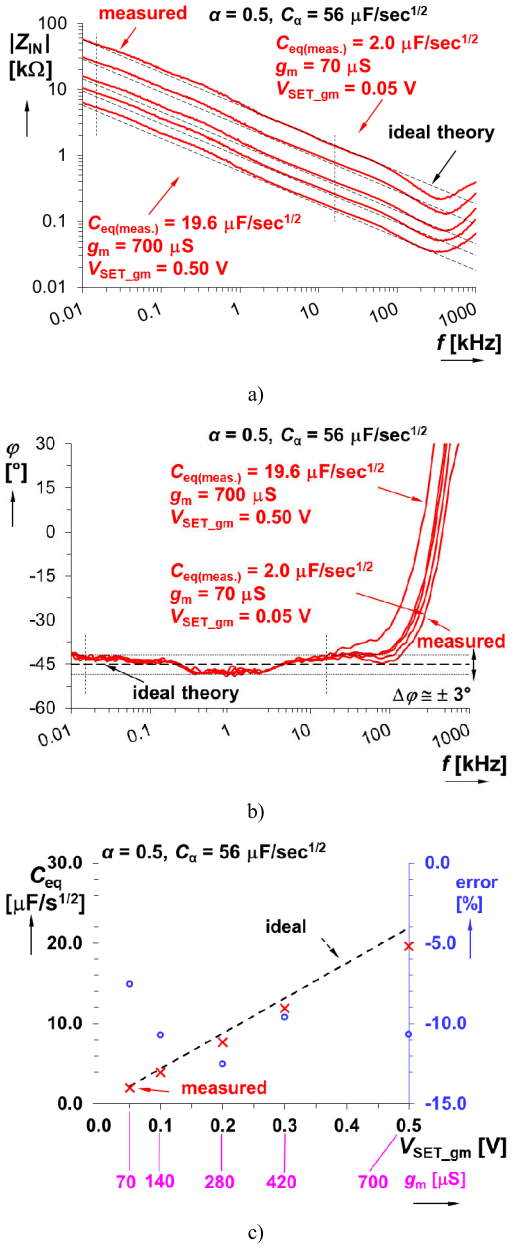

FIGURE 12. Experimental test of the fractional-order capacitance multiplier using $C_\alpha = 65\ \mu F/sec^{1/2}$ ($\alpha = 1/2$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured C_{eq} dependence on V_{SET_gm}.

$2.2 \rightarrow 21.9\ \mu F/sec^{1/2}$ and the experimentally tested range is $2.0 \rightarrow 19.6\ \mu F/sec^{1/2}$ in the bandwidth 15 Hz → 15.8 kHz.

Comparison of the ideal and experimental values yields the maximal error less than 11 %. However, it is an acceptable value when we consider inaccuracies of CPEs and their tolerances of magnitude and phase of impedance [50]. The results are shown in Fig.12 in a similar form as in the previous case.

The results for the third type of the CPE-s based RC ladder are shown in Fig. 13. The last example ($C_\alpha = 8.8\ \mu F/sec^{1/4}$, $\alpha = 3/4$) offers the readjustability of C_{eq} between $0.34 \rightarrow 3.45\ \mu F/sec^{1/4}$ (in theory). The experiments confirmed this operationability between $0.34 \rightarrow 3.11\ \mu F/sec^{1/4}$ with the maximal error up to 11 %. The frequency bandwidth in this case reaches approximately 10 Hz → 40 kHz.

B. FRACTIONAL-ORDER SYNTHETIC INDUCTANCE

The CPEs used in the previous case are tested also in the second configuration of the device representing a synthetic inductance L_{eq}. The first set of the results is captured in Fig. 14. The control of the driving voltage V_{SET_gm} (0.05 → 0.5 V) leads to the ideal range of adjustment from $1800 \rightarrow 180\ sec^{5/4}/F$ for $C_\alpha = 225\ \mu F/sec^{3/4}$ ($\alpha = 1/4$).

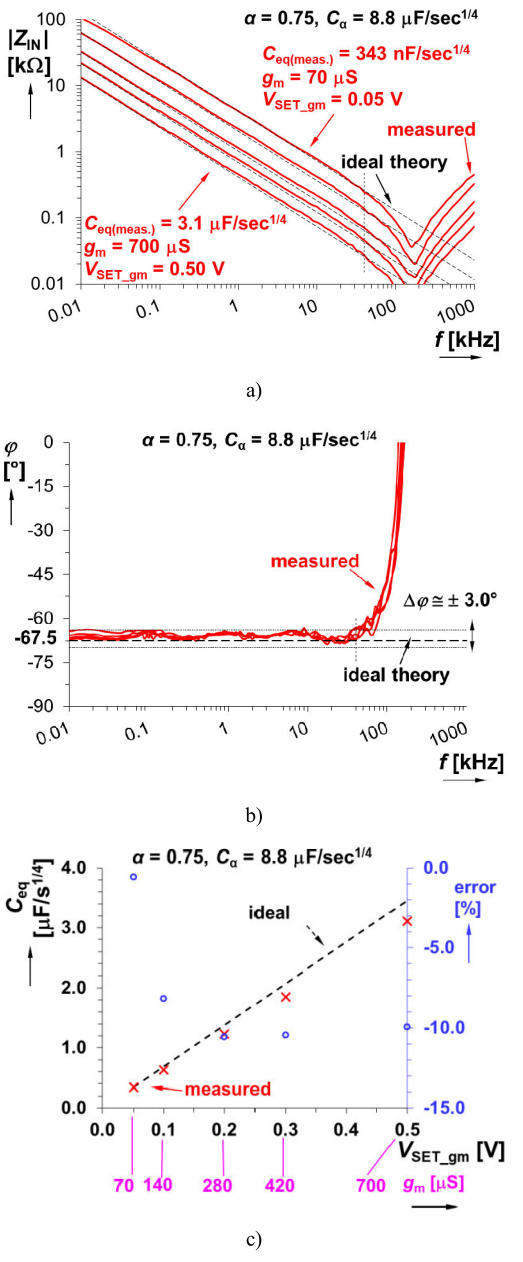

FIGURE 13. Experimental test of the fractional-order capacitance multiplier using $C_\alpha = 8.8\ \mu$F/sec$^{1/4}$ ($\alpha = 3/4$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured C_{eq} dependence on V_{SET_gm}.

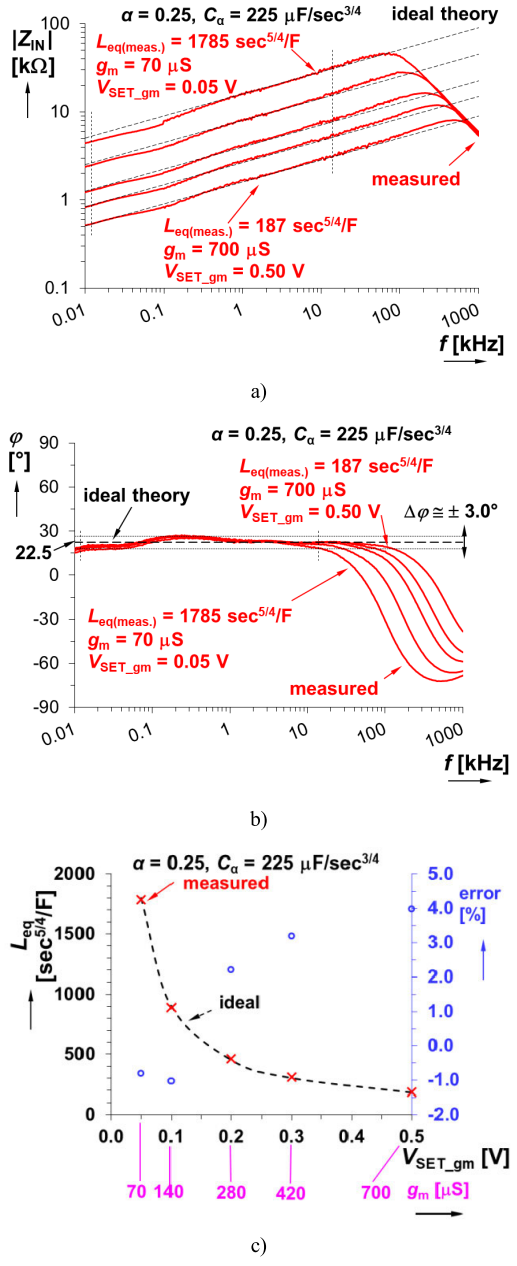

FIGURE 14. Experimental test of the fractional-order synthetic inductance using $C_\alpha = 225\ \mu$F/sec$^{3/4}$ ($\alpha = 1/4$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured L_{eq} dependence on V_{SET_gm}.

The experimental results are from 1785 up to 187 sec$^{5/4}$/F in the operational bandwidth 12 Hz → 13.7 kHz that yields a maximal error below 4 %.

The second value of the CPE $C_\alpha = 56\ \mu$F/sec$^{1/2}$ ($\alpha = 1/2$) brings the ideal value of L_{eq} between 448 and 44.8 sec$^{3/2}$/F (408 → 41 sec$^{3/2}$/F for the experiment). That results into a maximal error below 9%. As it is observed in Fig. 15, selecting the frequency bandwidth in the range from 14 Hz up to 4.7 kHz ensures the validity of the operation.

The results of the last set ($C_\alpha = 8.8\ \mu$F/sec$^{1/4}$, $\alpha = 3/4$) of tests are shown in Fig. 16. The available ideal L_{eq} variation 70 → 7 sec$^{7/4}$/F was confirmed experimentally in very similar values (68 → 6.5 sec$^{7/4}$/F). Overall, the maximal error in this range is around 11 %. The bandwidth covers the range from 40 Hz up to 2.4 kHz.

The performed experimental tests result into the following summarization. The integer-order elements (used in the structure) offer readjustability ranges of equivalent values between 3.8 and 39 nF (for C_{eq}) and 0.82 and 0.083 H with deviation from the ideal case 7% maximally and valid within

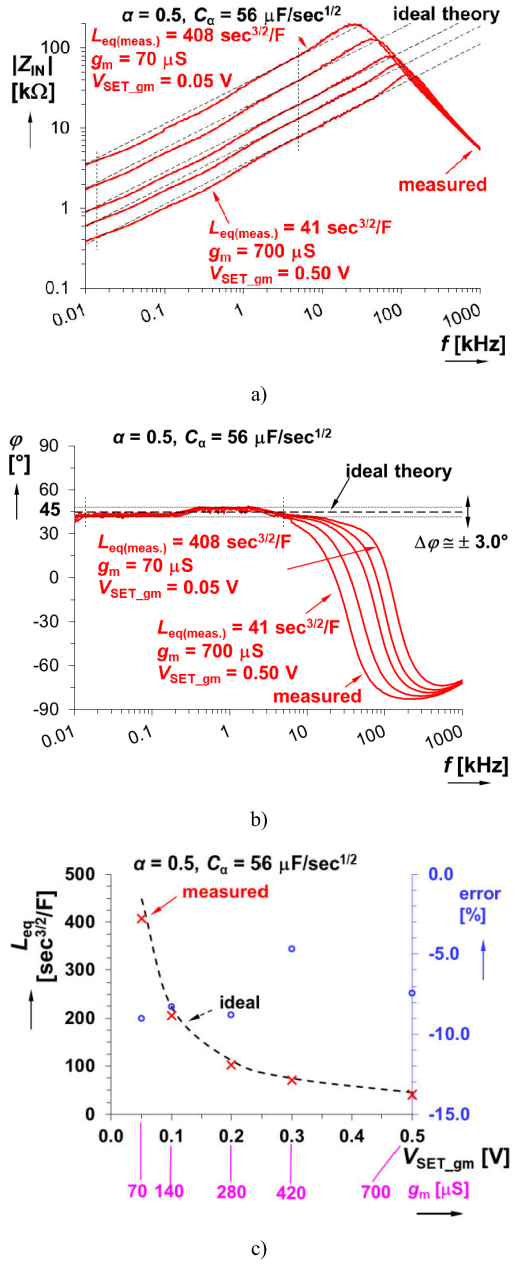

FIGURE 15. Experimental test of the fractional-order synthetic inductance using $C_\alpha = 56\ \mu F/sec^{1/2}$ ($\alpha = 1/2$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured L_{eq} dependence on V_{SET_gm}.

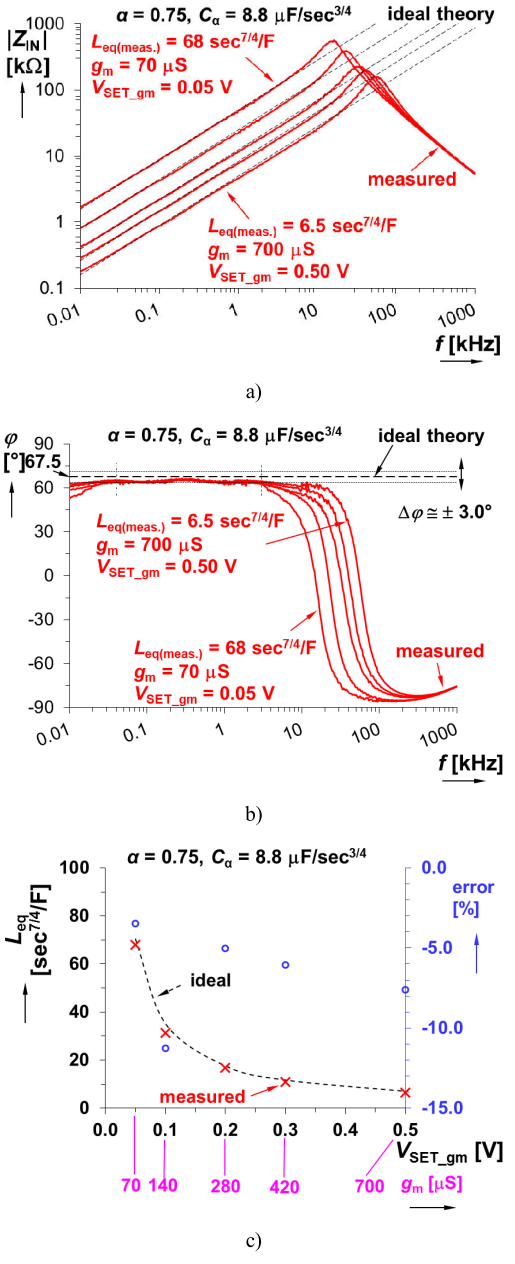

FIGURE 16. Experimental test of the fractional-order synthetic inductance using $C_\alpha = 8.8\ \mu F/sec^{1/4}$ ($\alpha = 3/4$): a) magnitude responses, b) phase responses, c) comparison of ideal and measured L_{eq} dependence on V_{SET_gm}.

the range from 100 Hz up to 50 kHz (C_{eq}) and 3 Hz up to 13 kHz (L_{eq}).

The fractional-order elements yield different ranges of L_{eq} in dependence on the order and C_α operating in the range from 40 Hz up to 2.4 kHz as the worst case (for the highest order $\alpha = 0.75$). Low values of the order yield a wider bandwidth (18 Hz → 27 kHz for $\alpha = 0.25$) as expected from the real behavior and the model using real parasitic elements. The overall L_{eq} value was changed (within all tested orders and C_α) from 6.5 up to 1785 $sec^{3/2}$/F with an error less than 11%.

The full tested C_{eq} range between 3.1 and 85.1 $\mu F/sec^{3/4}$ has been obtained whereas the lowest bandwidth was obtained for $\alpha = 0.5$ (15 Hz → 15.8 kHz). The maximal available bandwidth reaches 10 Hz → 40 kHz. Deviations of all values from the ideal case are again below 11% (as the worst case). All tests were performed for g_m variation 70 → 700 μS (by $V_{SET\_gm} = 0.05 \rightarrow 0.5$ V). All specific

TABLE 3. Summarization of the obtained Results for all tested cases.

α	1/4	1/2	3/4	1
C_α	225 μF/sec$^{3/4}$	56 μF/sec$^{1/2}$	8.8 μF/sec$^{1/4}$	100 nF
		Capacitance multiplier		
C_{eq} range (ideal)	8.8 → 88.2 μF/sec$^{3/4}$	2.2 → 21.9 μF/sec$^{1/2}$	0.34 → 3.45 μF/sec$^{1/4}$	3.9 → 39 nF
C_{eq} range (experimental)	9.2 → 85.1 μF/sec$^{3/4}$	2.0 → 19.6 μF/sec$^{1/2}$	0.34 → 3.11 μF/sec$^{1/4}$	3.8 → 39 nF
maximal C_{eq} error @ 1 kHz	5 %	11 %	11 %	3 %
bandwidth	18 Hz → 27.3 kHz	15 Hz → 15.8 kHz	10 Hz → 40 kHz	100 Hz → 50 kHz
		Synthetic inductance		
L_{eq} range (ideal)	1800 → 180 sec$^{5/4}$/F	448 → 44.8 sec$^{3/2}$/F	70 → 7 sec$^{7/4}$/F	0.8 → 0.08 H
L_{eq} range (experimental)	1785 → 187 sec$^{5/4}$/F	408 → 41 sec$^{3/2}$/F	68 → 6.5 sec$^{7/4}$/F	0.82 → 0.083 H
maximal L_{eq} error @ 1 kHz	4 %	9 %	11 %	7 %
bandwidth	12 Hz → 13.7 kHz	14 Hz → 4.7 kHz	40 Hz → 2.4 kHz	3 kHz → 13 kHz
$g_m = 70 \rightarrow 700$ μS ($V_{SET\_gm} = 0.05 \rightarrow 0.5$ V)				

details (separated ranges and order used in tests) are given in Table 3.

VIII. CONCLUSION

The simplicity, simple electronic adjustability and simple variability between the capacitive and inductive character allowing scalability of the equivalent value and between integer-order and fractional-order character are the most significant advantages of the proposed solution. The DC voltage driving offers a linear adjustment of equivalent values in one decade. The linearizing circuitry is not necessary in our case in comparison with standard OTA. The obtained results are summarized in Table 3. The frequency bandwidth operationability of the capacitance multiplier overcomes three decades. It was expected due to suitability of the presented CMOS devices and the selected values of external passive elements. The synthetic inductance has a lower maximal frequency and the workability can be guaranteed in more than two decades.

The CMOS devices based active circuitry (excluding conversion blocks) has low power consumption (below 20 mW at 3.3 V power supply). Thereby, these systems can be used especially in low-power low-frequency (in combination with presented parameters of CPEs) audio and biomedical applications. This work also indicates that the order and value of the used passive element (many previous works deal with the order only) have a significant influence on the value of C_{eq} or L_{eq} that can be useful for non-standard cases of very large values (especially in case of L_{eq}). The simply variable scalability of fractional-order elements (and generation of large values) together with their active representation, as presented in this paper, can significantly support adjustability of fractional-order oscillators [50]. The proposed circuitry can be directly used in resonators [43], [49] and oscillators [50] of known topologies. It allows obtainment of improved features (simplification and electronic tunability for example).

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