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Wide-Range Digital-Analog Mixed Calibration Technology of a DC Instrument Transformer Test Set

HAOLIANG HU[1,2], QI NIE[2], XIONG WU[2], FUCHANG LIN[1], (Senior Member, IEEE), FENG ZHOU[2], XIAOFEI LI[2], AND JICHENG YU[2], (Member, IEEE)

[1]School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China
[2]China Electric Power Research Institute Company Ltd., Wuhan 430074, China

Corresponding authors: Qi Nie (nieqi@epri.sgcc.com.cn) and Fuchang Lin (fclin@hust.edu.cn)

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ABSTRACT A DC instrument transformer test set (ITTS), as an error measurement device for DC instrument transformers, needs to be calibrated regularly to ensure its accuracy. Existing calibration technology can only achieve DC ITTS error calibrations within a zero analog standard error. This paper proposes a wide-range digital-analog mixed calibration scheme for a DC ITTS based on multistage serial proportional micro-difference technology and high-speed high-precision sampling and coding technology, achieving a digital-analog standard error of $\pm 1\%$ that can be fine-tuned in 0.001% steps. A prototype is developed, and the prototype test results show that the expanded uncertainty of the prototype does not exceed 1×10^{-4}, the maximum error of the standard error does not exceed $\pm 3 \times 10^{-5}$, and the output frequency of the digital protocol message is 4 kHz and 12.8 kHz. This scheme can achieve the error calibration of the analog and digital channels for the DC ITTS within a $\pm 1\%$ standard error and solve the error calibration problem of wide-range digital channels for DC ITTSs.

INDEX TERMS DC instrument transformer test set, standard error, digital protocol, error calibration, operational amplifier.

I. INTRODUCTION

With the implementation of the ''West-to-East Power Transmission'' strategy and the optimal allocation of power grid resources in China, ultra-high-voltage (UHV) DC transmission technology has matured and experienced large-scale applications [1], [2]. A DC instrument transformer is a measurement device for DC voltage and current, and its measurement accuracy affects both the control and implementation of DC transmission systems [3]. According to the Chinese national standards GB/T 26216.1-2019 [4] and GB/T 26217-2019 [5], the accuracy class of DC instrument transformers are 0.1, 0.2, 0.5, and 1, and the output signal types can be analog or digital in accordance with the international standard IEC 61869-9 (FT3) protocol [6]. A DC instrument transformer test set (ITTS), as an error measurement device for DC instrument transformers, generally adopts a direct measurement principle [7]–[9]. To evaluate the performance of a DC ITTS, regular error calibration is required to ensure its accuracy.

The standard error and standard digital protocol, which are the key standard parameters provided by a calibration device when calibrating the error measurement performance and digital channel performance of a ITTS, are the research focus of ITTS calibration technology. The standard error is achieved through the following schemes: 1) adjusted by signal sources and measured by auxiliary equipment [10], [11]; 2) adjusted by signal sources, voltage dividers or resistance-capacitance bridges [7], [12]–[15]; and 3) adjusted by program-based mathematical formulas [16], [17]. The standard digital protocol is achieved by 1) sampling with a digital multimeter or an A/D circuit [16], [17] or 2) utilizing a program-based protocol generator without sampling [10], [18]. The above schemes, except for the second standard error scheme, which uses an inductive voltage divider to adjust the standard error to calibrate a DC ITTS, are all used for AC ITTSs and are ill-suited for DC ITTSs because they use AC signal processing technology. Existing research on DC

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ITTSs has mainly focused on applying DC ITTSs to DC voltage divider traceability [19]–[22] rather than involving DC ITTS calibration technology. An electronic DC ITTS and calibration method were developed in [15]. This approach used an AC voltage source and an inductive voltage divider to achieve analog standard error calibration by setting different transformation ratios for the inductive voltage divider, which indirectly achieved DC ITTS error calibration through the AC standard error.

The above standard error scheme includes analog and program-based digital standard error schemes. The digital standard error scheme used program-based mathematical formulas to superimpose the DC offset component on the reference voltage's digital signal, which could achieve a high-accuracy error setting and adjustment [16]. However, at present, the digital standard error cannot be calibrated because it is generated by a program; there is no existing reference standard for calibration, and the traceability chain lacks continuity [23]–[25]. Thus, the digital standard error is generally evaluated equivalently through comparison or simulation [16]. Therefore, this paper does not adopt a digital standard error scheme, and similarly, a program-based digital protocol scheme will not be adopted.

To address the calibration of a DC ITTS, a wide-range digital-analog mixed calibration technology is proposed in this paper. A modular DC micro-difference device is developed based on an active operational amplifier's multistage serial proportional micro-difference technology, which can output adjustable high-accuracy and wide-range standard errors and achieve independent calibration. Based on an FPGA-based high-speed real-time hardware architecture, an improved implementation scheme for continuously sampling a digital message is designed to eliminate discontinuous sampling drawbacks. A prototype of the DC ITTS calibration device is developed based on the above technology, which can output a $\pm 1\%$ adjustable standard error and continuous digital protocol messages with an expanded uncertainty better than 1×10^{-4}. Thus, the DC ITTS can achieve error calibration for a digital channel within a wide-range standard error.

II. CALIBRATION PRINCIPLE OF THE DC ITTS

The accuracy class of a DC ITTS is generally 0.05, as specified in the Chinese power industry standard DL/T 1394-2007 [26], which is used for the error measurement of a DC instrument transformer with an accuracy class of 0.2 and below. According to the output signal type of a DC instrument transformer under a calibration test, the working mode of the DC ITTS is divided into an analog calibration mode and a digital calibration mode [27]. The DC ITTS simultaneously measures the analog voltage output by the standard instrument and the analog voltage or the FT3 protocol digital signal output by the tested DC instrument transformer and calculates the relative error as in (1):

$$\varepsilon = \frac{k_2 U_2 - k_1 U_1}{k_1 U_1} \tag{1}$$

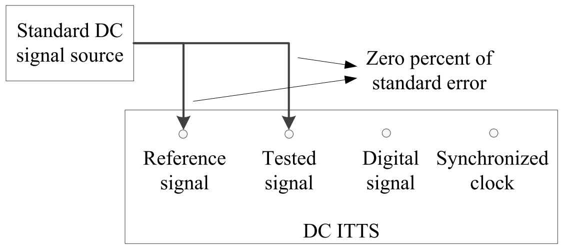

FIGURE 1. Existing calibration scheme of the DC ITTS.

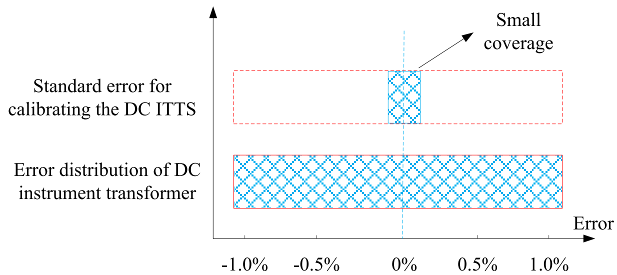

FIGURE 2. Distribution of the error calibration points of the DC ITTS.

where U_1 and k_1 are the output voltage and transformation ratio of the standard DC instrument transformer and U_2 and k_2 are the output voltage and transformation ratio of the tested DC instrument transformer, respectively.

The existing commonly used calibration scheme for a DC ITTS is depicted in Fig. 1. The reference and tested analog signal input terminals of the DC ITTS are used to measure the same standard analog signal and calculate the relative error using formula (1). This calibration scheme cannot set the standard error; it can only calibrate the DC ITTS with an analog input when the standard error is 0%. There are several problems with this calibration scheme: 1) The error calibration of the DC ITTS digital channel cannot be realized, which cannot meet the digital development requirements for DC instrument transformers. 2) The resolution and error measurement range for a DC ITTS specified in the Chinese power industry standard DL/T 1394-2007 [26] cannot be measured. 3) The sampling consistency of the dual analog channels does not fully reflect the error characteristics of the DC ITTS under differentiated inputs under normal operating conditions. The standard error cannot cover the wide error distribution range of the DC instrument transformer, as shown in Fig. 2, which is impractical for comprehensively evaluating the error measurement performance of a DC ITTS within the wide-range error distribution of the DC transformer.

III. CALIBRATION SCHEME

A. CALIBRATION SCHEME DESIGN

The error analysis and calibration scheme of the DC ITTS is shown in Fig. 3. DC ITTS errors are mainly derived from the sampling error (ε_1, ε_2) of the reference and the tested analog voltage, the quantization error ε_3 of the digital signal, the error ε_4 introduced by the calibration algorithm, the synchronization error ε_5, and the error ε_6 introduced by

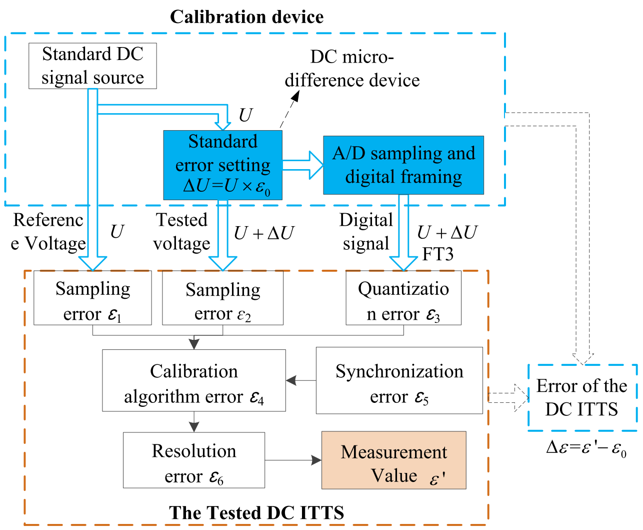

FIGURE 3. Error analysis and calibration scheme of the DC ITTS.

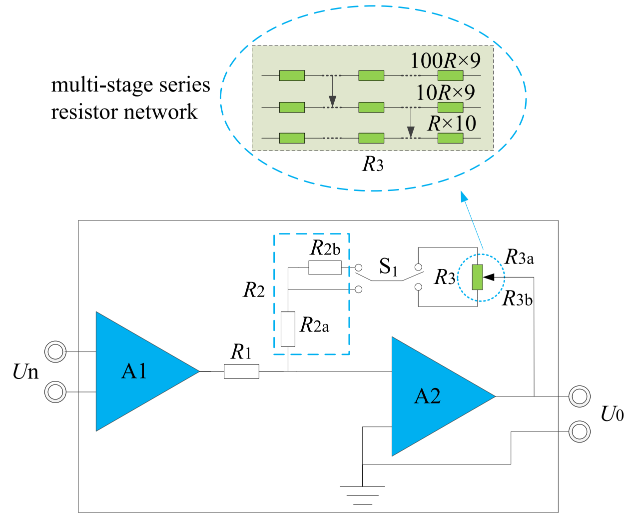

FIGURE 4. DC micro-difference device scheme.

the display resolution. The above errors are comprehensively embodied as the measurement error ε of the DC ITTS.

Therefore, the calibration device must provide the traceable reference voltage, tested voltage, digital signal, and standard error when calibrating the DC ITTS. The error of the DC ITTS can be calculated as in (2):

$$\Delta\varepsilon = \varepsilon' - \varepsilon_0 \tag{2}$$

where ε' describes the relative error between the reference and tested voltage measured by the DC ITTS and ε_0 represents the setting standard error.

The error calibration of the DC ITTS must meet the following requirements: 1) provide an analog signal and a digital signal that can simultaneously meet the analog and digital error calibration of the DC ITTS; 2) provide an accurate reference voltage, a tested analog voltage, and digital signal values better than 0.01%, thus reducing the influence of signal source ripples on the DC ITTS sampling error; 3) derive the reference voltage, tested analog voltage, and digital signal from the same standard signal source, thus reducing the influence of multiple signal source differences and signal fluctuations; and 4) produce an adjustable standard error within the error distribution range of the DC instrument transformer, where the introduced error does not exceed 1/10th of the DC ITTS error. DC voltage source technology is relatively mature at present, and a source with an accuracy of 0.01% can meet DC ITTS calibration requirements. The key problem to be solved is the realization of the digital signal and the standard error.

B. DIGITAL-ANALOG MICRO-DIFFERENCE SCHEME DESIGN

A DC micro-difference device scheme based on an active operational amplifier using multistage series proportional micro-difference technology is designed, as shown in Fig. 4.

The DC micro-difference device is mainly composed of a two-stage operational amplifier. The first-stage operational amplifier A1 is used for front-end signal amplification, which is mainly used for voltage and input impedance matching, where the gain coefficient is k_1 and set to -1. The second-stage operational amplifier A2 is used for multistage serial proportional amplification, where the gain coefficient is k_2. The standard error of the device's input and output is shown in (3):

$$\begin{aligned}\varepsilon &= \frac{U_0 - U_n}{U_n} = \frac{k_1 k_2 U_n + U_{\text{noise}} - U_n}{U_n} \\ &= k_1 k_2 - 1 + \frac{U_{\text{noise}}}{U_n}\end{aligned} \tag{3}$$

where U_{noise} describes the output noise voltage, which mainly derives from the signal source, the operational amplifier, the feedback network resistors and the offset voltage; $k_2 = -(R_2 + R_3)/R_1 = -(1+\varepsilon_0)$; and ε_0 represents the setting standard error, which is designed to be adjusted from -1% to 1% to ensure that it covers the error distribution range of the DC transformers currently in operation.

Assuming $R_1 = 100R_3$, $R_{2a} = 99R_3$, and $R_{2b} = R_3 = 1000R$, R_2 can be switched between R_{2a} and $R_{2a} + R_{2b}$; R_3 is an adjusted multistage series resistor network with a three-stage decimal structure in which the output resistance can be switched between R_{3a} and R_{3b} with $R_3 = R_{3a} + R_{3b}$ and can be adjusted arbitrarily from 0 Ω to 1 $k\Omega$ with a minimum number of resistors, thus reducing the impact of the resistance differences and loop impedance on proportional errors. The minimum resolution adjusting resistance $R = 1\ \Omega$; R_2 and R_3 are switched by S_1 simultaneously. The standard error ε can be calculated by (4) and (5):

$$u(t) = \begin{cases} 1 & (\varepsilon_0 \geq 0) \\ 0 & (\varepsilon_0 < 0) \end{cases} \tag{4}$$

$$\varepsilon = \frac{R_{2a} + R_{2b}u(t) + R_{3b} + (R_{3a} - R_{3b})u(t)}{R_1} - 1 + \frac{U_{\text{noise}}}{U_n} \tag{5}$$

When analyzed by formula (5), a very accurate standard error ε can be obtained by adjusting the resistance R_3 and controlling the noise voltage U_{noise}. The adjustment range of standard error is $\pm 1\%$, and the minimum adjustment resolution is 0.001% when controlling the noise coefficient U_{noise}/U_n so as not to exceed 1×10^{-5}. Related research [28] has focused on current noise suppression in terms of a large resistance and low gain and the compensation of the temperature drift with an adjustable gain. The focus of this paper is a high-stability design with an adjustable gain and resolution under the influence of temperature. In this paper, an OPA227U low-noise operational amplifier is selected for A1 and A2. According to the OPA227U datasheet, its typical input offset voltage is $\pm 5\ \mu$V, and its output noise voltage can be calculated according to its datasheet as in formula (6):

$$E_0 = \sqrt{(1 + \frac{R_2 + R_3}{R_1 + R_s})^2 e_n^2 + e_1^2 + e_2^2 + (i_n(R_2 + R_3))^2 + e_s^2} \tag{6}$$

where $R_{\text{s}} = 50\ \Omega$, which is the internal resistance of the signal source; e_{s}, e_1, and e_2 are the thermal noise of R_{s}, R_1, and $R_2 + R_3$, respectively. For the OPA227 series op amps at 1 kHz, $e_{\text{n}} = 3\text{n}V \Big/ \sqrt{\text{Hz}}$ and $i_{\text{n}} = 0.4pA \Big/ \sqrt{\text{Hz}}$.

Considering the influence of the resistance error, temperature change and temperature coefficient on the standard error, the standard error can be derived as (7), as shown at the bottom of the page, where $\varepsilon_{2\text{a}}$, $\varepsilon_{2\text{b}}$, $\varepsilon_{3\text{a}}$, $\varepsilon_{3\text{b}}$, and ε_1 indicate the fixed resistance error; $C_{2\text{a}}$, $C_{2\text{b}}$, $C_{3\text{a}}$, $C_{3\text{b}}$, and C_1 indicate the temperature coefficient that causes an additional resistance error when the temperature changes; T_{drift} is the temperature change; and ε_0 is the setting standard error.

Assuming that the temperature change during the test is 10°C, the influence of the resistance temperature coefficient is 10 times the influence of its resistance error on the standard error. The resistance error is usually fixed at a certain temperature and can be controlled to a very small range through the series-parallel connection of resistances, and the temperature coefficient may cause a differential change in the additional resistance error with the same temperature change. Therefore, the temperature coefficient is the key parameter that affects the accuracy of the standard error and needs to be carefully designed. The relationship among the temperature coefficient, the setting standard error and its deviation was simulated in LabVIEW software, as displayed in Fig. 5. It can be seen that the standard error deviation is very sensitive to changes in the temperature coefficients $C_{2\text{a}}$ and C_1 and exhibits the opposite phenomenon. The temperature coefficients $C_{3\text{a}}$ and $C_{2\text{b}}$ have similar effects on the standard error

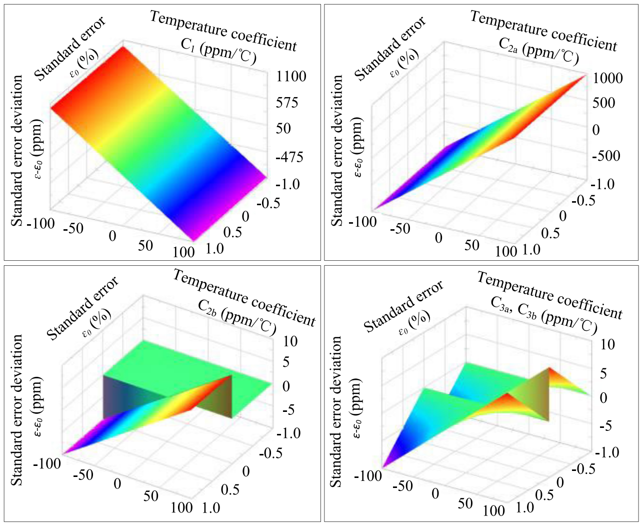

FIGURE 5. The influence of the resistance temperature coefficient C_{2a}, C_{2b}, C_{3a}, C_{3b}, C_1 and temperature change ($T_{drift} = +10°C$) on the standard error deviation within a standard error range of ±1%.

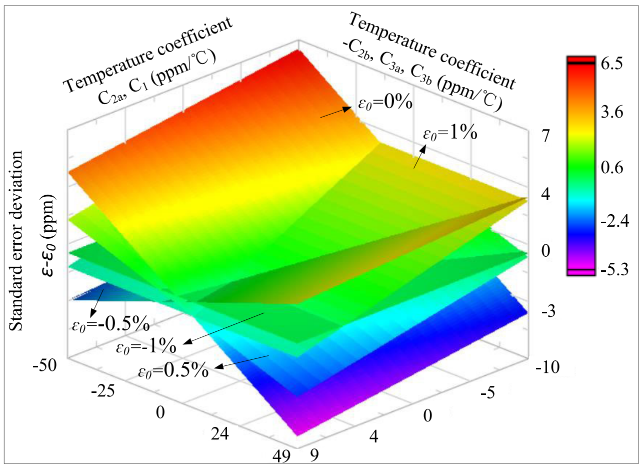

FIGURE 6. The influence of the resistance temperature coefficient on the standard error deviation with $C_{2a} = C_1$, $C_{3a} = C_{3b} = -C_{2b}$, and $T_{drift} = +10°C$.

deviation with a positive standard error. Therefore, it is possible to ensure that the standard error deviation is minimized by making $C_{2\text{a}} = C_1$ and $C_{3\text{a}} = C_{3\text{b}} = -C_{2\text{b}}$.

Assuming $\varepsilon_{2\text{a}} = \varepsilon_1 = 0.005\%$ and $\varepsilon_{2\text{b}} = \varepsilon_{3\text{a}} = \varepsilon_{3\text{b}} = 0.01\%$, the relationship among the temperature coefficient, the setting standard error and its deviation was resimulated, as shown in Fig. 6. The maximum change in the standard error deviation is less than 10 ppm when the temperature coefficient $C_{2\text{a}}$ and C_1 is less than ± 10 ppm/°C, the temperature coefficient $C_{3\text{a}}$, $C_{3\text{b}}$, and $C_{2\text{b}}$ is less than ± 50 ppm/°C,

$$\varepsilon = \begin{cases} \dfrac{0.99(1 + \varepsilon_{2a} + C_{2a}T_{drift}) + 0.01(1 + \varepsilon_{2b} + C_{2b}T_{drift}) + \varepsilon_0(1 + \varepsilon_{3a} + C_{3a}T_{drift})}{1 + \varepsilon_1 + C_1 T_{drift}} - 1 + \dfrac{U_{noise}}{U_n} & (\varepsilon_0 \geq 0) \\ \dfrac{0.99(1 + \varepsilon_{2a} + C_{2a}T_{drift}) + (0.01 + \varepsilon_0)(1 + \varepsilon_{3b} + C_{3b}T_{drift})}{1 + \varepsilon_1 + C_1 T_{drift}} - 1 + \dfrac{U_{noise}}{U_n} & (\varepsilon_0 < 0) \end{cases} \tag{7}$$

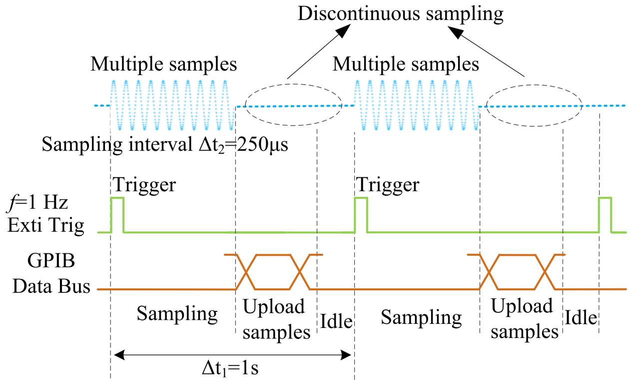

FIGURE 7. Digitalization scheme of serial discontinuous sampling at a sampling rate of 4 kHz.

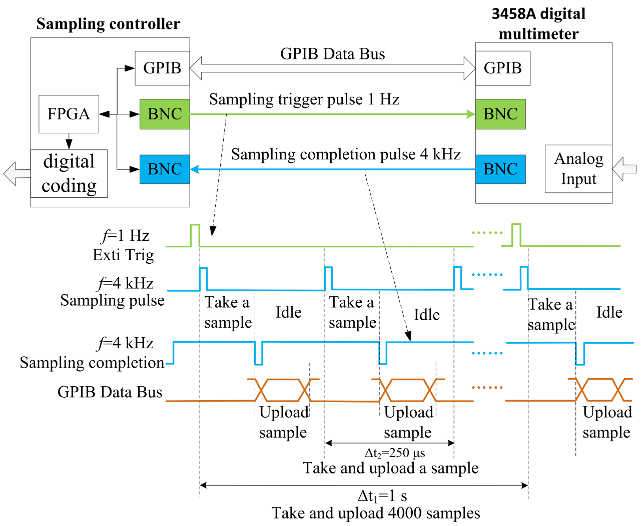

FIGURE 8. Continuous sampling digital signal implementation scheme at a sampling rate of 4 kHz.

thus meeting the minimum adjustment resolution requirements and ensuring that the standard error of the DC micro-difference device has good accuracy and stability.

The existing sampling digital signal scheme is based on the Windows operating system, and a digital multimeter is used to implement the sampling process of "trigger—multiple data sampling—upload", which follows serial processing rules and cannot achieve continuous sampling [17], as shown in Fig. 7. Within 1 second of the trigger period, a continuous 0.2 second interval from the trigger moment is used to sample data at a sampling interval of 250 μs, and the remaining time is used for data encoding and uploading. The uploaded data include sampled data and copies. For a nonsynchronous sampling DC ITTS, the copied digital signal may not be traceable to the real analog signal, and there is a large delay between the uploaded digital signal and the analog signal.

An improved continuous sampling scheme is proposed to obtain digital signals in this paper, as shown in Fig. 8.

A sampling controller is developed based on an FPGA real-time hardware architecture. The FPGA sets the parameters of the digital multimeter through a general-purpose interface

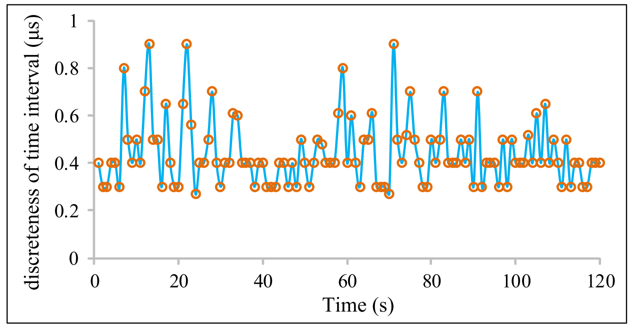

FIGURE 9. Discreteness of the time interval between the FT3 digital protocol frames and each value is the maximum value of the discreteness of 4000 FT3 protocol frames measured within 1 second.

bus (GPIB), including the sampling rate, integration time, trigger mode, DCV sampling mode and other parameters, and finally sets the digital multimeter to the trigger waiting state. A high-precision and high-stability crystal oscillator in the sampling controller is used to output a 1 Hz sampling trigger pulse after frequency division by the FPGA through a Bayonet Neill-Concelman (BNC) coaxial cable interface. At a sampling rate of 4 kHz, after receiving the trigger pulse, the digital multimeter takes 4000 samples continuously until the next trigger pulse arrives. The digital multimeter outputs the sampling completion pulse in real time after each sample is taken and then continues to take the next sample. When the FPGA receives the sampling completion pulse, it immediately uploads each sample and encodes it into an FT3 protocol frame, then sends it out in real time. The "trigger—single data sampling (upload)" parallel sampling process of immediate sampling and upload is realized through the above sampling process. This procedure does not occupy the sampling time during the data upload process, thus achieving high-speed continuous sampling with a sampling interval of 250 μs or 78.125 μs. The FPGA frames and encodes the uploaded data into the FT3 digital protocol frame and outputs data in a high-speed transparent mode. Additionally, each frame carries sampling time stamp information with a resolution of 10 ns. By measuring the interval of the sampling time stamp of the sent frame, the discreteness of the time interval between frames, which refers to the jitter of the transmission time interval of the FT3 protocol frame, is obtained, as shown in Fig. 9. As the results show in Fig. 9, the maximum time interval discreteness between FT3 digital protocol frames within 2 minutes does not exceed 1 μs, which indicates that the digital protocol meets the calibration requirements of the DC ITTS.

IV. TESTING AND ANALYSIS

A. ACCURACY TEST OF THE STANDARD ERROR

The actual output voltage of the micro-difference device with the input grounded is shown in Fig. 10.

The device reaches thermal stability after running for approximately 3 hours, and its output voltage fluctuates within 10 μV. Therefore, the device should be run for a period

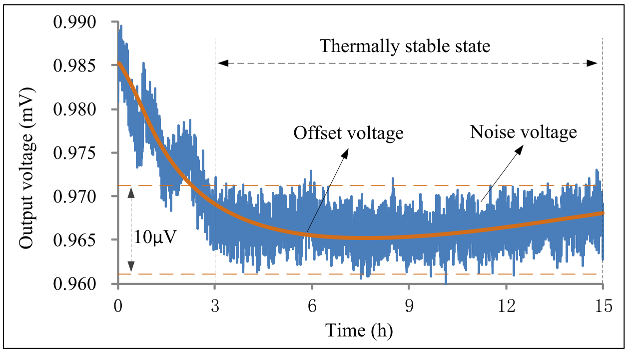

FIGURE 10. Noise voltage of the OPA227U operational amplifier, measured with the input grounded and offset voltage not adjusted.

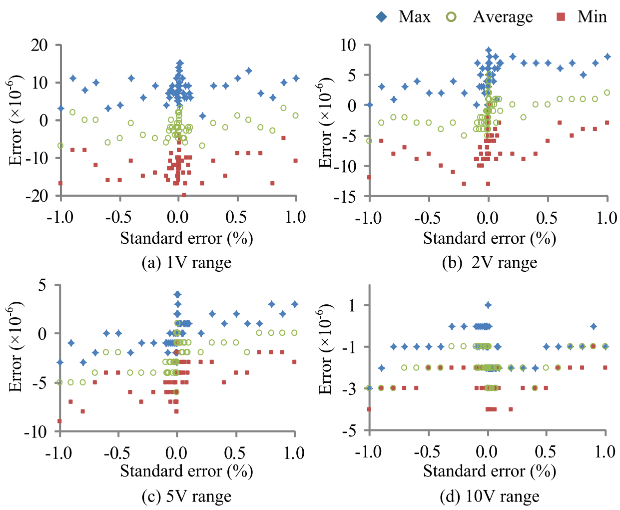

FIGURE 11. Standard error deviation and the setting standard error of the DC micro-difference device.

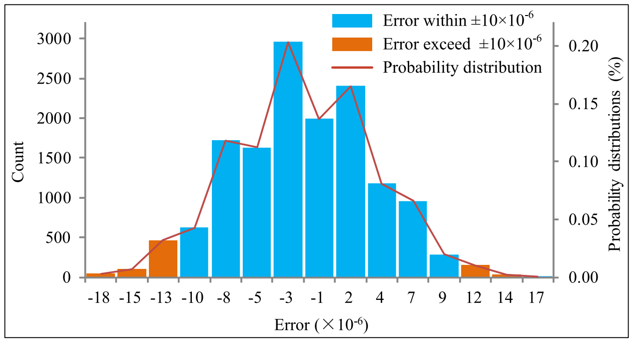

FIGURE 12. Short-term stability test results for the DC micro-difference device.

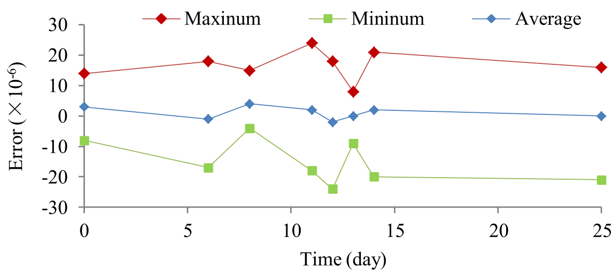

FIGURE 13. Long-term stability test results for the DC micro-difference device.

TABLE 1. Key technical specification of the DC micro-difference device.

Items	Technical Specifications
Input range	1 V-10 V
Offset voltage	Max: ±5 μV
Adjustment resolution	0.001%
Accuracy	Typical: $\pm 5\times10^{-6}$ 4 hours: $\pm 2\times10^{-5}$ 25 days: $\pm 3\times10^{-5}$
Standard deviation	Max: 5.6×10^{-6}

of time to reach a thermally stable state for best performance. By adjusting the offset voltage of the op amp, the output noise voltage of the device can be controlled within a range of $\pm 5\ \mu$V, ensuring that the standard error adjustment resolution of the device meets 0.001% in a range of 1 to 10 V.

An accuracy test of the DC micro-difference device was carried out. A standard DC voltage source with an accuracy higher than 0.01% was used to apply a standard DC voltage to the DC micro-difference device's input terminal. Two Agilent 3458A digital multimeters were used to measure the device's input and output voltage and calculate the relative error. The standard error deviation and the setting standard error are shown in Fig. 11. The test results show that the DC micro-difference device's standard error adjustment range is within ±1% under a voltage ranging from 1 V to 10 V, the maximum deviation from the setting standard error is not more than $\pm\, 2\times10^{-5}$, and the typical value does not exceed 5×10^{-6}.

The short-term stability test results for 4 hours and intermittent long-term stability test results for 25 days are shown in Fig. 12 and Fig. 13, respectively. During the long-term stability test, eight error measurement experiments were carried out over 25 days, and multiple repeated measurements were performed to obtain the maximum, minimum and average values each time. The test results show that the error within 4 consecutive hours and 25 days does not exceed $\pm\, 3\times10^{-5}$ with a maximum standard deviation of 5.6×10^{-6}. The measurement results in Fig. 13 show that approximately 95% of the measurement data is distributed within a range of $\pm\, 10\times10^{-6}$, which can meet the 0.001% adjustment resolution requirement, thus demonstrating good short-term and long-term stability.

The key technical specifications of the DC micro-difference device are summarized in Table 1.

B. DIGITAL ACCURACY TEST

A continuous sampling accuracy test of the DC ITTS calibration device was carried out with the Agilent 3458A digital multimeter. The sampling rate was set to 4 kHz and 12.8 kHz in a range from 1 V to 10 V, and the output digital signal under each range was 11585 to ensure that the quantization error remained unchanged. By analyzing and calculating the accuracy of the sampling value in the FT3 digital protocol, the test result is shown in Fig. 14.

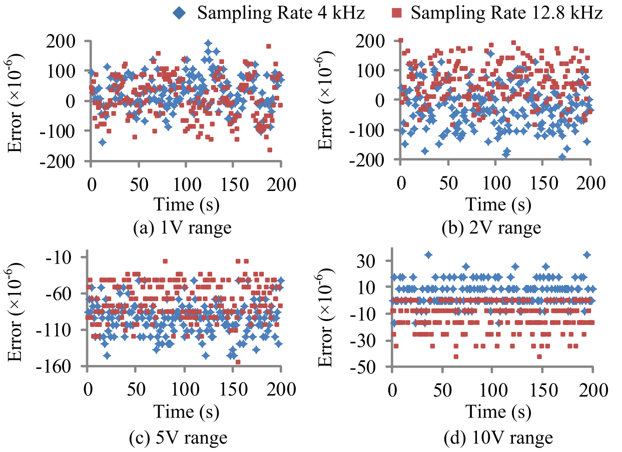

FIGURE 14. Continuous sampling accuracy test.

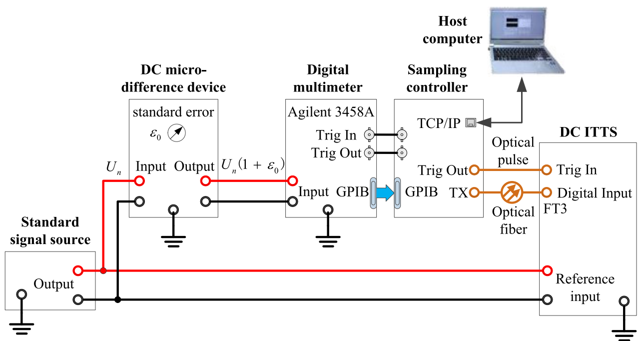

FIGURE 15. Calibration scheme of the DC ITTS.

The calibration device's sampling accuracy at 4 kHz and 12.8 kHz is similar, and the error is better than 2×10^{-4}. When the range is 1 V and 2 V, the error and the standard deviation is the largest. The maximum standard deviation of repeated measurements is approximately 7×10^{-5} at 1 V range and a 12.8 kHz sampling rate.

C. CALIBRATION TEST OF THE DC ITTS

A prototype calibration device for the DC ITTS was developed, as shown in Fig. 15.

A standard signal source outputs the standard reference DC voltage to the reference voltage input terminal of the tested DC ITTS with 0.05-class accuracy and the DC micro-difference device's input terminal. The DC micro-difference device converts the standard reference voltage U_n into the analog voltage U_n $(1+\varepsilon_0)$ according to the setting standard error ε_0 and then outputs it to the digital multimeter for A/D sampling. The sampling controller controls the Agilent 3458A digital multimeter for continuous sampling. The A/D samples are converted into an FT3 protocol digital message in real time. Then, the message is output to the digital input terminal of the tested DC ITTS. The DC ITTS simultaneously measures the analog reference voltage and the digital signal in the input terminal and calculates the relative error with formula (1). The error of the DC ITTS can be calculated with formula (2). Considering the error of the signal source, the DC micro-difference device and digital multimeter, the calculation formula of the DC ITTS's error can be modified from formula (2) to formula (8).

$$\begin{aligned}\varepsilon &= \varepsilon' - \varepsilon_0' = \varepsilon' - [(1+\varepsilon_0+\varepsilon_D)(1+\varepsilon_m)-1] \\ &= \varepsilon' - \varepsilon_0 - (\varepsilon_D + \varepsilon_m + \varepsilon_0\varepsilon_m + \varepsilon_D\varepsilon_m) \end{aligned} \tag{8}$$

where ε' and ε_0' describe the relative error measured and displayed by the DC ITTS and the actual relative error output by the calibration device, respectively, ε_0 represents the setting standard error, ε_D represents the additional error of the DC micro-difference device, ε_m represents the error of the digital multimeter. The error of standard signal source is not directly related to the error of the DC ITTS, but it is reflected in the measured error ε'. Compared with formula (2), the DC ITTS's error is also affected by the error of DC micro-difference device and digital multimeter.

The combined standard uncertainty u_c and expanded uncertainty U_{rel} with a coverage factor $k = 2$ for the DC ITTS's error can be calculated by formulas (9) and (10) [29].

$$\begin{aligned} u_c &= \sqrt{(\frac{\partial\varepsilon}{\partial\varepsilon'})^2 u'^2 + (\frac{\partial\varepsilon}{\partial\varepsilon_D})^2 u_D^2 + (\frac{\partial\varepsilon}{\partial\varepsilon_m})^2 u_m^2} \\ &= \sqrt{u'^2 + (1+\varepsilon_m)^2 u_D^2 + (1+\varepsilon_0+\varepsilon_D)^2 u_m^2} \qquad (9) \\ U_{rel} &= k u_c \qquad (10) \end{aligned}$$

where u', u_D, and u_m represent the standard uncertainty component introduced by the DC ITTS's measured value, DC micro-difference device, digital multimeter, and standard signal source, respectively. According to the error measurement result of the DC micro-difference device and the digital multimeter in section IV, it can be known that $\varepsilon_m = 2\times10^{-4}$ and $\varepsilon_D = 3 \times 10^{-4}$. Generally, the expanded uncertainty ($k = 2$) of the standard equipment does not exceed 1/3 of its maximum permissible error [30], Therefore, it can be assumed that $u_D = |\varepsilon_D|/6$, $u_m = |\varepsilon_m|/6$. u' reflects the standard uncertainty component u'_{rep} and u'_{res} introduced by the measurement repeatability and the display resolution of the DC ITTS, respectively, and depends on the larger one as in formula (11). u'_{rep} is affected by the error and quality of the standard signal source, and it is equal to the standard deviation of the DC ITTS's multiple measurements during the error calibration test. Since the resolution of the DC ITTS is 0.001%, u'_{res} can be calculated to be 2.9×10^{-6}.

$$u' = max\left\{u'_{res}, u'_{rep}\right\} \tag{11}$$

An error calibration test was carried out, as shown in Fig. 16, in which the prototype calibration device was used to calibrate a DC ITTS. The standard error within the range of ±1.0% was alternately applied under 10%, 20%, 50%, 80%, and 100% of the 10 V rated voltage to check the measurement error of the tested DC ITTS. The average value of 10 repeated measurements was taken as the measurement result in each test. A Fluke 5730A multifunction calibrator and a Keithley

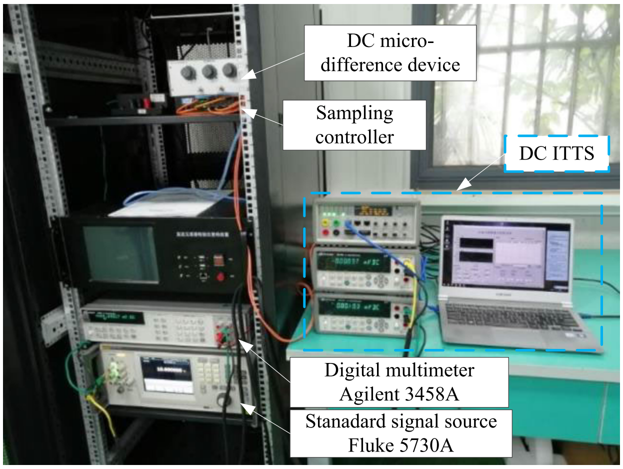

FIGURE 16. Calibration test diagram of the DC ITTS with Fluke 5730A used as the standard signal source.

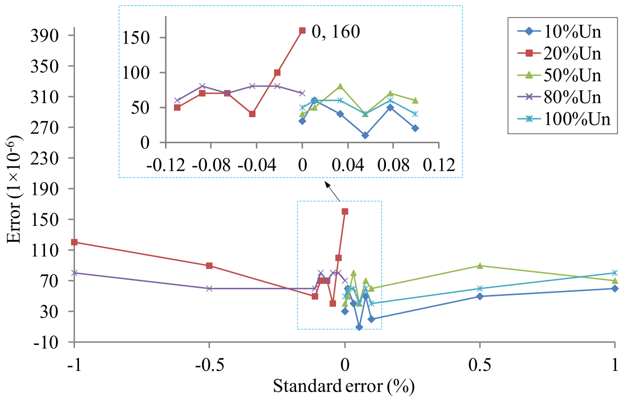

FIGURE 17. Error of the tested DC ITTS with a Keithley 2450 used as the standard signal source.

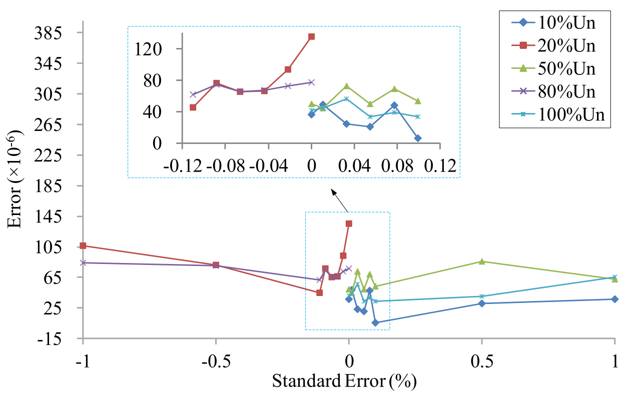

FIGURE 18. Error of the tested DC ITTS with a Fluke 5730A used as the standard signal source.

2450 interactive source-meter, which have different accuracy, were selected as the standard signal source, respectively.

The test data are illustrated in Fig. 17 and Fig. 18. When using Fluke 5730A and Keithley 2450 as the standard signal source, respectively, the deviation of the tested DC ITTS's error is small and does not exceed 3×10^{-5}, and the maximum error does not exceed 2×10^{-4}, which meets the error calibration requirements of the 0.05-class accuracy.

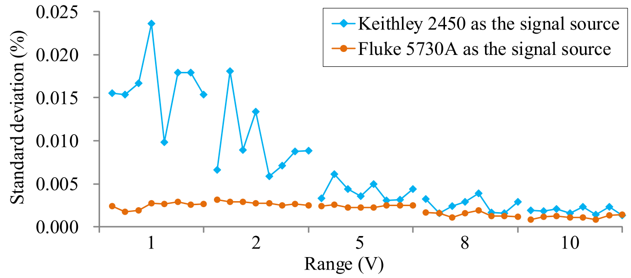

FIGURE 19. Standard deviation of the DC ITTS's repeated measurements with a Fluke 5730A and a Keithley 2450 used as the standard signal source.

TABLE 2. Uncertainty component of the calibration test.

Sources of uncertainty	Standard deviation/Error	Standard uncertainty component
Measurement repeatability	as shown in Fig. 19	
Resolution	0.001%	u_2=2.9×10^{-6}
DC micro-difference device	3×10^{-5}	u_D=5×10^{-6}
Agilent 3458A	2×10^{-4}	u_m=3.3×10^{-5}

The test results show that the developed calibration device can achieve a wide-range error calibration of the DC ITTS, ensuring that the DC ITTS meets the error calibration requirements of different DC instrument transformers with analog and digital signal outputs within the error distribution range of ±1%.

However, the standard deviation of the DC ITTS's repeated measurements differs greatly when using Fluke 5730A and Keithley 2450 as the standard signal source, as shown in Fig. 19. The accuracy of the standard signal source will directly affect the standard deviation of the DC ITTS's repeated measurements, thereby affecting the expanded uncertainty.

The standard uncertainties analyzed in formula (9) in the calibration test are listed in Table 2, which are derived from the actual measurement result.

The expanded uncertainty during the error calibration test can be calculated according to formula (9) and formula (10). When using Fluke 5730A as the standard signal source, the maximum expanded uncertainty is 9.1×10^{-5} in range from 1 V to 10 V. When using Keithley 2450 as the standard signal source, the expanded uncertainty is less than 1×10^{-4} in 8 V and 10 V range, and the maximum expanded uncertainty is 4.7×10^{-4} in range from 1 V to 5 V, which is a bit large and is not suitable for the calibration of the DC ITTS with a 0.05-calss accuracy [30]. Therefore, it is recommended to use a standard signal source with an accuracy better than 0.01% to reduce the standard uncertainty component introduced by the DC ITTS's measurements.

V. CONCLUSION

A calibration scheme for a DC ITTS based on an active operational amplifier using multistage series proportional micro-difference technology and FT3 digital real-time coding technology based on continuous sampling is proposed in this paper. A prototype calibration device for the DC ITTS was developed, and the performance test for the calibration device and internal components were carried out. The test results showed that the expanded uncertainty is better than 1×10^{-4}, the output range of analog standard error meets the range of $\pm 1\%$, and its maximum error does not exceed $\pm\ 3 \times 10^{-5}$. The accuracy of the FT3 digital message of the calibration device under a sampling rate of 4 kHz and 12.8 kHz is better than 2×10^{-4}, and the maximum standard deviation is approximately 7×10^{-5}. The calibration technology based on this scheme can solve the error calibration problem of digital channels for DC ITTSs in a wide standard error range and was successfully applied to the error calibration and testing of DC ITTSs in the National Center for High Voltage Measurement (NCHVM). Finally, the China National Accreditation Service for Conformity Assessment (CNAS) has approved the calibration test capability.

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HAOLIANG HU was born in Hubei, China, in 1984. He received the M.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2008, where he is currently pursuing the Ph.D. degree.

He is a currently a Senior Engineer with the China Electric Power Research Institute. His research interests include high-voltage and high-current metering, digital metering, calibration, and electronic instrument transformer applications. Mr. Hu was a recipient of the China Patent Silver Award, in 2020.

QI NIE received the B.S. and M.S. degrees in automation from the Wuhan University of Technology, Wuhan, China, in 2013 and 2015, respectively.

Since 2015, he has been a Research Engineer with the China Electric Power Research Institute. He is experienced in DC instrument transformer calibration technology and high-voltage measurement.

XIONG WU received the B.S. and M.S. degrees from the Wuhan University, Wuhan, China, in 1984 and 1987, respectively.

He is currently the Director of the Testing Center, China Electric Power Research Institute. His current research interests include the electromagnetic and insulation characteristics of AC-DC UHV transmission systems.

FUCHANG LIN (Senior Member, IEEE) received the Ph.D. degree in electrical and electronic engineering from the Huazhong University of Science and Technology, in 1996.

He is currently a Professor with the College of Electrical and Electronic Engineering, HUST. He has been working on pulsed power technology and high-voltage engineering.

FENG ZHOU received the Ph.D. degree in high-voltage and insulation technology from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2019. From 2006 to 2011, he was an Engineer with the State Grid Electric Power Research Institute, Beijing, China. In 2011, he worked with PTB, Brunswick, Germany, as a Guest Scientist for a half a year. He is presently a Professor, a Senior Engineer and the Director with the China Electric Power Research Institute. His research interests include high-voltage insulation and high-voltage and high-current measurement technology.

XIAOFEI LI received the B.S. and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2006 and 2015, all in electrical engineering.

Since 2019, he has been a Research Engineer with the China Electric Power Research Institute, Wuhan, China. His research interests include high-voltage metering, quantum electric metrology, and applications in power systems.

JICHENG YU (Member, IEEE) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2010, and the M.S. and Ph.D. degrees in electrical engineering from Arizona State University, Tempe, USA, in 2013 and 2017, respectively.

Since 2018, he has been a Research Engineer with the China Electric Power Research Institute, Wuhan, China. His research interests include sensors, smart meters, and big data analytics in power systems.