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An ESD and Interference-Robust Protection Circuit for Cascode Low-Noise Amplifier in CMOS-SOI Technology

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ABSTRACT In this paper, we propose a double diode network including an additional stacked diode, which provides robustness against Electrostatic discharge (ESD) and high-frequency interference signals. The proposed stacked diode in the conventional double diode network protects the integrated circuit from instantaneous voltage events by providing an additional current path to the double diode network. Also, it can structurally minimize the parasitic capacitance generated in the diode. The general operating principle and limitation of the conventional double diode network for ESD events and high-frequency interference signals were analyzed and simulated. For experimental verification, a cascode LNA with inductive source degeneration was designed in a 130nm CMOS Silicon-on-insulator (SOI) process for the time-division long-term evolution (TD-LTE) application at the coexistence band. The LNA with the proposed double diode network provides a noise figure of 1.08 dB and a small-signal gain of 18.7 dB at 2.65 GHz (Band 41). And it was measured to be able to protect the internal circuit at 2000 V HBM event, and the RF performances were not affected even with a high-frequency interference signal close to 30 dBm.

INDEX TERMS Electrostatic discharge (ESD), interference signal, low-noise amplifier (LNA), time division duplex (TDD), ESD protection circuit, double diode network.

I. INTRODUCTION

Wireless mobile communication has been rapidly evolving into the next fifth-generation (5G) system in response to the increase in user data traffic such as 2G/3G /4G-LTE and the demand for high-speed quality data transmission. To meet the demands, communication systems that provide efficient data services within insufficient frequency resources have been developed [1]–[6]. In the case of a mobile network for a 5G system, it is being considered that building a system through a high density of a microcell-based network which can improve the capacity and coverage of the wireless network. Also, as a method of increasing the frequency allocation efficiency, the conventional mobile systems use carrier aggregation (CA) of multi-carrier signals that simultaneously use frequency division duplexing (FDD) and time division duplexing (TDD). Here, the communication system in TDD is widely used in systems that require fast data traffic due to the high flexibility in user channel allocation. However, due to the coexistence frequencies, it is necessary to consider interference signals between devices [1]–[10].

TD-LTE system, which requires coexistence requirement in the frequency band from 2.3 GHz to 2.69 GHz, is defined as shown in Figure 1 to support representative band 41 and band 38 at the same time. As an example of interference signal scenarios, when a transmitted signal from other user equipment enters the receiver of user equipment, the internal circuit of the receiver IC can be damaged by the voltage signal of a high swing and the degree of damage

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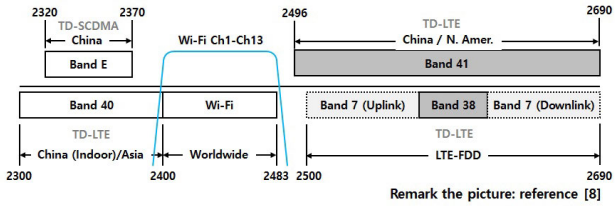


FIGURE 1. Spectrum of TD-LTE coexistence frequency (Wi-Fi, and cellular bands).

depends on the distance between devices. Therefore, it is necessary to protect the IC's internal circuit from interfering signals. The TD-LTE system has a burden of minimizing degradation in performance by using a filter with excellent attenuation due to adjacent frequency bands such as Wi-Fi. Likewise, the devices for 5G system are expected to be up and running in a complex interference environment with the rapid spread of devices that use the TDD scheme which increased the frequency allocation ratio is applied. In particular, the 5G systems for mobile terminals considered to use the TDD scheme will not be free from the interference signals due to coexistence frequencies such as TD-LTE [7]–[10].

For the typical receiver, various techniques have been studied to ensure a high linearity for in-band/out-of-band interference signals [11]–[14]. Among the methods, the feed-forward linearizer techniques have also been studied by the filtering method using additional up- and down-converters, or by controlling the resonant frequency of a notch filter to eliminate interference signals. However, it requires a high-precision sensing, which has the disadvantage of increasing circuit complexity and power consumption. There is a similar high voltage event that is known as ESD (electrostatic discharge). It is immediately generated in the processing and/or processing conditions of the chip and causes high voltage stress on the internal core transistor resulting in degradation of reliability. ESD events are divided into human body model (HBM), mechanical model (MM), and charging device model (CDM). Each event has different frequency response characteristics. To overcome ESD events, an ESD protection circuit is implanted inside the chip. However, interference signals from external devices must have faster discharge characteristics than ESD events due to high frequency. Therefore, it is inevitable that the reliability performance of the chip has degraded with only the ESD protection circuit.

In this paper, we propose a new double diode network with a stacked diode that can protect not only from the ESD events but also the interference signals. The protection circuit was designed and fabricated using the 130 nm CMOS-SOI process of excellent high-frequency behavior and low-power consumption. The designed LNA adopts a cascode structure with a degeneration inductor for both input matching and noise matching. This paper is organized as follows. Section II analyzes the operation and design considerations

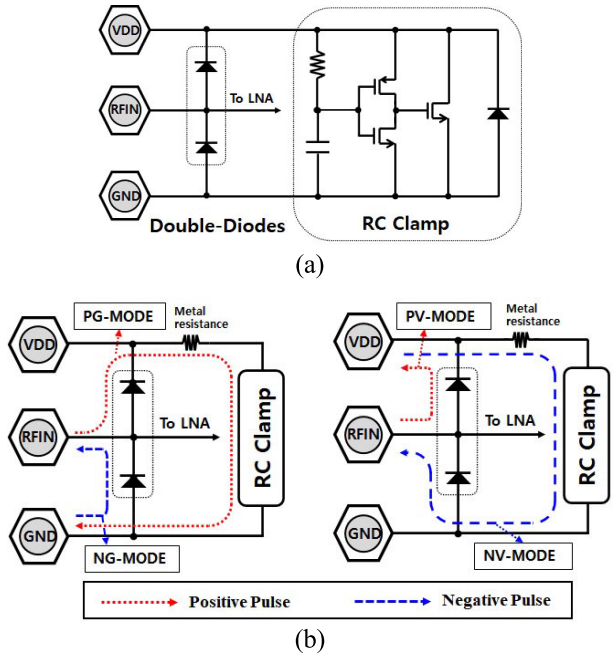


FIGURE 2. The operation principle of conventional ESD protection circuit: (a) Double diode network, and (b) Discharge current paths.

of conventional ESD protection circuits. It also shows the limitation with ESD events and high-frequency interference signals. Furthermore, based on the analysis, the solution is introduced. In Section III, the proposed LNA design method and a layout including the proposed protection circuit are presented. Section IV shows the comparison of simulation and experimental results before and after of ESD zapping and inserting interference signal. Finally, concluding comments are drawn in section V.

II. ESD PROTECTION CIRCUIT

A. CONVENTIONAL ESD PROTECTION CIRCUIT

As shown in Figure 2(a), the conventional double diode network using two diodes and an RC clamp on the pin is the most widely used in ESD protection strategy. This network includes one to the supply bus and the other to the ground bus, and it has an RC clamp for power clamping. The voltage level of the ESD events can exceed the breakdown voltage of the core transistors and destroy the circuit. Therefore, ESD protection must provide a preferred discharge current path to carry high currents. In normal operation, the network does not affect the internal circuit because the diodes and RC clamp are turned off, and it is turned on at only the high voltage level of the ESD event to provide a discharge current path of very low resistance. For the current path of low resistance, the layout of the ESD protection circuit must be designed using wide metal lines of low sheet resistance.

Figure 2(b) shows the discharge current path in accordance to the ESD event conditions. For a positive pulse at the RFIN pad to the GND pad, the double diode network provides

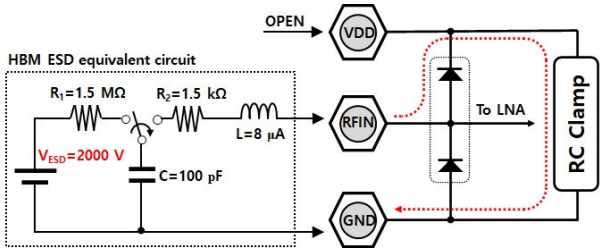
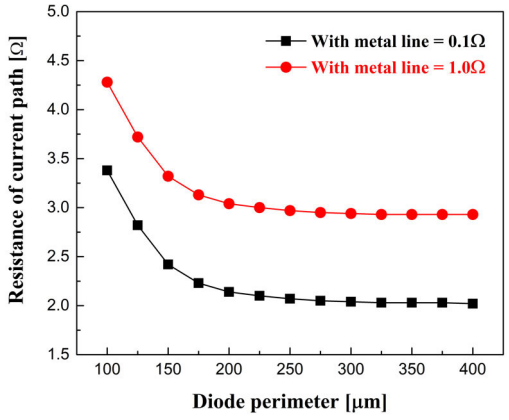
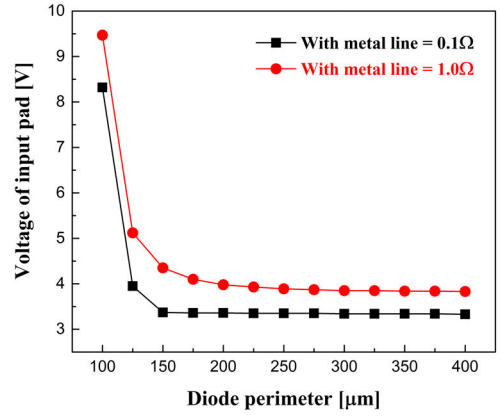


FIGURE 3. The HBM ESD equivalent circuit with the conventional double diode network.



(a)



(b)

FIGURE 4. The simulated results: (a) Resistance, and (b) Voltage on input pin according to the perimeter of diode.

the current path through the upper diode to the ground pin (PG-mode). For a negative pulse, the current passes through the lower diode and out the RFIN pin (NG-mode). Likewise, for a positive pulse at the RFIN pad to the VDD pad, the double diode network provides the current path through the upper diode to the VDD pin (PV-mode). For a negative pulse, the current passes through the low diode (NV-mode). Here, the PG-mode and NV-mode carry the current through the current path of the RC clamp. These discharge current paths should be designed in consideration of the current capacity according to the size of the RC clamp and the resistance of the metal line generated in the layout for the current path of low resistance.

For the simulation in Figure 3, a test-bench for 2000 V Human body model (HBM) was simply constructed as an HBM circuit that includes the 1.5 kΩ resistor (R_2), the 100 pF capacitor, and the 8 μH series inductor. Here, the optional stray capacitance of the resistor is neglected [15]. It was simulated using an HBM equivalent model with parasitic lumped elements regarding [15]–[18]. With a large series resistance (R_1) in the HBM model, the ESD test circuit can be modeled as a current source with a current waveform. The current peak is typically 1.2 – 1.48 A for 2 kV HBM ESD stress.

Figure 4 shows the resistance and voltage level of PG-mode current path according to the diode perimeter of the double diode. Each metal resistance for the simulation in Figure 2(b) was assumed to be 0.1 Ω and 1.0 Ω, respectively. The diode for the double diode configuration has a current characteristic of 7.28 mA/μm, the upper diode uses a P+/NW diode, and the lower diode uses an N+/SX diode. In Figure 4(a) and (b), the diode perimeter of 200 μm had a resistance of 2.14 Ω and a voltage of 3.36 V when the resistance of metal line was 0.1 Ω.

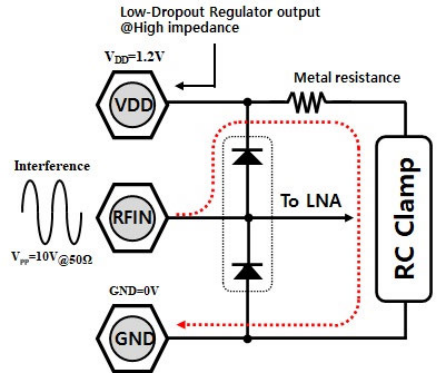
However, when the resistance of metal line is 1.0 Ω, the resistance of the current path has 3.0 Ω, and the simulated voltage is 3.98 V. As shown in the result of simulation, the resistance generated in the layout of the ESD protection circuit affects the protection level but cannot be removed. It can operate with a limit to the ESD protection level of the conventional double diode network.

B. THE LIMITATION OF PROTECTION FOR HIGH-FREQUENCY INTERFERENCE SIGNAL

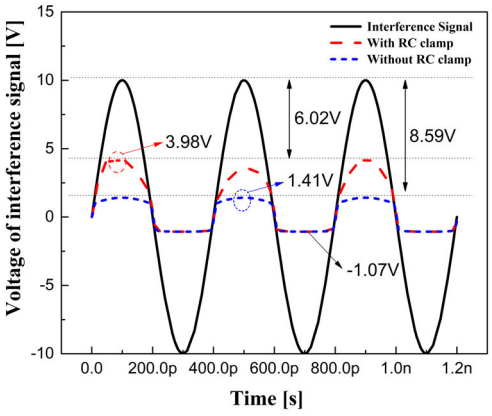
The double diode network operates in the PG-mode for high-frequency interfering signals, as shown in Figure 5(a). The PG-mode provides the current path of low resistance to ground through the upper diode and the RC clamp.

In the case of high-frequency interference signals, it must have a fast frequency response, however, PG-mode cannot protect the internal circuit to a sufficiently low voltage level due to the RC-constant delay of RC clamp. Therefore, it is difficult for the network to provide a sufficient discharge current path of low resistance. Figure 5(b) shows the interference signal and the simulated voltage at the input pin with and without RC clamp using the power level of 30 dBm with continuous wave (CW) at 2.5 GHz.

The input pin voltage of the double diode network with a 1.0 Ω metal resistance was simulated to be able to suppress a voltage of ± 10 V down to a positive pulse of 3.98 V and a negative pulse to −1.07 V. The positive pulse voltage of 3.98 V suppressed by the interference signal causes problems with the reliability of the IC due to continuous stress on the gate oxide of the internal circuit than the negative pulse voltage of −1.07 V. If the RC clamp is bypassed, the voltage of the input pin is 1.41 V and −1.07 V as shown in Figure 5(b), which can improve the reliability of



(a)



(b)

FIGURE 5. The PG-mode of double-diode network for interference signal: (a) Discharge current path, and (b) Voltage suppression results with and without RC clamp.

the integrated chip from the interference signal. For a high level of circuit protection against ESD event and interference signal, the current path of the PG-mode needs to be improved.

C. THE PROPOSED DOUBLE DIODE NETWORK WITH STACKED DIODE FOR ESD EVENTS AND INTERFERENCE SIGNALS

Figure 6 shows the circuit diagram of the proposed double diode network with a stacked diode. The stacked diode is directly connected to the input pin and the ground pin with double diode network to provide PG-mode current path for general ESD events and a current path for interference signal with fast frequency response characteristics. The interfering signal comes from an external device during the normal operation of the LNA being powered. Accordingly, the proposed stacked diode must be turned on with the same operating voltage as the upper diode for the additional PG-mode current path of double diode network. In addition, the stacked diode has an advantage of minimizing parasitic capacitance, while the diodes are connected in series and not in operation. If it is designed as a single diode, it turns on earlier than the upper diode and must endure the ESD event and interference signal alone. Furthermore, to be more strengthen,

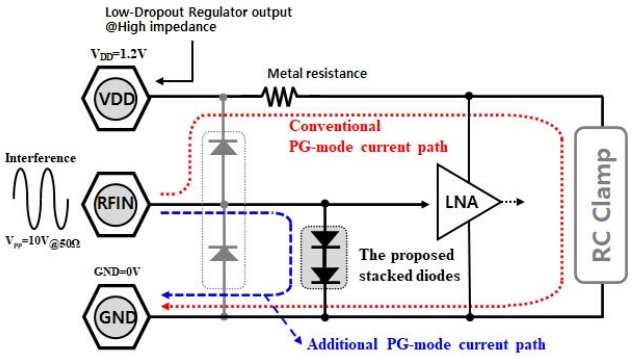
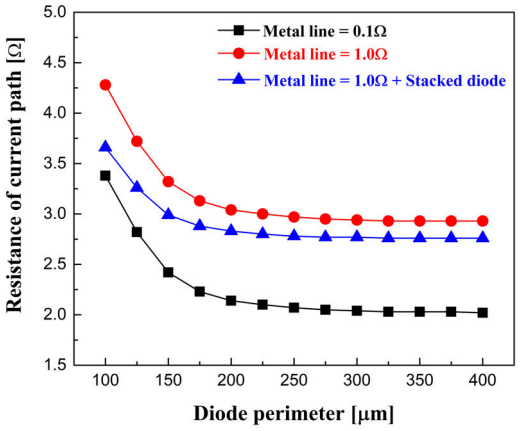
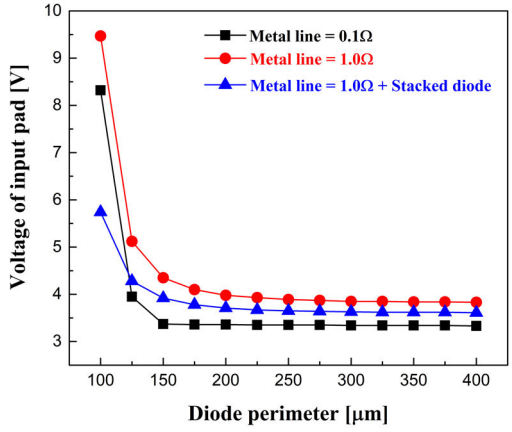


FIGURE 6. Discharge current path of the proposed double diode network with stacked diode.



(a)



(b)

FIGURE 7. The simulated results: (a) Resistance, and (b) Voltage on input pin according to the perimeter of diode.

it has large-sized diode perimeter and a large parasitic capacitance.

Figure 7 shows the simulated resistance of the current path and the input voltage according to the 2000 V HBM ESD event. For the simulation, the size of the stacked diode was indicated by the minimum size diode and it includes a metal resistance of 1.0 Ω and RC clamp circuit. A double diode

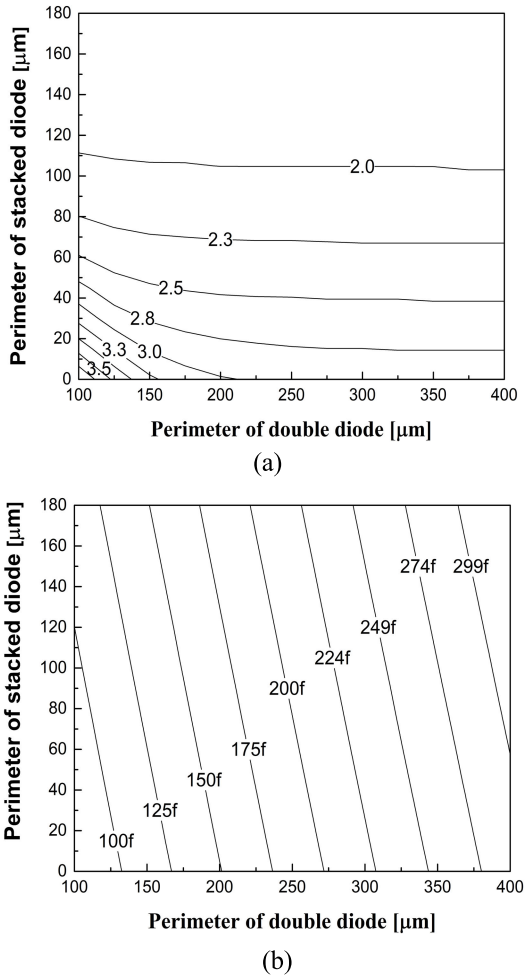


FIGURE 8. The simulated results: (a) Resistance, and (b) Capacitance on input pin according to the perimeters of stacked diode and double diode.

network of a 200 μm diode perimeter, including a stacked diode with 15 μm diode perimeter, was simulated by the resistance of 2.83 Ω. As a result, the proposed stacked diode can reduce the input voltage of 3.98 V to 3.71 V by reducing from 3.04 Ω to 2.83 Ω, respectively. This means that only the minimum-sized stacked diode applied to the simulation can improve the ESD protection level of the conventional double diode network. As explained using 2000 V HBM ESD simulation results, PG-mode current path and parasitic capacitance of the proposed double diode network according to the diode perimeter of double diode and stacked diode is shown in Figure 8.

We can select a proper diode size of the double diode and stacked diode to have low resistance and low parasitic capacitance for further optimization. For example, if the 200 μm double diode perimeter and 45 μm stacked diode perimeter are selected, the resistance can be reduced from 3.0 Ω to 2.48 Ω. In this case, the resistance cannot be obtained only by increasing the size of the conventional double diode network. The total parasitic capacitance is 157 fF. In addition, if 60 μm stacked diode perimeter is selected,

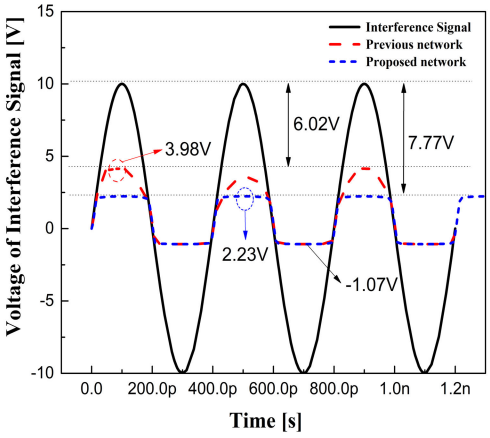


FIGURE 9. The simulation result of voltage suppression with and without stacked diode.

the resistance is 2.34 Ω. Here, the total parasitic capacitance of the proposed double diode network is 167 fF as shown in Figure 8(b). The simulation result shows the voltage suppression of the CW signal as shown in Figure 9. For the simulation, an interference signal having a power of 30dBm at 2.5GHz was used. The voltage at the input can be effectively suppressed from 3.98 V to 2.23 V using the proposed double diode network, indicating an excellent voltage suppression capability.

As a result, the proposed double diode network with stacked diode can protect the internal circuit from interference signals and the ESD events. Also, due to the low parasitic capacitance, the proposed stacked diode will have a minimal effect on LNA performance optimization.

III. LOW NOISE AMPLIFIER DESIGN

In LNA design, the input impedance is an important performance parameter that determines noise performance [19]–[26]. This input impedance was greatly affected by the parasitic capacitance generated in the peripheral circuit. Figure 10(a) shows the circuit diagram of the simple LNA design. It consists of an ESD protection circuit, pads for input and output, bumps for package, and an external high-Q inductor for matching.

Figure 10(b) shows the equivalent circuit of LNA. As shown, the equivalent parasitic capacitance of the double diode network, the total equivalent inductances for the degeneration inductor and bump inductor, and the external high-Q inductor and bump inductor are represented by C_{total}, L_s, and L_g, respectively. Here, C_{gd} neglects the parasitic capacitance between drain and gate regions. The LNA input impedance applying the equivalent model of this peripheral circuit is as follows.

$$R_S = \left(\frac{C_{gs}}{C_{gs} + C_{total}}\right)^2 \times L_S\omega_T \tag{1}$$

$$\omega_0^2 = \frac{1}{(L_g + L_s)(C_{gs} + C_{total})} \tag{2}$$

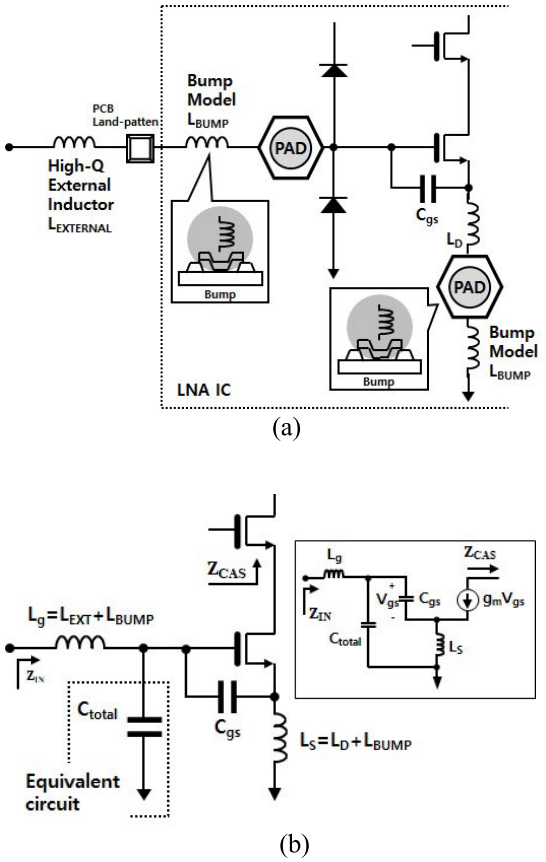


FIGURE 10. The schematic of LNA (a) With the parasitic components, and (b) The equivalent circuit.

Equations (1) and (2) show the real part of the input impedance of the LNA and the frequency of operation, Ω_0. Note that C_{gs} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate. Here, the equivalent capacitance of the double diode network, C_{total}, decreases the real part of the LNA impedance as shown in Equation (1). When the equivalent L_s inductance is used to compensate for the parasitic capacitance (C_{total}), a large L_s is required. However, the large degeneration inductance of the LNA leads to a degradation in the gain performance. Therefore, it is necessary to optimize the parasitic capacitance. However, applications requiring a high level of protection need a large-sized diode perimeter in protection circuit, and a large parasitic capacitance is inevitable.

The cascode LNA is designed and implemented for 2.65GHz in 700 μm $\times$ 400 μm size using the CMOS-SOI process. The proposed double diode network with stacked diode is arranged on pins for input and output, as shown in Figure 11. The diode perimeter for double diode was determined as 250 μm perimeter for 2000 V HBM ESD, and the stacked diode was designed as 60 μm perimeter. As shown in Figure 11, the LNA was designed as a Cascode-LNA including a degeneration inductor and a load inductor. For performance verification, the test-bench condition for measurement was performed while increasing the power of the continuous wave (CW) signal at 2.5 GHz, and 5 samples were

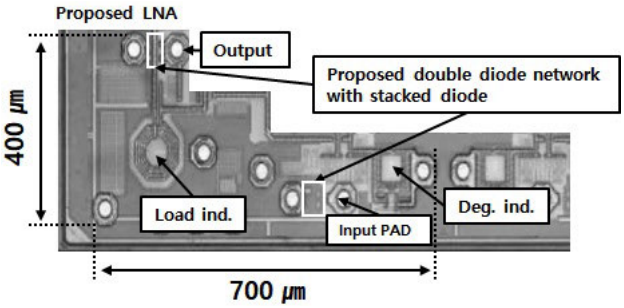


FIGURE 11. Photograph of the implemented LNA including proposed double diode network with stacked diode.

TABLE 1. Comparison of current before and after ESD zapping.

Samples	Before current [mA]	After current [mA]	DELTA	
			mA	|%|
1	8.29	8.26	0.03	0.003
2	8.31	8.33	-0.02	0.002
3	8.31	8.23	0.08	0.009
4	8.31	8.26	0.05	0.006
5	8.36	8.33	0.03	0.003

selected and measured according to the CW signal power during 10 minutes.

IV. EXPERIMENTAL RESULTS

ESD test was measured in PG-mode and NV-mode based on the input pin of RFIN as described in Section-II A. Injection pulses for 2 kV ESD events were performed with positive and negative stress pulses using 5 samples for measurement. The LNA current after ESD pulse zapping of each mode is compared with the current before ESD pulse zapping to verify any current changes which indicates that the ESD protection circuit is failed at the ESD stress level.

As in Table 1, which summarizes the results, the current of 5 samples were measured with changes of μA value. This level means that there is no current change in the 2 kV HBM measurement as a slight change that can change due to environmental conditions according to the measurement. As a result, the proposed double diode network with stacked diode satisfies the HBM stress of 2 kV. Also, the measured results of the s-parameter, NF, and linearity were no change, and the linearity (IIP_3) was measured as -5.9 dBm.

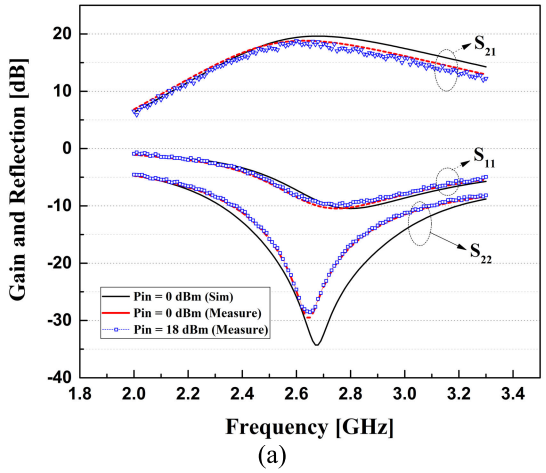
CW signal test using an adjacent frequency of 2.5 GHz was performed for the double diode network without stacked diode. Figure 12 shows the simulated and measured gain, reflection, and noise figure performance according to the power level of CW signal. The simulation and measurement results for linearity were not shown because there was no difference before and after the ESD zapping and the interference signal injection.

In Figure 12(a), when the interference signal was applied with 0 dBm, LNA was measured as the gain of 18.8 dB at a current of 8.26 mA, and S_{11} and S_{22} were measured as -9.5 dB and -29.4 dB, respectively. However, after applying

TABLE 2. Performance comparison to published lna with ESD protection circuit.

Reference	ESD Topology	Gain [dB]	NF [dB]	F_O [GHz]	V_{DD} [V]	P_{DC} [mW]	HBM [KV]	Interference [dBm]	Technology
[21]	SDeSCR	9.90	6.80	24.0	1.2	57.8	2.5	-	0.18um CMOS
[22]	Double diode network	13.8	0.98	0.90	1.2	5.2	2.5		0.13um CMOS
[23]	Double diode network	15.0	0.85	0.90	1.8	17.6	-3/2.3	-	0.35um CMOS
[24]	Two series diodes + reverse diode	19.2	0.65	1.57	2.8	16.5	2.5	-	0.18um CMOS-SOI
[25]	Trigger diode	13.0	3.60	2.40	1.2	6.5	2	-	0.13um CMOS-SOI
This work	Double diode network + stacked diode	18.7	1.08	2.65	1.2	9.8	2*	30dBm*	0.13um CMOS-SOI

* Mean value of 5 samples



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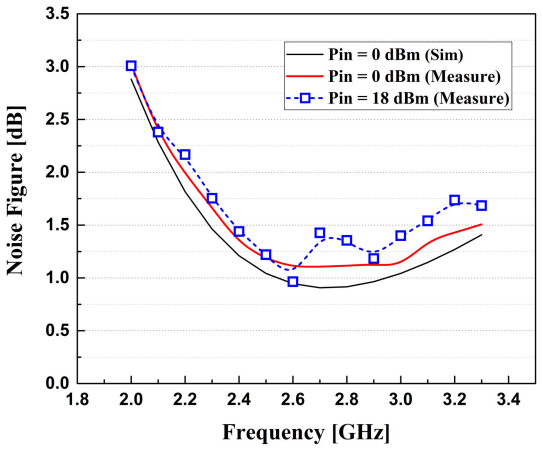
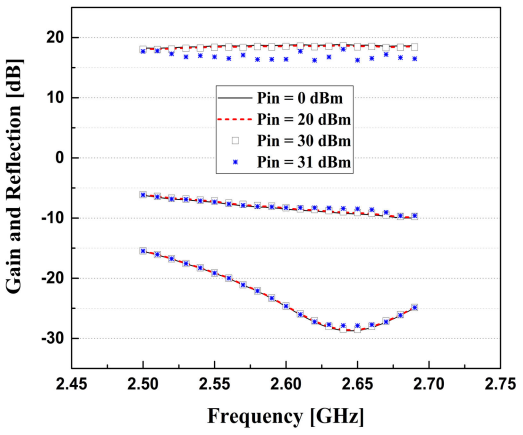


(b)

FIGURE 12. The LNA without the proposed double diode network: (a) S-parameters, and (b) Noise figure according to power level of CW signal.



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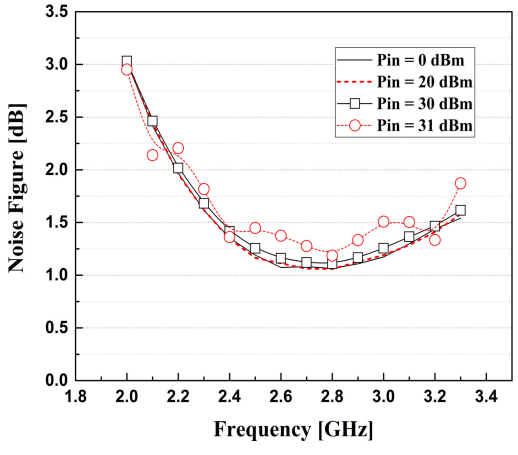

(b)

FIGURE 13. The LNA with the proposed double diode network: (a) S-parameters, and (b) Noise figure according to power level of CW signal.

a CW of 18 dBm for 10 min, the current of LNA decreased to 6.7 mA, and the gain was measured by 17.8 dB. And S_{11} and S_{22} were degraded to -8.8 dB and −28.5 dB, respectively. Figure 12(b) shows the noise figure degradation from 1.1 dB to 1.42 dB. LNA including a conventional double diode network cannot protect the circuit against interference signals of 18 dBm or more.

On the contrary, Figure 13 shows the measured gain, reflection, and noise figure performance according to the power

level of the CW signal. The measured results are used with 5 samples according to each power level and are shown as the average measurement result. The LNA was measured at an average current of 8.18 mA and a gain of 18.7 dB in the 2.65 GHz, and S_{11} and S_{22} were measured as −9.33 dB and −28.75 dB. At 30 dBm power of the CW signal, the LNA gained 18.45 dB at an average current of 8.0 mA, and S_{11} and S_{22} showed no significant difference as −9.1 dB and −28.5 dB, respectively. However, at 31dBm power of CW signal, the gain of LNA was measured as 16.23 dB, and S_{11} and S_{22} were measured −8.47 dB and −27.8 dB at an average current of 5.37 mA. The performance change according to the CW signal was largely observed in the noise measurement. As shown in Figure 13(b), up to 30 dBm power showed 0.4 dB noise performance degradation compared to 0 dBm power level. However, in the case of 31 dBm, the noise performance was significantly increased to 1.27 dB compared to 1.08 dB at 0 dBm power level. Table 2 summarizes and compares the performance. The CMOS-SOI LNA with the proposed double diode network exhibits good results in terms of the ESD event and interference signal. In addition, the measured results shown the average results using 5 samples for ESD event and interference signal.

V. CONCLUSION

The proposed double diode network has a sufficiently low resistance of the current path for ESD events and interference signals. For experimental verification, the cascode LNA and the proposed double diode network circuit were designed and fabricated using the 130 nm CMOS-SOI process. For ESD events and interference signal, the current path through the RC clamp provides a higher resistance than the current path in other modes, which limits the level of protection. To overcome the limitation, the proposed circuit uses a simple stacked diode structure to provide an additional current path at the same time as the current path of the RC clamp to protect the circuit from ESD events and interference signal. The LNA, including the proposed circuit, is designed with a gain of 18.7 dB at an average current of 8.18 mA, and S_{11} and S_{22} are designed as -9.33 dB and -28.75 dB. The designed LNA was measured to withstand high CW signal with only a change of 2.2 % current, 1.3 % gain, 2.4 %, and 3.3 % of S_{11} and S_{22} at a CW signal of 30 dBm. Also, the HBM of 2000 V required for general IC was satisfied in the designed LNA. The proposed double diode network is proposed for the protection circuit required for robust IC design in complex interference signal environments.

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REFERENCES

[1] N. Bhushan, J. Li, D. Malladi, R. Gilmore, D. Brenner, A. Damnjanovic, R. Sukhavasi, C. Patel, and S. Geirhofer, "Network densification: The dominant theme for wireless evolution into 5G," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 82–89, Feb. 2014.

[2] S. Hong, J. Brand, J. Choi, M. Jain, J. Mehlman, S. Katti, and P. Levis, "Applications of self-interference cancellation in 5G and beyond," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 114–121, Feb. 2014.

[3] D. Siafarikas, E. A. Alwan, and J. L. Volakis, "Interference mitigation for 5G millimeter-wave communications," *IEEE Access*, vol. 7, pp. 7448–7455, 2019.

[4] N. Peccarelli, B. James, R. Irazoqui, J. Metcalf, C. Fulton, and M. Yeary, "Survey: Characterization and mitigation of spatial/spectral interferers and transceiver nonlinearities for 5G MIMO systems," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2829–2846, Jul. 2019.

[5] W. A. Hassan, H.-S. Jo, S. Ikki, and M. Nekovee, "Spectrum-sharing method for co-existence between 5G OFDM-based system and fixed service," *IEEE Access*, vol. 7, pp. 77460–77475, 2019.

[6] K. Lim, "A 65-nm CMOS 2 × 2 MIMO multi-band LTE RF transceiver for small cell base stations," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1960–1976, Jul. 2018.

[7] K. Venugopal, M. C. Valenti, and R. W. Heath, Jr., "Device-to-device millimeter wave communications: Interference, coverage, rate, and finite topologies," *IEEE Trans. Wireless Commun.*, vol. 15, no. 9, pp. 6175–6188, Sep. 2016.

[8] (Dec. 11, 2015). *Qorvo Coexistence & Band-Edge Wi-Fi Filter Solutions*. [Online]. Available: https://www.qorvo.com/search?mode=1&key=qorvo-wifi-filter-brochure&des=&exact=&any=&none=

[9] A. V. Padaki, R. Tandon, and J. H. Reed, "Efficient spectrum access and co-existence with receiver nonlinearity: Frameworks and algorithms," *IEEE Trans. Wireless Commun.*, vol. 17, no. 10, pp. 6404–6418, Oct. 2018.

[10] R. A. Martins, I. Sousa, M. P. Queluz, and A. Rodrigues, "Interference cancellation techniques for device-to-device discovery in Out-of-Coverage networks," *IEEE Access*, vol. 9, pp. 10291–10303, 2021.

[11] R. Gharpurey, "Feedforward interference cancellation in narrow-band receivers," in *Proc. IEEE DCAS*, May 2006, pp. 67–70.

[12] S. Sadjina, R. S. Kanumalli, K. Dufrene, M. Huemer, and H. Pretl, "A mixed-signal circuit technique for cancellation of multiple modulated spurs in 4G/5G carrier aggregation transceivers," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 11, pp. 260–263, Nov. 2019.

[13] S. Pourbagheri, K. Mayaram, and T. S. Fiez, "A self-clocked blocker-filtering technique for SAW-less wireless applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 250–253.

[14] X. Zhang, Z. Chen, Y. Gao, F. Ma, J. Hao, G. Zhu, and B. Chi, "An interference-robust reconfigurable receiver with automatic frequency-calibrated LNA in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 11, pp. 3113–3124, Nov. 2017.

[15] O. Semenov, H. Sarbishaei and M. Sachdev, *ESD Protection Device and Circuit Design for Advanced CMOS Technologies*. Cham, Switzerland: Springer, 2008.

[16] *Electrostatic Discharge Sensitivity Testing-Human Body Model (HBM)—Component Level*, document JS-001-2012, Apr. 2012.

[17] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: Design concept and circuit implementations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 235–246, Feb. 2006.

[18] M.-D. Ker, C.-Y. Lin, and Y.-W. Hsiao, "Overview on ESD protection designs of low-parasitic capacitance for RF ICs in CMOS technologies," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 2, pp. 207–218, Jun. 2011.

[19] S. Voldman, D. Hui, L. Warriner, D. Young, R. Williams, J. Howard, V. Gross, W. Rausch, E. Leobangdung, M. Sherony, N. Rohrer, C. Akrout, F. Assaderaghi, and G. Shahidi, "Electrostatic discharge protection in silicon-on-insulator technology," in *Proc. IEEE Int. SOI Conf. Process.*, Jun. 1999, p. 68.

[20] P. Sivonen and A. Parssinen, "Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 4, pp. 1304–1313, Apr. 2005.

[21] C.-Y. Lin, G.-L. Huang, and M.-T. Lin, "Compact ESD protection design for CMOS low-noise amplifier," *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 33–39, Jan. 2020.

[22] A. Thakur and S. Chatterjee, "A 4.4-mA ESD-safe 900-MHz LNA with 0.9-dB noise figure," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 2, pp. 297–306, Feb. 2021.

[23] G. Gramegna, M. Paparo, P. G. Erratico, and P. De Vita, "A sub-1-dB NF±2.3-kV ESD-protected 900-MHz CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1010–1017, Jul. 2001.

[24] F. Song, S. C.-G. Tan, and O. Shanaa, "An ultra-low-cost ESD-protected 0.65 dB NF+ 10 dBm OP 1dB GNSS LNA in 0.18-μm SOI CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 341–344.
[25] M. El Kaamouchi, M. Si Moussa, P. Delatte, G. Wybo, A. Bens, J.-P. Raskin, and D. Vanhoenacker-Janvier, "A 2.4-GHz fully integrated ESD-protected low-noise amplifier in 130-nm PD SOI CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2822–2831, Dec. 2007.
[26] L. Belostotski and J. W. Haslett, "Noise figure optimization of inductively degenerated CMOS LNAs with integrated gate inductors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 7, pp. 1409–1422, Jul. 2006.
[27] A. O. Adan, T. Yoshimasu, S. Shitara, N. Tanba, and M. Fukurni, "Linearity and low-noise performance of SOI MOSFETs for RF applications," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 881–888, May 2002.
[28] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 5, pp. 1433–1442, May 2004.
[29] Y.-C. Wang, Z.-Y. Huang, and T. Jin, "A 2.35/2.4/2.45/2.55 GHz low-noise amplifier design using body self-biasing technique for ISM and LTE band application," *IEEE Access*, vol. 7, pp. 183761–183769, 2019.
[30] A. Madan, M. J. McPartlin, C. Masse, W. Vaillancourt, and J. D. Cressler, "A 5 GHz 0.95 dB NF highly linear cascode floating-body LNA in 180 nm SOI CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 4, pp. 200–202, Apr. 2012.

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