Silicon Carbide Multi-Chip Power Module for Traction Inverter Applications: Thermal Characterization and Modeling

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ABSTRACT Semiconductor power modules are the key hardware components of a traction inverter. It drives motor speed and torque, managing the energy exchange from battery to motor and viceversa. The increasing demand for electric and hybrid vehicle requests high performance power modules. Power semiconductor devices based on wide band gap compound, like silicon carbide (SiC), have excellent electrical properties in terms of on-state resistance, stray inductance and performance at high commutation frequency. One of the most promising solution is silicon carbide MOSFET power module in which each switch is made by several different dies placed in parallel. Embedded direct cooling system and novel materials with high conductivity (e.g., active metal brazed substrates) can be considered to enhance thermal performance. A robust method is needed to characterize and to predict power module temperature behavior considering the importance of the thermal performance to improve reliability and to optimize module weight and dimensions. According to several parallel dies inside each switch, classic method based on temperature electric sensitive parameter (TSEP) shall be validated with direct measurement. In this framework, it has been reported the thermal characterization of a power module for a traction inverter based on eight silicon carbide MOSFETs for each switch. Both TSEP and infrared measurements have been employed. Thermal behavior has been numerically reproduced, creating a simplified equivalent network and developing a predictive model by finite element method (FEM).

INDEX TERMS Power modules, SiC MOSFET, thermal measurements, numerical model.

NOMENCLATURE

τ	Time constant
AMB	Active metal brazed
BLT	Bond line thickness
BOM	Bill of material
C_{th}	Thermal capacitance
CFD	Computational fluid dynamics
DBC	Direct bonded copper
FEA	Finite element analysis
FEM	Finite element method
FFT	Fast Fourier transformation
I_{bd}	Body diode current
I_{ch}	Drain-source channel current

I_{Load}	Forcing current load
IR	Infrared
MWIR	Midwave infrared
OEM	Original equipment manufacturer
P	Dissipated power
R_{DSon}	Drain-source on-resistance
R_{th}	Thermal resistance
RC	Resistor-capacitor
T_{cool}	Cooling fluid temperature
T_{vj}	Virtual junction temperature
TSEP	Temperature sensitive electric parameter
V_{DS}	Drain-source voltage
V_g	Gate voltage
V_{SD}	Source-drain voltage
Z_{th}	Thermal impedance

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I. INTRODUCTION

The electric and hybrid vehicles demand is nowadays increasing with the mid-term forecast trend to become the dominant portion of the automotive market. These means of transportation face the severe energetic and pollution constrains to allow the sustainable development required by environment care, homologation policies and public opinion. The hybrid and electric vehicle massive diffusion strongly requests for reliable and high-performance traction inverter which is the crucial element for electric power conversion. The inverter commutes energy from battery to motor and viceversa. Its key hardware component is the power semiconductor module which drives the speed and torque according to a specific signal modulation [1]. Many aspects related to the power module design and engineering need to be optimized to fulfill the original equipment manufacturer (OEM) requirements in terms of performances and reliability capabilities. The optimization strategy deals with a multi-physic approach that covers the power module dimensional optimization, which facilitates the mechanical integration inside the powertrain and the lightening of the whole system, the thermal optimization by high heat exchange cooling systems and the parasitic optimization for the switching loss reduction. All these aspects are addressed to reach an overall efficiency enhancement that is fundamental to enlarge the vehicle driving range.

In this context, wide band gap materials, such as the silicon carbide (SiC) power MOSFETs, present superb capabilities in terms of electrical and physical properties. They allow to reduce both switching and conduction losses which guarantees higher switching frequency, to work with higher electric field and higher breakdown voltage, and to move forward the operative temperature constraints (above 200 °C) in comparison with conventional Si devices [2]. An additional advantage of SiC power MOSFET, with respect to conventional Si IGBT, is the lack of freewheeling diode. The diode is needed in IGBT module to create a suitable path during device switching off, avoiding the inductive high voltage peaks which could damage the switch. In SiC power module, the freewheeling diode is replaced by power MOSFET intrinsic body diode [3]. By contrast, in order to have the same current capability of equivalent power switches made by IGBTs, it is necessary to consider several SiC dies in parallel for each power switch. This issue is related to the higher intrinsic defectiveness of SiC devices in comparison with mature and debugged technologies like Si. These defects can be screened by dedicated over-inking at wafer level or by burn-in testing at die level. In order to maintain a high production yield, it is needed to manage device with limited die size in comparison with equivalent Si IGBTs.

Considering the mentioned SiC MOSFETs features, in combination with the increased temperature limit capability, it is possible to engineer lighter, more efficient and more compact modules. An optimized option for heat exchange is based on direct cooling concept in which the heatsink is integrated in the module itself and directly in contact with the coolant by pin-fins [4], [5]. A concomitant big effort for thermal optimization has been also done by improving the thermal properties, conductivity and thermal resistance of interfaces, of the whole bill of materials. In this framework, the direct-bonded-copper (DBC) technologies which constitute the module insulated substrate, made by two layers of copper interleaved by a thin layer of ceramic dielectric, have been replaced by the active metal brazed (AMB) ones. AMB substrates, thanks to the higher thermal conductivity of the dielectric layer (silicon nitride for AMB instead of alumina for DBC) represent both a significant improvement for the overall thermal stack and also an enhanced solution from a reliability point of view. The main limiting factors for power module durability are represented by lift-off wire bonding degradation and die attach solder delamination [6]. Silver sintering technology for die attach is one of the enabling factor to augment reliability, thermal performances due to better thermal conductivity and more robust bond line thickness (BLT) control. Due to silver high melting point compared with conventional tin-based solder alloy (e.g., SnAg), silver sintering permits to exploit a wider temperature range of the SiC devices without being limited by packaging constraints [7]–[10].

A robust experimental method is needed to quantify the power module thermal performance, reproducing as close as possible the operative thermal boundaries. The main challenge is related to the measurements of the real device temperature. It is possible to measure it by thermo-couple attached on the module or, when removing the module plastic cover and the potting gel over the dies, by infrared (IR) camera. By the way, considering that the proposed method is invasive, the most suitable method for power module thermal characterization without impacting its mechanical structure is to correlate the device virtual junction temperature (T_{vj}) with a temperature sensitive electric parameter (TSEP). Considering power MOSFET, the body diode voltage drop is considered as the temperature sensitive electrical parameter to estimate the device virtual junction temperature. Once a sensing current has been fixed, a linear relation between body diode voltage drop and device temperature could be found. SiC MOSFET power device must be driven with a negative gate voltage to avoid a parallel current path between MOSFET source-drain channel and body diode, ensuring correct and stable temperature measurements. In the specific case of power module with several parallel SiC MOSFET devices, using the electrical measurements of body diode voltage drop, it is not possible to point out the eventual thermal unbalancing among dies due to their spread in the drain-source on-resistance (R_{DSon}) values. A direct method for temperature estimation, such as IR camera measurements, has also been considered in this work as a validation method and to analyze the temperature distribution among the dies of a single switch.

Power module thermal behavior can be also numerically reproduced and calculated. Starting from measurements, it could be found a lumped network that easily describes switch temperature as later explained in section IV.

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Elaborating the so-calculated lumped network, it is possible to express "the distribution of thermal capacitance along the heat flow path, where the position on this path is expressed by the cumulative thermal resistance starting from the junction" [11]. This formulation can be translated in a thermal capacitance-thermal resistance plot that graphically represents the thermal behavior of material stack. The transition from a material to another is characterized by plot slope modification. The mentioned method is known as "structure function". By contrast to the graphical representation, the development of structure function requires an elaborated numerical transformation which can affect the result. Furthermore, this method is suitable to detect the transition between a material with high thermal conductivity (e.g., copper) and a material with a much lower thermal conductivity (e.g., die solder or alumina). When high thermal performance materials are introduced in the BOM (e.g., silver sintering in replacement of soft solder), material transition becomes smoother and more difficult to detect in structure function representation. Due to the difficulty to analyze the package thermal behavior using structure function, an approach based on finite element method (FEM) shall be considered. FEM is commonly used to analyze and predict power packages behavior under several points of view such as mechanical, hygroscopic, electric and thermal [12]. The aim of the present work has been the assessment of a robust temperature measurement method for a SiC-based power modules for traction inverter application with several devices in parallel. TSEP method and IR camera measurements have been performed. The overall thermal behavior has been described by an equivalent simplified RC-network and correlated by finite element method.

II. TEST VEHICLES

The test vehicles considered in this analysis have been Acepack^{TM} Drive power modules (Fig. 1) for traction inverter applications with minimized stray inductance and boosted speed capabilities. The topology of the power module is a "Six-pack" type with each switch made by eight SiC MOSFETs in parallel. The high heat exchange efficiency and therefore the reliability performances are guaranteed by liquid coolant directly in contact with the pin-fins of module's baseplate. These improvements are additionally enhanced by a proper material stack selection. Silver sintering die attach material has been used for its excellent thermal conductivity, its durability during the entire lifetime and to ensure a thin and constant bond line thickness (BLT). Active metal brazed (AMB) substrates have been introduced due to the high thermal conductivity of the their dielectric layers (Si_3N_4) and due to the superb reliability performance of metal-dielectric joint.

III. THERMAL IMPEDANCE MEASUREMENT

The thermal behavior has been characterized by means of Alpitronic's power cycling test bench in which the thermal boundaries have been imposed by an embedded hydraulic circuit that is capable to regulate the coolant flow rate
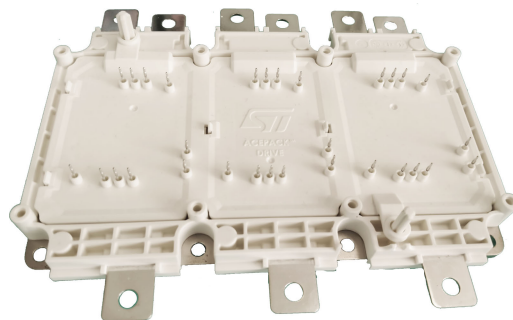

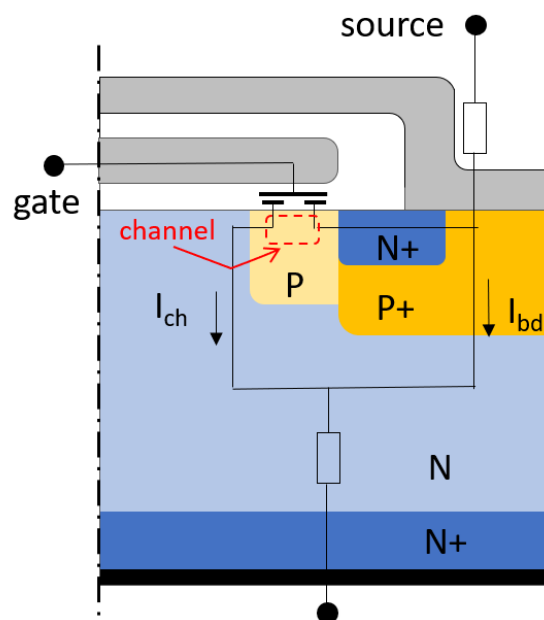**FIGURE 1.** Acepack drive automotive power module.

FIGURE 2. Possible current path during temperature sensing. A sufficient negative voltage (-8V) shall be applied to ensure all current flows across body diode (I_{bd}) and not along the MOSFET channel (I_{ch}).

and temperature [13]. All measurements have been performed in compliance with the current automotive normative, AQG 324 [14]. The temperature has been indirectly estimated by measuring the body diode voltage drop during the device off-state in which a sensing current of 100 mA flows. The choice of body diode drop voltage as TSEP has been in accordance with the standard approach for SiC power MOSFET [14]–[16]. Power module has been heated by self-heating effect induced by a current, in the order of some hundreds of A, that flows across SiC MOSFET channel. A dedicated controller manages gate voltage to ensure positive value during the current forcing and negative value of −8 V during the temperature sensing. This negative voltage is required to safely turn-off MOSFET channel, avoiding any current parallel between body diode (I_{bd}) and drain-source channel (I_{ch}), as depicted in Fig. 2. The eventual parallel might affect the temperature sensing, therefore application of negative voltage is mandatory for a reliable measurement [15].
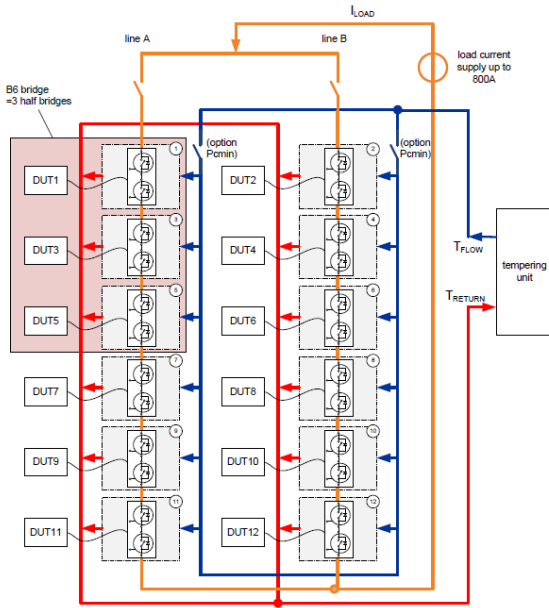
FIGURE 3. Power bench hydraulic and electric layout.

FIGURE 4. Calibration curve (a) and derating factor boxplot, coming from 202 measured switches (b).

Switches have been calibrated in a dedicated climatic chamber before testing. In this stage, power module is heated at different temperature values inside a controlled environment for enough time to stabilize thermal condition. After thermal steady-state is reached, the body diode drop voltage has been measured at a rated sensing current. Bench layout has been reported in Fig. 3.
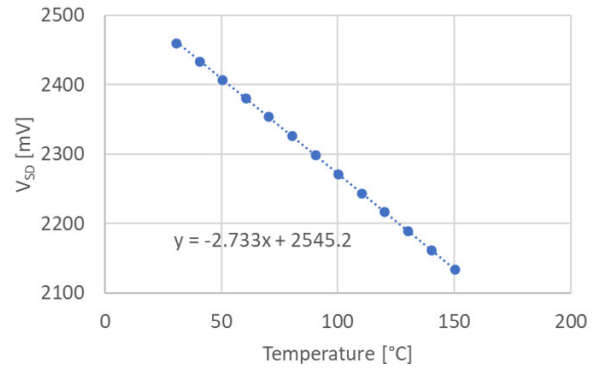
Thermal impedance has been extrapolated by a quite simple elaboration of the measured temperature profile, as reported in equation 1:

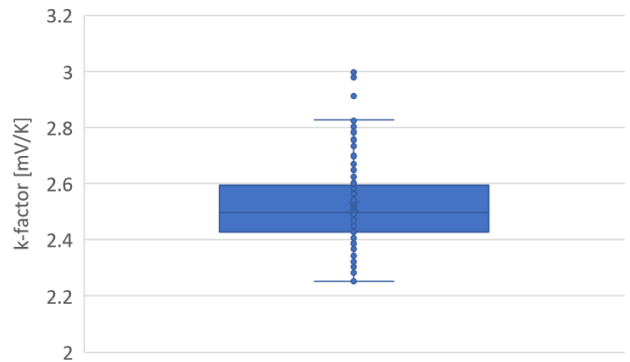$$Z_{th}(t) = \frac{(T_{vj}(t_0) - T_{cool}(t_0)) - (T_{vj}(t) - T_{fluid}(t)}{V_{DS,max} \cdot I_{Load}} \quad (1)$$

in which T_{vj} is the virtual junction temperature, T_{cool} the cooling fluid temperature, $V_{DS,max}$ the drain-source voltage and I_{Load} the forcing current load. t_0 represents the time when the first temperature measurement has been done after device switch-off (in this case, 100 μs).

A. CALIBRATION RESULT

Power module switches have been calibrated inside a thermal chamber and varying the temperature from 20 to 150 °C. Calibration output has been shown in Fig. 4a, in which there are reported all measurement points and the resulting linear regression fit. The graph highlights relation between V_{SD} and temperature is almost linear, with a calculated slope, so-named as *derating factor*, of 2.7 mV/°C. Analyzing the calibration results among over 200 switches and excluding few outliers, derating factor ranges between approximately 2.25 and 2.8, as depicted in in the boxplot analysis shown in Fig. 4b.

B. THERMAL IMPEDANCE RESULT

Thermal impedance measurement procedure has a duration of two minutes, split in two time equal parts. In the first, current load heats the power module switch, which reaches the steady-state condition. In the second part, device cools down and the temperature during the cooling is detected through the temperature sensitive parameter. According to equation 1, thermal impedance is indirectly obtained. In order to analyze the impact of coolant fluid temperature, the measurements have been performed fixing different inlet coolant temperatures. Experiments have been repeated on six different switches, fixing the inlet fluid temperature both at 50 and 75 °C. Fig. 5 shows temperature profile and resulting thermal impedance for one switch (#5). The thermal resistance results for all switches have been provided in the Table 1. According to the accuracy of voltage measurement (0.150 mV), R_{th} has been estimated with an error of 1×10^{-3} °C/W. Slightly higher R_{th} values have been observed at higher coolant temperature. A possible root cause has been given by material properties degradation increasing temperature.

C. THERMO-CAMERA VALIDATION

It is a well-established routine to measure the junction temperature in power MOSFET by the correlation with body diode drop voltage. Nevertheless, the measurements on SiC power module, in which the single switches are made by several parallel devices, is not a so-diffused standard.
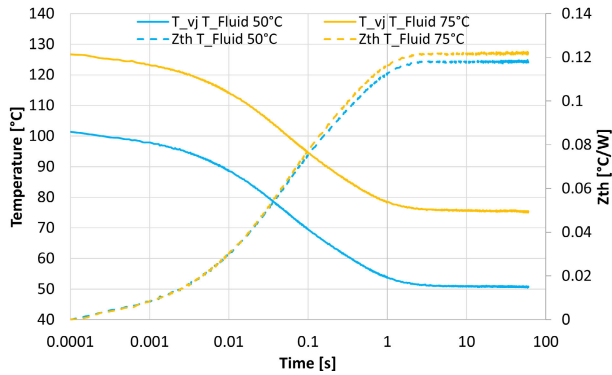
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FIGURE 5. Measured temperature and resulting Z_{th} for switch #5, at different fluid temperature. Thermal impedance is slightly worst at higher fluid temperature, resulting in higher thermal resistance value (0.116 **vs** 0.120 °C/W**).**

TABLE 1. Measured thermal resistance in °C/W at different inlet coolant temperature.

Switch #	T_{fluid} 50 °C	T_{fluid} 75 °C	Variation
1	0.115	0.117	2.4 %
2	0.116	0.122	5.1%
3	0.112	0.115	2.0%
4	0.118	0.124	4.8%
5	0.116	0.120	3.1%
6	0.112	0.116	3.4%

Furthermore, TSEP evaluation provides only an overview of switch average thermal behavior and it is not focusing on the single die behavior. Considering the process variability, the electric characteristics of single device might differ from the others, leading to an uneven temperature distribution inside the single switch. As consequence, an experimental procedure has been assessed to analyze the temperature distribution inside the switch and to validate the indirectly measured temperature by TSEP. The temperature evolution during a power cycle has been recorded using equipment FLIR X6580sc, which is a highly sensitive, high-speed, high definition midwave infrared (MWIR) camera. In order to enable accurate temperature measurements with IR camera, a power module has been assembled considering dedicated process flow, without insulating silicon gel. Before measurement, the sample has been painted with an insulated black matt paint. IR temperature acquisition has been performed during power cycle test, in which a current load of 353 A has been applied for 3.5 s. Device has been cooled for 4 s (total cycle duration: 7.5 s) and body diode drop voltage has been measured with sensing current of 100 mA and driving the gate voltage (V_g) at -8 V. The picture extracted at the maximum temperature has been shown in Figure 6, reporting a quite uniform thermal distribution inside four devices from the same switch. The average IR temperature inside the active area of four devices is 153 °C, while the virtual junction temperature acquired by TSEP correlation after 100 μs from switching off has been 152 °C. A temperature gradient of approximately 35 °C has been measured between the hottest point in the center and the coldest one at the device edges. It has been expected due to the previous literature findings
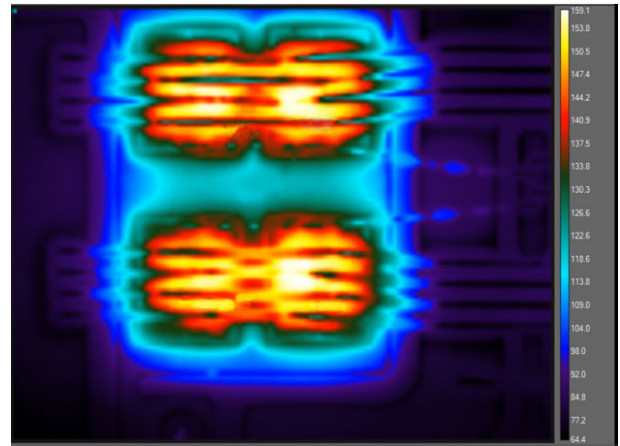

FIGURE 6. Frame extracted from IR temperature measurement at maximum temperature. Four different devices inside the same switch have been captured.

such as [17]. The quite good correlation between the average temperature detected by infrared camera and the indirect temperature estimated by TSEP has been aligned with other literature results for single SiC power MOSFET device [18] and IGBT power modules, also considering the behavior of two paralleled dies [19].

IV. LUMPED EQUIVALENT NETWORK

A numerical, easy-to-use, representation of power switch thermal behavior can help the design development. For example, a simplified thermal behavior mathematical description can be integrated into SPICE model in order to estimate device average junction temperature due to power losses [20]. A diffused approach inside power electronics is the construction of an equivalent RC network. The classic method is based on RC networks identification by frequency or time responses, as proposed by [21]. According to this methodology, all response functions are converted in frequency domain by convolution integrals. The identification of RC parameters of the equivalent Foster network is carried out deconvulating the calculated functions inside frequency domain. This method has been standardized by JEDEC association [11]. In this framework, a routine to calculate the equivalent RC Foster network has been implemented in SCILAB, transforming time data in frequency domain by means of Fast Fourier Transformation (FFT) algorithm, then the equivalent RC parameter and the related thermal impedance function has been obtained by deconvolution. The partial functions in Fourier domain and final thermal impedance have been plotted in Fig.7. Numerical curve has been calculated according to a lumped six-poles RC network. Its layout has been reported in Fig. 8, while RC parameters have been specified in Table 2. Resulting temperature, as time function, can be calculated according to this formula:

$$T(t) = P \cdot \sum_{i=1}^{6} R_{th,i} \cdot [1 - exp(-t/\tau_i)] \qquad (2)$$

in which P is dissipated power and it could be set equal to one due to thermal impedance definition. Time constants τ_i
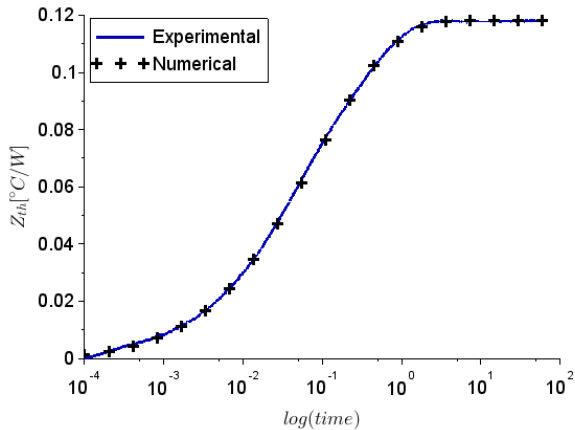
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FIGURE 7. Calculated thermal impedance according to lumped network and experimental Z_{th} measurements.
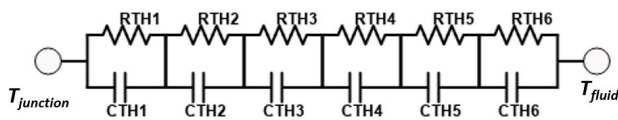

FIGURE 8. Calculated six-pole equivalent thermal network.

TABLE 2. Parameter of the thermal RC network which reproduced power module behavior.

Pole number	Resistance R_{th} [°C/W]	Capacitance C_{th} [Ws/K]	Time constant τ [s]
1	0.0022	0.1307	0.00029
2	0.0054	0.2489	0.00136
3	0.0156	0.4758	0.00741
4	0.0337	1.0729	0.03619
5	0.0393	4.4336	0.17420
6	0.0219	36.913	0.80982

are calculated according:

$$\tau_i = R_{th,i} \cdot C_{th,i} \qquad (3)$$

in which $C_{th,i}$ refers to the lumped thermal capacitance of the equivalent RC network, as shown in Fig. 8. The computed behavior is very close to the measured Z_{th}, Indeed, it could be implemented in simple way, e.g. in a spreadsheet, to make reliable prediction of average device temperature due to known power loss profile.

V. FINITE ELEMENT ANALYSIS

The mentioned numerical method has permitted to describe the power module thermal behavior by a simple electric diagram in which the temperature is extrapolated by Eq. (2). The main limit of the above methodology is that it cannot be predictive because it is based on a post-elaboration of thermal impedance. Numerical simulation is able to predict power module thermal behavior, accounting different design options. Furthermore, virtual model gives the opportunity to quantify the impact of single package component on the overall thermal behavior. Appropriate simulations could be set to characterize the heating dynamic, finding out how much time is needed by an interface to affect the heat flow. A correct determination of heating dynamic helps for the optimization of in-line testing during module manufacturing. By thermal
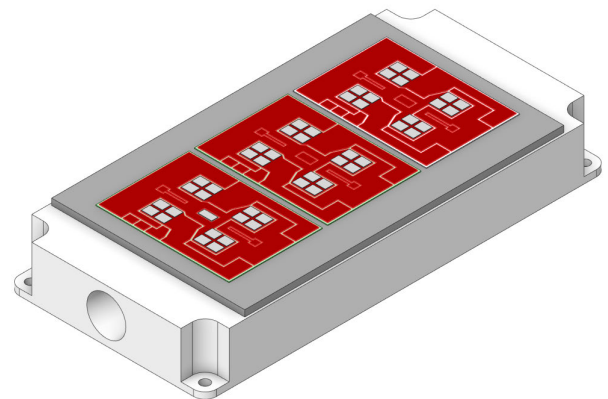

FIGURE 9. Simulated finite element model.

characterization results it is possible to set the most proper time to check interfaces or materials of power module. For the sake of example, FEA could help to understand when a not-good sintering die attach, e.g. with a partial sintered area, starts to get worst the thermal impedance. Testing time should be selected accordingly. Finally, the lumped equivalent network approach can be applied also on the temperature output coming from simulation model. Preliminary to theoretical considerations and design optimizations, the numerical model must be calibrated with a proper experimental dataset.

A Finite Element Model has been employed using COMSOL Multiphysics. The thermal exchange between power module baseplate and cooling fluid has been modeled according to the computational fluid dynamics (CFD) embedded in COMSOL tool. Simulation has reproduced the measurements reported in Fig. 7, in which the cooling media has been a mixture water/glycol (with the ratio of 50/50%), with inlet temperature fixed to 50 °C and flow rate of 10 l/min. Considering that the calculated Reynolds number inside cooling device which is approximately equal to 6300, flow regime has been modeled according K-epsilon turbulence model [22]. The assumption has been confirmed by the velocity field calculated by preliminary simulations. Module surfaces which can thermally exchange with surround environmental air have been assumed adiabatic. Due to the low thermal conductivity and accounting that heat inside the modules flows from device to baseplate, plastic cover has not been modeled. Considered model has been plotted in Fig. 9.

The heat source has been placed on the top side of SiC power devices, according to the fact most power losses occur in the MOSFET frontside. Heat source has been fixed to 1 W, equally partitioned among the eight dies (0.125 W for each die), to calculate the switch thermal impedance. Cooling performances have been estimated thanks to CFD.

The calculated Z_{th} has been benchmarked with the experimental one, as shown in Fig. 10. Furthermore, it has been simulated the thermal impedance during a realistic "in-line" thermal impedance test in which it is not feasible to reproduce the direct cooling to not block the production flow. Comparing FEA curves with and without direct cooling, cooling affects Z_{th} after 0.15 s.
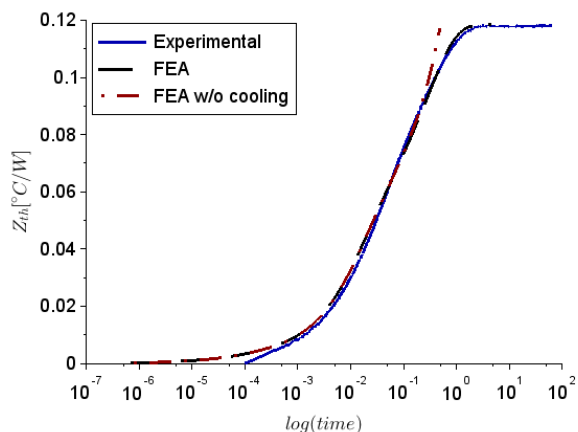
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FIGURE 10. Experimental and FEA calculated thermal impedance with direct cooling. FEA calculated thermal impedance in *testing condition*, without direct cooling, has also been reported.
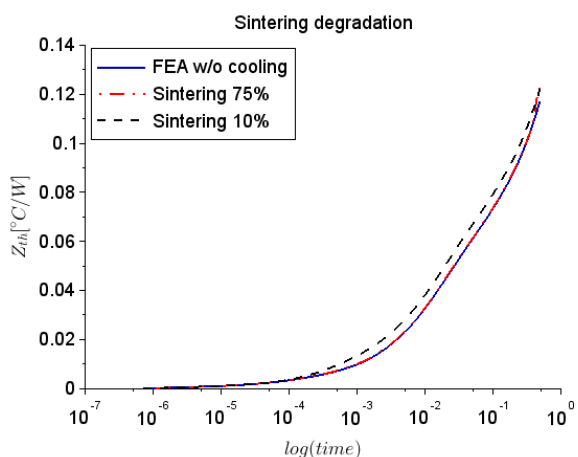

FIGURE 11. Simulated effect of sintering degradation on thermal behavior.
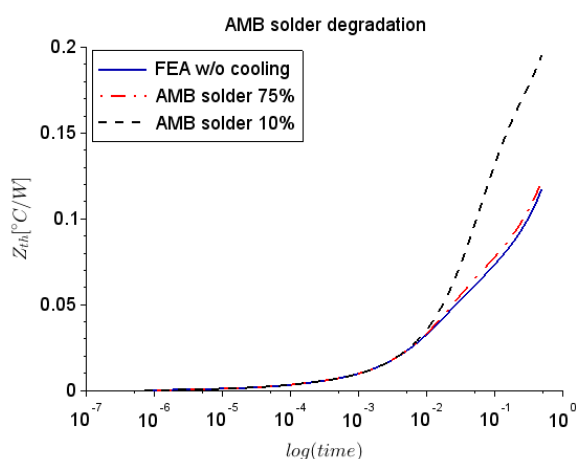

FIGURE 12. Simulated effect of AMB solder degradation on thermal behavior.

Once FEA had calculated the thermal impedance in testing condition (without cooling) considering nominal material properties, several analysis have been carried out virtually "damaging" some components, such as Ag sintering or AMB

solder attach layers. The damage has simulated multiplying the thermal conductivity and thermal capacitance by two given factors lesser than 1 (0.75 and 0.1). The time in which degraded material affects Z_{th} could be found by curves benchmarking. These analysis have been performed, as depicted in Fig. 11 and 12, respectively for Ag sintering and AMB solder layer. It has been observed AMB solder degradation affects, according to absolute Z_{th} value, the thermal impedance more than Ag sintering. Looking to the time value at which curves begin to diverge, it is possible to established when analyzed layers start to influence the temperature measurement. It has been found a time value of 5×10^{-4} s for Ag sintering and 0.05 s for AMB solder degradation.

VI. CONCLUSION

In the presented methodology it has been studied the temperature behavior of a SiC MOSFET based power module with several parallel devices for each switch. As proven by the dedicated IR camera measurements, the "classic" TSEP method, applying sufficient negative voltage during sensing phase, has provided an accurate temperature estimation with error smaller than 1 °C. According to this, TSEP method based on body diode voltage drop can be used to check goodness of power module assembly process by verifying its thermal impedance curve in accordance with some literature results previously discussed. In addition, it represents a reliable parameter to monitor the module thermal degradation during durability endurance tests, e.g. power cycling. The thermal unbalancing is moderate during the on-state condition. This is due to R_{DSon} increase versus temperature that reduces the current flow across the hottest dies, limiting the thermal imbalance among dies with different R_{DSon} characteristic. An equivalent theoretical RC network has been calculated to easily reproduce the module thermal behavior. A predictive calculation has been achieved by using finite element method assisted by computational fluid dynamics to model the thermal exchange between module and coolant fluid. Finally, the transient behavior has been numerically characterized, finding out at which time heat flow reaches silver sintering and AMB solder layers. This investigation helps to set in-line temperature measurement during assembly flow aimed to check the thermal goodness of the power modules at the end of manufacturing process and to have an electrical parameter to monitor the thermal degradation during reliability validation tests.

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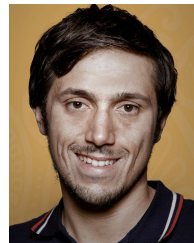
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