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Design of Compact Planar Lowpass Filters by Using Fragment-Type Structure With Multi-Bit Scheme

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ABSTRACT A novel design method for compact planar lowpass filter (LPF) with prominent roll-off rate and wide stopband suppression is proposed by using fragment-type structures (FTS) with multi-bit scheme. The proposed multi-bit FTS design has the potential to achieve higher LPF performance at higher optimization efficiency, without any prerequisite knowledge about the pivotal LPF structures needed in conventional LPF designs. The definition of multi-bit FTS and the implementation of LPF design with multi-bit FTS scheme are presented in detail. Compared to the LPF design with 1-bit FTS, the 2-bit FTS design may use smaller decision space, take fewer iterations in multi-objective optimization searching, and yet achieve sharper roll-off rate, higher stopband suppression and a wider stopband. For demonstration, planar LPFs on PCB using the 1-bit FTS and 2-bit FTS are designed and tested. The 2-bit FTS design yields a sharp roll-off rate of 123.3 dB/GHz, a relative stopband bandwidth of 165% referred to stopband suppression of 20 dB, and a high figure-of-merit of 21060. Effects of the geometry parameters of the 2-bit elements are further discussed to give some guide rule on using the 2-bit FTS design.

INDEX TERMS Fragment-type structure (FTS), lowpass filter (LPF), roll-off, wide stopband, multi-bit.

I. INTRODUCTION

Microwave lowpass filters (LPFs) play an important role in modern wireless systems because it may suppress harmonics and inter-modulation signals. Typical LPF frequency responses considered in the design include the return loss (RL) and insertion loss (IL) in the pass band, the 3-dB cutoff frequency (f_c), the roll-off rate (ξ), the relative stopband bandwidth (RSB), and the suppression factor (SF). Traditional LPFs implemented with high-low impedance resonators or open stubs may provide Butterworth and Chebyshev characteristics [1], usually with gradual cutoff frequency response and narrow stopband. Different design techniques have been developed to achieve better LPF performance such as large suppression in wide stopband and sharp roll-off in cutoff frequency response, with a LPF size compact as possible.

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Planar filters designed on PCB utilize planar resonators as the basic components to make up the filter response. Among various resonator configurations, stepped impedance hairpin resonator is the most typical one. In [2], a compact LPF based on step impedance hairpin resonator is first proposed, which has a narrow stopband bandwidth. To acquire a wide stopband, multiple cascaded stepped-impedance hairpin resonators are used in [3] and [4], stepped impedance hairpin units with one embedded in the other are considered in [5], and tap-connected stepped-impedance hairpin units with interdigital structure are suggested in [6] and [7]. The improved designs using hairpin resonators do have broadened the stopband to a remarkable extent, which give a highest RSB of 1.529 in [5] and highest roll-off rate ξ of 79.5 in [7].

To yield an ultra-wide stopband, LPF designs take the advantages of transformed open-circuited stubs, which include stepped impedance resonator (SIR) [8], [9] deformed open stubs [10], [11], [12] and combination of various types of resonators [13]. A hexangular unit SIR [8] and T-shaped

SIR [9] are proposed to extend the RSB reaching a maximum of 1.61 in [8]. Circular-shaped patches and multiple open stubs are adopted in [11] to achieve a sharp skirt characteristic and higher RSB of 1.65 further. In [12], a multi-stub LPF composed of open-circuited stubs improves the performance in both the transition and stopband regions. The designs with transformed open-circuited stubs yield a highest RSB of 1.74 in [12], highest roll-off rate ξ of 217 in [11] and 289 in [13], but a large LPF size is needed.

Several other planar resonators have also been proposed in planar LPF designs. The tapper resonator cell is proposed in [14], a lattice-shaped resonator is presented in [15]. In [16], three multimode resonators are considered. The designs report highest roll-off rate ξ of 100 in [15] and a highest RSB of 1.58 in [16]. In addition, complicated structures including vias, defected ground plan, and multilayer PCB are considered in LPF design as well. In [17], a LPF offering a very high roll-off rate ξ of 440 is designed by including two circle slots etched out in the ground plane. However, the RSB is 1.56 with suppression of 15 dB. In [18], the proposed LPF includes a two-layer design with open impedance subs on the one side and defected ground structure on the other. The lumped-element structure is used in [19], [20] to design the LP-BP filters.

To achieve LPF design with a high suppression in an ultra-wide stopband, a sharp roll-off in the transition band and a compact LPF size on PCB, without any additional or auxiliary structures, is still challenging. All the published planar LPF designs on single-layer PCB depend on the find of appropriate resonators with great potential. This could be quite empirical and may be unworkable if the designer cannot find a good resonator structure. At this point, design with optimal structure searching based on fragment-type structure (FTS) modeling is of great potential, because the FTS provide sufficient flexibility and great potential to form any potential planar LPF structures.

The FTS-based modeling has been suggested in different RF/microwave antenna and device designs. The FTS-based filter was proposed in [21] with a square patch bandpass filter as a reference model, but no performance preferable or comparable to those filters designed by using canonical PCB structures was acquired. The use of FTS-based structure makes it unpractical and unnecessary to follow the traditional designs based on EM/circuit analysis such as the LC equivalent circuit or transmission line model, because the FTS-based structures have the capability of providing necessary reactance for filter design. Moreover, the effective optimization technique [22], [23] may find such FTS so that it is becoming pivotal to yield good performance. Design of high-performance planar directional coupler has been reported by using conventional FTS (i.e., the 1-bit FTS) and multi-objective optimization searching [24]. No successful FTS-based high performance LPF design is reported because there exists severe challenge.

FTS-based design scheme for planar LPF design is shown in Fig. 1 in the 1-bit scheme. First, the design space on PCB is gridded into small cells (viz. the FTS elements), then the cells are encoded with either "0" or "1" (viz., the 1-bit or traditional FTS definition) to form a design matrix for multi-objective optimization. By metalizing all the cells represented by element "1" in the design matrix will define a FTS-based PCB structure. For desired LPF characteristics, the multi-objective optimization gives the optimized design matrix, which thus yields the optimal structure for FTS-based LPF.

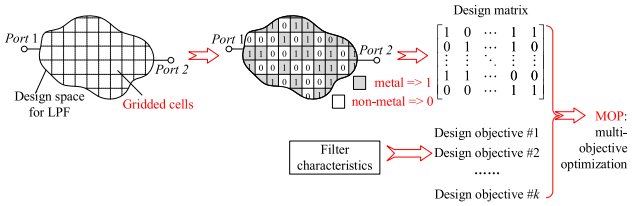

FIGURE 1. FTS-based planar LPF design in 1-bit scheme.

The challenge issue in the 1-bit FTS-based design is how to treat the fine structure searching without degrading the efficiency of optimization. Fine structures are necessary if certain LPF performance (such as the high roll-off rate) is to be challenged. With the 1-bit FTS description, the FTS cells should be small enough for including fine structures in the filter on PCB. Unfortunately, using smaller cell size means more cells in the design area on PCB, which yields large design matrix (viz., large decision space) and thus heavy optimization burden. In addition, the EM simulation for performance evaluation of a distributed FTS structure using smaller cells over the entire design area, not just in the parts necessary, will no doubt take more computation time. Therefore, novel and efficient FTS description scheme is essential.

An efficient FTS description scheme may include new elements with certain fine structures, such as narrow slit and thin line, as shown in Fig. 2. In addition to the traditional element "1" of fully metalized cell and "0" of the empty (air) cell, two more FTS elements, viz., an element with an etched narrow slit and an element with a thin metal line, may be added. By applying these elements for FTS description, thin lines or narrow slits may be included in some local area without using smaller cell size.

In this paper, we proposed a new FTS description scheme, viz., the multi-bit scheme, to replace the traditional 1-bit FTS scheme. The diversity of multi-bit FTS elements not only contains fine structures such as narrow slit and line for high performance design, but may also reduce the overall computation time for simulation design. Therefore, the design using the multi-bit scheme will be more efficient and may yield excellent planar filter performance in a smaller size.

This paper is organized as follows. Section II proposes the multi-bit FTS scheme for microwave planar PCB device design. In Section III, the multi-objective optimization scheme for multi-bit FTS is introduced, and demonstrated

by designing planar LPFs of ultra-wide stopband and sharp roll-off with FTS in 1-bit and 2-bit FTS scheme, respectively. In Section IV, a LPF design challenging high performance by using fine 2-bit FTS cells is reported. In Section V, the effects of fine geometry on the 2-bit FTS cells are illustrated by designing different 2-bit LPFs. Section VI concludes this paper.

II. MULTI-BIT DESCRIPTION SCHEME FOR FTS

To implement FTS-based design for high-performance circuits such as microwave filters, it is required to include FTS elements that provide the capability of constructing geometry with subtle structures. Although the traditional 1-bit FTS description [24] will provide this ability by using FTS cells being small enough, the very large decision space due to very small cell size will lead to extremely heavy burden for optimal structure searching and performance evaluation in the multi-objective optimization. An efficient FTS description scheme may include new elements with certain fine structures.

It is well-known that for a planar filter on PCB, transmission line with high characteristic impedance can be equivalent to an inductance. The thinner the line, the larger the impedance, and the stronger the inductiveness. In addition, narrow slit between two structures tends to yield strong electromagnetic coupling. Fine tuning of the inductance and electromagnetic coupling are necessary for high-performance planar filter design.

Therefore, the FTS description for planar filters can be improved by adding FTS elements with subtle structures such as narrow slit and thin metal line included. Figure 2 shows several FTS element structures under our consideration, where the gray parts will be metalized. In addition to the traditional 1-bit FTS elements shown in Fig. 2(a) and 2(b), partially metalized elements with narrow lines, slits, and crossed coupling lines and gaps are considered in Fig. 2(c)-2(h), which may provide transmission or coupling in the horizontal or vertical direction in the formed FTS planar circuits.

A. SELECTION OF THE FTS ELEMENT

A multi-bit FTS description scheme with the elements shown in Fig. 2 can be formed by following different guide rules. We list some as follows:

1) Elements (a) and (b), the two traditional 1-bit FTS elements, must be included to form the infrastructure.

2) Other FTS elements may be constructed or selected by considering the direction of current inducing in the design space, which is usually related to the port arrangement. The cells (c) and (d), (e) and (f) may provide different current inducing.

3) The elements may be constructed or selected by considering the direction of EM coupling in the design space, which is usually related to the function of the structure. The cells (c) and (d), (e) and (f), (g) and (h) may provide different EM coupling in the horizontal, vertical, and cross directions, respectively.

4) The equivalent circuit or principle of the designed structure may be used as an important reference for selection. For design of FTS directional coupler, the elements with gap will benefit, which is conducive to the fine control of coupling. For the planar LPFs, the FTS elements should ensure complementary capacitive and inductive elements so that different capacitors and inductors can be presented by combining different FTS elements, which will benefit the optimization searching of possible FTS to challenge the LPF performance.

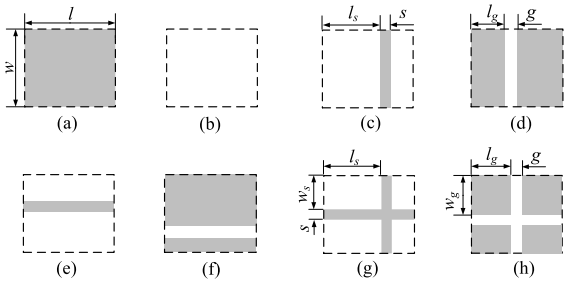

FIGURE 2. Alternative FTS elements for the multi-bit FTS scheme.

For the FTS elements shown in Fig. 2, Fig. 2(a) and Fig. 2(b) define the traditional 1-bit FTS cells. Fig. 2(c) and Fig. 2(d) are complementary with each other, so that elements in Fig. 2(a), (b), (c), and (d) may form a 2-bit FTS description scheme, where "11" = cell (a), "00" = cell (b), "10" = cell (c), and "01" = cell (d). With the narrow gap in Fig. 2(d), the FTS may include the capacitive effect through the gap.

The 2-bit FTS scheme may take other combinations among the cells in Fig. 2. We note that Fig. 2(e) and Fig. 2(f) complement each other, so that cells in Fig. 2(a), (b), (e), and (f) may form another 2-bit FTS description scheme. Since Fig. 2(g) and Fig. 2(h) are also complementary with each other, elements in Fig. 2(a), (b), (g), and (h) may form a different 2-bit scheme. Different 2-bit schemes may have different emphases in constructing FTS for different characteristics. In the above-defined 2-bit FTS scheme, the cells (c)-(f) have different emphasis on transmission or coupling in vertical or horizontal direction.

To define a more comprehensive FTS description, we may consider 3-bit scheme by including all the elements in Fig. 2. For the 3-bit encoding, we may assign "111" = cell (a), "000" = cell (b), "110" = cell (c), "101" = cell (d), "100" = cell (e), "011" = cell (f), "010" = cell (g), "001" = cell (h). Due to the complementarity among the cells, the balance of capacitance and inductance between each two cells is maintained. In the 3-bit scheme, the cells (c)-(h) have emphasis on transmission or coupling in both the vertical and horizontal directions. In addition, the cells (c)-(f) can be viewed as special cases of (g) and (h), where the position and width of the metal line or slot in the elements can be adjusted as needed by adjusting the w_s, l_s, and s or w_g, l_g and g.

B. ADVANTAGES

The advantage of multi-bit FTS description scheme shows in the very limited cost in searching time for the high-performance circuit geometry with subtle structures. Since multi-objective optimization searching in larger decision space requires much more time, the multi-bit FTS scheme saves time in a remarkable way. Suppose the designed FTS circuits should include subtle gap of width $g = 1/n$ or subtle line of width $s = w/k$, the traditional 1 -bit FTS scheme should take s as the cell width or g as the cell length to treat such subtle structure, so that the decision space will be enlarged by n or k times. If the circuits should include both the subtle gap of width $g = l/n$ and subtle line of width $s = w/k$, the traditional 1-bit FTS scheme should take s as the cell width and g as the cell length to treat such subtle structure, so that the decision space will be enlarged $n \times k$ times. While the decision space for the m-bit FTS scheme is enlarged m times, no matter what g and s are. Note that m is much smaller than n or k, thus the m-bit FTS scheme uses a much smaller decision space than that used by the 1-bit FTS scheme for subtle structures. Therefore, the multi-bit FTS scheme may benefit in both the performance and searching time.

Although the multi-bit FTS elements may take different shapes and include different subtle structures, it should be noted that the shape and position of subtle line and gap will affect the optimization process and EM simulation time. In the design of planar LPF, the subtle gap is set at the edge of the element cell, and capacitive coupling is mainly provoked between element cells, which will not only avoid too many isolated gaps but also save EM simulation time. In general, the FTS element structure should not be too complex, otherwise it will greatly increase the circuit complexity and simulation time.

For a planar FTS circuit design, it is not necessary to use excessively multiple bits in the FTS scheme. Otherwise there will be too much redundancy in modeling and unnecessary searching in decision space. For the above 3-bit FTS scheme, there are eight different cell shapes emphasizing different performance objectives. In the design of LPF in this paper, it is expected that the m-bit FTS may make up the difficulty in forming required capacitance and inductance by the traditional 1-bit scheme. Considering the time cost and number of objective in combination, the 2-bit FTS scheme is a good choice.

III. LPF DESIGN WITH 1-BIT AND 2-BIT FTS DESCRIPTION

To demonstrate the effectiveness of the proposed multi-bit FTS design scheme, we will design two planar LPFs with 1-bit and 2-bit scheme, respectively, by implementing the multi-objective optimization with MOEA/D-GO combining the HFSS [23]. The LPF designs may challenge high performance LPF by laying stress on the return loss, insertion loss, roll-off rate, ultra-wide relative stopband width, high suppression in the stopband, and even the figure of merit (FOM) [11], which can be guaranteed by properly defining the multiple optimization objectives. However, the multi-objective optimization searching for the best FTS will suffer from too heavy burden if we define too many objectives.

A. OBJECTIVE FUNCTIONS FOR LPFS

For a high-performance LPF, return loss (RL) in the pass band $[0, \omega_1]$, roll-off rate in the transition band $[\omega_2, \omega_3]$, and suppression in the stopband $[\omega_3, \omega_n]$ are the key performance indicators under our consideration. The multi-objective optimization problem can be expressed as:

$$\begin{aligned} &\text{minimize } F(x) = \left(\overline{f_1(x)}, \overline{f_2(x)}, \cdots, \overline{f_{\mathrm{m}}(x)}\right) \\ &\text{subject to } x \in \Omega \end{aligned} \tag{1}$$

$$\overline{f_1(x)} = \frac{\max\left(\alpha - \min\limits_{\omega\in[0,\omega_1]} \left|(S_{11})_{dB}\right|, 0\right)}{\alpha}, \tag{2}$$

$$\overline{f_2(x)} = \frac{\max\left(\xi_0 - \min\limits_{\omega\in[\omega_2,\omega_3]} \xi, 0\right)}{\xi_0}, \tag{3}$$

$$\overline{f_3(x)} = \frac{\sum\limits_{i=3}^{n-1} \max\left(\beta - \min\limits_{\omega\in[\omega_i,\omega_{i+1}]} \left|(S_{21})_{dB}\right|, 0\right)}{(n-3)\beta}, \tag{4}$$

where x is the design variable that defines the LPF, Ω is a decision space defined by the m -bit FTS scheme, $|S_{11}|$ (in dB) indicates the RL, α is the desired minimum RL in dB, $|S_{21}|$ (in dB) indicates the suppression in stopband, β is the desired minimum suppression in dB, and ξ_0 is the desired minimum roll-off rate.

The objective function $\overline{f_2(x)}$ is defined to guarantee a high RL in the passband if α is set large enough (e.g., $\alpha = 20$ dB). Because the filter can be taken as a lossless network, the small insertion loss (IL) can be guaranteed. The objective function $\overline{f_2(x)}$ ensures a sharp cutoff frequency response in the transition band if ξ_0 is set large enough (e.g., $\xi_0 = 200$). The objective function $\overline{f_3(x)}$ guarantees a wide stopband with large suppression if β is set large enough (e.g., $\beta = 20$ dB). Since the design will challenge a super wide stopband, we segment the stopband into $(n-3)$ sub-bands, as indicated in (4).

It should be remarked that some designers think another objective function for insertion loss (IL) should be defined in addition to the above three objective functions. In fact, IL objective may not be necessary owing to the low loss of PCB. Since there is a underlying relationship between $|S_{11}|$ and $|S_{21}|$ of LPF as

$$|S_{11}|^2 + |S_{21}|^2 = 1 - \delta\,, \tag{5}$$

where δ is a factor representing all the possible loss from the PCB and the LPF structures in the design space, the IL in LPF operation band, in terms of $|S_{21}|$, can be guaranteed by pursuing small $|S_{11}|$ or high RL in (2). As will be shown in Table 1 and 2, for RL no less than 20dB (by setting $\alpha = 20$ dB in (2)), the IL less than 0.3dB can be achieved without defining a specific objective function for the IL.

We also have two other remarks on the objective functions (2)-(4). First, all the objective functions are defined in normalization form because the roll-off rate can be quite larger than the RL and suppression if we challenge a very sharp cutoff in the LPF design. The normalization may seek the balance among the three objective functions [23]. Otherwise, the evolutionary algorithm will overwork on the roll-off rate and ignore the RL and suppression, which may degrade the searching efficiency by decelerating the convergence.

Second, the objective function (4) for suppression is defined in several sub-bands. In (4), the stopband is divided into m ($m = n - 3$) sub-bands. In a sub-band, the algorithm compares the minimum IL at each sampling frequency with β. For those IL $> \beta$ the objective (4) records 0 for the summation, otherwise records (β-IL) for further evolution searching. By doing so, it is ensured that the harmonic, if there is one in the sub-band, can be suppressed in an effective way. If there is only one large stopband set in (4), all harmonics in the stopband will be treated in a compound manner so that merely the structure with the highest minimum suppression level is considered as evolved object.

B. DESCRIPTION OF THE LPFS

For demonstration, we may suppose that the LPF structure have both lateral and vertical symmetry, so that the design area for FTS optimization searching is reduced to approximately quarter of the original design space. In addition, we suppose the LPF to be designed has a passband [0, ω_1] = [0, 1.5GHz], cut-off frequency f_c = 2.0 GHz, transition band [ω_2, ω_3]= [2.0GHz, 2.5GHz], and stopband [ω_3, ω_6] = [2.5 GHz, 15.0GHz]. We set $n = 6$ to divide the stopband into 3 sub-bands, viz., [2.5GHz, 5.0GHz], [5.0GHz, 10.0GHz] and [10.0 GHz, 15.0 GHz]. We set α = 20 in (2) to purse the RL greater than 20 dB in the passband, ξ_0 = 70 in (3) to guarantee a minimum roll-off rate of 70, and β = 20 in (4) to ensure the suppression in the entire stopband will reach 20 dB.

The design space for LPFs is restricted to a very small dimensions of 15.4mm × 15.2mm on Rogers 5880 PCB (with relative permittivity $\varepsilon_r = 2.2$, thickness of 0.787mm, and loss tan$\delta = 0.0009$). The lateral and vertical symmetry will reduce the design space to 7.7 mm × 7.6 mm, viz., a quarter of the total design space as shown in Fig. 3(a).

For the LPF, we have two other prime considerations. First, to ensure DC transmission between the two ports, a meander through line with a fixed width will be preset, as shown in Fig. 3(a). The width can be as thin as 0.1mm without introducing notable insertion loss, as will be shown in Table 1 and II. Second, the suppression in stopband and sharp roll-off rate can be achieved by loading the preset DC line with an optimized FTS. The preset DC line may be optimized in a specifically assigned subspace in the design matrix, not the entire design space, so that the optimization searching time can be reduced. Moreover, optimal DC line can be acquired by searching for the appropriate position and length of the DC line segments on the FTS, in a specified DC line subspace other than the space for FTS.

With the preset DC line, the FTS description of the LPF is shown in Fig. 3. For the FTS structure design, the quarter space of the LPF design area can be discretized into gridded cells as shown in Fig. 3(b), which are to be encoded with either "1" or "0" for the 1-bit scheme, or encoded as any one of the four states of "00", "01", "10" and "11" for the 2-bit scheme. All the 0/1 assigned to the cells may define a design matrix for the FTS structure, as shown in matrix I in Fig. 3(c). After metalizing the gray parts in the FTS elements, the binary matrix I will yield a planar circuit distribution.

For the DC line design, the meander line if Fig. 3(a) can be discretized into segments of the same length in direction parallel to the horizontal reference line (usually offsetting the horizontal symmetry axis). The DC line can thus be defined by the offset distance r_k of each segment of meander line, as shown in Fig. 3(b). Since the offset distance value can be expressed in binary, such as the binary for r_n = 8.6mm and r_m = 4.8mm illustrated in Fig. 3(c), a binary design matrix can thus be coded for the DC meander line, as shown by the matrix II in Fig. 3(c).

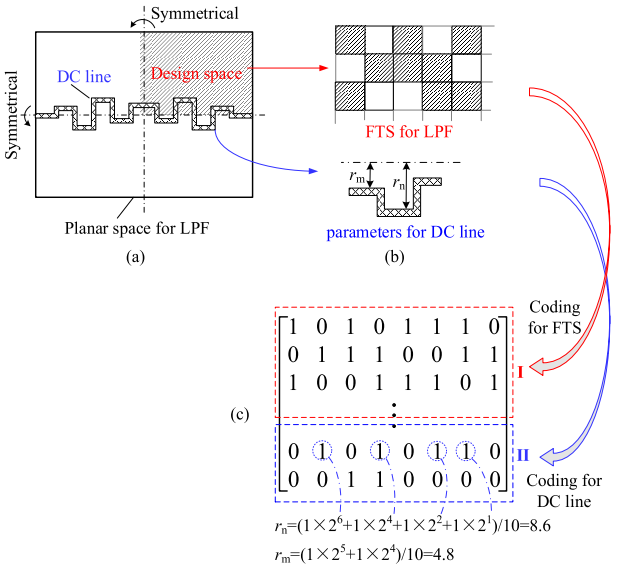

FIGURE 3. FTS description of LPF with preset DC line: (a) design space and DC line, (b) FTS for LPF and DC line, (c) design matrix for LPF optimization searching.

The combination of matrix I and matrix II makes up the decision matrix for the planar LPF, as shown in Fig. 3(c). By implementing the MOEA/D-GO optimization with the multi-objective functions defined for the LPF, the best FTS structure and the DC meander line can be obtained to give the LPF by metalizing the meander line and the gray parts in FTS elements.

It should be noted that the lower and upper bounds of the segment offset distance should be restricted so that the bit number of the binary coding is confined, which ensure a

moderate size of the matrix II. In this design, the bounds are set from –3 mm to 3 mm. We can use 6-bit binary encoding to cover 60 to ensure the accuracy of optimization of 0.1mm. As a result, a design matrix II with the size of 2×24 can meet the demand of optimization of a six-segment DC line.

C. 1-BIT CELL LPF

For the 1-bit FTS design, the size of the design space in Fig. 3(a) is set to be 7.7 mm $\times$ 7.78mm, which is a bit wider than the quarter of total design space. The reason is that we must set a row of element cells on the vertical symmetry axis to avoid the "double width effects" along the vertical symmetry axis due to the horizontal symmetry. This is not required along the horizontal symmetry axis because the meander line directly breaks overall vertical symmetry.

To construct a FTS matrix of size, say 7×24, the 1-bit FTS scheme may be set up with element cell "1" of dimensions of 1.1 mm $\times$ 0.34 mm (i.e., $w = 1.1$ mm and $l = 0.34$mm, except for the edge-row cells) and 0.01mm overlapping in horizontal direction between two adjacent cells, viz., $\Delta l = 0.01$mm in the zoomed area in Fig. 3(a). There is no overlap in the vertical direction, so that the diagonal connection between two adjacent metal cells can be avoided.

It should be remarked that, without loss of generality, adjacent to each port of the LPF, a column of small cells of dimensions must be added. The reason is that the assigned design space may not be exactly divided equally under the machining accuracy restriction, and the cells adjacent to the two ports could be quite sensitive to the current. Therefore, adopting edge row with smaller cells to compensate the space discretization is quite reasonable in all the FTS-based designs.

For the quarter design space, the edge-row cells have dimensions of 1.1mm $\times$ 0.18mm, so that in the horizontal direction the total width covered with the FTS cells is (0.34mm-0.01mm) $\times$ 23 +0.01mm +0.18mm = 7.78mm. In the vertical direction the height covered by the FTS cells is 1.1mm $\times$ 7 =7.7mm.

Following the procedure in LPF description in subsection B, the preset DC line and the FTS design space can be coded to generate the design matrix.

For the objective functions defined in (1)-(4) with the LPF characteristics in subsection B, optimization searching for the design matrix with MOEA/D-GO are run on a computer with Intel Core I5-4670@3.4GHz. The optimization searching was terminated after 40 iterations (about four days) because the evolution of the 1-bit FTS design shows that the objective function (4) related to the stopband level $\beta = 20$ cannot be met, instead it gives approximate 10 dB depression. Therefore, the 1-bit FTS design has no ability to achieve the suppression of 20 dB in the stopband for the LPF.

The MOEA/D-GO optimization gives three layouts of LPF, among which one is shown in Fig. 4(a). The optimized distances of the DC meander line from centerline are $r_1 = 1.2$mm, $r_2 = 0.7$mm, $r_3 = 0.1$mm, $r_4 = 1.6$mm, $r_5 = 0.3$mm, and $r_6 = 0.5$mm, respectively, and the length of each section

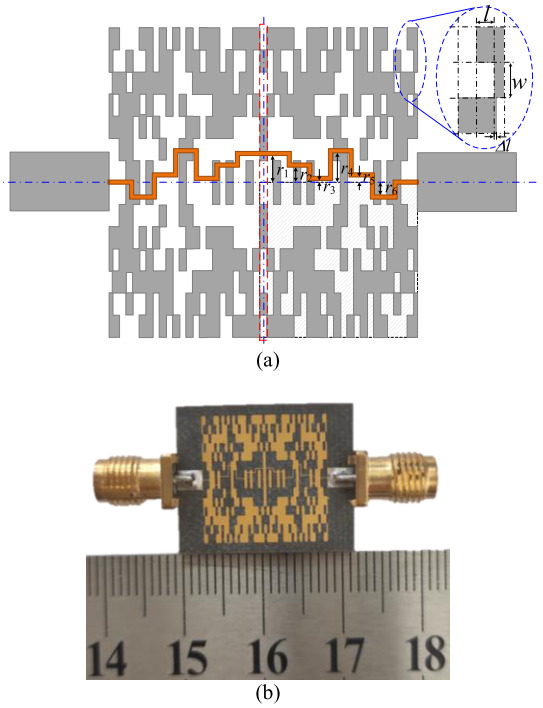

FIGURE 4. The designed 1-bit FTS LPF with 7 × 24 cells. (a) Layout. (b) Fabricated prototype.

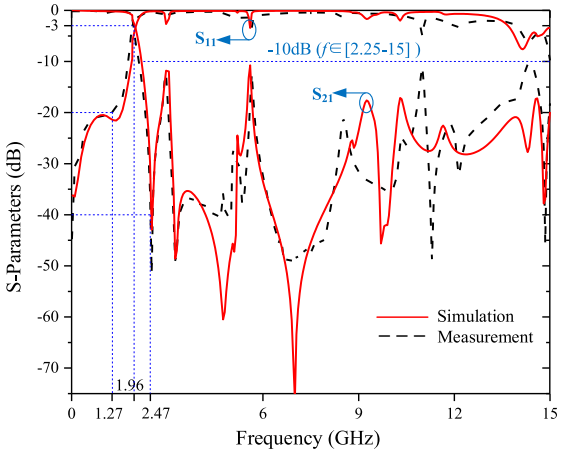

FIGURE 5. Simulated and measured results of the designed 1-bit LPF.

is 1.1mm. A prototype of the 1-bit FTS LPF is fabricated as shown in Fig. 4(b).

Simulated and measured S-parameters of the designed fragment-type 1-bit LPF are depicted in Fig. 5. The S-parameters are measured by Keysight Technologies network analyzer N5245B. It is observed that the measured results have a good agreement with the simulated ones. According to the measurement results, the 1-bit LPF has a 3-dB cutoff frequency equal to 1.96 GHz, RL better than 20 dB from DC to 1.27 GHz, suppression better than 10 dB in stopband ranging from 2.25 GHz to 15 GHz. The transition band ranges from 1.96 GHz to 2.47 GHz, with corresponding IL from -3 dB to -40 dB, which gives $\xi = 72.5$ dB/GHz.

D. 2-BIT CELL LPF

The 2-bit FTS scheme will double the decision space of the 1-bit FTS scheme if the design space is gridded in the same manner. For fair comparison to use the decision space same as the 1-bit FTS scheme, the 2-bit FTS scheme may use large FTS cell twice the dimension of the 1-bit FTS cell. As a result, the design space of 15.4mm × 15.2mm will take 7 × 12 cells in 2-bit FTS scheme, instead of the 7 × 24 cells in the 1-bit scheme. The reduced cell number implies large FTS cell size, which has dimensions of 1.1 mm × 0.85 mm.

The quarter design area for 2-bit FTS is 7.7 mm × 8mm after we set a row of cells on the vertical symmetry axis. For the 2-bit FTS design, we consider 0.2mm overlapping in horizontal direction between two adjacent cells, viz., $\Delta l = 0.2$ mm in the zoomed area in Fig. 6(a). There is no overlap in the vertical direction, so that the diagonal connection between two diagonal adjacent metal cells can be avoided. In addition, for the LPF design area and the above cell size, there is no edge row required. As a result, the total width in the horizontal direction covered with the FTS cells is (0.85mm-0.2mm) × 12 +0.2mm = 8.0mm. In the vertical direction the height covered by the FTS cells is 1.1mm × 7 = 7.7mm.

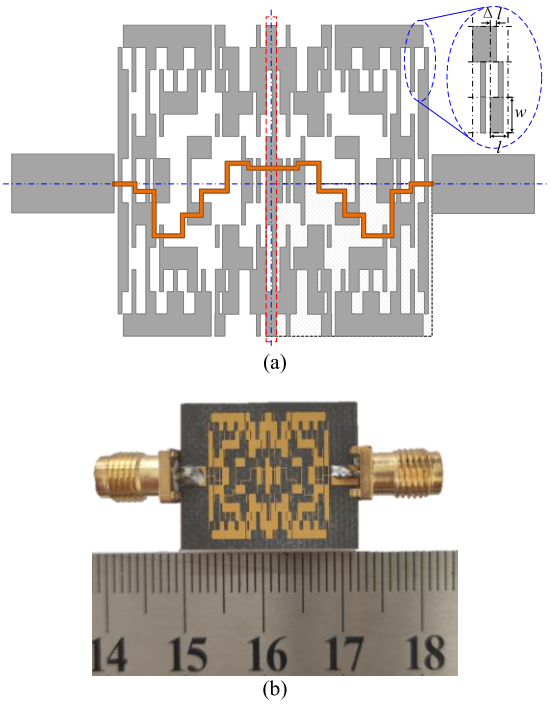

FIGURE 6. The designed 2-bit FTS LPF with 7 × 12 cells. (a) Layout. (b) Fabricated prototype.

To give the 2-bit FTS description scheme, we select (a), (b), (c), and (d) in Fig. 2 as the four FTS elements. The parameters defining the 2-bit cells are $l = 0.65$ mm, $w = 1.1$ mm, $g = 0.1$ mm, $s = 0.1$ mm, $l_g = 0.55$ mm, and $l_s = 0.45$ mm in the cells (c) and (d). With these parameters, we do not directly generate the fine coupling inside the cell, but form the coupling through the gap between two neighboring cells. Such technique may reduce the calculation time of the simulation software.

Following the procedure in LPF description in subsection B, the preset DC line and the FTS design space can be coded to generate the design matrix.

For the objective functions defined in (1)-(4) with the previous LPF characteristics, optimization searching for the candidate design matrix with MOEA/D-GO is run on the same computer with Intel Core I5-4670@3.4GHz. It takes 14 iterations (about 2.5 days) to achieve all the design objectives, and gives two layouts of LPF.

Fig. 6(a) shows one of the layouts. The optimized distance from the offset centerline of the meander line are 0.6 mm, 0.90 mm, 0.5 mm, 1.6 mm, 2.3 mm, 0.4 mm, respectively, and the length of each section is 1.1mm. A prototype of the 2-bit cell LPF is fabricated as shown in Fig. 6(b).

Figure 7 shows the simulated and measured S-parameters of the designed 2-bit cell LPF. It is observed that the measured results have a good agreement with the simulated ones.

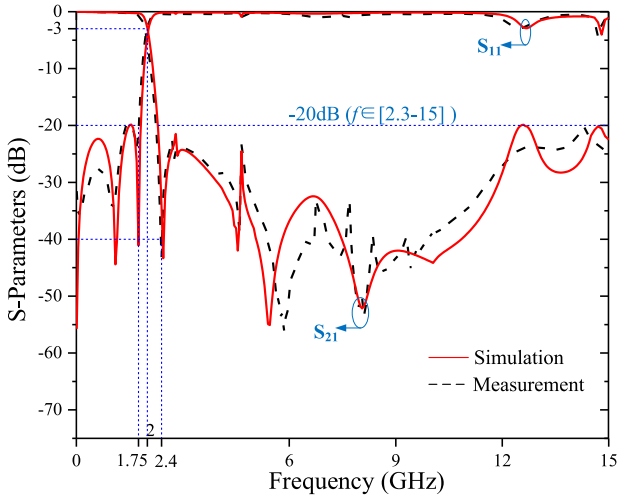

FIGURE 7. Simulated and measured S-parameters of the designed 2-bit LPF.

It can be seen from the Fig. 7 that the prototype LPF has a 3-dB cutoff frequency equal to 2.0 GHz, IL less than 0.2 dB and RL better than 20 dB in the passband from dc to 1.75 GHz. The suppression level is higher than 20 dB from 2.3 GHz to 15 GHz. The transition band ranges from 2.0 GHz to 2.4 GHz, with corresponding IL from −3 dB to −40 dB, which gives $\xi = 92.5$ dB/GHz.

E. PERFORMANCE AND EFFICIENCY COMPARISON

Table 1 compares the key characteristics of the two LPFs designed with the 1-bit FTS and 2-bit FTS scheme. It is easy to conclude that the 2-bit FTS scheme achieves superior performance with sharp roll-off and higher harmonic rejection. In the stopband, the harmonic suppression of the 2-bit FTS scheme is twice that of the 1-bit FTS scheme.

For the efficiency comparison, Figure 8 shows the iterative process of two key objectives, i.e., roll-off rate and stopband

suppression, in the optimization when the RL $\geq$ 20dB. Figure 8(a) depicts the evolution of the LPF design with 1-bit FTS scheme, where shows that the expectations of two goals cannot be achieved simultaneously in 40 iterations (about four days searching). The searching yields several results on the front line of optimization, such as (0, 0.39), (0.57, 0.16), (0.68, 0.1), and (0.73, 0.07). Among them (0, 0.39) gives the best comprehensive LPF performance, which we have used in Table one for performance comparison.

TABLE 1. Optimization results of proposed LPFs with different cells.

Scheme	f_c (GHz)	ξ	RSB	SF	IL	RL
1-bit	2.0	72.5	1.48	1	0.2	20
2-bit	2.0	92.5	1.47	2	0.2	20

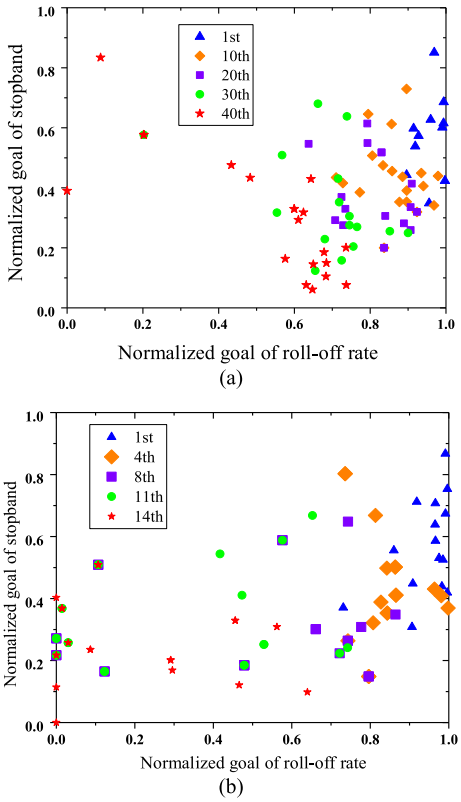

FIGURE 8. Iterations of the two designs. (a) 1-bit FTS scheme and (b) 2-bit FTS scheme.

Figure 8(b) shows the evolution of the LPF design with 2-bit FTS scheme. We find that the desired values (0, 0) of two objectives are achieved simultaneously after only 14 iterations (about 2.5 days searching), which is about half of the time with 1-bit FTS scheme.

In general, 2-bit FTS scheme design improves not only the performance of LPF but also the optimization efficiency.

IV. CHALLENGING HIGH PERFORMANCE LPF WITH 2-BIT FTS

The above planar LPF design using 2-bit FTS scheme is implemented on a decision space same as that for 1-bit FTS.

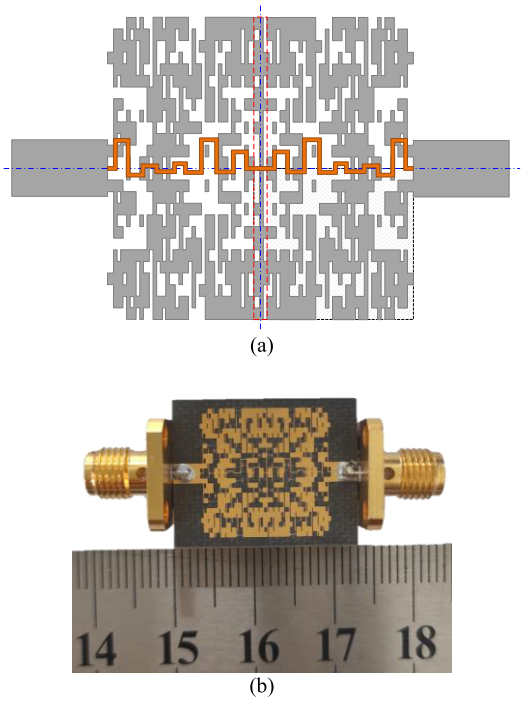

FIGURE 9. The designed 2-bit FTS LPF with smaller 2-bit cells. (a) Layout, (b) Fabricated prototype.

It is interesting to use the small 2-bit cells to challenge the high performance LPF design. For demonstration, we may consider FTS cells with compressed height and width.

In this challenge design, we select the same element cells (a), (b), (c), and (d) in Fig. 2 for 2-bit FTS scheme. The parameters defining these FTS cells are $l = 0.65$ mm, $w = 0.59$ mm, $g = 0.1$ mm, $s = 0.1$ mm, $l_g = 0.55$ mm, and $l_s = 0.45$ mm, which indicate cells compressed in height. The width Δl of overlapping in horizontal direction between two adjacent cells is still 0.2mm. As a result, the quarter design space of 7.7mm $\times$ 8mm will require matrix I of size 13 $\times$ 24. For the DC meander line, design matrix II with size of 3 $\times$ 24 is required for optimizing the eleven segments. Following the procedure in LPF description in subsection B, the preset DC line and the FTS design space can be coded to generate the design matrix.

This 2-bit cell LPF challenges a large roll-off rate by setting $\xi_0 = 120$ and an ultra-wide stopband ranging from 2.5 GHz to 20 GHz. We set n = 7 and divide the stopband into 4 sub-bands, which in GHz are [2.5, 5], [5, 10], [10, 15], and [15, 20], respectively.

For objective functions in (1)-(4) with the above challenging performance, we run the optimization searching for the design matrix with MOEA/D-GO on the same computer with Intel Core I5-4670@3.4GHz.

It takes 75 iterations (about 17days) for the optimization to achieve all the design objectives, and yields three layouts of FTS-based LPF. Figure 9(a) shows the layout of one of them. The optimized DC line has parameters of 0, 0.6mm, 0.1mm, 1.5mm, 0.3mm, 0.2mm, 0.1mm, 0.1mm, 0.3mm,

1.5mm, 0mm, respectively, and the length of each section is 0.7mm. Figure 9(b) shows the prototype of the designed LPF.

Figure 10 depicts the simulated and measured results. The S-parameters and group delay are measured by using Keysight network analyzer N5245B. It is observed that the measured results have good agreement with the simulated ones. The proposed LPF exhibits a measured IL less than 0.3 dB and RL larger than 20 dB in the passband from dc to 1.75 GHz. Besides, the 3-dB cut-off frequency is 2 GHz, and the first zero point of the stopband is located at 2.31 GHz, which yields a steep transition band. The response like transmission zeros are yielded during the optimization searching because the FTS design may form specified capacitors and inductors and proper mutual couplings automatically according to the filter requirements. Transmission zeros in desired band can be introduced in FTS design by defining objective function characterizing the positions of zeros. The frequency point for IL $= -40$ dB is 2.3 GHz so that the roll-off rate can be calculated as 123.3 dB/GHz in the transition region. Furthermore, a good stopband characteristic is obtained for the IL over 20 dB in a frequency range from 2.2 GHz up to 22.6 GHz and over 15 dB covering the band from 2.15 GHz to 30 GHz.

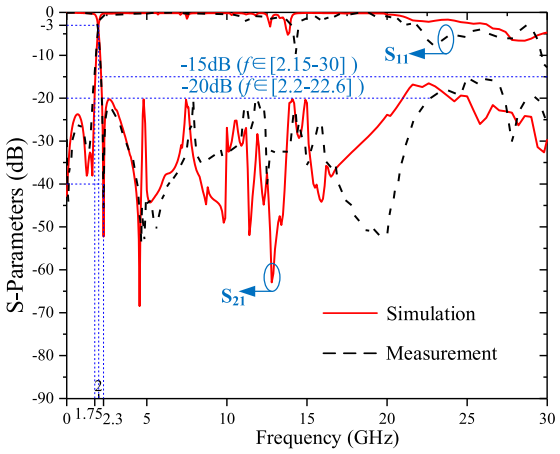

FIGURE 10. Simulated and measured S-parameters of the LPF with smaller 2-bit cells.

Figure 11 depicts the group delay of the LPF, which is less than 0.8 ns in the passband, lower than that in [12] and [17].

Figure 12 shows the surface current distribution at two frequencies, viz. at 1 GHz in the passband and 20 GHz in the stopband, when port 1 is set as the input port. As can been seen from the Fig. 12(a) that most of the energy is transmitted directly from the input port to the output port through the transmission line at 1 GHz. While at 20 GHz, most of the energy is trapped in the loaded resonator near the input port, as can be seen in Fig. 12(b). Since almost no energy is transmitted through the transmission line to the output port, the stopband of the LPF is formed.

An overall comparison of the LPFs designed with the proposed 2-bit FTS scheme with those LPFs previously

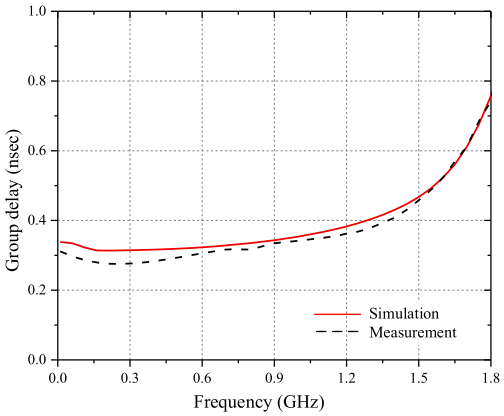

FIGURE 11. Group delay in the passband of designed LPF with small 2-bit cells for challenge.

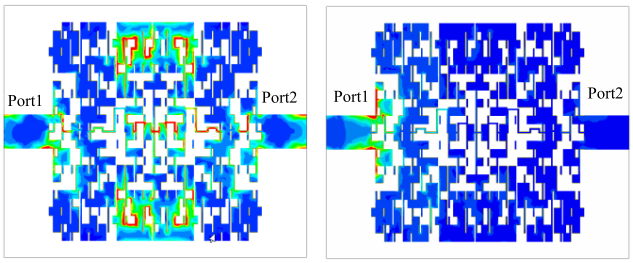

FIGURE 12. Surface current distribution (a) at 1 GHz and (b) at 20 GHz.

published as shown in Table 2. Compared with the literature in Table 2, we can see that the LPFs designed has good passband performance, with return loss higher than 20 dB and insertion loss lower than 0.2dB and 0.3dB. Secondly, compared with the designs in [3], [5], [6], [7], [8], [9], [12], [14], [16], and [18], the design LPFs have high roll-off rate and achieve steep transition characteristics. Thirdly, except for [12], 2-bit LPF in Section IV has a larger RSB than other references, and maintains a 20 dB stopband suppression. Therefore, good stopband characteristics are achieved. In addition, except for [12], the FOM of 2-bit LPF in Section IV is superior to other references, and the roll-off rate of 2-bit LPF in Section IV in this paper is significantly higher than that in [12]. Finally, we use a compact design area to achieve higher performance. Compared with [3], [7], [8], [9], [14], and [15], we achieve better performance of passband, transition band and stopband with a smaller design size. Compare with [10], [11], [13] and [17], 2-bit LPF in IV has higher RSB and higher RL in passband with a smaller design area. Compared with the remaining references [5], [6], [12], [16] and [18], we use the similar or slightly larger size to greatly improve the performance of the transition band.

V. DISCUSSION

In the geometry of the 2-bit cells (c) and (d) in Fig. 2, several geometry parameters may affect the design performance of

TABLE 2. Comparison of the proposed LPF with reported LPFs.

Ref.	f_c (GHz)	ξ (dB/GHz)	RSB	SF	RL (dB)	IL (dB)	AF	NCS (λ_g^2)	FOM
[3]	2.02	56.9	1.213	3.3	13.6	1	1	0.187	1216
[5]	1.6	52.8	1.529	2.0	20	0.3	1	0.00915	17640
[6]	1	74.0	1.197	2.0	20	0.4	1	0.012	14800
[7]	3.9	79.5	1.246	2.0	13	0.5	1	0.072	2752
[8]	2.8	48.5	1.61	2.0	16.5	0.1	1	0.021	7335
[9]	2.68	60	1.509	2.0	18.5	0.12	1	0.022	8051.2
[10]	2.24	308.3	1.54	2.2	18	0.3	1	0.058	18134
[11]	1.26	217	1.65	2.0	9	0.8	1	0.036	19931
[12]	1.0	74	1.74	2.4	20	0.3	1	0.012	25274
[13]	1.98	289	1.47	2.0	5.5	/	1	0.044	19049
[14]	1.3	52.86	1.525	2.0	19.5	1	1	0.029	5536.5
[15]	4.34	100	1.58	2.0	19	0.1	1	0.080	3959.9
[16]	1.8	46.25	1.58	1.5	10	0.5	1	0.0099	8959.5
[17]	1.95	~440	1.56	1.5	12	0.4	2	0.035	14644
[18]5th	1	78	1.628	2.0	19.8	0.3	2	0.016	7936.5
[19]	0.94	~102	1.11	2.0	20	0.3	1	0.011	20585
2-bit FTS design in III-D	2.0	92.5	1.47	2.0	20	0.2	1	0.019	13391.3
2-bit FTS design in IV	2.0	123.3	1.65	2.0	20	0.3	1	0.019	21060.6

Note: AF means the architecture factor. NSC is the circuit size normalized by λ_g, and λ_g is the guide wavelength at f_c. FOM = (ξ×RSB×SF)/(NSC×AF) is the figure of merit [11].

FTS-based LPF. In Section IV, we have shown the effects of using FTS cells with height compressed from $w = 1.1$ mm in Section III to $w = 0.59$ mm in Section IV. In the 2-bit FTS designs in Section III and IV, the positions of the thin line and slot in 2-bit cells are fixed as $l_g = 0.55$ mm and $l_s = 0.45$ mm, and widths of the thin line and gap are set as $g = s = 0.1$ mm, according to the fabrication precision of PCB milling machines.

In fact, different thin line/slot positions and widths can be considered. It is interesting to see the effects of the fine geometries, viz., l_g and l_s, g and s, on the LPF performance.

A. EFFECTS OF LG AND LS

For illustration, we may compare the performance of LPFs designed by using the 2-bit cells of the same l, w, g and s as in Subsection III-D, but different l_g and l_s. The LPF designs will be implemented with the same design objectives, the MOEA/D-GO algorithm and on the same computer.

Here we set $l_g = 0.35$ mm and $l_s = 0.25$ mm for comparison, which indicate thin line and gap near to the middle of the cells, as shown in Fig. 13. For comparison, the thin line and gap positions considered in previous designs are depicted as well.

It takes 22 iterations (about 4 days) to achieve the FTS-based LPF. Figure 14(a) shows one of the layouts. The optimized distance from the offset centerline of the meander line are 0 mm, 0.60 mm, 0 mm, 1.9 mm, 0 mm, 2.8 mm,

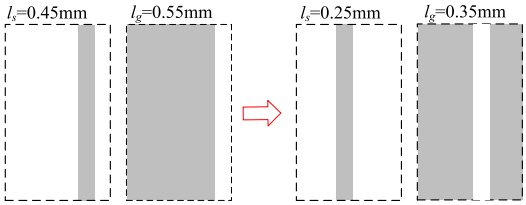

FIGURE 13. Cells with thin line and gap at different positions near the middle.

respectively. Figure 14(b) shows the simulated S-parameters of the designed 2-bit cell LPF.

From Fig. 14 (b), we find that this LPF has a 3-dB cutoff frequency equal to 2.0 GHz, IL less than 0.21 dB and RL better than 20 dB in the passband from dc to 1.64 GHz. The suppression level is higher than 20 dB from 2.42 GHz to 17.17 GHz. The transition band ranges from 2.0 GHz to 2.49 GHz, with corresponding IL from −3 dB to −40 dB, which gives $\xi = 78.7$ dB/GHz. Although ξ is slightly lower than that of the 2-bit design in Subsection III-D, it has already met our design goal $\xi_0 = 70$. Secondly, its stopband shows a better suppression level after meeting our design goal $\beta = 20$. That is, the suppression is higher than 25 dB from 2.47 GHz to 17.13 GHz. In general, the positions of thin line and gap do not affect the achievement of our design goals. Our design goal β is based on the design index of most published literature, so we can ignore the position factor.

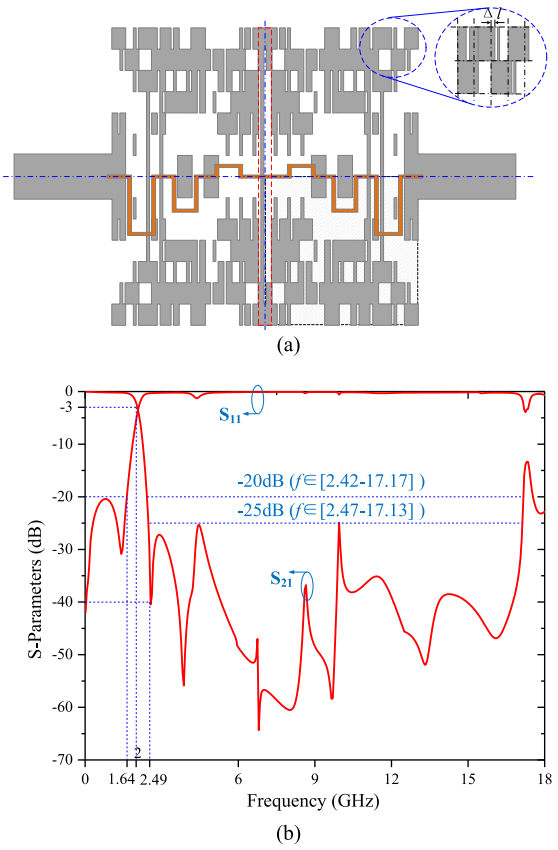

FIGURE 14. The designed 2-bit FTS LPF with lg = 0.35 mm and ls = 0.25mm. (a) Layout. (b) Simulated S-parameters.

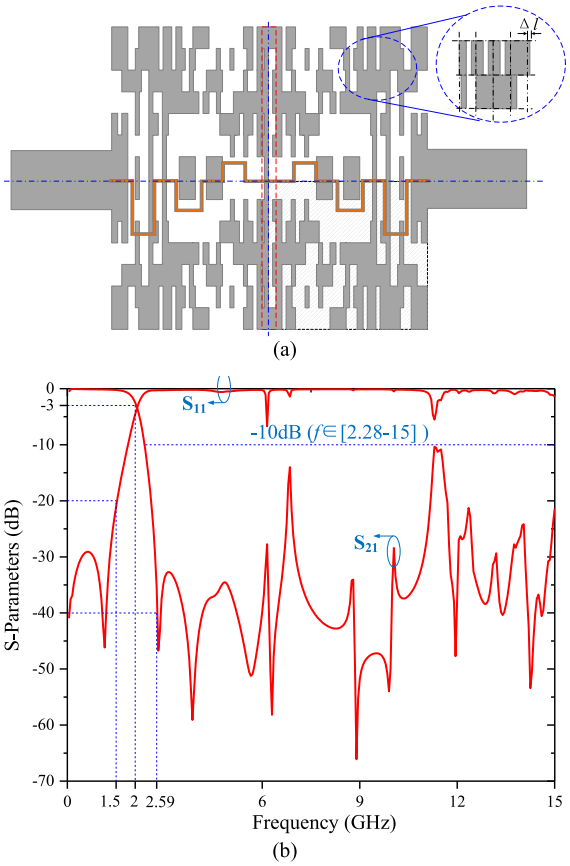

FIGURE 16. The designed 2-bit FTS LPF with g = s = 0.2mm. (a) Layout. (b) Simulated S-parameters.

B. EFFECTS OF G AND S

In above designs, the widths of thin line and gap are set as $g = 0.1$ mm and $s = 0.1$ mm, which imply the fabrication precision on PCB with milling machines. In practical design, this is the most straightforward manner to utilize the fine structures.

To show the effects of thin line and gap widths, we consider $g = 0.2$mm and $s = 0.2$mm on 2-bit cells of the same l and w as in the above design. This is a rather coarse structure because it is comparable to the $l = 0.34$mm in the 1-bit FTS in Section III-C. To ensure the thin line on cell in Fig. 2 (c) can always be connected to metal part of cell in Fig. 2 (d), we set $l_g = 0.35$ mm but $l_s = 0.15$ mm, as shown in Fig. 15.

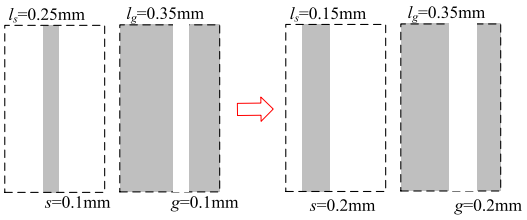

FIGURE 15. Cells with thin line and gap of width of g = s = 0.2mm.

For the same LPF design objectives and the same MOEA/D-GO running on the same computer, the optimization searching yields FTS layout as shown in Fig. 16(a) after 42 iterations, which takes about 6 days, a searching time longer than the above design. The optimized distance from the offset centerline of the meander line are 0 mm, 0.90 mm, 0 mm, 1.5 mm, 0 mm, 2.8 mm, respectively. Figure 16 (b) shows the simulated S-parameters of the designed 2-bit cell LPF.

From Fig. 16 (b), we find that the LPF has a 3-dB cutoff frequency equal to 2.0 GHz, IL less than 0.17 dB and RL better than 20 dB in the passband from dc to 1.5 GHz. However, the suppression level is merely higher than 10 dB from 2.34 GHz to 15 GHz, while the design objective is 20 dB. In addition, the transition band ranges from 2.0 GHz (with IL = −3dB) to 2.59 GHz (with IL = −40 dB), which gives $\xi = 62.7$ dB/GHz, while the design target is $\xi_0 = 70$ dB/GHz.

Therefore, the performance of LPF designed with 2-bit FTS using $g = s = 0.2$mm is worse than the performance of the LPSs shown in Fig. 14 (b). The width of the gap and thin line have significant effects on both the design performance of LPF and efficiency of optimization searching.

It is remarked that the LPF performance in Fig. 16 (b) is even worse than that of the LPF with 1-bit FTS shown in Fig. 5, where we have $\xi = 72.5$ dB/GHz. The reason is that $g = s = 0.2$mm in 2-bit FTS is comparable to $l = 0.34$mm in the 1-bit FTS, and the 2-bit FTS use cell size twice as the 1-bit cell size ($l = 0.65$ mm in 2-bit FTS *vs* $l = 0.34$mm in 1-bit FTS, to ensure almost the same decision space).

In order to take advantage over the 1-bit FTS design, it is thus suggested that the 2-bit FTS design should use thin line or narrow gap of width being at most half of the 1-bit cell dimension. For example, $g < l/2 = 0.171$ mm in the above 2-bit FTS design is a good setting.

VI. CONCLUSION

Now that the structures decide the frequency response of a planar LPF, it is quite reasonable that optimization searching of the appropriate structure may benefit the high-performance LPF design. A novel design strategy based on multi-objective FTS optimization searching is proposed in this paper, without any prerequisite knowledge about the LPF structure. To ensure a high-performance LPF can be achieved, FTS with multi-bit scheme is proposed to guarantee the necessary fine structure can be acquired, without apparent increase of the optimization searching time.

The power of the proposed multi-bit FTS design scheme has been demonstrated by comparing LPF designs with 1-bit FTS and 2-bit FTS. High performance LPF with a sharp roll-off rate, ultra-wide stopband and high stopband suppression can be easily achieved in days.

The multi-bit FTS can be generalized by considering different schemes of forming the FTS cells. For planar structure design on the PCB, thin line and slot of different shapes, vias and even lumped circuit elements can be involved in the FTS cells, which will lead to further work with FTS-based design.

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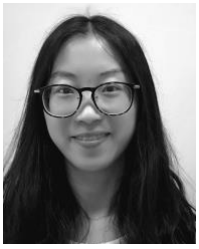

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