IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 22, 2021, accepted May 1, 2021, date of publication May 7, 2021, date of current version May 18, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3078300

A Single Phase, Single Stage AC-DC Multilevel LLC Resonant Converter With Power Factor Correction

ANTONY K. PETER, (Member, IEEE), AND JAISON MATHEW, (Senior Member, IEEE)
Government Engineering College, Thrissur 680009, India, affiliated to APJ Abdul Kalam Technological University
Corresponding author: Antony K. Peter (antonykannanaykal@gmail.com)

ABSTRACT Single stage LLC resonant converters with inherent power factor correction are getting popularity in AC-DC converters due to its reduced size and weight. However, single stage topologies are usually less efficient in regulating the dc bus capacitor voltage pertaining to line and load transients. This paper proposes a multi-level flying capacitor based single stage AC-DC LLC topology to address the issue of voltage balancing of dc-bus capacitor and to reduce the voltage stress of the switching devices. The proposed three-level inverter topology guarantees zero voltage switching, less circulating currents, reduced switching stress and losses. The converter uses bridgeless rectification scheme for better efficiency and the power factor is made nearly unity by operating the source-side inductor in discontinuous current conduction. Variable switching frequency control is used to regulate the output voltage of the converter and pulse width modulation is used to control the dc-bus voltage. This dual control scheme is very effective to keep the dc-bus voltage nearly constant over a wide range of line and load variations. The proposed topology and control scheme have been validated by hardware results on a 250W resistive load.

INDEX TERMS LLC resonant converters, AC-DC converters, soft switching, PFC, THD, DC bus.

I. INTRODUCTION

Soft switching of switching devices, inherent short circuit and open circuit protection, and high efficiency are some of the benefits of LLC resonant converters [2]–[4]. They can work at very high switching frequency which reduces the size and weight of the converter and are well suited for applications like electric vehicle battery charging. However, in AC-DC applications, a front end boost power factor correction (PFC) stage is usually needed to improve the power factor [3]. The recent trend is to use a single power converter for controlling both the power factor stage and LLC stage (see Fig. 1) where the operation of the input inductor in the discontinuous conduction mode helps to shape the average input current without any closed loop control thereby improving the power factor [5], [6]. However, the average output power of the converter may not be equal to that of the PFC stage during load variations and transients. This power imbalance causes the DC bus capacitor voltage to vary until energy balance is achieved [5]. These variations can lead to unstable operation of the converter or even to the destruction of bus capacitor due to over-voltage.

To avoid this issue and to achieve energy balance with a reasonable DC bus voltage, the controller generally shifts the switching frequency of the converter and at low loads, the switching frequency of the converter may reach extreme levels causing high switching losses and control difficulties. In [7]–[9], a burst mode control scheme is used where the controller pauses the switching action for a certain time intervals based on the bus capacitor voltage and output DC voltage when the switching frequency increases to extreme high levels. This leads to transients in the voltage and current waveforms and the normal functioning of the controller gets disrupted. Furthermore, the burst mode of operation introduces low frequency components in the voltage necessitating extra filtering.

In [10], a modular multilevel based LLC resonant converter has been proposed which is capable of operating the converters over a narrow frequency range for a wide range of input voltage variations with the help of an additional feed forward control by switching in and out of modules. However, the requirement for a large number of switching devices and the charge balancing requirement of the modules limits them

The associate editor coordinating the review of this manuscript and approving it for publication was Sze Sing Lee.

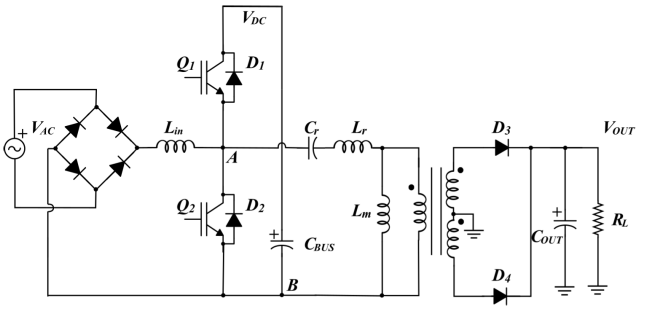


FIGURE 1. Conventional single-stage LLC converter.

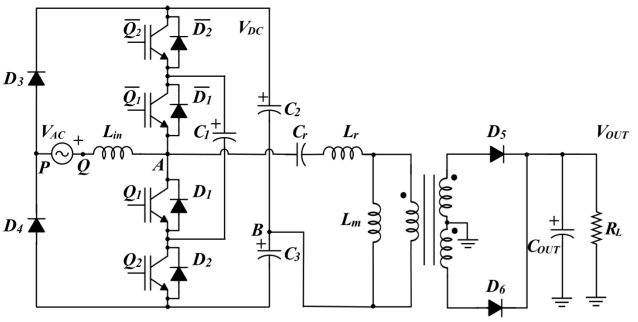
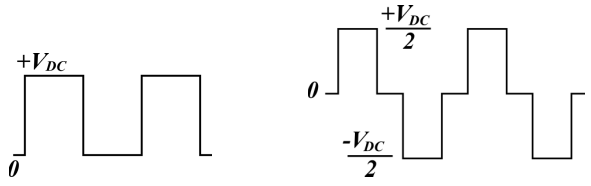


FIGURE 2. Proposed three-level single stage LLC converter.



(a) Conventional topology (b) Proposed Topology

FIGURE 3. Input voltage to the LLC stage V_{AB}.

for high voltage applications. In [6], a bridgeless topologies for AC/DC resonant converters have been proposed. The converter can return additional energy stored in the DC bus capacitor back to the supply thus regulating the DC bus voltage. However, returning power to the grid distorts the current waveform and increases the total harmonic distortion (THD).

High voltage stress experienced by the switching devices is another drawback of these converters. In [1], [11]–[18], multilevel inverters are used for reducing the voltage stress across switching devices and to increase the power range of LLC resonant converters. Different types of single stage bridgeless PFC topologies have been presented in literature [19]–[23]. However, they suffer from shortcomings such as poor DC bus voltage regulation, High switching frequency at light loads, requirement of more switching devices and high voltage stress.

This paper proposes a novel bridgeless topology based on a three-level flying capacitor inverter. The multilevel configuration reduces the voltage stress across switching devices. The bridgeless operation reduces conduction loss. The three-level voltage waveform of the topology gives additional freedom to control the duty ratio of the PFC stage (refer Fig. 3b). The output voltage of the converter is regulated by switching frequency control and the DC bus capacitor voltage is regulated by controlling the duty ratio of switches. But during light loads, duty ratio control is used to regulate the output DC voltage keeping the switching frequency constant. This prevents the converter from extreme high switching frequency during low loads. The topology guarantees zero voltage switching for all the IGBT switches. The converter is operated in discontinuous conduction mode, which is useful in achieving natural power factor correction.

The paper is organized as follows: Section II discusses the proposed topology and section III presents the different modes of operation. Section IV is about the steady-state analysis. A comparison of the proposed topology with conventional topology is given in section V. Control strategy is discussed in section VI. The experimental results and analysis are presented in Section VII. Finally, part VIII concludes the work.

II. PROPOSED TOPOLOGY

In the proposed topology, a three-level flying capacitor-based inverter constitutes the rectification stage, boost stage as well as the inverter stage (see Fig. 2). The same switches control both the LLC and the boost stages. Here, the converter operates in discontinuous conduction mode, which assures unity displacement power factor. The voltage applied to the LLC stage contains three discrete levels (see Fig. 3b) unlike the two level waveform in conventional single-stage converters (See Fig. 3a) [5]. This three-level voltage pattern helps the controller to adjust the duty ratio without disturbing the waveform symmetry and thereby regulating the DC bus voltage. Controlling the DC bus voltage is crucial for the protection of capacitors and for limiting the voltage stress of the switching devices for a wide range of load and input variations. In the proposed topology, zero voltage switching (ZVS) of the IGBT switches is naturally achieved by incorporating LLC based resonant stage. A full-wave Schottky rectifier with a filter capacitor comprises the output side of the converter. In order to get voltage symmetry across the LLC terminal, the voltage across capacitors C_1, C_2, and C_3 should be at the same voltage level ($V_{DC}/2$). The switch pairs Q_1, $\overline{Q_1}$ and Q_2, $\overline{Q_2}$ operates in a complementary fashion. The working of LLC resonant converter is similar to that of conventional converters and is not repeated here [24], [25]. This paper focuses on the issue of capacitor balancing and the modes of operation are outlined in the next section.

III. MODES OF OPERATION

The eight different operational modes of the proposed converter are presented in Fig. 4. Modes 1 to 4 describe operation for positive half cycle of the input AC supply whereas modes 5 to 8 are related to negative half cycle of the input AC supply.

Mode 1 (See Fig. 4a): Switches Q_1 and Q_2 are turned ON. The current in the input inductor L_{in} increases and energy is stored in the inductor. The voltage across LLC terminals is the voltage across capacitor C_3 ($V_{AB} = -V_{DC}/2$).

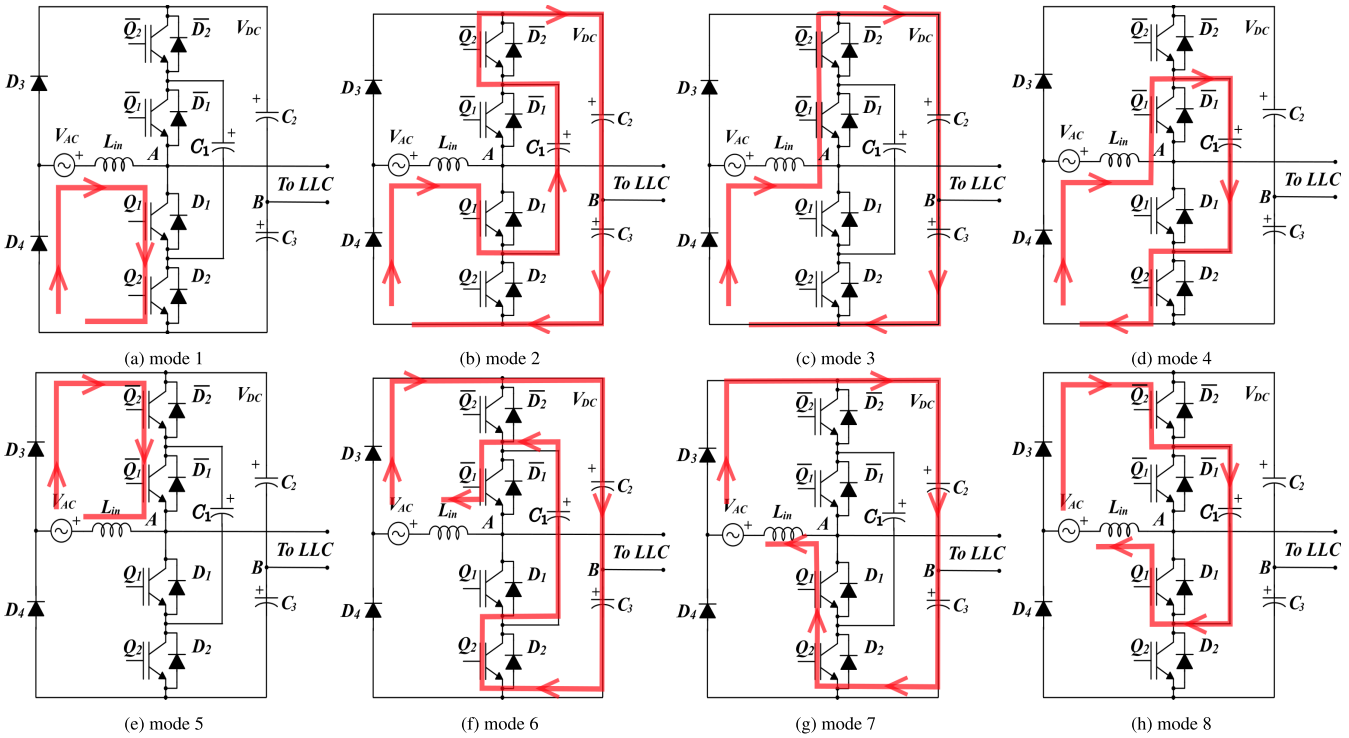


FIGURE 4. Different operating modes of the converter. Modes (1-4) and (5-8) represents the different modes during the positive and negative half cycles of the input supply V_{AC}.

Mode 2: Switch Q_2 is turned OFF. Inductor current decays through C_1 and $\overline{D_2}$. The voltage across $\overline{Q_2}$ now falls to zero making it ready to turn ON at ZVS. $\overline{Q_2}$ is then turned ON. In this mode, the input inductor current discharges C_1 and charges capacitors C_2 and C_3. The voltage across LLC is zero ($V_{AB} = 0$) in this mode. Fig. 4b represents this mode of operation.

Mode 3: Switch Q_1 is turned OFF. Current completes its path through $\overline{D_1}$. Voltage across the switch $\overline{Q_1}$ drops to zero. $\overline{Q_1}$ is then turned ON at ZVS. Input inductor charges capacitors C_2 and C_3. The voltage across LLC is equal to the voltage across capacitor C_2 ($V_{AB} = +V_{DC}/2$). Fig. 4c shows the mode.

Mode 4: In this mode, the switch $\overline{Q_2}$ is turned OFF. The current flowing through the LLC turns ON the diode D_2 making the switch Q_2 ready to be turned ON at ZVS. The switch Q_2 is then turned ON. Capacitor C_1 gets charged up. The voltage across the LLC terminals falls to zero ($V_{AB} = 0$). Fig. 4d depicts the mode. At the end of this mode, input inductor completely discharges but the lagging current flowing through the LLC circuit turns ON the diode D_1 and D_2. Now the switches Q_1 and Q_2 are ready to be turned ON at ZVS (mode 1).

The working modes 5 to 8 during the negative half cycle of the input supply (see Fig. 4) are similar to the modes 1 to 4 of the positive half cycle and is not explained here.

Fig. 5 shows the timing diagram of gate pulses, input inductor current, and LLC voltage (V_{AB}) for different modes of

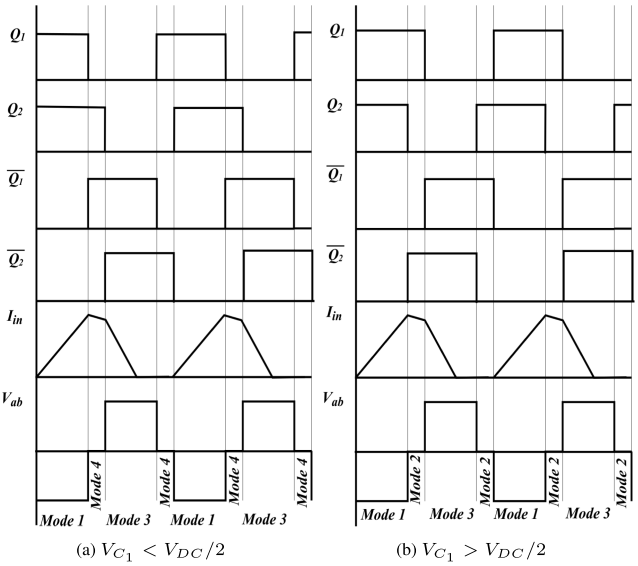


FIGURE 5. Timing diagram based on different modes of operation.

operation. It also explains how to balance the flying capacitor voltage V_{C1}. Mode 4 charges C_1 and mode 2 discharges it. Hence if V_{C1} is less than $V_{DC}/2$ then mode 2 will not be used in that cycle of the converter (refer Fig. 5a). Similarly, to decrease V_{C1}, mode 4 is withdrawn and mode 2 is inserted in that cycle of converter (see Fig. 5b). So in any cycle of the converter (during positive cycle of input supply) either

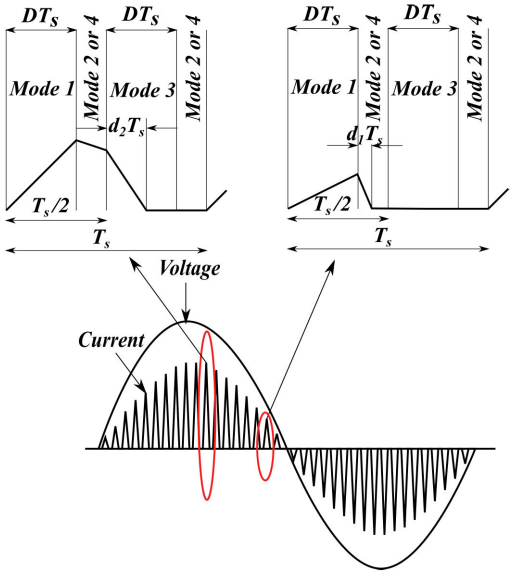


FIGURE 6. Input current and voltage in discontinuous conduction mode.

mode 2 or mode 4 is used to balance V_{C1}. During the negative half cycle of the input supply, mode 6 and mode 8 are used to charge and discharge C_1 respectively.

IV. STEADY STATE ANALYSIS

In this section, the relationship between DC bus voltage, power, frequency and duty ratio for the boost stage and LLC stages of the converter are analyzed with mathematical equations and plots. The steady-state equations for the LLC stage are derived based on the first-order approximation (FHA) technique [26]. The accuracy of the first order approximation method is greatest when the frequency of the input square wave is near to the series resonant frequency.

A. BOOST STAGE

In discontinuous conduction mode the input inductor current starts and ends at zero in each switching cycle. Input inductor, L_{in} stores energy during mode 1 (refer Fig. 4) and the peak value of inductor current at the end of mode 1 is given by (refer Fig. 6):

$$v_{AC} = L_{in}\frac{di_{Lin}}{dt}; (0 \le t \le DT_s) \tag{1}$$

$$I_{Lin\_peak} = \frac{v_{AC}DT_s}{L_{in}}; (t = DT_s) \tag{2}$$

where

i_{Lin}	is the current through input inductor;
I_{Lin_peak}	is the maximum value of i_{Lin};
'D'	is the duty ratio;
v_{AC}	is the instantaneous value of input ac voltage;
T_s	is the switching frequency.

Mode 1 is followed by mode 2 or by mode 4 where, input inductor current i_{Lin} decays to a lower value (refer Fig. 4). The expression for i_{Lin} during this mode assuming $i_{Lin} > 0$ through out this mode is given by (refer Fig. 6):

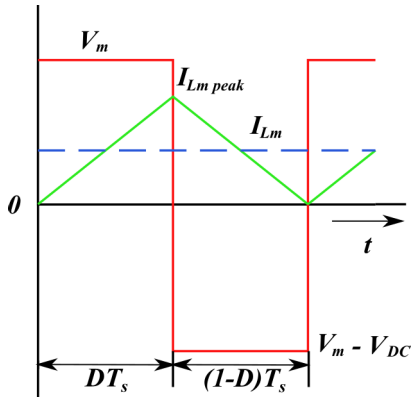


FIGURE 7. Boost stage converter at the boundary of Continuous – discontinuous mode.

$$v_{AC} - \frac{V_{DC}}{2} = L_{in}\frac{di_{Lin}}{dt}; (DT_s \le t \le \frac{T_s}{2}) \tag{3}$$

$$i_{Lin} = \frac{(2v_{AC} - V_{DC})(1-2D)T_s}{4L_{in}} + I_{Lin\_peak};\ t = \frac{T_s}{2} \tag{4}$$

By substituting the value of I_{Lin_peak} from (2) in (4), the condition for which i_{Lin} greater than zero within mode 2 can be determined as shown below:

$$i_{Lin} = \frac{(2v_{AC} - V_{DC})(1-2D)T_s}{4L_{in}} + \frac{v_{AC}DT_s}{L_{in}} \ge 0; \quad t = \frac{T_s}{2} \tag{5}$$

$$v_{AC} > \frac{(1-2D)V_{DC}}{2} \tag{6}$$

If the condition given in (6) is not satisfied, then the input current i_{Lin} reaches zero before the end of mode 2. Let d_1T_s be the time taken for i_{Lin} to reach zero before the end of mode 2. The expression for I_{Lin_peak} can be calculated from the decay slope of mode 2 and is given by:

$$I_{Lin\_peak} = \frac{(\frac{V_{DC}}{2} - v_{AC})d_1T_s}{L_{in}} \tag{7}$$

By equating (2) and (7), d_1 can be expressed as:

$$d_1 = \frac{Dv_{AC}}{\frac{V_{DC}}{2} - v_{AC}} \tag{8}$$

If the input inductor current i_{Lin} has not decayed to zero completely in mode 2, the value of i_{Lin} at the beginning of mode 3 can be obtained from the decay slope of i_{Lin} (refer Fig. 6) :

$$v_{AC} - V_{DC} = L_{in}\frac{di_{Lin}}{dt}; \quad (\frac{T_s}{2} \le t \le (\frac{T_s}{2} + d_2T_s)) \tag{9}$$

$$i_{Lin} = \frac{(V_{DC} - v_{AC})d_2T_s}{L_{in}}; (t = \frac{T_s}{2}) \tag{10}$$

where d_2T_s is the time required for the inductor current to reach zero. By equating (4) and (10) an expression for d_2 can

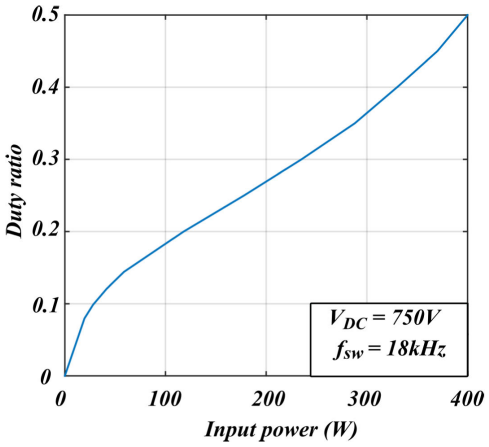


FIGURE 8. Input power of the boost stage converter vs. duty ratio, f_{sw} = 18kHz, V_{DC} = 750V.

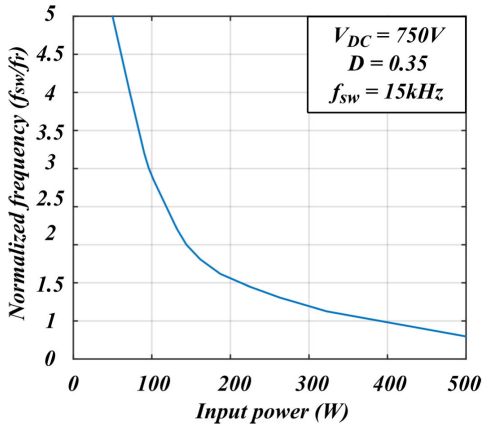


FIGURE 9. Input power of the boost stage converter vs. frequency, f_r = 15kHz, V_{DC} = 750V, D = 0.35.

be derived as given below:

$$d_2 = \frac{2v_{AC} + V_{DC}(2D-1)}{4(V_{DC} - v_{AC})} \tag{11}$$

The converter should be able to ensure discontinuous conduction mode under all operating conditions. The maximum value of input inductance to guarantee discontinuous conduction mode can be derived by applying the boundary conditions when the converter is operated at 50% duty ratio and when the input supply voltage at its maximum V_m (refer Fig. 7). The average value of input inductor current I_{Lm} for this switching cycle is given by:

$$I_{Lm} = \frac{I_{Lm\,peak}}{2} = \frac{V_m D T_s}{2L_{in}} \tag{12}$$

where, $I_{Lm\,peak}$ is the peak value of inductor current for the maximum input supply voltage V_m. At the boundary between continuous and disconduction modes, the output voltage of the converter is given by:

$$V_m = (1-D)V_{DC} \tag{13}$$

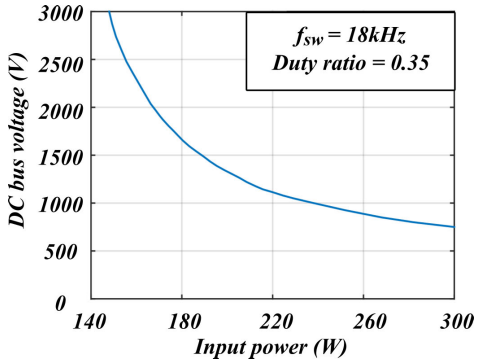


FIGURE 10. Input power of the boost stage converter vs. DC bus voltage, f_{sw} = 18kHz, D = 0.35.

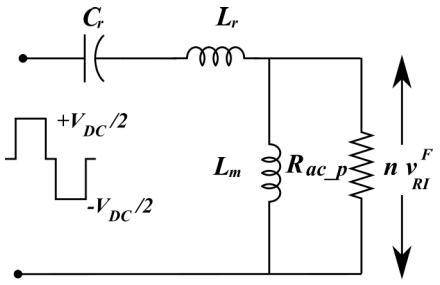


FIGURE 11. Equivalent representation of LLC referred to the primary side.

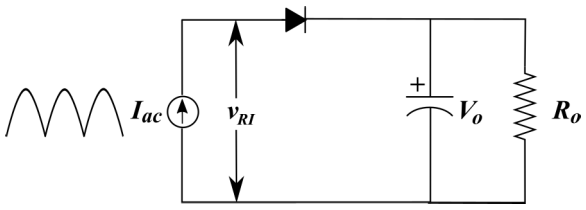


FIGURE 12. Equivalent representation of the secondary side of the transformer.

Substituting (13) into (12) gives the maximum value of input inductance.

$$L_{in} \leq \frac{V_{DC}D(1-D)T_s}{2I_{Lm}} \tag{14}$$

The average input inductor current over one switching cycle is given by:

$$i_{Lin\_avg} = \frac{1}{T_s}\left(\int_0^{DT_s} i_{Lin}dt + \int_{DT_s}^{\frac{T_s}{2}} i_{Lin}dt + \int_{\frac{T_s}{2}}^{\frac{T_s}{2}+d_2T_s} i_{Lin}dt\right) \tag{15}$$

The average input power of the converter can be found by substituting the value of average input current from (15) into the following equation:

$$P_{in\_avg} = \int_0^{T_s} (i_{Lin\_avg} \times v_{AC})dt \tag{16}$$

The equation (16) is simulated and the effect of duty ratio on the input power is plotted in Fig. 8. The variation of

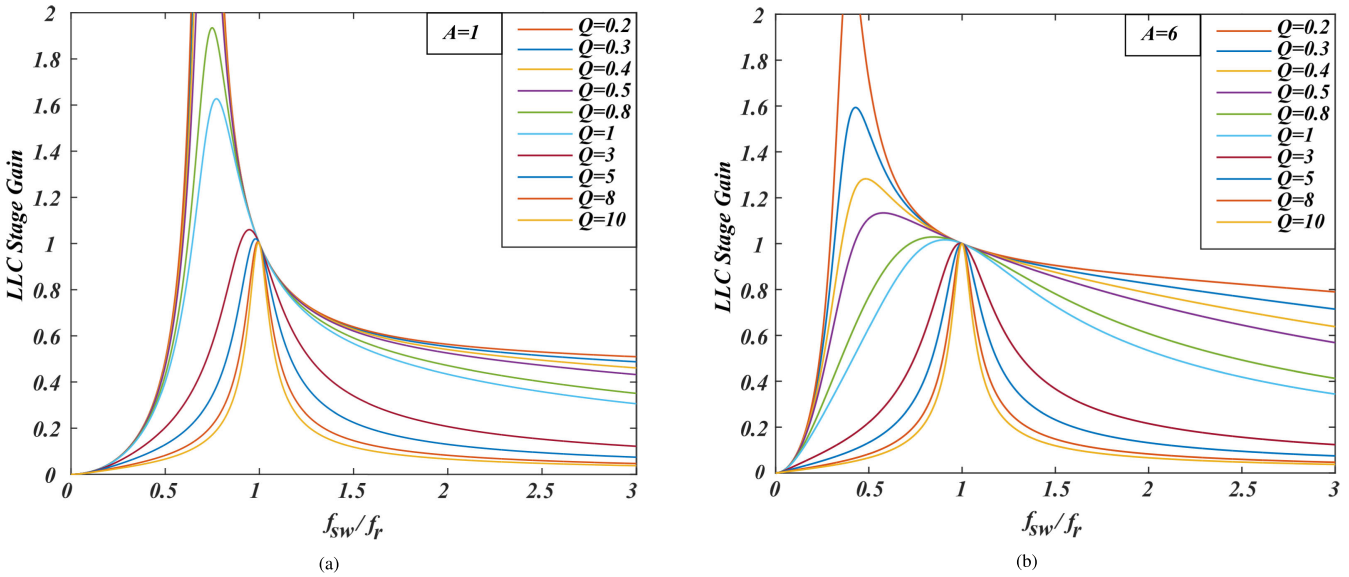


FIGURE 13. Plots of LLC voltage gain function (M) vs. normalized frequency (f_{sw}/f_r), (a) A=1, (b) A=6.

duty ratio is almost proportional to the input power of the converter. Therefore regulating duty ratio provides a good control over the input power of the converter. The input power is inversely proportional to the normalized switching frequency of the converter (see Fig. 9). At high switching frequencies, the variation in input power is small. Fig. 10 shows the variation in DC bus voltage with input power due to load variation without having frequency or duty ratio control. The high DC bus voltage at lower input power can even lead to the destruction of the capacitor which necessitates the importance of regulating the DC bus voltage.

B. LLC STAGE

The equivalent representation of LLC converter referred to primary is shown in Fig. 11. The input voltage to the primary circuit is assumed to be a stepped square wave having peak voltage $\pm\frac{V_{DC}}{2}$. The fundamental component of input voltage to LLC stage is given by

$$v_{in}^{F} = \frac{8V_{DC}sin(\frac{D}{2})}{2\pi}sin\,\omega t \tag{17}$$

On the output side (refer Fig. 11 & Fig. 12), the fundamental component of voltage nv_{RI}^{F} is given by:

$$nv_{RI}^{F} = \frac{4nV_o}{\pi}sin\,\omega t \tag{18}$$

where 'n' is the turns ratio.

The voltage gain of LLC stage (M) can be found from the equivalent circuit representation shown in Fig. 11.

$$M = \frac{n\,v_{RI}^{F}}{v_{in}^{F}} = \frac{\frac{4nV_o}{\pi}sin\,\omega t}{\frac{8V_{DC}sin(\frac{D}{2})}{2\pi}sin\,\omega t} = \frac{nV_o}{sin(\frac{D}{2})V_{DC}} \tag{19}$$

$$M = \left|\frac{(\frac{\omega}{\omega_o})^2 A}{[\frac{\omega}{\omega_o}^2(A+1)-1]+j(\frac{\omega}{\omega_o}^2-1)\frac{\omega}{\omega_o}AQ}\right| \tag{20}$$

where A is the ratio of magnetizing inductance L_m to resonant inductance L_r; f_o is the resonant frequency which is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_rC_r}} \tag{21}$$

Q is the quality factor which is given by:

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac\_p}} \tag{22}$$

$$R_{ac\_p} = \frac{8n^2R_o}{\pi^2} \tag{23}$$

where R_{ac_p} is AC equivalent of load resistance referred to primary. R_o is the output load resistance.

From (20) it is obvious that the voltage gain of the LLC stage depends on Q, f_{sw} and A. Fig. 13 shows possible variations of voltage gain for different values of Q (0.2-10) and ($\frac{L_m}{L_r}$). Based on the required frequency range of operation and desired voltage gain, Q and A values can be selected from the plot. The desired voltage gain M needed for the converter can be found from the equation (19).

Since the output load of the converter is known, LLC stage power can be calculated as given below:

$$P_{LLC} = \frac{V_o^2}{R_o} \tag{24}$$

The value of V_o can be found by equating (19) & (20). It is then substituted into (24).

$$P_{LLC} = \frac{sin^2(\frac{D}{2})V_{DC}^2}{n^2R_o} \cdot \left(\left|\frac{(\frac{\omega}{\omega_o})^2 A}{[\frac{\omega}{\omega_o}^2(A+1)-1]+j(\frac{\omega}{\omega_o}^2-1)\frac{\omega}{\omega_o}AQ}\right|\right)^2 \tag{25}$$

From (25), it is clear that the power of the LLC stage depends on the duty ratio. Fig. 14a & 14b shows the variation

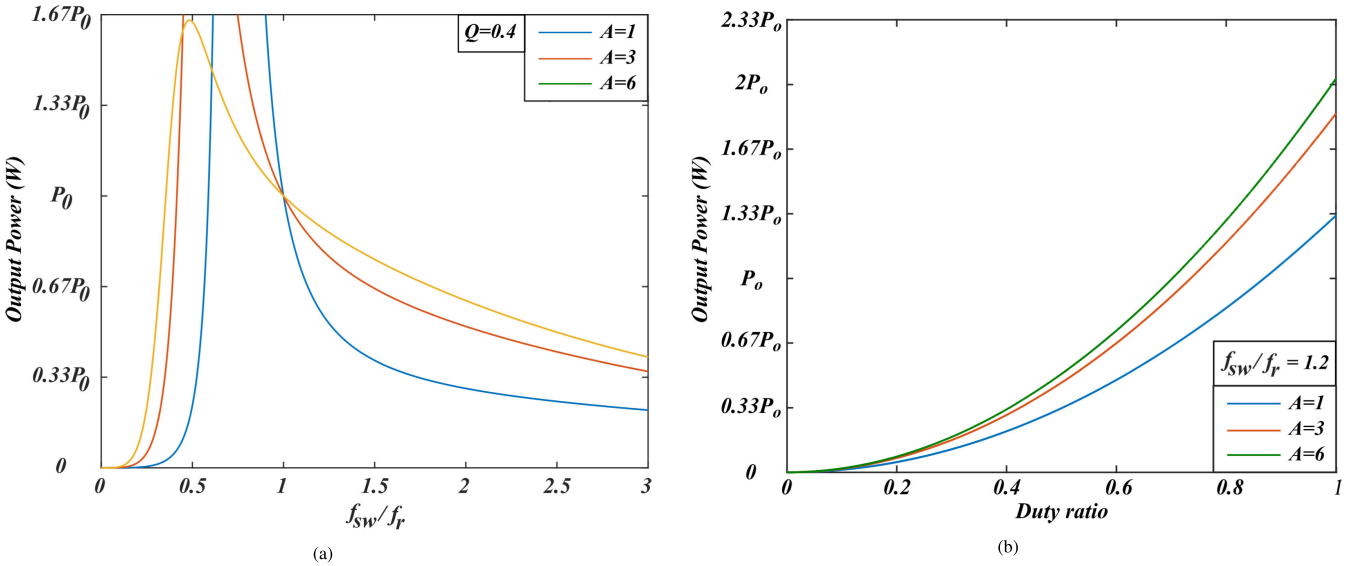


FIGURE 14. Plots of LLC stage power, (a) Output power P_o vs. normalized frequency (f_{sw}/f_r) (Duty ratio constant), (b) Output power P_o vs. duty ratio (frequency constant).

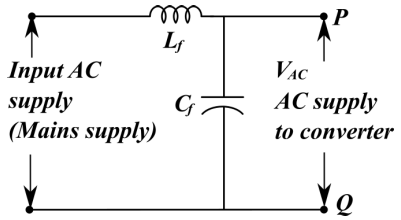


FIGURE 15. LC Filter circuit.

of output power with normalized frequency and duty ratio, respectively. Increasing the ratio $\frac{L_m}{L_r}$, make the curve much flatter. However, for a wide range of output power, the converter requires extremely large variation in frequency. Operating the converter at low frequencies away from series resonance increases the circulating current through the LLC and increases the losses [26]. For switching frequencies greater than series resonant frequency, the magnitude of circulating current is small but higher switching frequency increase switching losses. Flow of circulating current is similar to that of conventional LLC converters [26] and therefore it is not explained here. The operation and working of the resonant tank are similar to that in conventional topology. Hence the small signal analysis can found be in [27].

C. INPUT FILTER DESIGN

A normal LC filter can be introduced before the converter for filtering the input current (refer Fig. 15). The cut-off frequency f_c of the LC filter is taken as 0.7 times the series resonant frequency f_r, which is taken as the minimum operating frequency of the converter.

$$f_c = \frac{1}{2\,\pi\,\sqrt{L_f C_f}} \tag{26}$$

where L_f and C_f are filter inductance and capacitance.

V. COMPARISON WITH CONVENTIONAL SINGLE STAGE AC-DC LLC RESONANT CONVERTERS

The proposed topology has all advantages of conventional topologies [5]–[9] such as natural power factor correction, single-stage operation and zero voltage switching. The additional advantages of the proposed topology compared to conventional topologies are as follows. The proposed topology uses 6 switching devices (2 diodes and 4 IGBT) to generate a three-level voltage to the LLC stage with two control parameters (duty ratio and switching frequency). The conventional topologies use the same number of switching devices (4 diodes and 2 IGBT) to generate two-level voltage for the LLC stage with a single control variable (switching frequency). The bridgeless topologies [6] use only 4 switching devices. However, they don't have the following benefits:

Dual control variables is a major advantage of the proposed topology. The controller can regulate the DC bus voltage and output DC voltage separately by varying duty ratio and switching frequency. In conventional two-level single-stage converters, to maintain the voltage symmetry of the LLC stage, their duty ratio must be fixed at 50%. To ensure discontinuous operation, the inductor current's decay slope must be greater than the rising slope. For this, the DC bus voltage must be at least two times greater than the maximum input supply voltage V_m [5]–[9]. But for the proposed converter inductor current decaying time can be increased and therefore the DC bus voltage can have lower values. Furthermore, in the proposed topology, due to the multilevel configuration, the voltage stress across the switching devices is half the voltage stress in the conventional topology (refer Fig. 1).

In conventional topologies [5]–[9], switching frequency is the only control variable. To operate the converter at 33% of the full load, the frequency must be nearly three times the series resonant frequency [5] (refer Fig. 14a). To avoid these

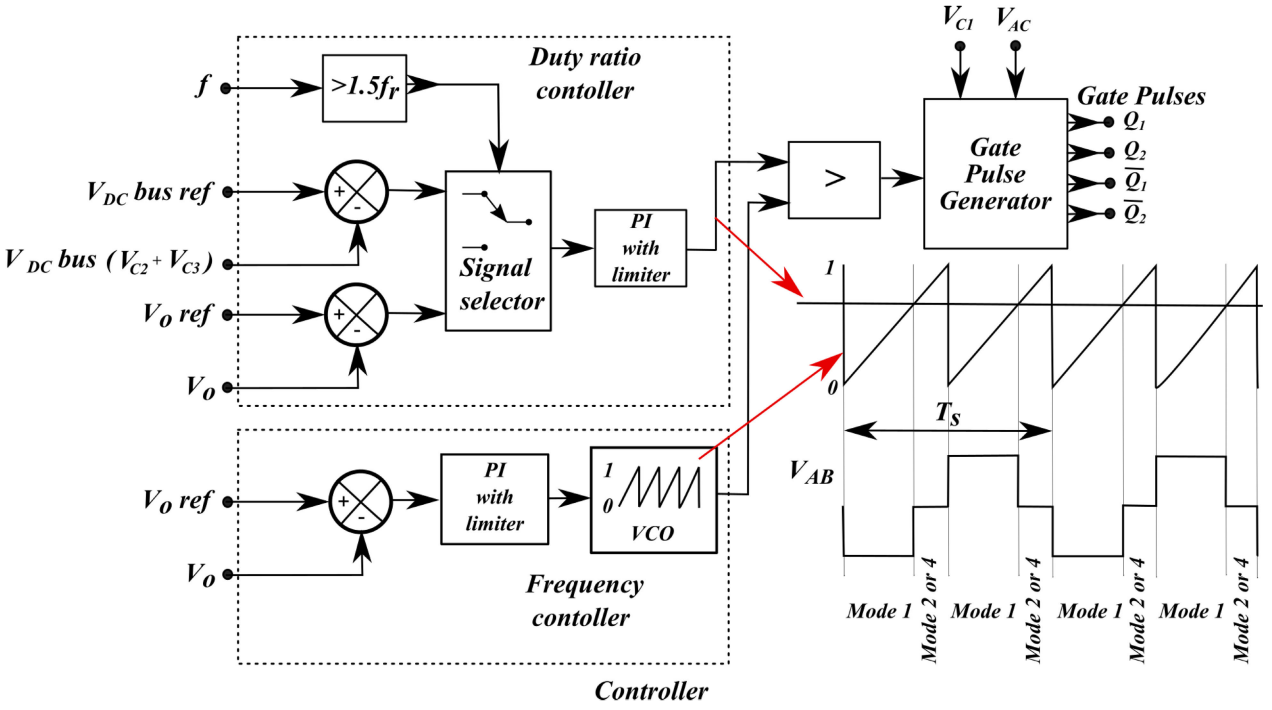


FIGURE 16. Control block diagram.

extreme high switching frequencies, the conventional system enters into burst mode when the frequency reaches (2-3) times the resonant frequency. However, in the proposed topology, the maximum switching frequency is fixed at 1.5 times the series resonant frequency. Beyond that, duty ratio control is activated to control the output power. This is explained in the next section. By using duty ratio control, the load can be reduced to no load keeping the switching frequency constant at 1.5 times the resonant frequency f_r.

VI. CONTROL STRATEGY

In contrast with traditional AC-DC LLC based single-stage converters, the proposed topology gives an additional freedom of controlling the duty ratio apart from switching frequency control. The duty ratio of the three-level voltage is varied to vary the energy stored in the inductor. Increasing the duty ratio increases the energy stored by the input inductor. This stored energy ultimately reaches the capacitor during the energy discharge cycle, raising the DC bus voltage.

Fig. 16 shows the control block diagram of the proposed circuit. During regular operation, the duty ratio controller regulates the DC bus voltage by varying the duty ratio. The controller estimates the duty ratio from the error in DC bus voltage. The frequency controller regulates the output DC voltage by varying the switching frequency of the converter. From the error in output voltage, PI generates a control signal. The signal is used together with a counter logic to generate a sawtooth waveform, which has its maximum value equal to the control signal. The sawtooth waveform is then compared with the duty ratio signal from the duty ratio controller (refer Fig. 16). The flying capacitor voltage is balanced V_{c_1} by using the switching state redundancies in mode 2 and mode 4 ($V_{AB} = 0$). The charging and discharging modes of the capacitors are shown in Table 1.

TABLE 1. Charging discharging modes of capacitors.

Modes	Capacitor states		
	C1	C2	C3
1	0	0	0, -2
2	-1, -2	1, -2	1
3	0	1, -2	1
4	1	0	0, -2
5	0	0, -2	0
6	1	0, -2	0
7	0	1	1, -2
8	-1, -2	1	1, -2

1 = Charging through input inductor L_{in}
0 = Not affected
-1 = Discharge through input inductor L_{in}
-2 = Discharge to load

From the analysis in the previous section, it is clear that the switching frequency of the converter increases with a reduction in load (see Fig. 14a). To avoid these extreme high frequencies, the PI controller with limiter limits the converter's switching frequency to 1.5 times the resonant frequency. Once the frequency controller reaches its maximum saturation, duty ratio control is used to regulate the output DC voltage. To decrease the output power, the duty ratio controller reduces the duty ratio (refer Fig. 14b). For this, error in DC bus voltage is replaced with output DC voltage error using a signal selector (refer Fig. 16). (Note: The DC

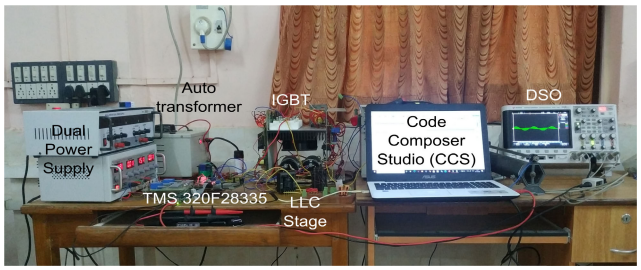


FIGURE 17. Experimental setup.

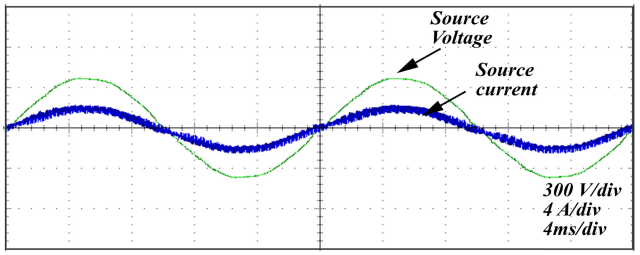


FIGURE 18. Source voltage and current waveform.

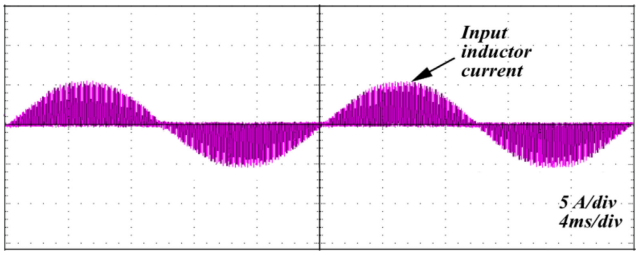


FIGURE 19. Input current waveform through input inductor.

bus voltage will not rise above the maximum reference value because the duty ratio of the converter is further reduced to reduce output power.)

The initial frequency of the controller is set at 1.5 times the resonant frequency. Both the frequency and duty ratio affects the output DC voltage. So for smooth operation, the frequency control loop is controlled very fast compared to the duty ratio control. Therefore for any changes in the load or input, the frequency controller shifts to its new frequency very fast. Duty ratio control loop slowly regulates the DC bus voltage and obtain necessary regulation. The discontinuous conduction mode of the proposed converter automatically shapes the average input current to be nearly sinusoidal and in-phase with the input voltage providing unity displacement power factor without any closed-loop control (See Fig. 6).

VII. EXPERIMENTAL RESULTS

A 48V, 250W converter prototype is designed, and implemented. The converter ratings are: input supply voltage: 190-300 Vrms, output voltage: 48V, resonant frequency: 15kHz, DC bus voltage: 700-850 Vrms. Table 2 gives detailed converter parameters.

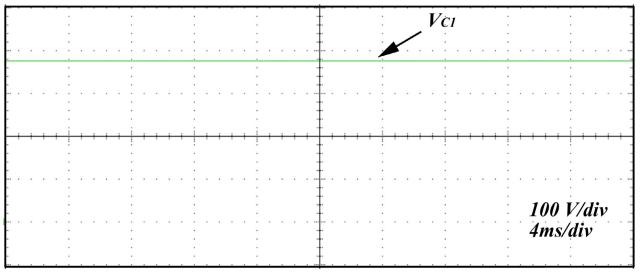


FIGURE 20. Flying capacitor voltage waveform, V_{C1}.

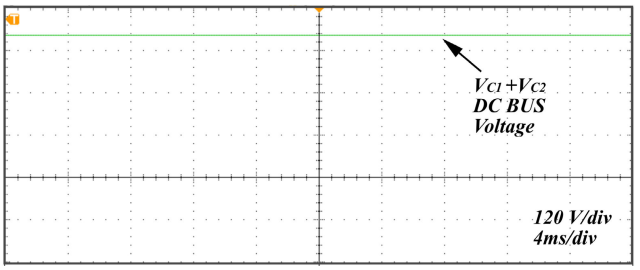


FIGURE 21. DC bus voltage waveform, $V_{C1} + V_{C2}$.

TABLE 2. Converter parameters.

Parameter	Value
Input Voltage, V_{AC}	190-300 Vrms
Output Voltage, V_o	48V
Resonant frequency, f_r	15kHz
Minimum switching frequency, f_m	11kHz
Input filter,	0.6mH, 3μF
Input inductor, L_{in}	1mH
Diodes primary side	MBR20200
Diode secondary side	MUR860
IGBT	SKM75GB12V
Transformer turns ratio N_1/N_2	5
Series resonant inductor, L_r	7.4mH
Series resonant capacitor, C_r	15nF
Magnetising inductance, L_m	18 mH
DC bus capacitor, C_2, C_3	2200μF
Output filter capacitor, C_{out}	1000μF

The hardware is realized by using TMS320f28335 DSP processor as the controller. Output DC voltage, DC bus voltage, flying capacitor voltage and input supply voltage are sensed using voltage sensor LV-20P. A second-order butterworth low pass filter based on a high slew rate Op-amp MC34074 filters the feedback voltage signals. The hardware setup of the work is shown in Fig. 17.

Fig. 18 shows the hardware result of source voltage and current at full load. These figures confirm the near unity power factor of the converter. Fig. 19 shows the discontinuous current through the input inductor L_{in}. The input inductor current is filtered using an LC filter. The filtered waveform is in Fig. 18 Hardware results for flying capacitor and DC bus voltages are shown in Fig. 20 and 21. The flying capacitor voltage is held constant at half the DC bus voltage. The ripples in the capacitor voltages are very low. Fig. 22 shows the output DC voltage regulated at 48V. The ripple magnitude of

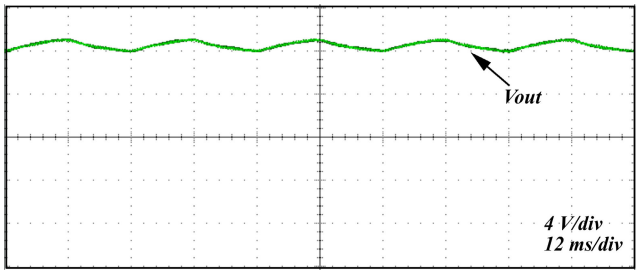


FIGURE 22. Output DC voltage waveform, V_o.

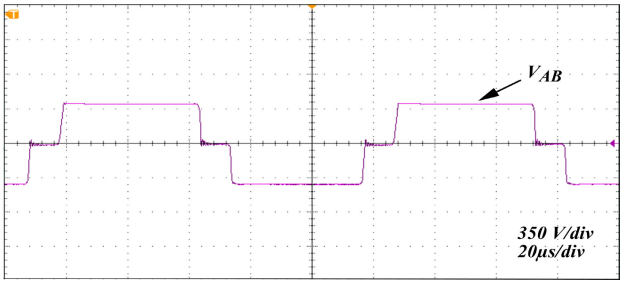


FIGURE 23. Voltage waveform across LLC terminals, V_{AB}.

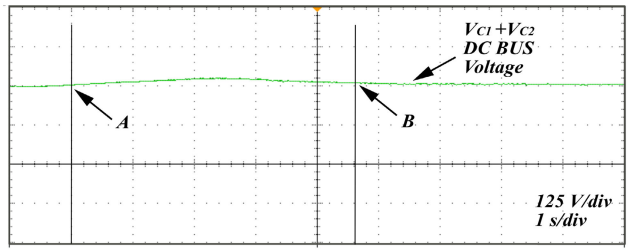


FIGURE 24. The transient response of DC Bus voltage when the load reduced by 30% of full load.

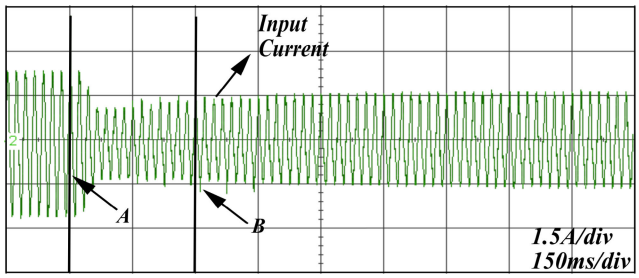


FIGURE 25. The transient response of input supply current when the load reduced by 30% of full load.

output DC voltage is found to be less than 1%. The three-level voltage applied to LLC terminals V_{AB} operating at a duty ratio of 70% is shown in Fig. 23.

Transient response of the DC bus voltage when the load is reduced by 30% from full load at instant A as shown in Fig. 24, where the capacitor voltage rises by 3% and settles to the reference bus voltage in 4.5 seconds. The variation in line current when 30% of the load is reduced from full load

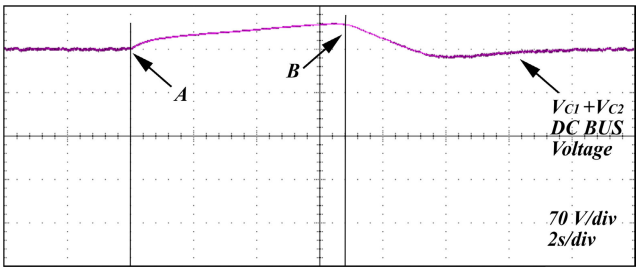


FIGURE 26. The transient response of DC Bus voltage when the DC bus controller is deactivated at instant A and reactivated at instant B.

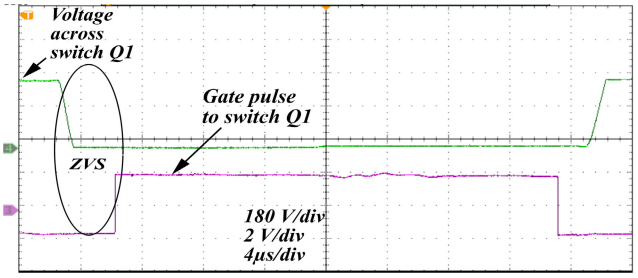


FIGURE 27. Voltage across switch Q_1 (green color) and its gate pulse (pink color).

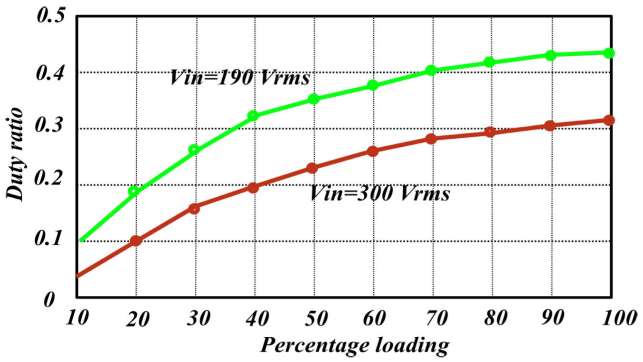


FIGURE 28. Duty ratio vs. percentage load.

at the instant A is shown in Fig. 25. It is visible the current shifts to its new value without any transient overshoot. Fig. 26 shows the transient response of DC bus voltage when the DC bus controller is deactivated at instant A. The DC bus voltage comes into steady state within 3 sec once the control action is reinstated. This shows the effectiveness of the controller. The Fig. 27 shows the ZVS turn ON of switch Q_1. The gate pulse to Q_1 is applied when the voltage across the switch Q_1 is zero, which confirms ZVS operation. All the four switches can be turned ON at ZVS.

The variation of duty ratio with load is depicted in Fig. 28. The proposed topology is capable of regulating DC bus voltage at a constant value in the region between 0%-100% of full load (see Fig. 29). Though the converter's experimental power factor shows a very slight decrease with a decrease in load, the power factor is greater than 0.95 for load variation of 20% to 100% (refer Fig. 30).

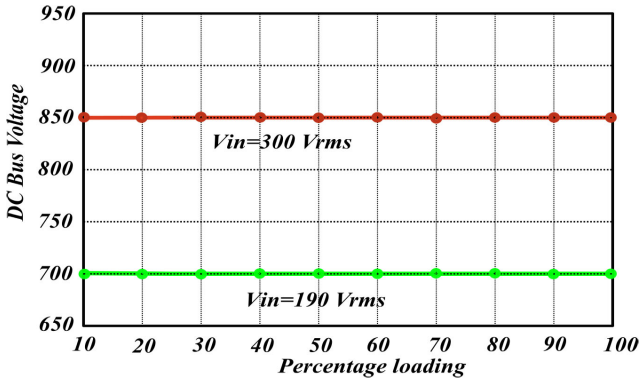


FIGURE 29. DC bus voltage vs. percentage load.

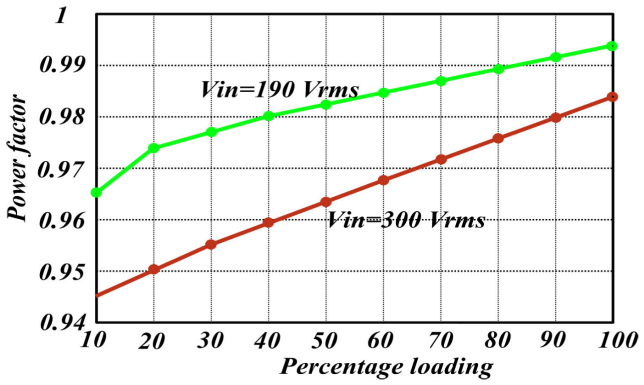


FIGURE 30. Power factor vs. percentage load.

VIII. CONCLUSION

This paper has proposed a three-level flying capacitor based topology for AC/DC LLC resonant converters. The converter has a bridgeless topology which reduces the number of conducting devices. The controller uses a dual control scheme which varies duty ratio and frequency to regulate DC bus and output DC voltages respectively. The converter is designed to operate in discontinuous conduction mode to obtain a near unity power factor without having any active current control techniques. Furthermore, the topology provides low voltage stress, ZVS for all the four switches, and reduces losses. For verification, a 250W, 230V to 48V AC-DC converter prototype has been designed and implemented. The DC bus voltage is held constant at 750V with a peak overshoot of 3.3% even when the load is reduced by 30% from full load.

ACKNOWLEDGMENT

This article is an extension of the work presented in the conference paper "A Three-Level Half-Bridge Flying Capacitor Topology for Single-Stage AC-DC LLC Resonant Converter" [1]. This article was presented at the IEEE International Conference on Power Electronics Drives and Energy Systems (PEDES), December 2018.

REFERENCES

[1] A. K. Peter and J. Mathew, "A three-level half-bridge flying capacitor topology for single-stage AC-DC *LLC* resonant converter," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, Dec. 2018, pp. 1–6.

[2] A. Hillers, D. Christen, and J. Biela, "Design of a highly efficient bidirectional isolated *LLC* resonant converter," in *Proc. 15th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Sep. 2012, pp. DS2b–13.

[3] J.-H. Kim, M.-Y. Kim, C.-O. Yeon, and G.-W. Moon, "Analysis and design of boost-*LLC* converter for high power density AC-DC adapter," in *Proc. IEEE ECCE Asia Downunder*, Jun. 2013, pp. 6–11.

[4] Y. Qiu, W. Liu, P. Fang, Y.-F. Liu, and P. C. Sen, "A mathematical guideline for designing an AC-DC *LLC* converter with PFC," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 2001–2008.

[5] S.-Y. Chen, Z. R. Li, and C.-L. Chen, "Analysis and design of single-stage AC/DC *LLC* resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1538–1544, Mar. 2012.

[6] A. K. Peter, P. M. Amalraj, B. Philip, and J. Mathew, "Design and analysis of an AC-DC *LLC* resonant converter with new bus voltage stabilization technique," in *Proc. IEEE Transp. Electrific. Conf. (ITEC-India)*, Dec. 2017, pp. 1–5.

[7] B. Wang, X. Xin, S. Wu, H. Wu, and J. Ying, "Analysis and implementation of *LLC* burst mode for light load efficiency improvement," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 58–64.

[8] W. Feng, F. C. Lee, P. Mattavelli, D. Huang, and C. Prasantanakorn, "*LLC* resonant converter burst mode control with constant burst time and optimal switching pattern," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2011, pp. 6–12.

[9] Y.-C. Chen, T.-J. Liang, W.-J. Tseng, J.-Y. Lee, and L.-S. Yang, "Design and implementation of *LLC* resonant converter with high efficiency at light load condition," in *Proc. 2nd Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2010, pp. 538–542.

[10] S. Shao, Y. Li, J. Sheng, C. Li, W. Li, J. Zhang, and X. He, "A modular multilevel resonant DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7921–7932, Aug. 2020.

[11] M. S. Agamy and P. K. Jain, "A three-level resonant single-stage power factor correction converter: Analysis, design, and implementation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2095–2107, Jun. 2009.

[12] O. Kirshenboim and M. M. Peretz, "Combined multilevel and two-phase interleaved *LLC* converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.

[13] H. Haga, H. Maruta, and F. Kurokawa, "A comparative study of voltage gain tolerance in conventional and three-level *LLC* converters against circuit variation," in *Proc. IEEE Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Nov. 2016, pp. 153–157.

[14] F. Jin, F. Liu, X. Ruan, and X. Meng, "Multi-phase multi-level *LLC* resonant converter with low voltage stress on the primary-side switches," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 4704–4710.

[15] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 612–622, Sep. 2001.

[16] G. Chen, H. Li, X. Sun, and Y. Wang, "A method for designing resonant tank of half-bridge three-level *LLC* converter," in *Proc. Chin. Autom. Congr. (CAC)*, Nov. 2018, pp. 2312–2316.

[17] H. Haga and F. Kurokawa, "Dynamic analysis of the three-level *LLC* resonant converter for a rectifier in HVDC distribution system," in *Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC)*, Oct. 2015, pp. 1–6.

[18] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level *LLC* series resonant DC/DC converter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 781–789, Jul. 2005.

[19] C.-H. Chang, H.-Y. Chen, C.-T. Cho, and J.-Y. Chiu, "A novel single-stage *LLC* resonant AC-DC converter with power factor correction feature," in *Proc. 6th IEEE Conf. Ind. Electron. Appl.*, Jun. 2011, pp. 2191–2196.

[20] S. Esmailirad, R. Beiranvand, S. Salehirad, and S. Esmailirad, "Analysis of a bridgeless single stage PFC based on *LLC* resonant converter for regulating output voltage," in *Proc. IEEE 31st Int. Conf. Microelectron. (MIEL)*, Sep. 2019, pp. 353–356.

[21] B. Ku, W. Cai, and B. Fahimi, "Low-power *LLC* resonant AC-DC converter for phone charging applications," in *Proc. IEEE Dallas Circuits Syst. Conf. (DCAS)*, Oct. 2016, pp. 1–4.

[22] C.-E. Kim, J.-I. Baek, and J.-B. Lee, "High-efficiency single-stagellcresonant converter for wide-input-voltage range," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7832–7840, Sep. 2017.

[23] M. Ghasemi, R. Beiranvand, and M. Jami, "Analyzing a bridgeless single stage *LLC* resonant PFC converter controlled by frequency and pulse width modulations techniques," in *Proc. 6th Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2015, pp. 89–95.
[24] S. Abdel-Rahman, "Resonant LLC converter: Operation and design," Infineon Technol. North Amer., Durham, NC, USA, Appl. Note AN 2012-09, Sep. 2012. [Online]. Available: https://www.infineon.com/dgdl/Application_Note_Resonant+LLC+Converter+Operation+and+Design_Infineon.pdf?fileId=db3a30433a047ba0013a4a60e3be64a1
[25] H. Choi, "Half-bridge *LLC* resonant converter design using FSFR-series Fairchild power switch (FPST)," Fairchild Semicond., Sunnyvale, CA, USA, Appl. Note AN-4151, 2014.
[26] H. Huang, "Designing an *LLC* resonant half-bridge power converter," in *Proc. Texas Instrum. Power Supply Design Seminar, (SEM)*, vol. 3, 2010, pp. 2010–2011.
[27] B. Yang, "Topology investigation of front end DC/DC converter for distributed power system," Ph.D. dissertation, Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2003.

ANTONY K. PETER (Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from the Mangalam College of Engineering, Kottayam, India, in 2010, and the M.Tech. degree in power electronics from the Sree Narayana Gurukulam College of Engineering, Ernakulam, India, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Government Engineering College, Thrissur, affiliated to APJ Abdul Kalam Technological University. His research interests include power converters and motor drives.

JAISON MATHEW (Senior Member, IEEE) received the B.Tech. degree in electrical engineering from the Rajiv Gandhi Institute of Technology, Kottayam, India, in 1998, the M.Tech. degree in power systems from the College of Engineering Trivandrum, India, in 2001, and the Ph.D. degree in power electronics from the Indian Institute of Science, Bengaluru, in 2014. He is a Faculty Member with the Department of Electrical Engineering, Government Engineering College, Thrissur, India. His research interests include multi-level inverters, motor drives, and power quality.