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In-Depth Design Space Exploration of 26.5-to-29.5-GHz 65-nm CMOS Low-Noise Amplifiers for Low-Footprint-and-Power 5G Communications Using One-and-Two-Step Design Optimization

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ABSTRACT Low-noise amplifiers (LNAs) play a significant role in modern millimeter-wave (mmWave) integrated circuits for fifth-generation (5G) communications systems. However, the proper analysis of their design tradeoffs that allow for a realistic topology comparison is impractical. The many conflicting specifications that must be carefully balanced make the problem intractable. In this paper, the 148-dimensional performance spaces of three 28-GHz LNAs are fully explored for a 65-nm CMOS technology node, using an enhanced electronic design automation tool. One- and two-step many-objective optimizations provide up to 1024 different LNAs for each of the considered topologies, enabling a thorough assessment of their performance tradeoffs. The first optimizes all the design parameters at once. In contrast, the latter optimizes the spiral inductors in a first step. Then, in a second step, it optimizes the remaining parameters. The resulting designs provide new insight on the tradeoffs between gain, noise figure, power, and circuit's footprint for current 5G specifications. Process, voltage, and temperature corners impact the LNAs' performance severely. Still, the optimization shows that proper sizing of these topologies compete with the most-recent mmWave LNAs and can play a role in the challenging 28-GHz band.

INDEX TERMS 5G communication, automatic synthesis, CMOS, low-noise amplifier, many-objective, millimeter-wave.

I. INTRODUCTION

An enormous investment has been made in the past recent years to the rapid development and prototyping of 26/28-GHz transceiver front-end CMOS interfaces to keep up with the fifth-generation (5G) communication systems demands. Notably, the low-noise amplifier (LNA), as the first block in the receiver path, plays a vital role in such a modern low-cost millimeter-wave (mmWave) integrated circuits (IC) for multi-standard transceivers. Furthermore, LNAs have been subject to continuous research efforts to enable base stations with a superior energy efficiency or extended operating time of portable devices. Researchers keep on pushing the boundaries of the LNA's gain, linearity, and low noise figures (NFs), while pursuing a small footprint and minimal power consumption [1]–[4]. In order to aid designers, some analytical methodologies have been used in order to reach initial solutions, however they are transistor-oriented

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and not specification-oriented and therefore the methodologies may not lead to optimal designs directly (e.g., gm/Id methodologies) [5]–[7]. Moreover, such methods became more difficult to apply in modern multi-dimensional design performance spaces. Also, such classical ''experience and trial'' design methods, have long deployment cycles and a realistic analysis of a given topology design tradeoffs for a target application is a cumbersome task, leading to sub-optimal mmWave design at state-of-the-art integration technologies. At lower frequency ranges of the radio spectrum up to several gigahertz, the application of electronic design automation (EDA) tools [8] was critical in exploring complex design spaces. These EDA tools use an optimization engine to interact with the circuit simulator and size the circuits [9]–[18]. However, reports of applying these methodologies to mmWave IC design are almost inexistent, with only a few trials conducted [19]–[21].

This paper applies and adapts the state-of-the-art EDA framework used in [16] to bypass the difficulties faced during the sizing of complex mmWave IC blocks. In this study, three topologies for 26.5-to-29.5-GHz LNAs are considered. The 28-GHz band is selected based on the recommended frequency spectrum for 5G communications [22]. The significant contributions of this work can be summarized as follows: (1) enhancement of an EDA framework to fully optimize 28-GHz LNAs for modern 5G specifications at a 65-nm CMOS technology node; (2) analysis and comparison of the complete tradeoffs between gain, noise figure, power consumption, and circuit's footprint of the different LNAs for 5G specifications, obtained with many-objective optimization runs whose setup is transversal to all studied topologies; (3) unlike most recent research contributions in mmWave sizing optimization that focus on smaller design variable and performance spaces [19]–[21], here, complex 26-to-38-dimensional design variable spaces are used to explore a 148-dimensional performance space, that balances all the design tradeoffs simultaneously between different process, voltage and temperature (PVT) corners without manual intervention; and finally, (4) the advantages of complementing the one-step design with a two-step bottom-up design methodology for mmWave design are studied. The first optimizes all the design parameters at once. The latter optimizes the spiral inductors first, creating a reduced subset of optimized inductor sizing solutions. The second step optimizes the LNA's remaining parameters, considering the inductors from the first step instead of the full design space. This is the first time the two-step design fashion with pre-optimized inductors is applied in mmWave circuits' design to the best of our knowledge.

This document is organized as follows. In Section II, the adopted LNAs are overviewed. In Section III, the optimization framework details are provided. Afterward, in Sections IV and V, the complete transversal setup details for the one- and two-step design fashions, respectively, are outlined. In Section VI, the optimization results are discussed, and in Section VII, the conclusions are addressed.

II. MMWAVE LOW-NOISE AMPLIFIERS

Several distinct topologies of CMOS LNAs are suitable to be used mmWave narrowband receivers. However, in tuned applications, LNA circuits based on the cascode topology are widely used. It provides excellent output-input isolation (reduced reverse transmission). While simultaneously attaining high gain, low NF, low current consumption, good input and output matching, and unconditional stability [1], [23]–[25]. Fig. 1 shows the three LNA topologies used in this work, henceforward designated by LNA1, LNA2, and LNA3. LNA1 and LNA2 are based on the traditional cascode (DC coupled). LNA3 uses an AC-coupled cascode (two-stage cascode). In LNA1 and LNA2, the gate voltage (V_{G1}) of the common-source transistor (M_1) controls the bias. In LNA3, the bias of the transistors (in both stages) is independent of each other. Additionally, the circuits include the input and output signal pads since their shunt capacitances impact the performance.

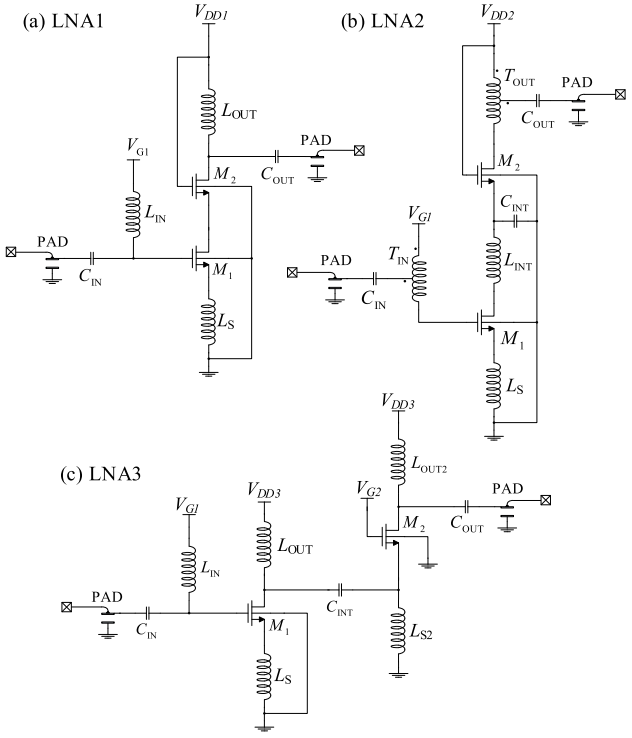


FIGURE 1. LNA schematics of: (a) LNA1, V_{DD1} = 1.2-V; (b) LNA2, V_{DD2} = 1.2-V; and (c) LNA3, V_{DD3} = 0.6-V.

LNA1 is a typical inductively degenerated cascode. L_S is used to obtain a gate input impedance with a real part close to 50 Ω [23], [26] (L_S has the same function in the other two). This LNA uses the shunt inductor (L_{IN}) for bias. In association with the input series capacitance (C_{IN}), L_{IN} allows the LNA to attain the desired input impedance matching under good noise performance. LNA2 uses T-coils (auto-transformers) instead of inductors in its input and output matching circuits. It has a series inductor (L_{INT}) and a shunt capacitor (C_{INT}) between the common-source (M1) and the

common-gate (M_2) transistors. In association with M_1 and M_2 capacitive parasitics, these elements form an artificial T-line allowing it to match the transistors' impedance to each other, improving the gain and noise figure [25]. Since the cascode of LNA3 is AC-coupled, this topology maintains the performance characteristics of the DC-coupled cascode, with the advantage that it works with lower voltage supplies. Therefore, in this work LNA3 will be supplied at $V_{DD3} = 0.6$-V whereas LNA1 and LNA2 will be supplied at $V_{DD1} = V_{DD2} = 1.2$-V. However, its area should be higher than LNA1 and LNA2.

III. OPTIMIZATION FRAMEWORK

Fig. 2 illustrates the general flow of the automatic many-objective simulation-based design methodology. The proposed tool enhances the framework of [16], based on many-objectives, many-constraints evolutionary optimization, to use Cadence's Spectre as the mmWave performance evaluator. The optimization process can follow the one-step or two-step design methodology. Only the topmost loop of Fig. 2 is carried (2nd Step LNA Optimization) in the one-step design fashion. T*he optimization engine proposes P candidate circuit (LNA) sizing solutions*, each being a unique combination of all design variables. The device models provided by the foundry support the change of different dimension parameters. At each iteration, the framework simulates the K test benches (different analysis, corners, etc.) whose netlists are altered for each sizing in P. At this point, custom Python scripts extract the desired measures from the simulations' output (*raw* and mdl-generated files). Additionally, the *measure-processing unit* offers an interface to combine any of the measures, from the same and different test benches, into composed expressions that can be used as target specifications. For example, the figure-of-merit and stability conditions are computed in the measure processing unit.

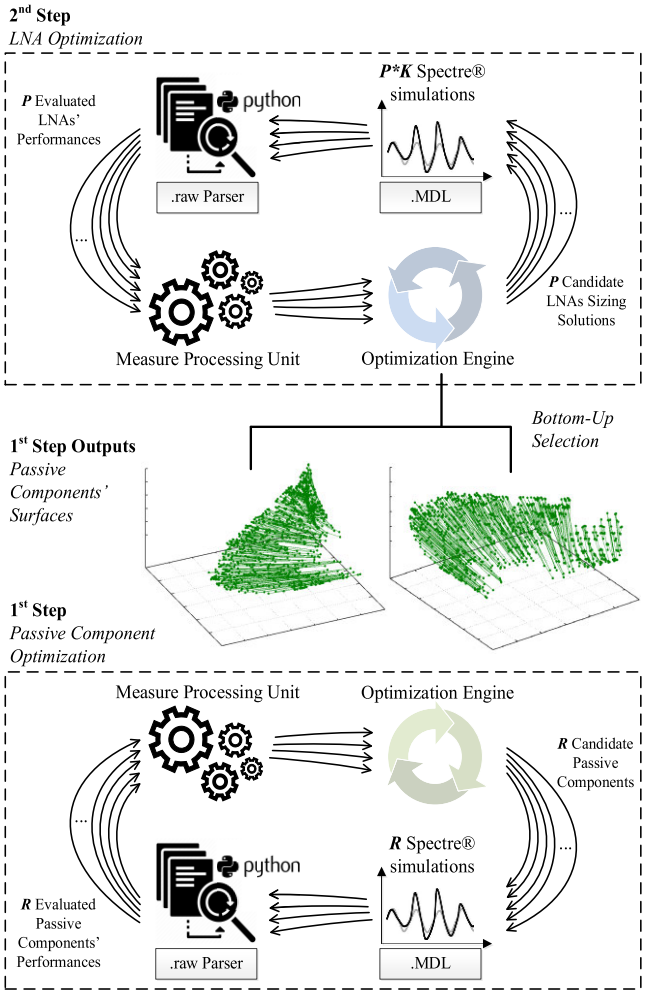


FIGURE 2. The general flow of the RF IC sizing optimization.

Additionally, the two-step design fashion where the bottommost loop of Fig. 2 is carried *a priori* (**1st Step** *Passive Component Optimization*) is also studied. The topmost loop's exact optimization mechanism is taken, but only the passive components are optimized, one per optimization. The output (**1st Step Outputs**) is a Pareto optimal surface of inductors made available before any circuit optimization

Eeckelaert *et al.* [32] introduced the concept of using Pareto fronts for electronic design automation. Later it was successfully applied by several authors to hierarchical bottom-up sizing of analog, mixed-signal [32], [34], and RF circuit classes [33]. Only in [12] the authors propose this bottom-up design fashion for inductor design but at lower frequency ranges. In [12], the desired inductor topology was not readily available in the process design kit (PDK). The optimization loop interacted with an electromagnetic (EM) simulator to obtain the Pareto front with the best inductors for the problem defined, significantly speeding up the second step. In this work, this is not the case.

The foundry's inductor models are used to simulate the different choices of design parameters, as the modeling error reported on the documentation of the PDK was considered satisfactory. Therefore, from the adopted PDK, standard spiral inductors in ultra-thick metal were selected, and for the T-coils, only symmetric center-tapped spiral inductors in ultra-thick metal were assumed, as no asymmetric PCELL for the T-coil is provided. Nonetheless, the major goal is not to accelerate the simulation and bypass the EM simulator but to provide the **2nd Step** *LNA Optimization* only a reduced inductor design space during circuit sizing. This approach was also reported to achieve a significant speedup convergence for circuits working on 2.4GHz and 5GHz. Given the number of inductors used within each LNA topology, i.e., from 3 to 5, such a speedup can be significant. However, the 1st step does not contemplate interactions that can be significant between the inductor's parasitic devices and the other circuit's devices.

IV. ONE-STEP DESIGN FASHION SETUP

In this section, the complete optimization variables, PVT corners, design specifications, and optimization objectives for the one-step design fashion are fully detailed.

A. OPTIMIZATION VARIABLES

The netlists of the three mmWave LNAs were fully parameterized (inductors, capacitors, and transistors). Table 1 shows the range and grid of the 26 optimization variables of LNA1. Where **lin_ir**, **lin_nt**, **lin_s**, **lin_w** and **lin_gd** are the inner radius, number of turns, spacing between conductors, conductor width and guard ring distance, respectively, of the *standard spiral inductor in ultra-thick metal* (STDSI) L_{IN}; **ls_ir**, **ls_nt**, **ls_sp**, **ls_w** and **ls_gd** the inner radius, number of turns, spacing between conductors, conductor width and guard ring distance, respectively, of the STDSI L_S; **lout_ir**, **lout_nt**, **lout_s**, **lout_w** and **lout_gd** the inner radius, number of turns, spacing between conductors, conductor width and guard ring distance, respectively, of the STDSI L_{OUT}; **cin_l** and **cin_w** are the length and width of the *RF* metal-insulator-metal (*MIM*) *capacitor* C_{IN}; **cout_l** and **cout_w** are the length and width of the *RF MIM capacitor* C_{OUT}; **m1_l**, **m1_w** and **m1_nf** are the length per finger, width per finger and number of fingers, respectively, of the *NMOS RF transistor* M_1; **m2_l**, **m2_w** and **m2_nf** are the length per finger, width per finger and number of fingers, respectively, of the *NMOS RF transistor* M_2; and, $\mathbf{V_{G1}}$ is the gate bias voltage ($\mathbf{V_{G2}} = \mathbf{V_{G1}}$).

The 9 additional optimization variables for the LNA2 are described in Table 2. Where **lint_ir**, **lint_nt**, **lint_s**, **lint_w,** and **lint_gd** are the inner radius, the number of turns, spacing between conductors, conductor width, and guard ring distance, respectively, of the STDSI L_{INT}; **cint_l** and **cint_w** are the length and width of the *RF MIM capacitor* C_{INT}; and, **lin_nt** and **lout_nt** override the definition of Table 1, as L_{IN} (T_{IN}) and L_{OUT} (T_{OUT}) in the LNA2 are T-coils, i.e., *center-tapped spiral symmetric inductors in ultra-thick metal* (SSYMI).

TABLE 1. Ranges/Grid of the 26 optimization variables of LNA1.

Variable	Units	Min.	Grid	Max.
lin_iradius, ls_iradius, lout_iradius	µm	15	1	90
lin_nturns, ls_nturns, lout_nturns	-	0.5	1	5.5
lin_spacing, ls_spacing, lout_spacing	µm	2	0.1	4
lin_width, ls_width, lout_width	µm	3	0.1	30
lin_gdis, ls_gdis, lout_gdis	µm	10	5	50
cin_length, cin_width, cout_length, cout_width	µm	4	0.1	40
m1_length, m2_length	nm	60	10	240
m1_width, m2_width	µm	0.6	0.2	6
m1_nf, m2_nf	-	1	1	32
V_{G1}	V	0.4	0.01	1.2

Finally, the 12 additional optimization variables for the LNA3 are described in Table 3, where **ls2_ir**, **ls2_nt**, **ls2_s**, **ls2_w,** and **ls2_gd** are the inner radius, number of turns, spacing between conductors, conductor width, and guard ring distance, respectively, of the STDSI L_{S2}; **lout2_ir**, **lout2_nt**, **lout2_s**, **lout2_w,** and **lout2_gd** are the inner radius, number of turns, spacing between conductors, conductor width and guard ring distance, respectively, of the STDSI L_{OUT2}; and, **cint_l** and **cint_w** are the length and width of the *RF MIM capacitor* C_{INT}.

TABLE 2. Ranges/Grid of the additional variables of the LNA2 (Refer to table i for the remaining variables, 35 in total).

Variable	Units	Min.	Grid	Max.
lint_iradius	µm	15	1	90
lin_nturns, lout_nturns	-	1	1	6
lint_nturns	-	0.5	1	5.5
lint_spacing	µm	2	0.1	4
lint_width	µm	3	0.1	30
lint_gdis	µm	10	5	50
cint_length, cint_width	µm	4	0.1	40

TABLE 3. Ranges/Grid of the additional variables of the LNA3 (Refer to table i for the remaining variables, 38 in total).

Variable	Units	Min.	Grid	Max.
ls2_iradius, lout2_iradius	µm	15	1	90
ls2_nturns, lout2_nturns	-	0.5	1	5.5
ls2_spacing, lout2_spacing	µm	2	0.1	4
ls2_width, lout2_width	µm	3	0.1	30
ls2_gdis, lout2_gdis	µm	10	5	50
cint_length, cint_width	µm	4	0.1	40

B. PERFORMANCE METRICS AND PVT CORNERS

For each LNA, the simulations are carried to extract the S-parameters, NF at 26.5/28.0/29.5-GHz, the power consumption at DC, and the input-referred third-order interception point (IIP3). Additionally, the Rollet stability factor, Kf, and the intermediate-term, B1f, defined as:

$$Kf = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}|\,|S_{21}|} \tag{1}$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2 \tag{2}$$

where,

$$\Delta = |S_{11}S_{22} - S_{21}S_{12}| \tag{3}$$

are computed for 26.5/28.0/29.5-GHz using the measure-processing interface. Additionally, to ensure the robustness of the solutions and account for PVT variations during the many-objective optimization, as a proof-of-concept, additional test-benches were added to the previous typical (TT) setup for each LNA: slow/slow (SS) process corner library, fast/fast (FF) process corner library, supply voltage set to 50-mV below standard supply (VDD-50mV), supply voltage set to 50-mV above standard supply (VDD+50mV), temperature set for 0°C (T0°C), and, temperature set for 70°C (T70°C). The process corner libraries provided by the foundry affect MOSFETs, capacitors, and inductors. On a different node or operating conditions, the corners to include may vary. Still, the methodology supports any number of PVT variations. It requires only a minimal setup effort since the setup is transversal to all LNAs under study.

C. DESIGN SPECIFICATIONS

We choose to accept only solutions with S11 and S22 below −12-dB, gain above 10-dB, NF below 7-dB, power below 50-mW, and Kf and B1f values that ensure unconditional stability. Additional constraints were also set to ensure a

flat gain above and below the 28-GHz. Table 4 shows the complete set of design specifications. These 148 optimization constraints spread through the different PVT corners. The optimizer does not produce sizing solutions that do not meet all the specifications in all corners.

TABLE 4. Specifications transversal to all mmWave LNA topologies under study.

Specifications	Units	Target
S11@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0ºC, T70ºC}	dB	≤ -12
S22@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0ºC, T70ºC}	dB	≤ -12
S21@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0ºC, T70ºC}	dB	≥ 10
NF@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0ºC, T70ºC}	dB	≤ 7
IIP3 {TT}	dBm	≥ -15
power@DC {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, 0ºC, 70ºC}	W	≤ 0.05
flat gain up[1] {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, 0ºC, 70ºC}	dB	≤ 1.5
flat gain down[2] {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, 0ºC, 70ºC}	dB	≤ 1.5
Kf@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, 0ºC, 70ºC}	-	≥ 1
B_{1f}@26.5GHz/28.0GHz/29.5GHz {TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, 0ºC, 70ºC}	-	≥ 0

[1] | S21@29.5GHz - S21@28.0GHz |; [2] | S21@28.0GHz - S21@26.5GHz |

D. OPTIMIZATION OBJECTIVES

The last step of the setup is the definition of the optimization objectives. Four objectives for the constrained many-objective optimization were set, as outlined in Table 5. These are: maximize the gain at 28.0-GHz, minimize the NF and power consumption at 28.0-GHz, and minimize the circuit's footprint. The footprint metric offers an estimate of the floorplan area occupied during layout design, given by the sum of the inductors' area of the tentative sizing solution.

TABLE 5. Optimization objectives transversal to all mmWave LNA topologies under study.

Objectives	Units	Target
S21@28.0GHz {TT}	dB	Maximize
NF@28.0GHz {TT}	dB	Minimize
power@DC {TT}	W	Minimize
circuit footprint	m^2	Minimize

V. TWO-STEP DESIGN FASHION SETUP

In this section, the optimization setup for the two-step design fashion is fully detailed.

A. PASSIVE COMPONENTS' OPTIMIZATION SETUP

In the two-step design fashion, the passive components are optimized *a priori*. For use in LNA1 and LNA3, an STDSI is parameterized. Table 6 details the range and grid of its 5 optimization variables, where **stdsi_ir**, **stdsi_nt**, **stdsi_s**, **stdsi_w,** and **stdsi_gd** are its inner radius, number of turns, the spacing between conductors, conductor width, and guard ring distance, respectively. Additionally, LNA2 uses T-coils (SSYMIs). This component is parameterized separately in two different ways depending on how its center tap connection is made to the remaining circuitry. When it is connected as L_{IN} it is designated by $SSYMI_{OUT-0-IN}$, and when it is connected as L_{OUT} it is designated $SSYMI_{IN-0-OUT}$. As illustrated in Fig. 3, the evaluation of the input and output central-tapped symmetric spiral inductors of the LNA2 use traditional 2-port characterization. This is possible since one of the terminals of the T-coils can be considered as an AC ground. Table 7 details the range and grid of the 5 optimization variables of the SSYMI inductive elements, where **ssymi_ir**, **ssymi_nt**, **ssymi_s**, **ssymi_w,** and **ssymi_gd** are its inner radius, number of turns, the spacing between conductors, conductor width and guard ring distance, respectively.

TABLE 6. Ranges/Grid of the 5 optimization variables of STDSI.

Variable	Units	Min.	Grid	Max.
stdsi_ir	µm	15	1	90
stdsi_nt	-	0.5	1	5.5
stdsi_s	µm	2	0.1	4
stdsi_w	µm	3	0.1	30
stdsi_gd	µm	10	5	50

TABLE 7. Ranges/Grid of the 5 optimization variables of SSYMI.

Variable	Units	Min.	Grid	Max.
ssymi_iradius	µm	15	1	90
ssumi_nturns	-	1	1	6
ssymi_spacing	µm	2	0.1	4
ssymi_width	µm	3	0.1	30
ssymi_gdis	µm	10	5	50

For each inductor type, an *sp* analysis is carried from 100-kHz to 29.5-GHz. It is used to compute its inductance *L* and quality factor *Q*. Therefore, three objectives for the constrained many-objective optimization were set, these are: maximize the *L* at 29.5-GHz, maximize the Q at 29.5-GHz and minimize the inductor's footprint. It is important to note that additional specifications can also be chosen, e.g., ensure some *L* flatness or specific *Q* evolution through the band. Nonetheless, for a direct comparison with the one-step design fashion, the inductors' optimizations are left unconstrained.

B. PASSIVE COMPONENTS' SURFACES

The optimization of the inductors was carried with populations of 1000 elements for 1000 generations each. The maximum and minimum values found are shown in Table 9, and the projections L@29.5GHz *versus* Q@29.5GHz of the non-dominated solutions are illustrated in Figures 4 and 5 for STDSI and SSYMI, respectively.

TABLE 8. Specifications and objectives transversal to all inductor topologies under study.

Objectives	Units	Target
L@29.5GHz	H	Maximize
Q@29.5GHz	-	Maximize
inductor footprint	m^2	Minimize

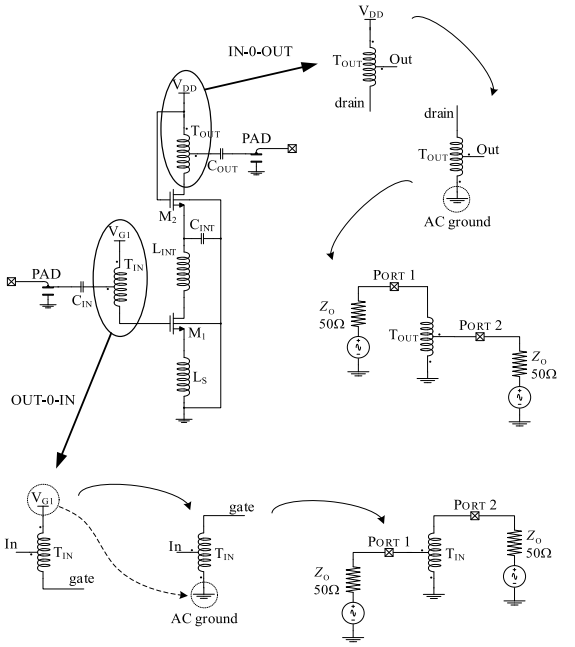


FIGURE 3. OUT-0-IN and IN-0-OUT characterization process of the LNA2's T-coils.

TABLE 9. Minimum and maximum values found for the optimizations of the STDSI and SSYMI.

		STDSI	$SSYMI_{OUT-0-IN}$	$SSYMI_{IN-0-OUT}$
#non-dominated solutions		962	987	988
L@29.5GHz (pH)	Min.	55.8	42.7	22.5
	Max.	7529.1	2609.6	382.4
Q@29.5GHz (-)	Min.	0.905	0.853	12.827
	Max.	54.992	46.239	144.86
Footprint (mm^2)	Min.	0.001	0.002	0.002
	Max.	0.027	0.038	0.177

C. 2nd STEP VARIABLES, METRICS, SPECIFICATIONS, AND OBJECTIVES

In a two-step design fashion, as explained in Section III, the **2nd Step** *LNA Optimization* only has access to a reduced inductor design space to use during circuit sizing. Therefore, for LNA optimization, only the inductor-related design variables of Tables 1, 2, and 3 are changed. For example, instead of searching in the full **lin_ir**, **lin_nt**, **lin_s**, **lin_w,** and **lin_gd** design space of inductor L_{IN}, which represents ∼23M different combinations ($76 \times 6 \times 21 \times 271 \times 9$), the search is made in terms of L@29.5GHz, Q@29.5GHz and *footprint* only from the 962 inductors of Fig. 4. Additionally, the performance metrics and PVT corners of Section IV.B, design

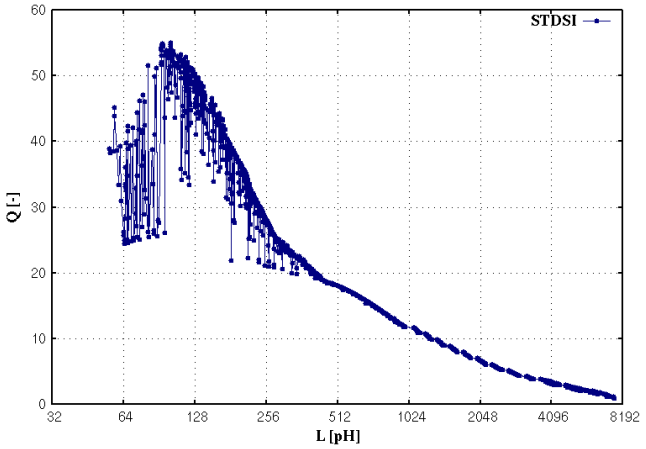


FIGURE 4. Projection Q@29.5GHz versus L@29.5GHz of the 962 non-dominated sizing solutions obtained with the optimization of STDSI.

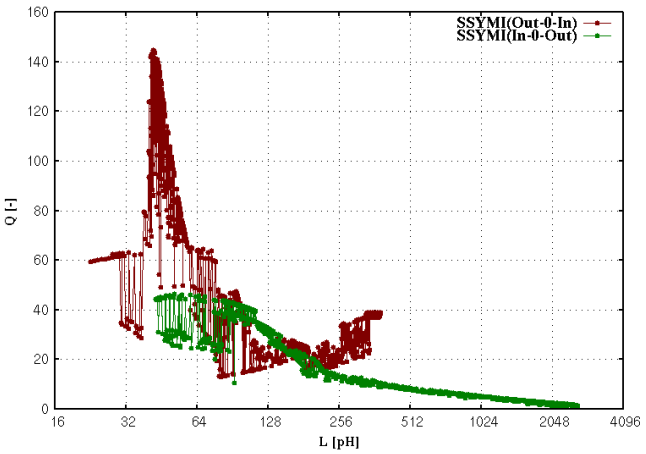


FIGURE 5. Projection Q@29.5GHz *versus* L@29.5GHz of the 987 and 988 non-dominated sizing solutions obtained with the optimizations of SSYMI.

specifications of Section IV.C, and optimization objectives of Section IV.D are kept the same for the two-step design fashion.

VI. RESULTS & DISCUSSION

The optimization setups detailed in Sections IV and V were used to study each LNAs with and without PVT corners, and also, the advantages of using combined one-and-two-step design fashions, the latest with pre-optimized inductor surfaces.

A. OPTIMIZATIONS (OPT. TT) USING ONE-STEP DESIGN FASHION

The optimizations without PVT corners, i.e., only TT, and using the one-step design fashion were carried with populations of 1024 elements optimized through 1000 generations. The three LNAs were able to satisfy all Table 4 design specifications, and their optimization provided approximately 1024 non-dominated sizing solutions each. The maximum and

minimum values found are shown in Table 10, and projections of the non-dominated solutions are illustrated in Fig. 6, namely, NF *versus* gain, power *versus* gain, and circuits' footprint *versus* gain tradeoffs.

TABLE 10. Minimum and maximum values found for the Opt. TT and Opt. Crn with a one-step design fashion (1024/1000).

One-Step Design Fashion		$LNA1_{1024/1000}$ One-Step		$LNA2_{1024/1000}$ One-Step		$LNA3_{1024/1000}$[2] One-Step	
		Opt. TT	Opt. PVT[1,3]	Opt. TT	Opt. PVT[3]	Opt. TT	Opt. PVT[3]
#non-dominated solutions		1023	1024	1024	1024	1024	298
S21@28.0G Hz (dB)	Min.	10.51	10.97	10.50	11.06	10.33	11.25
	Max.	11.41	11.26	11.65	11.57	12.73	12.25
NF@28.0 GHz (dB)	Min.	2.93	3.02	3.25	3.49	2.76	2.98
	Max.	3.55	3.35	4.49	4.04	4.35	3.81
power@ DC (mW)	Min.	9.99	17.71	17.92	21.75	4.06	9.86
	Max.	20.10	21.43	27.18	25.21	19.88	17.57
Footprint (mm^2)	Min.	0.012	0.016	0.016	0.019	0.029	0.056
	Max.	0.029	0.032	0.046	0.034	0.097	0.087

[1] With design specification of S22@26.5GHz/29.5GHz{FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0ºC, T70ºC} relaxed by 20%;

[2] VDbias = 0.6V; [3] Non-dominated solutions obtained with Opt. TT used as initial population.

B. OPTIMIZATIONS WITH PVT CORNERS (OPT. PVT) USING ONE-STEP DESIGN FASHION

The optimizations without PVT corners, i.e., TT, FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0°C, and T70°C, and using the one-step design fashion were carried with populations of 1024 elements optimized through 1000 generations, and, starting from the fronts obtained in Section VI.A.

From these optimizations, LNA2 and LNA3 were able to satisfy all design specifications of Table 4, and their optimization provided 1024 and 298 non-dominated sizing solutions, respectively. LNA1 attained no feasible solutions, and thus, a new optimization was carried with the specification of S22 relaxed by 20% on the extremes of the band, i.e., 26.5/29.5-GHz for the FF, SS, V_{DD}-50mV, V_{DD}+50mV, T0°C, and T70°C corners, which ultimately provided 1024 non-dominated sizing solutions. The summary of these runs is also shown in Table 10, and the projections of the non-dominated solution superimposed in Fig. 6. Each optimization with PVT corners took approximately 154 hours in an Intel E5-2630-v3@2.40GHz workstation using 4 Cadence's Spectre licenses for parallel evaluation.

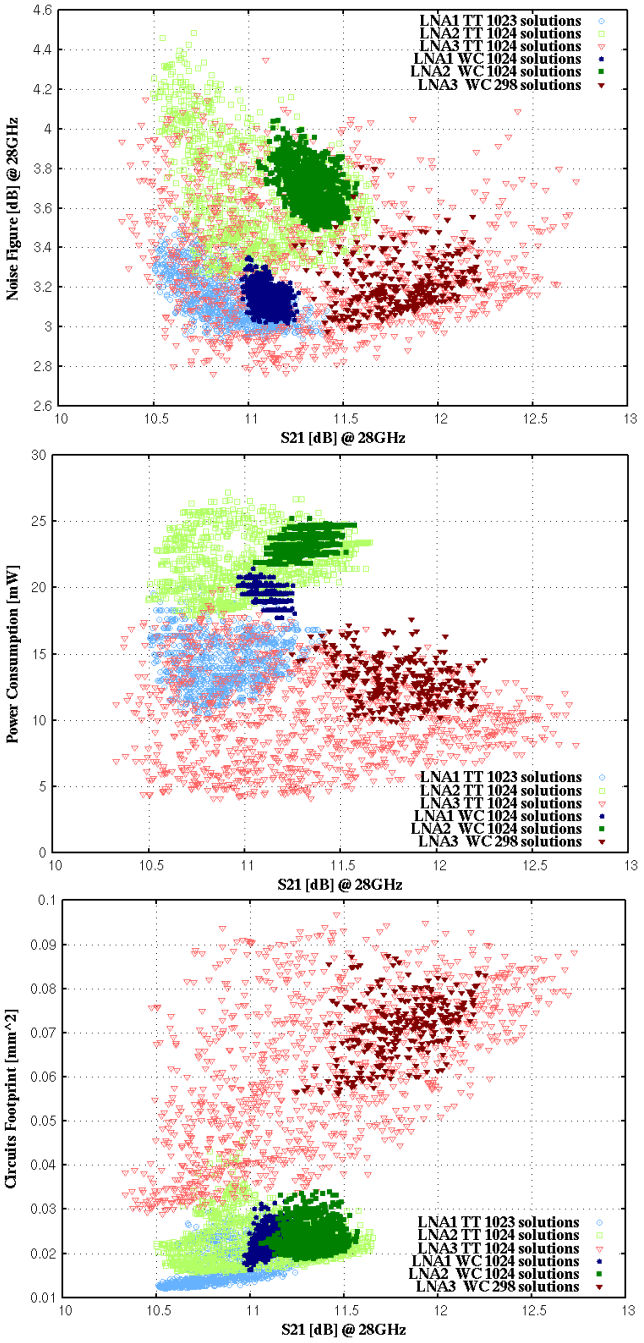


FIGURE 6. Projections of the non-dominated sizing solutions obtained with the many-objective optimizations without PVT corners, i.e., TT only, and optimizations with PVT corners.

C. PERFORMANCE COMPARISON USING ONE-STEP DESIGN FASHION: OPT. TT VERSUS OPT. CRN

By observing the fronts of Fig. 6 obtained with the one-step design fashion optimizations, the performance space of LNA3 dominates the two remaining LNAs, with up to ∼6% and ∼59% of NF and power reduction, respectively, to LNA1, and, up to 9% improvement of gain to LNA2. The drawback of LNA3 is the circuit footprint, whose estimation occupies more than ∼1.8 times the area of LNA2. As observable by Table 10 and Fig. 6, the introduction of PVT corners during optimization resulted in a significant increase in the minimum NF and reduced the maximum gain values found. Power consumption is considerably degraded in corners, especially for LNA1 and LNA3, presenting sub-10mW solutions pre-PVT corners. This is because the optimization engine is forcing the fulfillment of the 148 constraints of Table 4, and thus, by ensuring that the specifications are met on the edges of the band for the FF, SS, V_{DD}-50mV, V_{DD}+50mV,

TABLE 11. Detailed performances of extremes solutions of $LNA3_{1024/1000}$.

Measure/Corner		Units	Max. S21		Min. NF		Min. power	
			Opt. TT	Opt. PVT	Opt. TT	Opt. PVT	Opt. TT	Opt. PVT
S11@28.0GHz	TT	dB	-26.6	-19.4	-17.9	-17.1	-20.5	-19.9
S22@28.0GHz	TT	dB	-16.1	-26.8	-19.4	-23.7	-19.4	-18.5
S21@ 28.0GHz	TT	dB	**12.73**	**12.25**	11.09	11.42	11.34	11.79
	SS		n/d	11.61	n/d	10.91	n/d	10.85
	FF			12.23		11.23		11.63
	V_{DD}-50mV			11.95		11.17		11.56
	V_{DD}+50mV			12.50		11.63		11.99
	T0ºC			12.73		11.85		12.23
	T70ºC			11.47		10.72		11.08
NF@ 28.0GHz	TT	dB	3.73	3.18	**2.76**	**2.98**	3.67	3.38
	SS		n/d	3.14	n/d	3.06	n/d	3.49
	FF			3.52		3.10		3.64
	V_{DD}-50mV			3.21		3.01		3.41
	V_{DD}+50mV			3.16		2.95		3.35
	T0ºC			2.89		2.69		3.05
	T70ºC			3.68		3.46		3.92
IIP3	TT	dBm	-2.93	-0.86	2.81	2.43	-5.91	0.50
power@ DC	TT	mW	8.12	14.52	12.64	15.56	**4.06**	**9.86**
	SS		n/d	10.55	n/d	10.80	n/d	6.14
	FF			18.98		20.96		14.35
	V_{DD}-50mV			12.99		13.88		8.75
	V_{DD}+50mV			16.09		17.29		11.02
	T0ºC			14.58		15.52		9.66
	T70ºC			14.42		15.60		10.12
circuit footprint		mm^2	0.088	0.083	0.074	0.086	0.087	0.086

TABLE 12. Minimum and maximum values found for the Opt. TT with a one- and two-step design fashions (1024/2000).

		$LNA1_{1024/2000}$			$LNA2_{1024/2000}$			$LNA3_{1024/2000}$[1]		
		Opt. TT			Opt. TT			Opt. TT		
		One-Step	Two-Step	Diff.	One-Step	Two-Step	Diff.	One-Step	Two-Step	Diff.
#non-dominated solutions		699	1021	-	1024	1024	-	1024	1024	-
S21@28.0GHz (dB)	**Min.**	10.60	10.59	0%	10.52	10.59	+1%	10.24	10.41	+2%
	Max.	11.50	11.47	0%	11.79	10.92	-7%	12.86	12.44	-3%
NF@28.0GHz (dB)	**Min.**	2.98	2.94	-1%	3.24	3.61	+10%	2.77	2.82	+2%
	Max.	3.49	3.38	-3%	4.68	4.35	-7%	4.41	4.42	0%
power@DC (mW)	**Min.**	10.62	10.57	0%	17.89	18.59	+4%	3.08	4.58	+33%
	Max.	18.65	18.51	-1%	28.29	20.54	-38%	18.74	18.51	-1%
Footprint (mm^2)	**Min.**	0.015	0.007	-53%	0.014	0.008	-43%	0.027	0.015	-44%
	Max.	0.055	0.031	-44%	0.060	0.227	+278%	0.108	0.023	-79%

[1] VDbias = 0.6V.

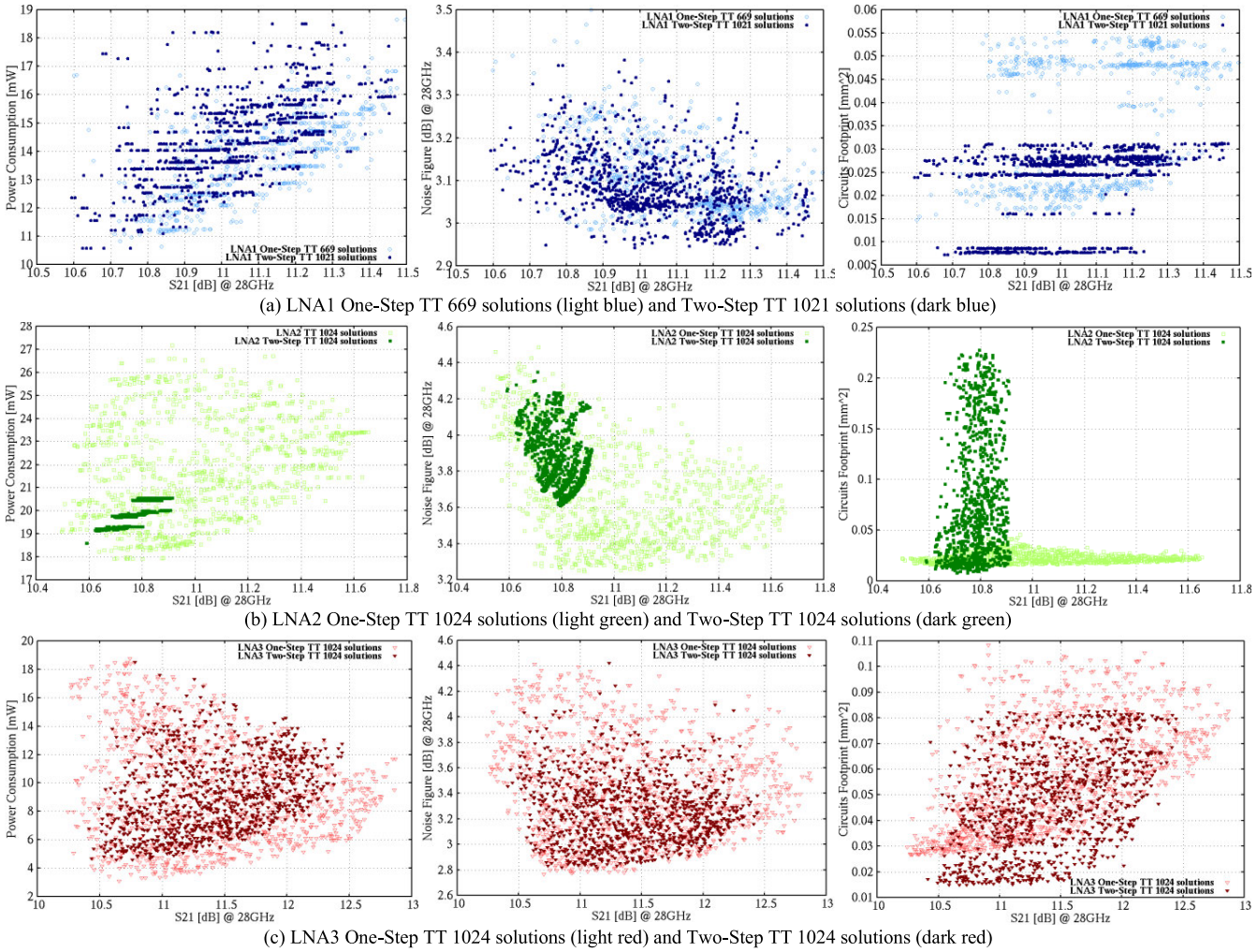
T0°C, and T70°C corners, it results in sizing solutions whose TT performances are degraded. Nonetheless, this shows the three LNAs' expected performance space degradation in worst-case conditions, whose tradeoffs of Fig. 6 follow the same trends observed on TT only. The detailed performances of six different sizing solutions of LNA3 are highlighted in Table 11, i.e., the minimum extreme solutions of NF, power, and gain, achieved in both optimizations with and without PVT corners.

D. TYPICAL OPTIMIZATIONS (OPT. TT) USING TWO-STEP DESIGN FASHION

To study the advantages of using a combined one-and-two-step design fashion, the optimizations without PVT corners, i.e., only TT, were carried with populations of 1024 elements optimized through 2000 generations, using the non-dominated surfaces of Figures 4 and 5 as inductors' design spaces. Longer runs are used here to study the convergence of each of the optimization objectives and the feasibility. The three LNAs were able to satisfy all Table 4 design specifications, and their optimization provided approximately 1024 non-dominated sizing solutions each. The maximum and minimum values found are shown in Table 12. The projections of the non-dominated solutions are illustrated in Fig. 7, namely, NF *versus* gain, power *versus* gain, and circuits' footprint *versus* gain tradeoffs.

E. OVERALL RESULTS OF THE COMBINED ONE-AND-TWO-STEP DESIGN FASHIONS

For a fair experiment, using the one-step design fashion, the LNAs were re-optimized with 1024 elements through 2000 generations in the same conditions of Section VI.A,



(a) LNA1 One-Step TT 669 solutions (light blue) and Two-Step TT 1021 solutions (dark blue)

(b) LNA2 One-Step TT 1024 solutions (light green) and Two-Step TT 1024 solutions (dark green)

(c) LNA3 One-Step TT 1024 solutions (light red) and Two-Step TT 1024 solutions (dark red)

FIGURE 7. **Projections of the non-dominated sizing solutions without PVT corners, i.e., TT only, obtained with the one- and two-step design fashions.**

but, starting from the same random initial populations used in Section VI.D for the two-step design fashion (only the inductor-related design variables differ). The resulting projections are superimposed in Fig. 7, and maximum and minimum values are found in Table 12.

By observing the results in Table 12, it is possible to confirm that the two-step design fashion was capable of attaining gain, NF, and power the results of the one-step design fashion (complete inductor design spaces). The significant exception (variations above 10%) is the minimum power found of LNA3, where the two-step design fashion only found a solution with 33% higher power. These limitations may arise from the interactions between the inductors and the other circuit devices that were not accounted for during the inductor optimization. Still, an inductor design space larger than the one adopted, which contains only 962 different inductors, could, in theory, enable the two-step design fashion to reach these power consumption levels. However, in terms of footprint, the gains of the two-step design fashion are immense, as this approach was capable of reducing approximately 53%, 43%, and 44% minimum footprint values found for LNA1, LNA2, and LNA3, respectively. This improvement in the area results from the inductors' design space containing devices that were previously optimized towards minimum footprint, and thus, competitive inductors' configurations for similar L and Q with the larger area were filtered out from the circuit-level optimization. This is also observable in the non-dominated fronts of Fig. 7 for LNA1 and LNA3, where the circuits' footprint *versus* gain fronts of the two-step design fashion present several well-defined steps (i.e., several different competing sizing solutions with the same footprint value) instead of the stochastic behavior of the one-step design fashion. In LNA2, these footprint steps are not present, as the inductors are selected from three distinct design spaces, i.e., STDSI, $\text{SSYMI}_{\text{OUT}-0-\text{IN}}$, and $\text{SSYMI}_{\text{IN}-0-\text{OUT}}$.

It is also important to note that the two-step design fashion is not trivial to adopt, especially in mmWave circuits and systems where a slight change in device value or parasitics can highly affect a circuit's performance. For more complex devices, such as T-coils (or integrated transformers), where

TABLE 13. Performance comparison with state-of-the-art (2016-2020) single-stage mmWave LNAs.

Ref., Year	Node (nm)	Gain (dB)	Freq (GHz)	-3-dB BW (GHz)	NF (dB)	IP1dB (dBm)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FOM1 (dB/mW)	FOM2 (W^{-1}) [4]
[27], 2016	45 SOI	8.5	27.0	12	3	-4	--	12.4	0.16	0.69	574
[24], 2018	45 SOI	12.8	26.5	17	1.4	-5	5	15	0.3	0.85	3340
[29], 2019	22 FDSOI	12	26.5	15.1	1.46	-7.6	3	9.8	0.12	1.22	4047
[2], 2019	45 SOI	8.5	28.5	12	2.7	-3	--	12	0.15	0.71	684
[28][1], 2019	65 Bulk CMOS	12.5	24.5	25.4	3.7	-11.8	--	5.4	0.25	2.31	2450
[25], 2020	22 FDSOI	10.2	26.7	11.2	2.2	-3	7.5	15	0.12	0.68	1058
LNA1 HighG[2]	65 Bulk CMOS	11.41	28.0	8.86	3.1	-9.8	0.45	16.5	--	0.69	805
LNA1 LowNF[2]		10.8		10.44	2.82	-8.87	2.15	16.16	--	0.67	814
LNA1 LowP[2]		10.74		8.78	3.15	-10	0.59	9.99	--	1.08	1114
LNA2 HighG[2]	65 Bulk CMOS	11.7	28.0	10.1	3.57	-9.2	1.26	23.4	--	0.50	496
LNA2 LowNF[2]		10.9		11	3.25	-8.8	1.83	21.34	--	0.51	518
LNA2 LowP[2]		10.7		12.24	3.64	-8.3	2.46	17.92	--	0.60	500
LNA3 HighG[2]	65 Bulk CMOS	12.73	28.0	6.91	3.73	-14	-1.68	8.12	--	1.57	1697
LNA3 LowNF[2]		11.1		11.2	2.76	-9.63	2.48	12.64	--	0.88	1148
LNA3 LowP[2]		11.3		7.6	3.67	-13.1	-1.86	4.06	0.28	2.78	2502

[1]Post-layout; [2]Simulation with input and output signal pads.

the optimal device performance are not so directly defined and depend on how the device is excited and interacts with the remaining circuitry, the usage of two-step methodologies undertakes a certain risk, as seen in LNA2 with a considerably shorter design space coverage. Its fast convergence characteristics are still guaranteed, which is an important aspect, but further optimization within the entire T-coil design space may be needed for a fine improvement of the results. Both design fashions have their advantages, and their combination allows for an in-depth exploration of each LNAs' design space.

F. COMPARISON WITH STATE-OF-THE-ART LNAS

Table 13 compares the key performance parameters of extreme solutions - high gain (HighG), low noise figure (LowNF), and low power (LowP) variants - of LNA1, LNA2, and LNA3 with other state-of-the-art single-stage single-ended LNAs, all covering the same interest band but with the usage of different technologies, topologies, and approaches to maximize their performance. LNAs reported in [27] (45-nm CMOS SOI), and [29] (22-nm CMOS SOI) use cascode inductively degenerated source topologies with the traditional gate inductor to attain the desired input impedance match. The inductive source degeneration in [29] is accomplished with a ground-shielded transmission line. The topology used in these LNAs is similar to the one used in LNA1, differing only in the input matching circuit topology. The LNA in [28] (65-nm CMOS) uses a current-reused topology with two common-source (CS) transistors stacked together. Moreover, the LNA employs techniques to improve gain and input impedance match for wideband operation using two transformers. In [25] (22-nm CMOS SOI), the LNA uses a cascode based topology with an input transformer to enhance the gain, input impedance matching, and noise performance. It should be noted that all the LNAs reported in Table 13, except [28], which uses a 65-nm CMOS technology similar to the one employed in this work, use more advanced CMOS Silicon-On-Insulator (SOI) technologies of smaller dimensions (lower nodes) than the one used to develop the LNA1, LNA2 and LNA3.

As can be seen in Table 13, the performances of all variants of the LNA1 and LNA3 are in line with the ones reported by the other works. Due to the power consumption, the same observation does not apply to the variants of the LNA2. However, all the other performance characteristics of the LNA2 variants are in the same range of values that the other amplifiers. The higher power consumption of the LNA2 variants may be related to using only symmetric type T-coils during the sizing optimization procedure, limiting the variable space. Consequently, to attain all the optimizations objectives and restrictions, the electric current must be increased to maintain the optimal transistor sizes. Adding a new degree of freedom for the center tap point could help to improve the results. However, this option was readily discarded, first, due to the inexistence of asymmetric T-coils in the technology PDK and also because one of the objectives of this work was to show that it is possible to design state-of-the-art LNAs using only the components available in foundries PDKs. Thus, the approach followed in this work leads to a minimum design effort as it is not necessary, first, to characterize the technology (silicon substrate) and then perform time-consuming electromagnetic simulations, especially in a trial-and-error design methodology. Due to the higher power consumption of the LNA2 variants, when compared to those of the other amplifiers, they will not be considered in the detailed performance comparison of the LNAs of Table 13 that follows in the next paragraphs.

The gains of all variants of the LNA1 and LNA3 (10.74-dB to 12.73-dB) are near the maximum gain value (12.8-dB)

presented in Table 13. It should be noted that this is attained when the power consumptions of the LNA1 and LNA3 variants (4.06-mW to 16.5-mW) and the ones of the other amplifiers (5.4-mW to 15-mW) are in the same values range. The same applies to the achieved noise figures. As observable, the LNA1 and LNA3 variants present noise figures (2.76-dB to 3.73-dB) that are in the interval defined by the noise figures of the other LNAs (1.4-dB to 3.7-dB). The −3-dB bandwidths of the LNA1 and LNA3 variants (6.91-GHz to 11.2-GHz) are lower than those of the other LNAs. Nevertheless, the attained bandwidths are wide enough for most of the applications in the 28-GHz band (e.g., 5G n257 band). However, it should be noted that the bandwidth was not one of the objectives of the sizing optimization procedure, as presented in Table 5. Moreover, the unique consideration taken to the gain flatness was that it must be within an interval of 1.5-dB in the frequency range between 26.5-GHz and 29.5-GHz, as presented in Table 4. The obtained simulated results show that all the variants of all the LNAs fulfill this constraint. It is interesting to note that the LNA 2 variants present higher bandwidths than those of LNA1 and LNA3, showing that the T-coils usage could be advantageous if the asymmetrical type was employed. Finally, the results showed that all the variants of LNA1, LNA2, and LNA3 are unconditional stable.

In Table 13, all the LNAs are also characterized by two figures-of-merit (FOMs). FOM1, expressed by:

$$FOM1 = \frac{Gain\,[dB]}{P_{DC}\,[mW]}, \tag{4}$$

shows that LNA3 LowP has the best efficiency among all the other LNAs. It is also interesting to note that the second-best FOM1 LNA was also developed in a 65-nm bulk CMOS [28]. LNA3 HighG variant achieves the third-best efficiency. The second FOM, FOM2, is given by [4]:

$$FOM2 = \frac{Gain\,[\text{lin.}] \cdot 1000}{(NF\,[lin.] - 1) \cdot P_{DC}\,[mW]}, \tag{5}$$

which includes the noise figure, besides the gain and power consumption. Among all the other FOMs that could be used to characterize the global performance of an LNA, FOM2 is the one that most closely assesses the performance of the sizing optimization tool since it includes the main optimization objectives used in the automatic many-objective simulation-based design methodology. The FOM2 shows that the low power variant of LNA3 is the third-best LNA, closely followed by the one reported in [28]. It is important to refer that the optimization tool finds LNA circuits with performances that compete with other LNAs, but using only the PDK's components, where integrated transformers are usually not available, and thus, without using techniques to improve gain and input/output impedance match that requires the use of transformers. Finally, note that the two higher FOM2 LNAs are both implemented in more advanced lower nodes SOI technologies.

A finer assessment of the performances of the LNA1 variants shows that the gains are close to 11-dB, which is higher than the ones of the[2], [25], and [27] LNAs. Although the HighG and LowNF variants of the LNA1 attain a higher gain than the LNAs reported in [2], [25], and [27], they consume a little more power (1.5-mW to 4.5-mW). However, the LNA1 LowP variant obtains a gain higher than the LNAs reported in [2], [25], and [27] with less power consumption (2-mW to 5-mW). The noise figures of the LNA1 variants are close to 3-dB. This value is near to the maximum NF of the other LNAs (3.7-dB). However, if the LNA1 LowNF variant is considered, it can be seen that its NF is better than the ones of the LNAs reported in [27], [28] and close to that of [2], but at the expense of a little more power consumption. Nonetheless, if the LowP variant of LNA1 is compared with the LNA of [27], which is developed in a 45-nm CMOS SOI, it is observable that the NF of the amplifiers is similar, but the gain and power consumption of the LNA1 variant are significantly better. The linearity of the LNA1 circuits, demonstrated by the input 1 dB compression point (IP1dB) and IIP3 values, is slightly worse than those developed in lower CMOS SOI nodes [2], [24], [25], [27], [29]. However, the linearity is better than the one reported in [28], which is the only LNA designed in the same technology node considered in this work. Nevertheless, it should be noted that the linearity maximization was not used as an objective during the optimization but only as a constraint.

The selected variants of LNA3 present gains between 11.1-dB and 12.73-dB, with a power consumption of 4.06-to-12.64-mW. These values are very competitive with the ones of the other reported LNAs. One of the reasons why LNA3 achieves a very low power consumption is due to the usage of a supply voltage (V_{DD}) of 0.6-V, and not 1.2-V. This is only possible due to the topology used in the LNA3. The same cannot be made in the topologies of the other LNAs presented in Table 13, including the LNA1. The high gain variant of LNA3 presents a gain (12.73-dB) very close to the reported maximum one (12.8-dB) and the second-lowest power consumption (8.12-mW). These performance parameters outperform the ones of the LNAs implemented in deeper CMOS SOI technology nodes [2], [24], [25], [27], [29]. Even the NF (3.73-dB) is very close to that of the LNA reported in [28], which is developed in similar CMOS technology. The results also show that LNA3 (LowNF variant) can achieve low NF (2.76-dB) and high gain (11-dB) at the expense of slightly higher power consumption (12.64-mW), however, lower than those obtained in [24] and [25]. The LowP variant of the LNA3 is the one that presents the lowest power consumption (4.06-mW) and the best FOM1. As can be seen, this amplifier maintains a high gain of 11.3-dB and a NF (3.67-dB) lower than the reported maximum one. Through the comparison of this variant with the LNA developed in similar technology, it can be concluded that LowP LNA3 outperforms all the performance characteristics of the LNA reported in [28], except the IP1dB, although very close. This observation can also be taken based on the values of FOM1 and FOM2 of both amplifiers. Indeed, the LowP variant is very competitive with

all the other reported LNAs, especially for high frequency very low power applications.

G. PERFORMANCE ANALYSIS

To fully analyze the performance of an LNA, it is necessary to consider their performance parameters with frequency. Moreover, the performance analysis should be assessed with all the parasitics associated with the amplifier layout. LNA3 LowP variant was chosen to be studied and analyzed in detail since it presents the best performance among all the variants of the LNA1, LNA2, and LNA3. In Fig. 8, it is depicted the layout of the LNA3 LowP variant, where its components are identified by the designations given in Fig. 1(c). The bias decoupling capacitors are also identified in Fig. 8. The area of the LNA3 LowP is approximately 0.28-mm^2 (also provided in Table 13), which is similar to the one reported in [28].

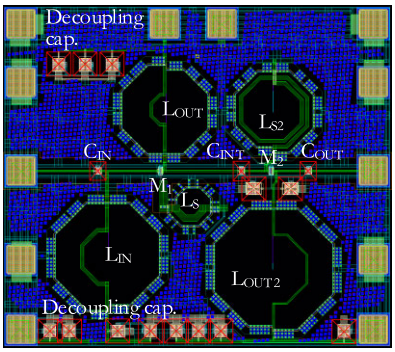


FIGURE 8. Layout of the LowP LNA3.

The pre- and post-layout simulated S-parameters (S11, S22, S21, and S12), noise figures (NFmin and NF), and stability parameters (Kf and B_{1f}) of the LowP LNA3 variant are shown in Figures 9, 10, 11, and 12. It is important to note that the LNA performance achieved at the higher end of the frequency range shown in these four figures are obtained considering that the models of the components are still valid on those frequencies.

The pre-layout performance parameters illustrated in Figures 9 to 12 (SCH curves) were obtained with the component's parameters (optimization variables) found by the optimization algorithm (given in Table 14). Relatively to the post-layout simulations, there are two distinct types of results: one obtained with all the layout parasitics and the components found by the optimization procedure (EXTopt curves) and the other, also achieved considering the layout parasitics, but with the inductors L_{IN}, L_{OUT}, L_{OUT2} and capacitors C_{IN}, C_{INT} and C_{OUT} slightly retuned (EXTret) to re-center the LNA operation again to 28-GHz. No adjustments were made in biasing or in any other of the LNA's components. The layout parasitics include resistors, capacitors, inductors, and mutual inductances since RLCK extraction was performed.

During the fast retuning, only one parameter in each component was varied. The inner radius was the only dimension adjusted in the inductors, while in the capacitors, it was the

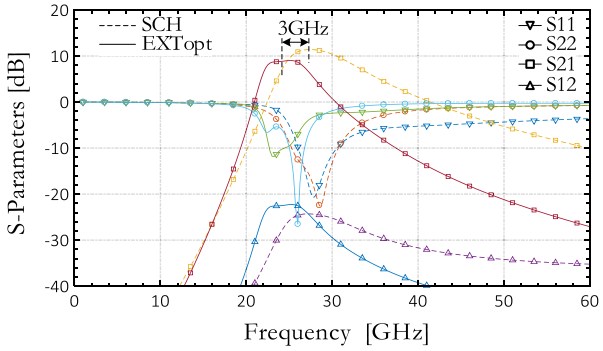


FIGURE 9. Pre-layout (SCH) and post-layout (EXTopt - with the optimized components values) LowP LNA3 S-parameters: S11, S22, S21 and S12.

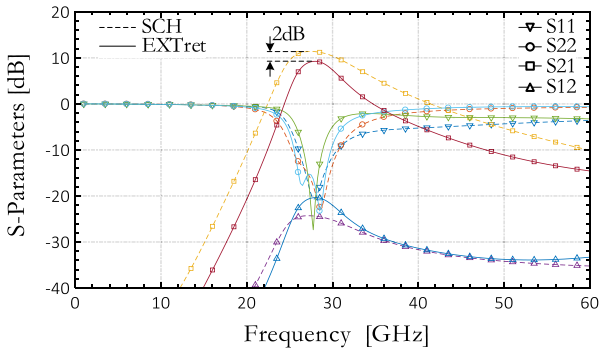


FIGURE 10. Pre-layout (SCH) and post-layout (EXTret - with the optimized components values retuned) LowP LNA3 S-parameters: S11, S22, S21 and S12.

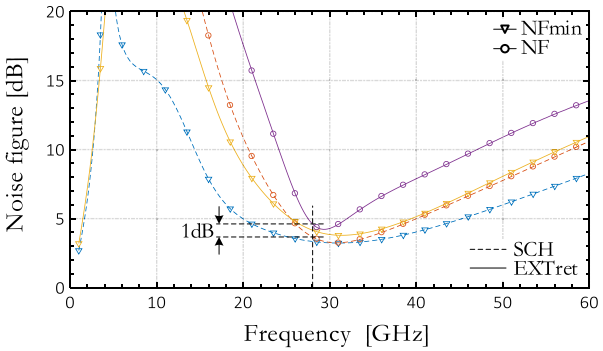


FIGURE 11. Pre-layout (SCH) and post-layout (EXTret - with the optimized components values retuned) LowP LNA3 noise figure (NF) and minimum noise figure (NFmin).

length, as illustrated in Table 14. As can be seen, the inductances of the three inductors decreased approximately 30%, and the length of the three capacitors changed less than 10%. Although the capacitors were adjusted, this was not strictly necessary since it is possible to re-center the LNA operation only by adjusting the three inductors above-mentioned, however, with slightly worse performance. This retuning methodology allowed obtaining good results in a short time interval (a couple of hours). Therefore, the initial values of the components, found by the sizing optimization tool, were crucial to minimizing the design time of the LNA.

TABLE 14. Components parameters of LNA3 variants.

LNA3 Components (Fig. 1)	Component designations (Fig. 1)	Performance parameters	LNA3 HighG	LNA3 LowPN	LNA3 LowP	LNA3 LowP (retuned)	
Transistors	M_1	Fingers length [nm]	60	60	60	--	
		Total Width [µm]	43.2	51.2	43.1	--	
	M_2	Fingers length [nm]	80	70	80	--	
		Total Width [µm]	84	93	63.8	--	
Inductors	L_{IN} @ 28-GHz	Inductance [pH]	290	295	286	198 (-31%)	lin_iradius_opt = 69 µm
		Quality factor	24	24	25	34	lin_iradius_ret = 42.02 µm
	L_{S1} @ 28-GHz	Inductance [pH]	56	61	60	--	
		Quality factor	37	37	38	--	
	L_{OUT1} @ 28-GHz	Inductance [pH]	225	243	251	155 (-38%)	lout_iradius_opt = 54 µm
		Quality factor	32	24	28	37	lout_iradius_ret = 22.71 µm
	L_{S2} @ 28-GHz	Inductance [pH]	836	923	734	--	
		Quality factor	10	7	11	--	
	L_{OUT2} @ 28-GHz	Inductance [pH]	306	281	333	254 (-24%)	lout2_iradius_opt = 77 µm
		Quality factor	23	23	20	25	lout2_iradius_ret = 56.46 µm
Capacitors	C_{IN}	Capacitance [fF]	67	108	77	69 (-10%)	cin_length_opt = 8.3 µm cin_length_ret = 7.5 µm
	C_{INT}	Capacitance [fF]	78	134	76	82 (7.9%)	cint_length_opt = 6.8 µm cint_length_ret = 7.4 µm
	C_{OUT}	Capacitance [fF]	65	89	66	69 (4.5%)	cout_length_opt = 6.8 µm cout_length_ret = 7.15 µm

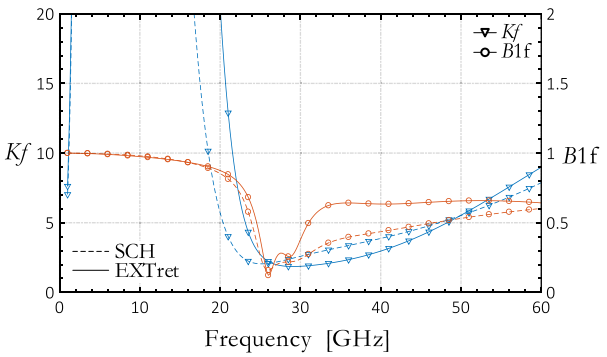


FIGURE 12. Pre-layout (SCH) and post-layout (EXTret - with the optimized components values retuned) LowP LNA3 stability parameters.

The SCH curves (pre-layout results) depicted in Figures 9 to 12 show that all the performance parameters comply with the specifications illustrated in Table 4. Fig. 9 shows that the S21 parameter is higher than 10-dB from 25.28-to-30.48-GHz (5.2-GHz). However, the −3-dB bandwidth is approximately 7.57-GHz (24.58-to-32.15-GHz). The input and output reflection coefficients are lower than −10-dB from 26.05-to-30.55-GHz (4.5-GHz) and 25.3-to-30.7 GHz (5.4-GHz), respectively. Fig. 9 also shows that the reverse transmission is low, as intended. The S-parameter curves show that the optimization algorithm was able to obtain the best S-parameters at the center of the desired frequency band (26.5-to-29.5-GHz). Fig. 9 also illustrates the S-parameters of the post-layout amplifier with the original (optimized) components (EXTopt curves). As can be seen, the S-parameters suffered a shift of approximately 3-GHz, being now centered at 25-GHz, instead of 28-GHz. Moreover, the maximum gain decreased and the input and output impedance matching, now at 25-GHz, are worse than those obtained initially (pre-layout results). The NF (not shown) increased, but the amplifier continues to be unconditionally stable. This performance deterioration is normal and is a consequence of the layout parasitics, which were not considered during the automated design approach. As referred above, the performance issues can be mitigated by retuning some of the LNA components.

Fig. 10 presents the S-parameters of the retuned LNA (EXTret curves), which are all centered at 28-GHz, as desired. The maximum gain decreased 2-dB, from 11.3-dB to 9.3-dB, but the input and output reflection coefficients are similar to the original ones (SCH curves). In the frequency range from 26.5-GHz and 29.5-GHz, the LNA gain (S21) flatness and the output reflection coefficients comply with the specifications given in Table 4. The input reflection coefficient at the extremes of the considered frequency range does not comply with the specifications since it is approximately −10-dB at 26.5-GHz and −6-dB at 29.5-GHz. However, these values can be considered normal compared with the ones of other LNAs.

The minimum noise figure (NFmin) of the pre-layout amplifier (SCH curves) is 3.2-dB at 30.9-GHz, as illustrated in Fig. 11. Although the minimum value is not located at 28-GHz, as desired, the NFmin value at that frequency is only slightly higher than the minimum value since the NFmin curve is very flat at the 30-GHz frequencies. As shown, NFmin only varies 0.5-dB from 24.83-to-37.9-GHz (13.07-GHz), which covers the target

band. The minimum attainable NF of the LowP LNA3 is 3.25-dB at 30.7-GHz, which is slightly shifted from the desired center frequency of 28-GHz. However, its value at the center of the interest frequency band is only 0.42-dB above, as given in Table 13. This slight frequency shift is explained by the type of optimization, i.e., in the LowP solution, the optimized exploited the compromise between the S-parameters and noise performances to attain the minimum power consumption. Still, it is evident that the optimization algorithm could find the input matching circuit that assures that NF closely approaches NFmin. The LNA noise performance shows, once again, that the optimization algorithm performs well.

When the parasitics associated with the layout are considered, the minimum NFmin and NF values are obtained at a lower frequency, and their values increased, as stated before. To re-center both curves, the inductors and capacitors mentioned above were adjusted (see Table 14). The obtained NF and NFmin curves (EXTret) are also shown in Fig. 11. Both curves are centered at approximately 28-GHz, their values slightly higher than the ones of the pre-layout LNA. The post-layout NF is 1-dB higher than the one of the pre-layout but continues to be close to the NFmin, showing that the LNA maintains a good noise match at its input.

Finally, Fig. 12 results demonstrate that the pre- and post-layout LowP LNA 3 variant are unconditionally stable since Kf and B_{1f} are always higher than one and zero, respectively. The results shown in Figures 9, 10, 11, and 12 clearly demonstrate that LowP LNA3 presents a good performance between 26-to-30.5-GHz. The results presented above show that the LNA3 AC-coupled cascode topology using only available components from the technology, i.e., without using transformers, competes with state-of-the-art cascode and stacked CS-CS topologies when sized adequately.

Table 14 shows the components properties found by the optimization algorithm for the three LNA3 variants and the new values of L_{IN}, L_{OUT}, L_{OUT2}, C_{IN}, C_{INT} and C_{OUT} used in the retuned LowP LNA3. As can be seen, all the components sizes and values found by the optimization tool are easily implementable and are in the same values range that the components of other state-of-the-art LNAs. It is interesting to note that the optimization algorithm selected a low inductance inductor to degenerate M_1 transistor (L_{S1}) and a high inductance inductor for the M_2 source (L_{S2}) in order to isolate the signal path from the ground. Moreover, the inductors L_{IN}, L_{OUT1}, and L_{OUT2} have low to moderate inductances with high quality factors. This allows improving the gain and noise performances and simultaneously enhance layout area since inductors with inductances in the range of 250-pH can be implemented in low areas. All these algorithm decisions are in accordance with what would be performed during a design developed manually. Once again, the components parameters found by the optimization algorithm show that it is an important auxiliary design tool. Although only the components for the LNA3 variant were shown, the components of the LNA1 and LNA2 variants are also all easily implementable.

VII. CONCLUSION

The sizing results of three 28-GHz LNAs were presented for a 65-nm technology node, where EDA tools balance the design tradeoffs comprehensively over all the performance figures, and, additionally, through several different processes, voltage, and temperature corners, without manual intervention. The optimization of these complex and highly constrained design spaces provided many-objective fronts of non-dominated solutions that allow a truthful analysis of the performance boundaries and tradeoffs that fit the target application. The application of both one- and two-step design fashions shows that the design space's complexity reduction using bottom-up two-step provided impressive circuits' footprint reductions. However, the one-step fashion can further account for interactions between the inductor and the rest of the components, improving the obtained solutions set' performance ranges. The final results allowed us to position the optimized LNAs in relation to the most-recent single-stage mmWave LNAs available in the literature and discuss their role in the 28-GHz band. Although traditional inductor-based cascode LNA topologies were used in this work, any mmWave LNA topology can be optimized as long as the passive model is available in the PDK from the foundry. If not available, as it is usually the case of integrated transformers, a priori design space sampling of the transformer or electromagnetic-simulation in-the-loop would allow for such an experiment. Finally, as a future research direction, it is desired to apply EDA tools at the layout level and apply a layout-aware sizing optimization loop [30], [31] to unify pre- and post-layout mmWave IC design stages.

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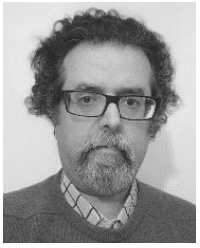

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