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Theoretical Optimization of the Si GSS-DMM Device in the BaSIC Topology for SiC Power MOSFET Short-Circuit Capability Improvement

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ABSTRACT The BaSIC(DMM) topology has been experimentally demonstrated to improve the short-circuit time for a 1.2 kV SiC power MOSFET product from 4.8 μs to 7.9 μs with a 17% increase in on-state resistance by utilizing a commercially available 100 V rated Gate-Source-Shorted (GSS) Si Depletion-Mode power MOSFET (DMM). The optimization of the Si GSS-DMM is discussed in this paper to achieve even superior performance, namely larger short-circuit time with less increase in on-resistance. It is theoretically demonstrated for the first time that a highly desirable short-circuit time of 10 μs, similar to Si IGBTs, can be achieved for two SiC power MOSFET products with less than 3% increase in on-resistance. This was accomplished by reducing the breakdown voltage rating of the Si GSS-DMM from 100 V to 30 V, altering the cell design parameters, and utilizing the trench-gate design. The theoretical analysis provided in this paper provides valuable design guidelines for manufacturers of Si GSS-DMM devices to achieve optimum performance for use in the BaSIC(DMM) topology.

INDEX TERMS Power MOSFET, robustness, short-circuit currents, optimization.

I. INTRODUCTION

Silicon IGBTs are commonly used for motor drives in industrial and electric vehicle applications [1], [2]. One of the attributes of the Si IGBT is a short-circuit (SC) time (t_{SC}) of more than 10 μs, which allows SC detection followed by turning off the gate drive voltage to prevent device failure. A significant switching power loss reduction in the inverters is achieved by substituting SiC power MOSFET in place of Si IGBTs [3], [4]. Using SiC power MOSFETs allows increasing the operating frequency of the inverters. This reduces the inverter size and weight due to smaller inductors, capacitors and filters.

Unfortunately, commercially available 1.2 kV SiC power MOSFETs are designed to minimize their on-resistance resulting in <5 μs SC time with 800 V DC supply voltage if operated using the standard datasheet gate drive of 20 V [5]–[7]. This SC time is too short to detect the SC event and turn-off the gate drive voltage when using the conventional low cost Si IGBT gate drive circuits that are based on the DESAT method. This can produce destructive failure of the SiC power MOSFETs.

It has been shown that SC failure of SiC power MOSFETs is caused by temperature rise above 700 °C producing melting of the aluminum source metal [8]. Decreasing the SC current inhibits the increase in temperature preventing device failure. Reduction of SC current can be achieved by decreasing the gate drive voltage. Alternately, the SiC power MOSFET device structure can be changed to increase the channel length. Both of these methods produce a significant increase of the SiC power MOSFET on-state resistance [9], [10].

It has been recently demonstrated that the short-circuit time (t_{SC}) for SiC power MOSFETs can be extended by using the **Ba**liga **S**hort-circuit **I**mprovement **C**oncept (BaSIC) [11], [12]. The BaSIC(DMM) topology makes use of a *gate source-shorted* (GSS) silicon *depletion-mode MOSFET* (DMM) connected in series with the source electrode of the SiC power MOSFET as shown in Fig. 1. In principle, the Si GSS-DMM device acts as a non-linear resistance. It has a low resistance at the on-state current levels of the SiC power MOSFET device minimizing its impact on on-state and switching power losses. The voltage drop across the Si GSS-DMM

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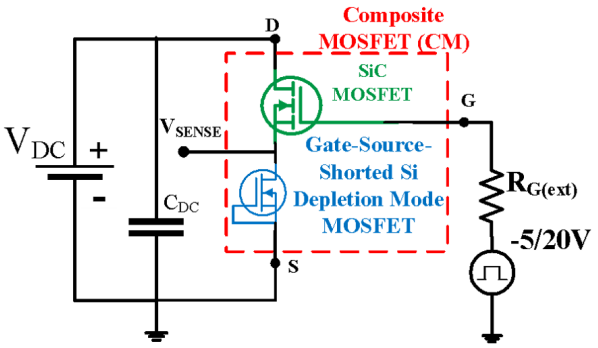

FIGURE 1. Schematic of the short circuit characterization test setup for the BaSIC(DMM) topology.

during on-state operation subtracts from the gate drive voltage applied to the SiC power MOSFET. In principle, this could result in an increase of the on-resistance of the SiC power MOSFET. However, the Si GSS-DMM is selected with a low on-resistance such that the reduction in the gate-source voltage for the SiC power MOSFET, and hence the increase in its on-resistance, is negligible. This is discussed in more detail later in the paper with quantitative examples. During the SC event, the Si GSS-DMM enters its drain current saturation region and limits the current to a lower value than the saturation current of the SiC power MOSFET. The drain potential of the Si GSS-DMM increases to 6-8 V during the SC event. This voltage opposes the gate drive voltage (20 V) applied to the SiC power MOSFET. Consequently, the gate-to-source voltage across the SiC power MOSFET is reduced until its saturation current *automatically* matches that of the Si GSS-DMM device. Experimental demonstration of the Si GSS-DMM has been accomplished by using commercially available devices [12].

The silicon power semiconductor industry manufactures enhancement-mode MOSFETs with a wide range of blocking voltages and on-resistances. In contrast, very few Si depletion-mode MOSFETs are available. For example, the lowest breakdown voltage for a Si DMM product (BSS159N) by Infineon is 60 V with a high on-resistance of 3.9 Ω and saturation current of only 0.32 A [13]. Similarly, the IXYS application note AN-500 for Si DMM products lists part CPC3701 with the lowest blocking voltage of 60 V and a high on-resistance of 1 Ω [14]. The only commercially available device with an acceptable on-resistance of 60 mΩ for the BaSIC(DMM) topology was a 100 V Si depletion-mode power MOSFET (IXTH16N10D2) [15]. A short-circuit time (t_{SC}) for a 1.2 kV SiC power MOSFET (C2M0280120D) product was increased by a factor of 1.65x (from 4.8 μs to 7.9 μs) by utilizing this Si GSS-DMM device. The net on-resistance increased by 17% in this case [12]. It was also shown that the trade-off between enhancing t_{SC} and increase in R_{ON} with the BaSIC(DMM) approach is much superior to employing a series ballast-resistor [16].

In general, a better trade-off curve between the SC capability and the increase in on-resistance for the BaSIC(DMM) topology can be achieved when the trade-off curve between the saturation current and on-resistance of the Si GSS-DMM is improved as demonstrated in detail in this paper. The best trade-off curve for the Si GSS-DMM exhibits both a smaller saturation current and on-resistance simultaneously. Analysis of the Si GSS-DMM device structure is therefore required to determine the structural parameters that will improve the trade-off curve between the saturation current and on-resistance for these devices. This analysis has not been performed and published previously because most commercially available Si power MOSFETs are enhancement-mode devices.

The goals of this paper are: (a) to theoretically demonstrate that a much better trade-off between increase in t_{SC} and increase in R_{ON} is achievable by reducing the blocking voltage of the Si GSS-DMM device from 100 V; (b) to theoretically demonstrate that the trade-off between increase in t_{SC} and increase in R_{ON} can be further improved by making selective changes to the Si DMM cell structure; (c) to theoretically demonstrate that a better trade-off curve can be achieved with the trench-gate Si GSS-DMM structure compared with the planar gate Si GSS-DMM structure; and (d) to theoretically quantify the improvement in the trade-off curve between increase in t_{SC} and increase in R_{ON} achieved by using the new optimized Si GSS-DMM devices in the BaSIC(DMM) topology for several commercially available SiC power MOSFETs as examples.

The information provided in this paper is valuable to the semiconductor power device industry to create improved Si depletion-mode power MOSFETs for utilization in the BaSIC(DMM) topology to enhance the short-circuit performance of SiC power MOSFETs. Many power semiconductor companies make both Si and SiC power MOSFETs. They can make use of the information in this paper to make a chip set (Si DMM device and SiC power MOSFET device) that can be co-packaged to make BaSIC(DMM) composite transistors with superior short-circuit capability for motor control applications in electric vehicles and industrial drives.

This paper is a theoretical study performed to encourage the Si semiconductor manufacturers to fabricate the proposed improved GSS-DMM device. Experimental validation can be achieved only after the Si device are commercially available for employment in the BaSIC(DMM) topology. The theoretical analysis is however validated in this paper using available data for an existing 100 V Si DMM product.

II. ANALYSIS OF SI DMM STRUCTURE

As in the case of Si enhancement-mode power MOSFETs [9], the Si GSS-DMM devices can be fabricated using either the D-MOS or U-MOS structure. The D-MOS planar-gate device structure is shown on the left-hand side in Fig. 2. The U-MOS trench-gate structure is shown on the right-hand side in Fig. 2. Both of these structures can operate as either an enhancement-mode device with a positive threshold voltage or a depletion-mode device with a negative threshold voltage by adjusting the doping concentration of the P-base region [9]. The optimization of both structures is performed

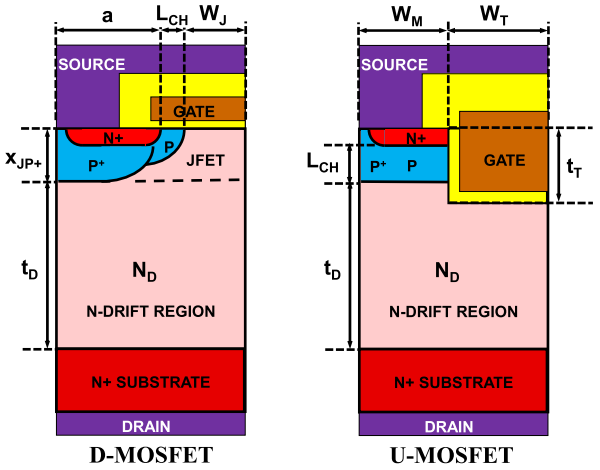

FIGURE 2. Cross sections of the Silicon DMM Devices.

in this paper for comparison of their performance in the BaSIC(DMM) topology to improve the short circuit capability of SiC power MOSFETs.

A. SI D-MOSFET OPTIMIZATION

The 100 V Si depletion-mode power MOSFET (IXTH16N10D2) used for the experimental demonstration of the BaSIC(DMM) approach has a D-MOS structure. In order to perform the optimization of the Si GSS-DMM structure, a 100 V Si depletion-mode D-MOSFET structure was first analyzed as a bench-mark device. This allowed obtaining the device structural parameters that produce the same on-resistance, saturation current, and threshold voltage as the IXTH16N10D2 product. The device structural parameters are defined in Fig. 2.

The on-resistance of the Si D-MOSFET structure can be analytically modelled using the equations in the textbook [9]. There are 8 components of the on-resistance of which the channel, accumulation layer, JFET, and drift region values are dominant. The drift region doping (2.5×10^{15} cm^{-3}) and thickness (8.0 μm) for the 100 V device were obtained by assuming that the edge termination limits the blocking voltage to 80 % of the ideal parallel plane value. Typical values for the JFET region doping concentration (2×10^{16} cm^{-3}) and width ($W_J = 1.5$ μm) were selected with a P^+ region junction depth (x_{JP+}) of 1.5 μm. The cell parameter 'a' in Fig. 2 of 3 μm was chosen to allow making the source and base ohmic contacts based up on typical alignment tolerances. The gate oxide thickness and channel mobility were assumed to have typical values of 500 Å and 100 cm^2/V-s for the benchmark 100 V device structure. The device active area was estimated to be 0.1 cm^2 based on the on-resistance of 64 mΩ for the IXTH16N10D2 product and the typical specific on-resistance of Si MOSFETs with blocking voltage of 150 V measured for this device. The channel width (Z) is 183 cm for this device using the parameters chosen for the MOSFET cell. The magnitude of Z can be obtained by diving the active area by the cell width shown in Fig. 2.

The channel resistance for a power MOSFET is given by [9]:

$$R_{CH} = \frac{L_{CH} t_{GOX}}{Z \mu_{ni} \varepsilon_{OX} (V_G - V_{TH})} \tag{1}$$

where L_{CH} is the channel length, t_{GOX} is the gate oxide thickness, Z is the channel width, μ_{ni} is the channel inversion layer mobility, ε_{OX} is the gate oxide dielectric constant, V_G is the gate bias voltage, and V_{TH} is the threshold voltage. Most commercially available Si power MOSFETs are enhancement-mode structures that are turned on using a positive gate bias due to the positive threshold voltage required for most applications. An unusual feature of the Si GSS-DMM device being analyzed here for use in the BaSIC(DMM) topology is that the gate bias (V_G) is zero and the threshold voltage (V_{TH}) is designed to be negative to obtain current flow with gate shorted to the source. The channel resistance for the Si GSS-DMM device is then:

$$R_{CH} = \frac{L_{CH} t_{GOX}}{Z \mu_{ni} \varepsilon_{OX} V_{TH}} \tag{2}$$

where V_{TH} is the magnitude of the threshold voltage. A negative threshold voltage can be obtained by proper choice of the peak P-base doping concentration [9]. Other components of the on-state resistance can be modelled by using the equations in the textbook, which have been validated by performing numerical simulations [9]. Among these components, the drift region component is determined by the doping concentration (N_D) and thickness (t_D) of the drift region which are a strong function of the blocking voltage capability. It is worth pointing out that the channel resistance component ranges from 30 to 60 percent of the total on-resistance depending up on the blocking voltage, channel length, gate oxide thickness, and threshold voltage.

The saturation current of the D-MOSFET is given by [9]:

$$I_{D,SAT} = \frac{Z \mu_{ni} \varepsilon_{OX} (V_G - V_{TH})^2}{2 L_{CH} t_{GOX}} \tag{3}$$

The saturation current is exclusively determined by the channel properties, namely the channel length, gate oxide thickness, and threshold voltage [9]. The saturation current of the Si GSS-DMM device is given by:

$$I_{D,SAT} = \frac{Z \mu_{ni} \varepsilon_{OX} V_{TH}^2}{2 L_{CH} t_{GOX}} \tag{4}$$

because the gate bias is zero in this case. Comparing equations (2) and (4), it can be seen that there is an interplay between the channel resistance and the drain saturation current for the Si GSS-DMM device. For example, the saturation current increases and the channel resistance decreases when the magnitude of the negative threshold voltage increases.

With the chosen device structural parameters for the D-MOS structure, a channel length (L_{CH}) of 1 μm produces a saturation current of 25 A that matches the value in the IXTH16N10D2 product datasheet while simultaneously producing an on-resistance of 66 mΩ consistent with the datasheet value (64 mΩ). These values are obtained with a

threshold voltage of -2 V which also matches the value for this device in the datasheet. These results validate the choice of the structural parameters used for the analytical model for the Si GSS-DMM D-MOS device.

1) BENCHMARK 100 V D-MOS STRUCTURE

Using the validated structural parameters for the 100 V Si GSS-DMM D-MOS device, the variation of both the saturation current and the on-resistance can be modelled with changes made to the threshold voltage while keeping all structural parameters and active area unaltered. The threshold voltage can be modified by adjusting the doping concentration of the base region [9]. It can be observed from the purple line in Fig. 3 that the on-resistance for the benchmark Si GSS-DMM D-MOS device increases when the saturation current is reduced. This behavior is observed for all the Si GSS-DMM structures as shown later. The data point shown in orange on the figure is the operating point of the commercially available 100 V IXTH16N10D2 product. It can be seen that the analytical model precisely matches the available data on the 100 V GSS-DMM D-MOS device.

2) BASELINE 30 V D-MOS STRUCTURE

It is well known that the on-resistance of Si enhancement-mode power MOSFETs decreases with reduction in the blocking voltage capability [9]. This behavior can also be expected for the Si depletion-mode MOSFETs but has not been previously reported. Analysis of the Si GSS-DMM D-MOS device was therefore performed with a reduced blocking voltage of 30 V by increasing the drift region doping to 1.3 x 10^{16} cm^{-3} and reducing its thickness to 2 μm. The same channel length (1 μm) and gate oxide thickness (500 Å) were used as the benchmark 100 V D-MOS case. The resulting trade-off curve obtained for this baseline 30 V Si GSS DMM D-MOS device is shown in green in Fig. 3. It can be seen the trade-off curve has improved by reducing the blocking voltage capability from 100 V to 30 V. As an example, the same saturation current of 50 A is obtained for the baseline GSS-DMM D-MOS case with an on-resistance of 39 mΩ compared with 52 mΩ for the 100 V benchmark device.

3) INTERMEDIATE 30 V D-MOS STRUCTURE

It was found that improvement of the trade-off curve could be obtained by reducing the channel length of the 30 V Si GSS-DMM D-MOS device. Analysis of the Si GSS-DMM D-MOS was performed with a reduced channel length of 0.3 μm keeping other parameters unchanged. This type of reduced channel length has been successfully used to make enhancement-mode, planar-gate, Si power MOSFETs by Silicon Semiconductor Corporation with very low specific on-resistance and gate charge [17]. The trade-off curve for this intermediate 30 V Si GSS-DMM D-MOS device is shown in blue in Fig. 3. It can be seen that the trade-off curve has been improved by reducing the channel length. As an example, the same saturation current of 50 A is obtained for the intermediate D-MOS case with an on-resistance of 30 mΩ compared with 39 mΩ for the baseline 30 V device.

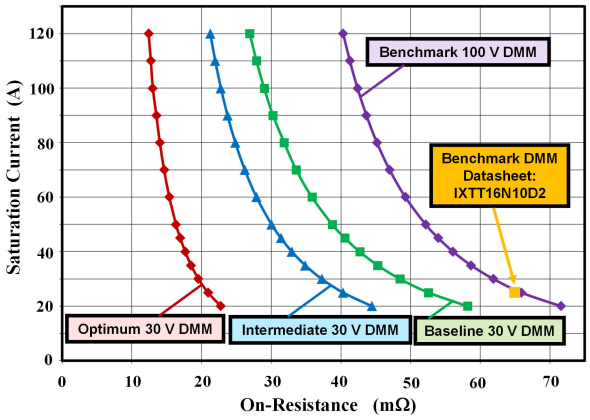

FIGURE 3. Trade-off curve between saturation current and on-resistance for D-MOS planar-gate Si GSS-DMM devices.

4) OPTIMUM 30 V D-MOS STRUCTURE

Even further improvement of the trade-off curve could be obtained by reducing the gate oxide thickness of the 30 V Si GSS-DMM D-MOS device. Analysis of the Si GSS-DMM D-MOS was performed with a reduced gate oxide thickness of 100 Å and channel length of 0.3 μm. A thin gate oxide of 100 Å can be grown by reducing the gate oxide growth time and is still larger than oxide thicknesses typically used for modern VLSI CMOS devices. A smaller gate oxide thickness of 100 Å is acceptable for the Si GSS-DMM device because no gate bias is applied that could stress the gate oxide. In this D-MOS case, the trade-off curve shifts to the red line in Fig. 3. The trade-off curve has been improved significantly by reducing the gate oxide thickness. As an example, the same saturation current of 50 A is obtained for the optimum D-MOS case with an on-resistance of 16 mΩ compared with 30 mΩ for the intermediate 30 V device.

B. Si U-MOSFET OPTIMIZATION

The trench-gate (or U-MOS) structure shown in Fig. 2 on the right-hand-side was adopted by the silicon power semiconductor industry in the 1990s to reduce the on-resistance of enhancement-mode power MOSFETs [9]. This structure can also be utilized to improve the performance of the Si depletion-mode MOSFETs discussed in this paper. The JFET resistance component is eliminated with the U-MOS structure allowing reducing the cell width. This produces a much larger channel density which increases the channel width (Z) for the same active area as a D-MOS structure. A larger channel width reduces the channel resistance component according to equation (2). However, a large channel width also increases the saturation current according to equation (4).

Analytical modelling of the on-resistance for the U-MOS silicon GSS-DMM U-MOS device structure was performed using the equations in the textbook [9]. These models have been validated using numerical simulations. The saturation

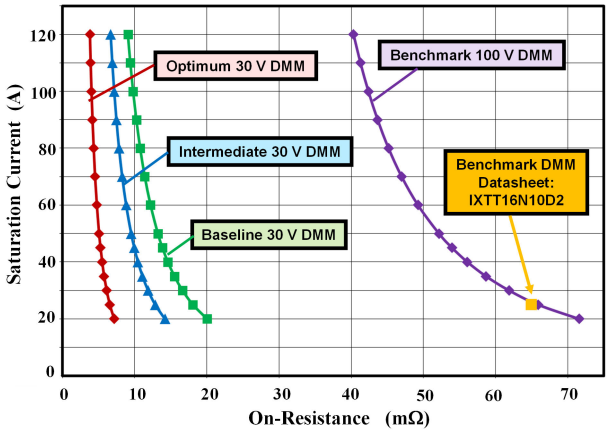

FIGURE 4. Trade-off Curve between saturation current and on-resistance for U-MOS trench-gate Si GSS-DMM devices.

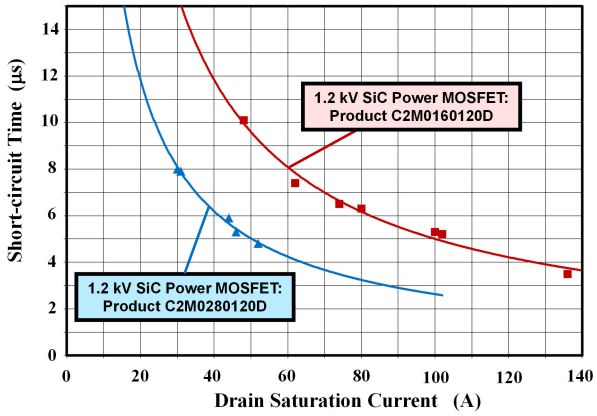

FIGURE 5. Measured trade-off curve between short-circuit time and drain saturation current for the 1.2 kV SiC power MOSFET C2M0280120D and C2M0160120D products.

current was modelled using equation (4). Typical values for the trench width ($W_T = 0.5\ \mu$m) and mesa width ($W_M = 2\ \mu$m) were assumed. This results in a larger channel width (Z) of 333 cm for an active area of 0.1 cm^2, which was kept the same as the previous D-MOS cases.

1) BASELINE 30 V U-MOS STRUCTURE

The baseline Si GSS-DMM U-MOS device was designed with a channel length of 1 μm and gate oxide thickness of 500 Å to match the baseline D-MOS case. The trade-off curve between saturation current and on-resistance for the baseline 30 V GSS-DMM U-MOS device was obtained by adjusting the threshold voltage. It is shown in Fig. 4 as the green line. The benchmark 100 V GSS-DMM case is included in Fig. 4 for comparison (purple line). It is obvious that the baseline 30 V GSS-DMM U-MOS structure has a much superior trade-off curve due to reduction of the on-resistance. As an example, the same saturation current of 50 A is obtained for the baseline 30 V GSS-DMM U-MOS case with an on-resistance of 13 mΩ compared with 52 mΩ for the 100 V benchmark D-MOS device.

2) INTERMEDIATE 30 V U-MOS STRUCTURE

This 30 V Si U-MOSFET structure was analyzed with a reduced channel length of 0.3 μm to match the intermediate 30 V D-MOS structure while keeping its other parameters unchanged. The trade-off curve for this intermediate 30 V Si GSS-DMM U-MOS device is shown in blue in Fig. 4. It can be seen that the trade-off curve gets better by reducing the channel length. The same saturation current of 50 A is obtained for the intermediate U-MOS case with an on-resistance of 10 mΩ compared with 13 mΩ for the baseline U-MOS device.

3) OPTIMUM 30 V U-MOS STRUCTURE

Further improvement of the trade-off curve was obtained by reducing the gate oxide thickness to 100 Å with a channel length of 0.3 μm. The trade-off curve for this case shifts to the red line in Fig. 4. The trade-off curve has been improved significantly by reducing the gate oxide thickness as previously noted for the D-MOS structure. For example, the same saturation current of 50 A is obtained for the optimum U-MOS case with an on-resistance of 5 mΩ compared with 10 mΩ for the intermediate U-MOS device.

III. IMPROVEMENT IN SiC POWER MOSFET SHORT-CIRCUIT CAPABILITY

The improved trade-off curves for the Si GSS-DMM D-MOS and U-MOS structures using the proposed changes in cell design parameters directly translate to improvements in the short circuit capability of SiC power MOSFETs achieved by using the BaSIC(DMM) topology. The expected improvement in performance is theoretically quantified in this section for the case of two 1.2 kV SiC power MOSFET products.

4) 1.2 kV SiC POWER MOSFET C2M0280120D PRODUCT WITH SI D-MOS DEVICES

This product has a typical on-resistance of 280 mΩ with a maximum value of 370 mΩ according to the datasheet [18]. The measured value for the procured devices was 346 mΩ which is consistent with the datasheet. The presence of the Si GSS-DMM device in series with the source of the SiC power MOSFET has negligible impact on its on-resistance as mentioned in the introduction. Even for the worst case 100 V Si DMM device with on-resistance of 60 mΩ, the voltage drop across it at the on-state current of 6 A for this SiC power MOSFET in its datasheet is only 0.36 V. In the BaSIC(DMM) topology, the gate-source voltage for this SiC power MOSFET is then reduced to 19.64 V. This produces negligible increase in the on-resistance for the device according to the figures in the datasheet. The voltage drop across the optimized Si MOSFETs described in this paper are much smaller making the even lower impact on the SiC power MOSFET on-resistance.

The short-circuit time and the corresponding drain saturation current was reported for the C2M0280120D product in previous publications [12], [16]. This data is plotted in Fig. 5 as the blue triangles. A polynomial fit, shown by

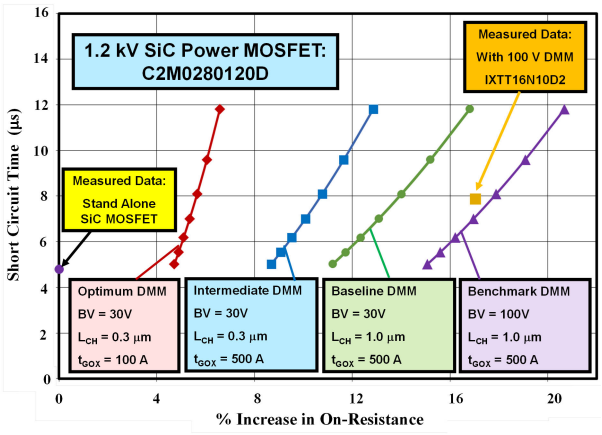

FIGURE 6. Trade-off curves between short-circuit time and increase in on-resistance for the 1.2 kV SiC power MOSFET C2M0280120D with various cases of the Si GSS-DMM devices.

the blue line in Fig. 5, for the trade-off curve between the short-circuit time and the saturation current for this device is:

$$t_{SC} = 194 \times I_{D,SAT}{}^{-0.934} \tag{5}$$

The saturation currents obtained by the analysis in the previous section for the various Si GSS-DMM devices can be translated into a corresponding short-circuit time by using this polynomial fit.

The trade-off curves between the short-circuit time (at DC drain bias of 800 V and gate bias of 20 V) and the increase in on-resistance obtained for BaSIC(DMM) topology for the 1.2 kV SiC power MOSFET C2M0280120D product are shown in Fig. 6. The results in Fig. 6 were derived using the information in Fig, 3 for the various Si GSS-DMM D-MOS cases. The green line corresponds to the baseline 30 V D-MOS device, the blue line for the intermediate 30 V D-MOS device and the red line for the optimum 30 V D-MOS device. The purple line is the trade-off curve obtained for the benchmark 100 V D-MOS case.

The measured short-circuit time of 4.8 μs [12] for the stand-alone SiC power MOSFET product (for a DC supply voltage of 800 V and gate drive voltage of 20 V) is also shown in Fig. 6 with no increase in on-resistance as a reference point. In addition, the orange point shows the measured short-circuit data point [12] obtained for the BaSIC(DMM) topology with the 100 V IXTT16N10D2 product with a short-circuit time of 7.9 μs with 17 % increase in on-resistance. It can be seen that the measured data point falls close to the purple line providing validation of the analytical modelling described in the previous section.

From Fig. 6, it can be seen that a desirable short-circuit time of 10 μs is achievable for the BaSIC(DMM) topology with the baseline 30 V D-MOS device with 15 % increase in on-resistance. For the intermediate 30 V D-MOS device, an increase in on-resistance of 12 % occurs to achieve a short circuit time of 10 μs. The same desirable short-circuit time of 10 μs is achievable for the BaSIC(DMM) topology with the optimum 30 V D-MOS device accompanied by an increase in on-resistance of 6 %. The benefit of the optimization of the Si GSS-DMM D-MOS device performed in the previous section is a reduction by about 3x in the % increase in on-resistance.

5) 1.2 kV SiC POWER MOSFET C2M0160120D PRODUCT WITH SI D-MOS DEVICES

This product has a typical on-resistance of 160 mΩ according to its datasheet with a maximum value of 196 mΩ. The procured devices had a measured value of 168 mΩ, consistent with the datasheet. The addition of a Si GSS-DMM device in series with the source of the SiC power MOSFET produces negligible impact on its on-resistance. In the case of the 100 V Si DMM device with on-resistance of 60 mΩ, the voltage drop across it at the on-state current of 10 A for this SiC power MOSFET in its datasheet is only 0.6 V. The gate-source voltage for this SiC power MOSFET is then reduced to 19.4 V in the BaSIC(DMM) topology. This results in negligible increase in its on-resistance according to the figures in the datasheet.

The measured short-circuit time and the corresponding drain saturation current for the C2M0160120D product was reported in a previous publication [19]. This data is plotted in Fig. 5 as the red squares. The polynomial fit, shown by the red line in Fig. 5, for the trade-off curve between the short-circuit time and the saturation current for this device is:

$$t_{SC} = 378 \times I_{D,SAT}{}^{-0.939} \tag{6}$$

The saturation currents for the various Si GSS-DMM devices obtained by the analysis in the previous section can be converted by using this polynomial fit into the corresponding short-circuit time for this SiC power MOSFET product.

The trade-off curves between the short-circuit time (at DC drain bias of 800 V and gate bias of 20 V) and the increase in on-resistance obtained for BaSIC(DMM) topology for the 1.2 kV SiC power MOSFET C2M0160120D product is shown in Fig. 7. The results in Fig. 7 were generated using the information in Fig, 3 for the various Si GSS-DMM D-MOS cases. The purple line is the trade-off curve obtained for the benchmark 100 V GSS-DMM D-MOS case. The green line corresponds to the baseline 30 V GSS-DMM D-MOS device, the blue line for the intermediate 30 V GSS-DMM D-MOS device and the red line for the optimum 30 V GSS-DMM D-MOS device. The short-circuit time measured for this stand-alone SiC power MOSFET product C2M0160120D (for a DC supply voltage of 800 V and gate drive voltage of 20 V) is 3.5 μs as shown in Fig. 7 with no increase in on-resistance as a reference point [17].

The benchmark Si 100 V GSS-DMM D-MOS structure produces a large increase in on-resistance of 31.5 % to achieve a short-circuit time of 10 μs because of its high blocking voltage rating. Better trade-off curves can be obtained by using the improved 30 V GSS-DMM D-MOS devices described in the previous section. A t_{SC} of 10 μs is obtained for the BaSIC(DMM) topology with the baseline 30 V GSS-DMM D-MOS case with 23 % increase in

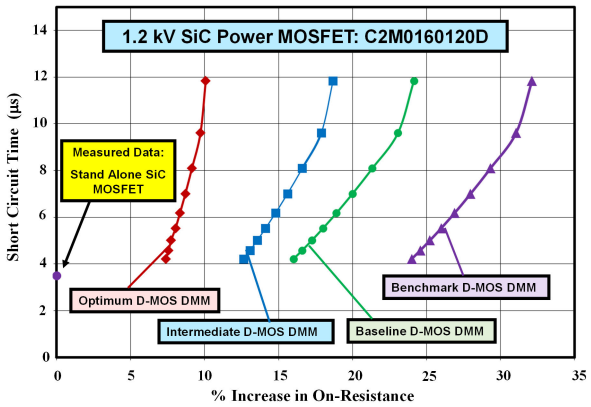

FIGURE 7. Trade-off curves between short-circuit time and increase in on-resistance for the 1.2 kV SiC power MOSFET C2M0160120D with various cases of the Si GSS D-MOS devices.

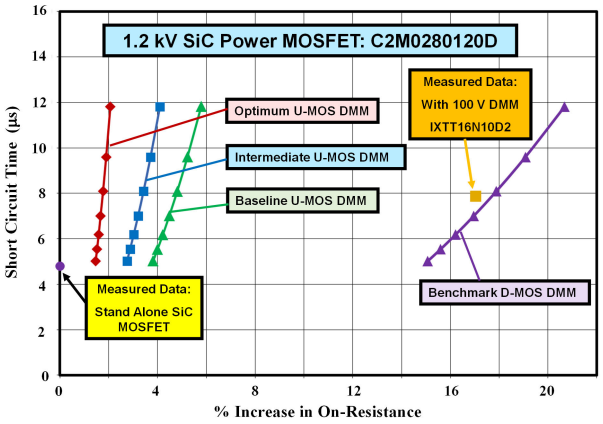

FIGURE 8. Trade-off curves between short-circuit time and increase in on-resistance for the 1.2 kV SiC power MOSFET C2M0280120D with various cases of the Si GSS U-MOS devices.

on-resistance. The increase in on-resistances reduces to 18 % for the BaSIC(DMM) topology with the intermediate 30 V GSS-DMM D-MOS case and to 10 % for the BaSIC(DMM) topology with the optimum 30 V GSS-DMM D-MOS case.

The trade-off curves between short-circuit withstand time and increase in on-resistance are much better when the 30 V U-MOS device structure is employed in the BaSIC(DMM) topology for both of the elected SiC power MOSFET products as discussed below.

6) 1.2 kV SiC POWER MOSFET C2M0280120D PRODUCT WITH SI U-MOS DEVICES

The same procedure used in the previous sections can be applied to the C2M0280120D product with the values shown in Fig. 4 for the trade-off curve between saturation current and on-resistance for the various GSS-DMM U-MOS device cases. Combining this information with the trade-off curve for short-circuit time versus saturation current in Fig. 5 results in the plots shown in Fig. 8. The benchmark (purple line), and data-points for the stand-alone and measured case with the 100 V GSS-DMM D-MOS product are included for comparison. A t_{SC} of 10 μs is obtained for the BaSIC(DMM) topology using the 30 V GSS-DMM U-MOS devices with 5.3, 3.8, and 2.0 % increase in on-resistance for the baseline, intermediate and optimum GSS-DMM U-MOS cases, respectively. This is substantially (about 3x) better than the results observed for the 30 V Si GSS-DMM D-MOS devices.

7) 1.2 kV SiC POWER MOSFET C2M0160120D PRODUCT WITH SI U-MOS DEVICES

The similar procedure can be applied to the C2M0160120D product with the values shown in Fig. 4 for the trade-off curve between saturation current and on-resistance for the various GSS-DMM U-MOS device cases. The plots shown in Fig. 9 were obtained by combining this information with the trade-off curve for short-circuit time versus saturation current in Fig. 5. The benchmark 100 V GSS-DMOS case (purple line), and data-point for the stand-alone SiC power MOSFET case are included for comparison. A t_{SC} of 10 μs

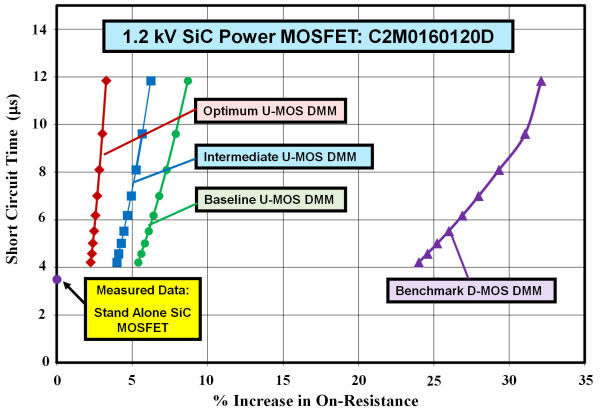

FIGURE 9. Trade-off curves between short-circuit time and increase in on-resistance for the 1.2 kV SiC power MOSFET C2M0160120D with various cases of the Si GSS U-MOS devices.

is obtained for the BaSIC(DMM) topology using the 30 V GSS-DMM U-MOS devices with 8, 6, and 3 % increase in on-resistance for the baseline, intermediate and optimum cases, respectively. This is substantially (about 3x) better than the results observed for the 30 V Si GSS-DMM D-MOS devices.

IV. CONCLUSION

The following goals of this paper cited in the introduction section were accomplished.

1) It was theoretically shown that a much better trade-off between increase in the short-circuit time and increase in on-resistance for the BaSIC(DMM) topology can be achieved by reducing the blocking voltage of the Si GSS-DMM device from 100 V to 30 V;
2) It was theoretically demonstrated that the trade-off between increase in t_{SC} and increase in R_{ON} for the BaSIC(DMM) topology can be significantly improved by reducing the channel length from 1.0 to 0.3 μm in the Si DMM cell structure;
3) It was theoretically demonstrated that the trade-off between increase in t_{SC} and increase in R_{ON} for the

BaSIC(DMM) topology can be significantly improved by reducing the gate oxide thickness from 500 Å to 100 Å in the Si DMM cell structure;

4) It was theoretically demonstrated that the trade-off between increase in the short-circuit time and increase in on-resistance for the BaSIC(DMM) topology is obtained with the trench-gate (U-MOS) Si GSS-DMM structure compared with the planar-gate (D-MOS) Si GSS-DMM structure; and
5) A significant improvement in the trade-off curve between increase in short-circuit time and increase in R_{ON} is theoretically achievable by using the proposed optimized Si GSS-DMM devices in the BaSIC(DMM) topology for two commercially available SiC power MOSFETs.

The main scientific contribution of this paper is the first analysis of Si Depletion-Mode-MOSFETs in terms of the trade-off between on-resistance and drain saturation current. The specific scientific contributions include showing for the first time the impact on performance of Si Depletion-Mode-MOSFETs of reducing the blocking voltage, channel length, and gate oxide thickness for both the DMOS and UMOS structures.

Many power semiconductor companies manufacture both silicon power MOSFETs and SiC power MOSFETs. However, they make very few depletion-mode Si power MOSFETs because applications usually require normally-off transistors. The BaSIC(DMM) topology creates a new high volume commercial opportunity for silicon depletion-mode MOSFETs when paired with SiC power MOSFETs whose market is growing rapidly for electric vehicle and industrial motor drives. The silicon depletion-mode MOSFET optimization information provided in this paper is valuable to the semiconductor power device industry to enhance the short-circuit performance of SiC power MOSFETs in these applications.

The performance improvements are theoretically quantified in this paper to encourage manufacturers to fabricate and commercialize the optimized Si GSS-DMM devices. The theoretically predicted enhanced performance in this paper cannot be experimentally validated until Si manufacturers commercialize the proposed Depletion-Mode-MOSFET device. The predicted performance enhancements described in this paper can be experimentally validated once the improved devices are manufactured and made available as products by the semiconductor companies.

Manufacturers can also build a co-packaged chip set consisting of the SiC power MOSFET device and the Si GSS-DMM device to make the BaSIC(DMM) composite transistors. These transistors will provide the desired 10 μs short-circuit capability for SiC power MOSFETs, needed in motor control applications within electric vehicles and industrial drives that is not presently provided by stand-alone SiC power MOSFET products. In addition, the BaSIC(DMM) topology has been previously shown to enable efficient on-state current monitoring and short-circuit detection by using a sense terminal connected to the drain of the Si GSS-DMM device [12]. It can be applied to SiC power MOSFETs with over a broad range of voltage and current ratings to create a versatile technology that can enhance the utilization of SiC power MOSFETs in industrial and transportation applications.

The BaSIC(DMM) topology has also been used to improve the short-circuit capability of GaN HEMT devices [20]. The available 100 V Si GSS-DMM IXYS product was used for that work. The short-circuit time was improved from 0.33 μs to 4.5 μs using the BaSIC(DMM) topology with 29 % increase in on-resistance. Using the optimum Si DMM U-MOS device described in this paper will reduce the increase in on-resistance to only 2.5 % to achieve a short-circuit time of 4.5 μs for the GaN HEMT device. The optimization performed for the Si DMM device in this paper is therefore very useful for enhancing the performance of GaN power transistors as well. It is noteworthy that the increase in on-resistance of less than 5 % achieved with the BaSIC(DMM) topology using the optimized Si DMM devices is within the typical to maximum variation of on-resistance in datasheets for SiC and GaN power FETs.

In addition, the BaSIC(DMM) topology has been shown to improve the trade-off between the on-state voltage drop and short-circuit capability of Si IGBTs designed with low on-state voltage drop [21]. These results were reported using the available 100 V Si GSS-DMM IXYS product. Using the optimum Si DMM U-MOS device described in this paper will significantly improve the trade-off between short-circuit capability and on-state voltage drop for the Si IGBTs as well.

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