Multistep Transitions From Microstrip and GCPW Lines to SIW in 5G 26 GHz Band

ALFONSO GÓMEZ GARCÍA[ID], **YOLANDA CAMPOS-ROCA**[ID],
RAFAEL GÓMEZ ALCALÁ[ID], **(Member, IEEE),**
AND JESÚS RUBIO[ID]

Departamento de Tecnologías de los Computadores y de las Comunicaciones, Escuela Politécnica, Universidad de Extremadura, 10003 Cáceres, Spain

Corresponding author: Alfonso Gómez García (alfonsogg@unex.es)

ABSTRACT Substrate integrated waveguides (SIW) are a topic of interest for many researchers, due to their power handling capabilities and compatibility with planar processing techniques. These advantages make this technology an attractive candidate for fifth generation of cellular networks applications (5G). Thus, transitions from more common planar technologies to SIW have been designed to obtain a good performance. Several techniques have been used in these transitions, from the use of via holes as probes to the inclusion of lumped elements. We propose the use of cascaded linear tapers as a multistep transition in order to obtain a better performance, optimizing the designs for the 5G $n258$ band. As result, several transition configurations are optimized, measured and compared to simulations. The design process is performed using an heuristic approach, by just increasing the number of iterations. The optimization of sixteen transition topologies (four different configurations, with four different numbers of steps), is carried out by electromagnetic simulation in CST Microwave Studio. A comparison between the response of the different designs, and the number of iterations used to obtain them, is also presented. Simulations with an in-house full-wave solver are performed to validate the transitions. All the transitions have been manufactured in a low-cost single-layer printed circuit board technology on Rogers 4003C. A microstrip-to-SIW 4-step configuration, tested as a back-to-back prototype, exhibits an insertion loss between 2.0 dB and 2.2 dB and a return loss better than 20 dB dB, from 24.25 GHz to 26.5 GHz, including the effect of the end-launch connectors. Another GCPW-to-SIW 3-step configuration, tested also as a back-to-back prototype, experimentally shows from 24 GHz to 26.5 GHz a minimum return loss of 13 dB, and an insertion loss between 2.6 dB and 2.9 dB. The overall performance of the sixteen configurations validates the usefulness of the proposed design process.

INDEX TERMS Substrate integrated waveguide (SIW), microstrip, grounded coplanar waveguide (GCPW), fifth-generation cellular networks (5G), planar transition, multistep taper, single-layer printed circuit board (PCB).

I. INTRODUCTION

Substrate integrated waveguides (SIW) have been a topic of interest in the recent years, since they combine the high-power capabilities of traditional rectangular waveguides with standard planar fabrication techniques, such as those used in printed circuit boards (PCBs). Their design is based on the use of metallized via holes that connect the two metal layers of a dielectric substrate, where these via holes must comply with

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size and separation rules [1], [2]. If these rules are met, then the SIW has a perfect equivalence to a traditional rectangular waveguide in the monomode TE_{10} band [3].

SIW-based circuits and antennas have extensive applications in microwave and millimeter-wave bands. With the emergence of fifth-generation (5G) cellular networks, new opportunities and challenges related to the use of this technology arise, with low-cost solutions being also a priority to develop successful large-scale commercial solutions. Since SIW is a planar compatible technology, transitions operating in 5G frequency bands will be required to interface

with other common planar technologies, such as microstrip, coplanar waveguide (CPW) or grounded CPW (GCPW). Although some experimental examples of microstrip-to-SIW and GCPW-to-SIW transitions operating in K-band have been proposed [4]–[10], there is still a research gap in terms of obtaining a better performance at a lower cost. For example, [5] requires multilayer manufacturing, which increases manufacturing complexity and cost in comparison to a single-layer standard PCB technology. And, in the case of [7], [8], the RT/Duroid 5880 substrate is used, which has very low dielectric losses, but a high price in comparison to other alternatives. Therefore, there is a need to establish a generic procedure applicable to single-layer designs, with independence of the chosen substrate.

Equations to calculate the correct length and width of a microstrip taper as a transition to SIW were presented in [7]. There are improvements to the basic taper transition, such as locating via holes at a certain distance from the center of the transition [11], using lumped elements [12], introducing an additional taper element to increase the adaptation [13], using exponential curves for the taper instead of linear ones [14], or even using a fork structure with a tuning via to excite a resonant slot etched in one of the SIW metallic layers [15].

Transitions from CPW, and its alternative GCPW, have also been designed and reported. Although some designs used a probe transition from GCPW to SIW [4], [5], the use of coupling slots, with in some cases a quarter-wavelength stub, has been widely reported in the literature [6], [8], [10], [16]–[18]. There have been examples of using a GCPW taper for both the central conductor and the adjacent etched surfaces, in a similar fashion to the microstrip taper [9], [19]–[22]. This taper has also been improved using a V-slot in the final section of the space between conductors [23].

Many of the cited previous work use one step in their transition design, that is, they only have an initial dimensional state, and a final one. Over the years, there have been reports of using multistep transitions between microstrip and CPW lines, where various increments in width values are used [24]–[26]. In these examples, discrete width increases are used to adapt the technologies, producing a staircase like structure. These same ideas have also been used to create transitions to SIW [27], [28].

In this work, we present a methodology for the design of high-performance transitions from microstrip and GCPW lines to SIW. This methodology is based on full-wave optimizations on multistep topologies using tapers to vary from one width to the next one, and has been applied in the design and comparison of several multistep transitions. Different configurations of the transitions, with different step count, are simulated and optimized for the 5G *n*258 band, using CST Studio Suite 2019 [29]. These multistep transitions are the result of an heuristic approach, increasing only the number of iterations used in the optimization, and not the complexity of the process itself. The designs are compared

to the obtained results of an in-house Finite Element Method (FEM) full-wave solver, and are validated with experimental measurements. For this purpose, back-to-back circuits for all the transitions have been manufactured in a single-layer PCB technology on low-cost Rogers 4003C substrate. Finally, the improvements and incremental computational costs of adding these extra steps is discussed and rated, and the results are assessed in the light of the literature.

II. DESIGN OF MULTISTEP TRANSITIONS

Tapers are used to create a continuous variation of impedance between two different values. Their length is related to frequency, since quarter-wavelengths are usually recommended, providing a maximum adaptation at a certain frequency point [7], [13]. Even with the multiple improvements seen in the literature over the basic transition described in [7], [17], very few scientific works use more than one taper. In [13], two microstrip tapers (one with a linear variation and one with an exponential variation) were used to increase the adaptation in a band. In this work, we propose the use of several cascaded linear tapers as a multistep transition to increase adaptation in the 24.25 GHz to 27.5 GHz band, which corresponds to the *n*258 band of 5G New Radio (5G NR) [30]. The selected substrate is RO4003C ($\varepsilon_r = 3.55$, $\tan \delta = 0.0027$), due to its reduced price compared to other substrates, with a height of 0.508 mm and a 35 µm copper thickness.
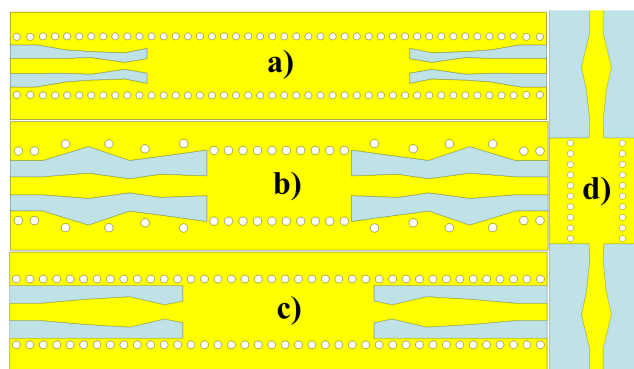
FIGURE 1. Models of the studied types of transitions, with four linear tapers cascaded: a) GCPW Enclosed, b) GCPW Line, c) Microstrip Enclosed, d) Microstrip Line.

We will examine the use of two planar technologies, microstrip and GCPW lines, in two different configurations: with the linear tapers being within the SIW (these cases will be called "enclosed"), and with the linear tapers being outside the SIW (which will be called "line"). Fig. 1 shows a top view of four of the different models studied, each one using a cascade of four different linear tapers. The GCPW enclosed configuration, Fig. 1.a, is inserted within a 4.0 cm long SIW. On the other hand, the microstrip enclosed configuration, Fig. 1.c, is embedded within a 3.6 cm long SIW. The line configurations, Fig. 1.b and Fig. 1.d, connect to a 1.0 cm long SIW, with 10 pairs of via holes.
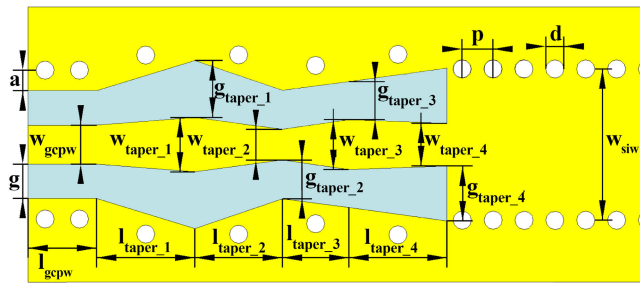
FIGURE 2. Dimensions used in the design of the 4 step GCPW line to SIW transition.

Fig. 2 illustrates the physical meaning of each dimension, using a 4 step GCPW line to SIW transition as basis. All the studied designs have a 2.0 mm 50 Ω line as feeding point (length denoted as l_{gcpw} if it is a GCPW transition, or l_{micro} if it is a microstrip one). This impedance corresponds to a microstrip width of 1.151 mm (w_{micro}), while the central conductor of the GCPW has a width of 1.132 mm (w_{gcpw}) with a separation between conductors of 1.0 mm (g). The separation between the outer conductor border in the 50 Ω line section and the additional via holes is 0.6 mm (a). The SIW width between the via holes center is 4.4 mm (w_{siw}), with a via diameter of 0.6 mm (d) and a via pitch of 0.9 mm (p).

The width of each taper (w_{taper}) will be specified at the end of it, starting from the 50 Ω line. In the case of the GCPW transitions, the same criteria will be applied to define the separation between conductors (g_{taper}). The length of each linear taper will be denoted as l_{taper}. Microstrip designs follow the same taper naming convention, therefore, an illustrative figure is omitted. In the specific case of the GCPW line configurations, an additional via hole is placed in each taper step at its middle point in terms of length.

In [20], it can be observed that the GCPW taper has a maximum total end width similar to that of the SIW. Furthermore, it can be extracted that the width of the central conductor and the separation between conductors (gap width) share a similar value, with less than a 3 percent difference between them. Therefore, we initially set the end separation between conductors to 1.35 mm and the central conductor end width to 1.4 mm as the starting point for the GCPW taper dimensions. In the case of the microstrip designs, the formulas provided in [7] will be used as starting point, obtaining a recommended taper width of 0.85 mm. The starting length for both the microstrip and GCPW taper will be $\lambda_g/4 = 2.40$ mm (calculated at 26 GHz in the interior of the SIW). All the tapers used in the different steps will share the same starting dimensions.

Each one of the taper variables will be optimized using the genetic algorithm provided with CST Studio Suite 2019. We will set as goals to minimize insertion losses, while maximizing return losses at the same time. Simulations will consider losses in both the dielectric substrate and the copper conductor. A comparative study of the total number of

iterations used in each optimization process will be conducted in the next section.

Each one of the taper variables will be optimized using the genetic algorithm provided with CST Studio Suite 2019. We indicate the genetic algorithm of CST to simulate 30 generations, with 16 individuals per variable optimized. The genetic algorithm determines the maximum number of iterations from these two parameters as the result of $(m + 1) \cdot n/2 + 1$, where m represents the number of generations and n the number of individuals per generation. An HP Z2 SFF G4 Workstation, with an Intel(R) Xeon(R) E-2176G CPU (12 CPUs @ 3.7 GHz) and 128 GB RAM, will be the computing unit. The CST frequency domain solver will be used, with a minimum precision of 25 meshcells per wavelength. We will set as goals to minimize insertion losses, while maximizing return losses at the same time. The optimizer will use a sum of all goal criteria to evaluate the total performance of each iteration. Simulations will consider losses in both the dielectric substrate and the copper conductor. A comparative study of the total number of iterations used in each optimization process will be conducted in the next section.

III. OPTIMIZED MULTISTEP TRANSITIONS

Before we discuss the optimized results obtained for each configuration, we will introduce how they will be presented. For each configuration, we will study the use of one to four cascaded linear tapers. This number of linear tapers used in each case will be referred to as the number of steps. Each design will be named after the number of steps used, the technology it uses (microstrip or GCPW), and its configuration (enclosed or line). Therefore, a microstrip with an enclosed configuration that uses two cascaded linear tapers will be a 2 step microstrip enclosed transition. We will present a comparative plot of all the obtained S-Parameters for the analyzed step counter for each configuration. A table with all the different values of width and length used for each linear taper will also be presented. These values will be grouped by step counter, with a number designating its correspondence with the variables shown in Fig. 2. The total number of iterations used in the optimization process to obtain the presented results will be included in said table.

Additional simulations with an in-house FEM full-wave solver [31] are performed in order to validate the optimized designs. The analyzed mesh and the solver characteristics differ from the ones used by CST Studio Suite 2019, and as such, some discrepancies between these results and the ones obtained with CST are to be expected.

A. GCPW ENCLOSED
The optimized results for the GCPW enclosed configuration can be observed in Fig. 3. It can be easily noted how the $|S_{11}|$ is greatly reduced to −35 dB with the 2 step transition, while using 3 steps decreases the magnitude to a maximum value of −45 dB in the 24.25 GHz to 27.5 GHz band of study. The insertion losses in the band achieve a maximum value of 1.3 dB at 24.25 GHz in the 1 step case. It can be seen
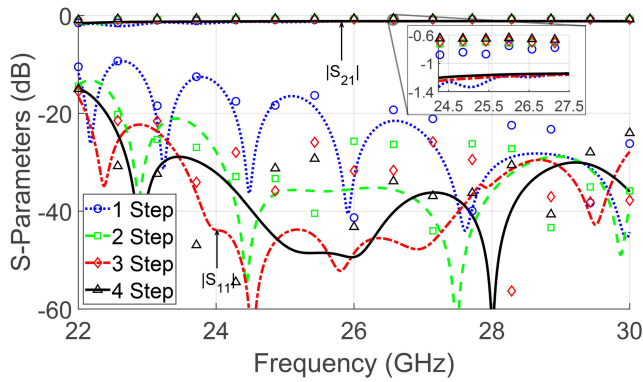
FIGURE 3. S-Parameters magnitude of the simulated GCPW enclosed configurations, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. The lines correspond to the results obtained with CST Studio Suite 2019, while the discrete symbols correspond to the in-house full-wave solver.

FIGURE 4. S-Parameters magnitude of the simulated GCPW line configurations, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. The lines correspond to the results obtained with CST Studio Suite 2019, while the discrete symbols correspond to the in-house full-wave solver.

how the highest insertion losses correspond to the 1 step case, due to its worse value in terms of return losses. Since, in this configuration, the distance between the feeding points remains constant independently of the step number, the main variation in $|S_{21}|$ comes from the different $|S_{11}|$ values.

The results obtained by the in-house full-wave solver follow the tendency of the CST results, i.e., the return losses in the *n*258 band are lowered with the additional steps. The difference between the solvers is prominent for the 3 step design, which does not follow the same tendency that in the CST results. In general terms, low $|S_{11}|$ values require very few differences between meshes and analysis methodologies, which we have been unable to provide since both solvers use different approaches to model the emitted radiation. Therefore, it is to be expected that longer transitions exhibit higher discrepancies.

TABLE 1. Dimensions (in *mm*) and number of iterations of the simulated GCPW enclosed configurations.

Steps used	w_{taper}	l_{taper}	g_{taper}	No. of iterations
1	$1^{st} = 2.118$	$1^{st} = 1.035$	$1^{st} = 1.132$	1117
2	$1^{st} = 0.601$	$1^{st} = 2.454$	$1^{st} = 0.584$	1489
	$2^{nd} = 1.280$	$2^{nd} = 1.562$	$2^{nd} = 0.858$	
3	$1^{st} = 1.461$	$1^{st} = 2.842$	$1^{st} = 0.722$	2223
	$2^{nd} = 0.622$	$2^{nd} = 2.370$	$2^{nd} = 0.847$	
	$3^{rd} = 1.102$	$3^{rd} = 1.578$	$3^{rd} = 0.964$	
4	$1^{st} = 1.109$	$1^{st} = 2.122$	$1^{st} = 0.643$	2977
	$2^{nd} = 1.253$	$2^{nd} = 1.899$	$2^{nd} = 0.438$	
	$3^{rd} = 0.526$	$3^{rd} = 2.530$	$3^{rd} = 0.712$	
	$4^{th} = 1.079$	$4^{th} = 1.653$	$4^{th} = 0.765$	

Table 1 exhibits the optimized dimensions obtained for the GCPW enclosed designs. The maximum CPU time per iteration has been measured to be 9 minutes in the case of the 4 step design. We should note that we use more iterations per variable optimized in all the 1 step cases, since these designs are considered to be closer to the transitions presented in the literature. Obtaining the best possible performance in these cases will allow for a fairer comparison to the literature.
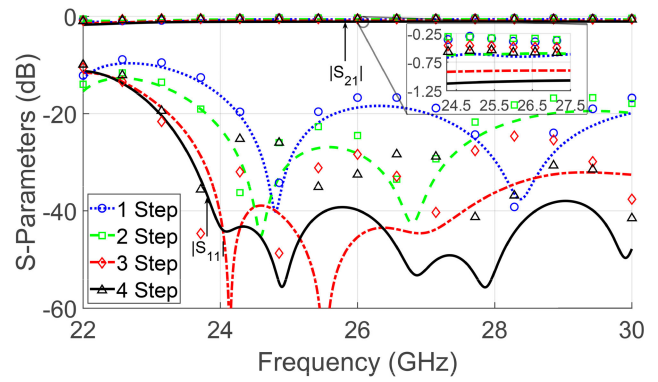
B. GCPW LINE

Fig. 4 shows the optimized results of the GCPW line configurations. In this case, the 1 step design provides a better performance in terms of matching than its GCPW enclosed counterpart. There is also a significant increase in adaptation with the 3 step design, with a maximum value $|S_{11}|$ value of -38.92 dB in the *n*258 band. The 4 step variation improves this value to a maximum of -39.24 dB. The insertion losses have a maximum value of 1.1 dB for the 4 step case. Since in this configuration, the higher the number of steps used implies a longer design, it is logical to have higher insertion losses in the 4 step design.

The results obtained by the in-house full-wave solver follow the tendency of the CST results, showing better return loss performance for an increasing number of steps up to the 3 step case. In this case, the 4 step design achieves similar $|S_{11}|$ values to the 3 step design, a tendency also shared with the CST results.

**TABLE 2.** Dimensions (in *mm*) and number of iterations of the simulated GCPW line configurations.

Steps used	w_{taper}	l_{taper}	g_{taper}	No. of iterations
1	$1^{st} = 1.094$	$1^{st} = 2.320$	$1^{st} = 2.362$	1117
2	$1^{st} = 0.967$	$1^{st} = 2.037$	$1^{st} = 1.264$	1489
	$2^{nd} = 1.468$	$2^{nd} = 0.750$	$2^{nd} = 1.559$	
3	$1^{st} = 0.907$	$1^{st} = 2.634$	$1^{st} = 1.114$	2223
	$2^{nd} = 1.781$	$2^{nd} = 2.005$	$2^{nd} = 1.076$	
	$3^{rd} = 1.199$	$3^{rd} = 2.961$	$3^{rd} = 1.468$	
4	$1^{st} = 1.583$	$1^{st} = 2.867$	$1^{st} = 1.653$	2977
	$2^{nd} = 0.891$	$2^{nd} = 2.550$	$2^{nd} = 1.131$	
	$3^{rd} = 1.452$	$3^{rd} = 1.938$	$3^{rd} = 1.103$	
	$4^{th} = 1.243$	$4^{th} = 2.862$	$4^{th} = 1.603$	

Table 2 provides the optimized dimensions obtained for the GCPW line designs. The number of variables to optimize in each of these configurations is equal to their enclosed counterparts, therefore, the number of iterations per design is the same. For this configuration, the CPU time per iteration varies with the dimensions of each individual evaluation.

For the final 4 step design, it has been measured to be 8 minutes. The smaller times are explained by the reduced size of this 4 step design compared to its enclosed counterpart.

C. MICROSTRIP ENCLOSED

The microstrip enclosed configuration designs, whose optimized results are shown in Fig. 5, present low insertion losses, with a maximum value of 1.04 dB in the $n258$ band. This configuration clearly exhibits an improvement with each increment in the number of steps, obtaining less than -35 dB with 4 steps from 24.25 GHz to 27.5 GHz.
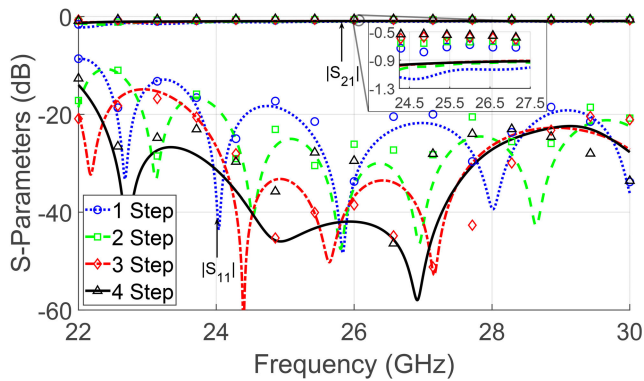
FIGURE 5. S-Parameters magnitude of the simulated microstrip enclosed configurations, with detailed zoom of the $|S_{21}|$ parameters in the $n258$ band. The lines correspond to the results obtained with CST Studio Suite 2019, while the discrete symbols correspond to the in-house full-wave solver.

Once again, the highest insertion losses correspond to the 1 step case, since it has the worst response in terms of $|S_{11}|$.

For this configuration, the in-house full-wave solver follows the tendency of the CST results, i.e., the return losses in the $n258$ band are reduced with the additional steps. The 4 step design presents the highest difference between solvers, but once again, this is to be expected. A longer microstrip transition implies a higher difference due to the different used emitted radiation model.

**TABLE 3.** Dimensions (in *mm*) and number of iterations of the simulated microstrip enclosed configurations.

Steps used	w_{taper}	l_{taper}	No. of iterations
1	$1^{st} = 1.094$	$1^{st} = 2.320$	745
2	$1^{st} = 0.850$ $2^{nd} = 1.110$	$1^{st} = 2.462$ $2^{nd} = 1.026$	993
3	$1^{st} = 2.072$ $2^{nd} = 1.232$ $3^{rd} = 1.582$	$1^{st} = 2.565$ $2^{nd} = 2.188$ $3^{rd} = 0.658$	1489
4	$1^{st} = 2.547$ $2^{nd} = 1.696$ $3^{rd} = 1.145$ $4^{th} = 1.264$	$1^{st} = 2.884$ $2^{nd} = 1.947$ $3^{rd} = 2.608$ $4^{th} = 1.463$	1985

Table 3 provides the optimized dimensions obtained for the microstrip enclosed designs. Since microstrip lines have only two design variables, width and length, the number of

iterations per step is much lower. The maximum CPU time per iteration has been measured to be 8 minutes in the case of 4 step design. Once again, we have used more iterations in the 1 step case to obtain a better transition, and perform a fairer comparison with the literature.

D. MICROSTRIP LINE

The results of the optimized microstrip line designs, shown in Fig. 6, show a good behavior with the 1 step design. Furthermore, only the 3 step design exhibits a substantial improvement over the initial design, with maximum $|S_{11}|$ values in the $n258$ band of -34.2 dB at 24.25 GHz. This configuration also creates longer designs the higher the step counter, with higher insertion losses. In this case, the 4 step insertion losses have a maximum value of 1.05 dB in the studied band.
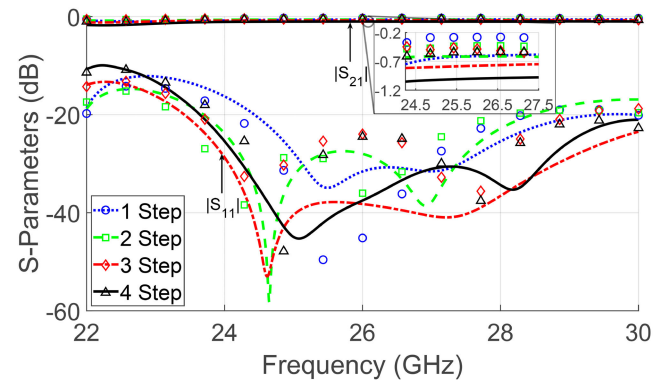
FIGURE 6. S-Parameters magnitude of the simulated microstrip line configurations, with detailed zoom of the $|S_{21}|$ parameters in the $n258$ band. The lines correspond to the results obtained with CST Studio Suite 2019, while the discrete symbols correspond to the in-house full-wave solver.

For this configuration, the results obtained by the in-house full-wave solver show higher discrepancies for the 3 step and 4 designs in terms of $|S_{11}|$ values. Once again, the differences are suspected to be related to the higher amount of emitted radiation of the microstrip sections, which the in-house full-wave solver models using a different method from that of CST Studio Suite 2019.

TABLE 4. Dimensions (in *mm*) and number of iterations of the simulated microstrip line configurations.

Steps used	w_{taper}	l_{taper}	No. of iterations
1	$1^{st} = 3.115$	$1^{st} = 1.012$	745
2	$1^{st} = 0.894$ $2^{nd} = 1.670$	$1^{st} = 1.609$ $2^{nd} = 1.175$	993
3	$1^{st} = 1.543$ $2^{nd} = 0.832$ $3^{rd} = 1.750$	$1^{st} = 3.642$ $2^{nd} = 3.214$ $3^{rd} = 1.027$	1489
4	$1^{st} = 1.699$ $2^{nd} = 2.044$ $3^{rd} = 0.961$ $4^{th} = 1.456$	$1^{st} = 3.106$ $2^{nd} = 2.958$ $3^{rd} = 2.308$ $4^{th} = 1.225$	1985

Table 4 provides the optimized dimensions of each microstrip line design. The number of variables optimized does not vary from the microstrip enclosed configuration,

therefore, the same number of iterations has been performed. In this case, the CPU time per iteration varies with the dimensions of each individual evaluation. For the final 4 step design, it has been measured to be 6 minutes. Once again, the smaller times are explained by the reduced size of the 4 step design compared to its enclosed counterpart.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, we will provide a comparison between simulations of the designed circuits with attached connectors, and measurements of them. For this purpose, an N9918A Keysight FieldFox Handheld Microwave Analyzer, specified up to 26.5 GHz, will be used. The used RF-cables (models N9927-60024 and N9927-60025) and electronic calibration module (model N7555A), both supplied also by Keysight, share the same upper frequency limit. The end launch connectors used have been manufactured by Southwest (models no. 292-05A-6 and 292-06A-5), and have been provided with a recommended layout for the microstrip and GCPW connection. In the case of the GCPW, this recommended layout uses a central conductor width of 0.6858 mm and a separation between conductors of 0.1778 mm. An additional transition has been made for the GCPW configurations, using a 4.31 mm long linear taper to connect these two 50 Ω GCPW lines. In the case of the microstrip enclosed configuration, the central microstrip line has been extended 6.0 mm out of the SIW to recreate the recommended layout for the end launch connector.
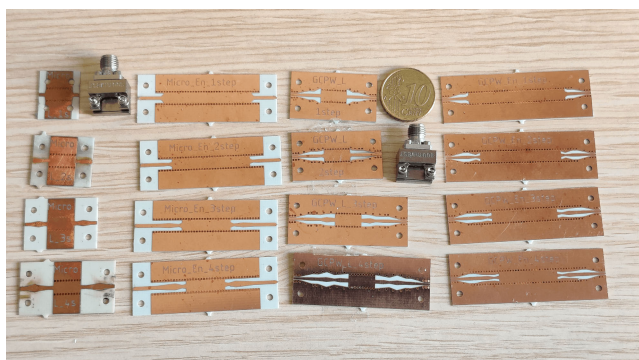
FIGURE 7. Photograph of the fabricated back-to-back prototypes with the used coaxial connectors.

All the presented transitions have been fabricated and measured with the specified equipment. Fig. 7 shows a detail of all the fabricated back-to-back prototypes, with the end-launch connectors used for measurements. Simulations of the measurement conditions, using a simplified model of the end launch connectors and realistic values of the copper roughness [32], have also been realized. The roughness value has not been considered in the optimization process due to its massive impact in terms of computation times. This self-built simplified model allows not only to approximate the simulations to the actual measurement, but also to real applications where end-launch connectors have to be used.
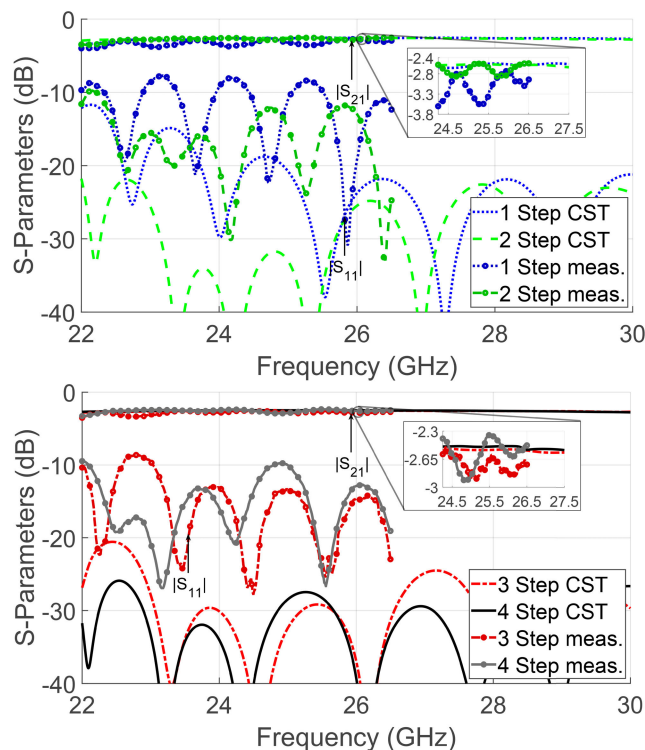
FIGURE 8. Simulated and measured S-Parameters of the GCPW enclosed transitions, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. Upper graph with 1 and 2 steps, lower with 3 and 4 steps.

The performed measurements will be compared with these simulations.

A. MEASUREMENTS RESULTS

Fig. 8-11 show the results obtained from the measurements and realistic simulations performed for the GCPW enclosed transitions, GCPW line transitions, microstrip enclosed transitions, and microstrip line transitions, respectively.

A good agreement between measurements and simulations in terms of $|S_{21}|$ can be observed. The GCPW enclosed transitions present insertion losses between 2.57 dB and 2.81 dB at 26 GHz, with a maximum difference with the simulations of 0.4 dB at the same frequency. The microstrip enclosed transitions have similar insertion losses, between 2.71 dB and 2.91 dB at 26 GHz. In this case, the difference with the simulation is less than 0.3 dB at 26 GHz. Both the GCPW line and microstrip line transitions exhibit greater insertion losses the greater the number of steps is, varying from 1.55 dB and 1.59 dB (respectively) at 26 GHz in the 1 step case, to 2.41 dB and 2.01 dB at 26 GHz in the 4 step. For all the GCPW line and microstrip line transitions, the difference with the simulations is not greater than 0.2 dB and 0.5 dB, respectively, also at 26 GHz.

In the case of the $|S_{11}|$, a difference in maximum values can be observed. This difference is to be expected, as the performed simulations are not perfect replicas of the measurement conditions, but rather an approximation.
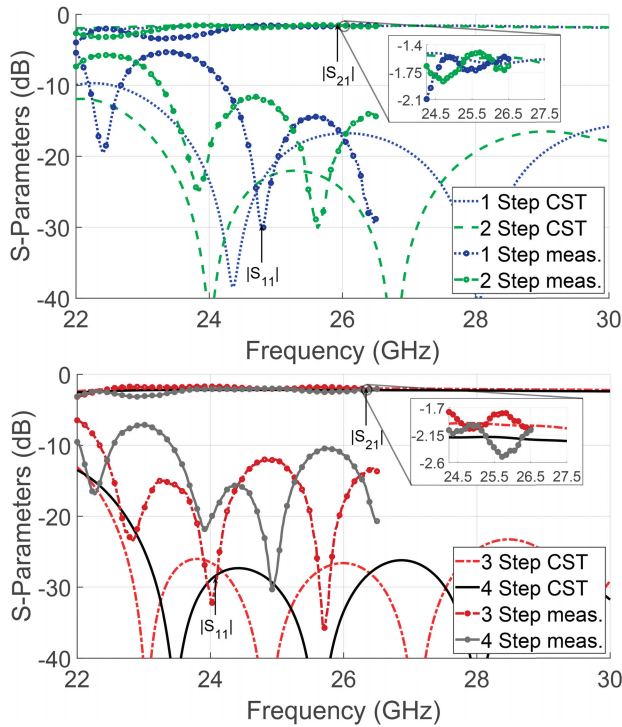
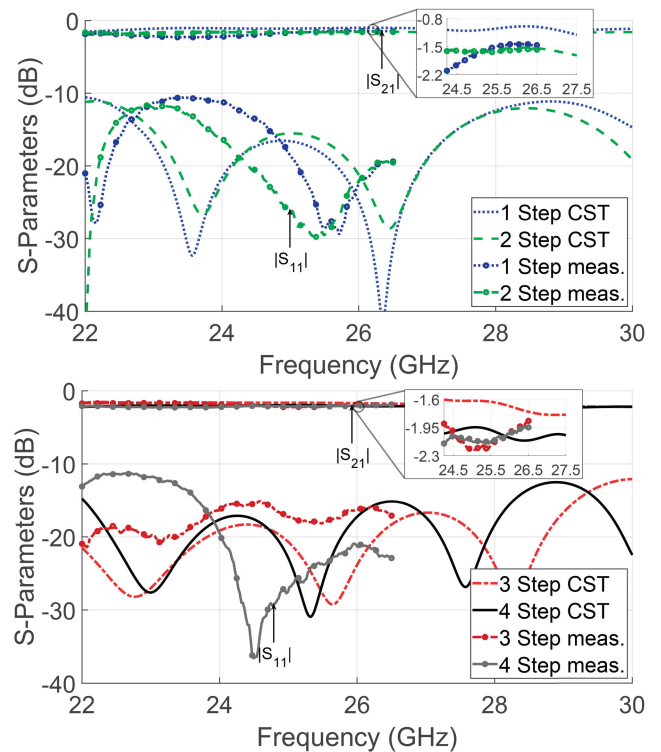**FIGURE 9.** Simulated and measured S-Parameters of the GCPW line transitions, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. Upper graph with 1 and 2 steps, lower with 3 and 4 steps.
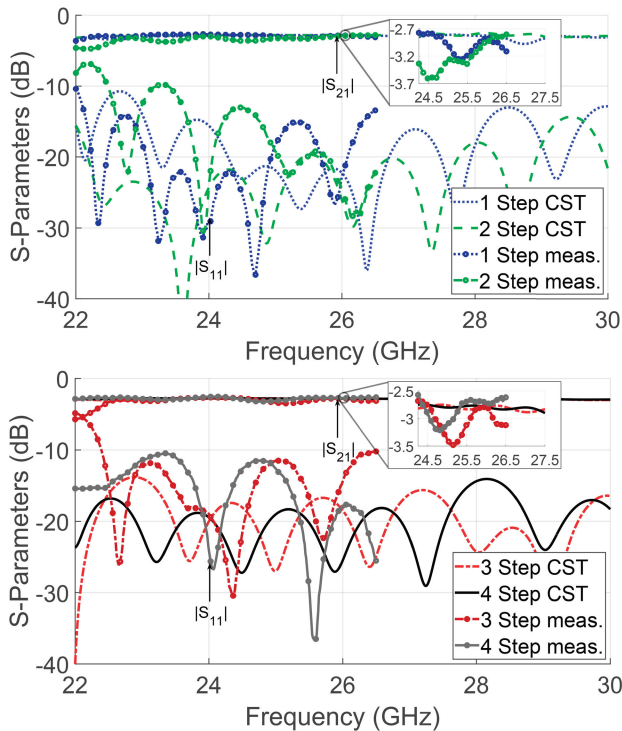
FIGURE 10. Simulated and measured S-Parameters of the microstrip enclosed transitions, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. Upper graph with 1 and 2 steps, lower with 3 and 4 steps.

The self-built 3D end-launch connector model used in the simulations has been simulated with a perfect electrical conductor (PEC), and the housing is approximated using a set of

FIGURE 11. Simulated and measured S-Parameters of the microstrip line transitions, with detailed zoom of the $|S_{21}|$ parameters in the *n*258 band. Upper graph with 1 and 2 steps, lower with 3 and 4 steps.

various boxes. The dimensions supplied by the manufacturer for the coaxial probe has been used, but the specifics of the transition from the end-launch termination to the SMA coaxial have not been provided. It can also be seen that the measurements of the GCPW transitions have higher differences from the simulations, which could be due to the higher impact of fabrication defects in coplanar structures. Nevertheless, the results show how, in general terms, a higher step number decreases the maximum value of $|S_{11}|$ in the 24.25 GHz to 27.5 GHz band, both in the measurements and in the simulations. This trend observed in the experimental results validate the tendency exposed in the simulations.

Excluding the 1 step GCPW enclosed transition, only $|S_{11}|$ levels inferior to -10 dB have been measured in the 24.25 GHz to 26.5 GHz band (due to the upper limit in frequency of the measurement equipment). Furthermore, in the case of the 2 step and 3 step microstrip line transitions, maximum values of -15 dB in the same band have been obtained, while the 4 step microstrip line configuration has a maximum value of -20 dB. The better performance of the microstrip line transitions is suspected to be related to the higher tolerance of microstrip technology to fabrication defects.

B. DISCUSSION

The presented transition design procedure, heavily based on an heuristic approach, has allowed to improve the response of

TABLE 5. Simulated performance comparison between the back-to-back prototypes of published works and this paper (ordered by published year). For this work, we include only the 3 step GCPW and 4 step microstrip enclosed designs, as they obtained the best results in terms of return losses.

Reference	Line type	Method used	Chosen substrate (ϵ_r, $\tan\delta$)	Frequency range (GHz)	Transition length	Minimum Return Loss	Maximum Insertion Loss
[4]	GCPW	Current probe	$\epsilon_r = 2.94$	$26.0 - 30.0$	$4.22\,\text{mm}$	$20\,\text{dB}$	$0.5\,\text{dB}$
[5]	CPW	Elevated-CPW	Taconic (2.33, 0.0012)	$20.0 - 28.0$	$7.19\,\text{mm}$	$16\,\text{dB}$	$1.5\,\text{dB}$
[7]	Microstrip	Linear taper	RT/Duroid 5880 (2.2, 0.0009)	$24.0 - 38.0$	$1.57\,\text{mm}$	$25\,\text{dB}$	$0.5\,\text{dB}$
[8]	Microstrip GCPW	Linear taper	RT/Duroid 5880 (2.2, 0.0009)	$17.0 - 30.0$	—	$15\,\text{dB}$ $20\,\text{dB}$	$1.0\,\text{dB}$ $0.3\,\text{dB}$
[19]	GCPW	Linear taper	RO4003C (3.55, 0.0027)	$7.0 - 14.0$	$4.08\,\text{mm}$	$15\,\text{dB}$	$0.4\,\text{dB}$
[27]	CPW	Stepped-Impedance Resonator	$\epsilon_r = 2.2$	$2.5 - 4.0$	$13.0\,\text{mm}$	$10\,\text{dB}$	$< 1.0\,\text{dB}$
[9]	CPW	Linear taper	RT/Duroid 6002 (2.94, 0.0012)	$18.0 - 28.0$	$3.18\,\text{mm}$	$20\,\text{dB}$	$1.45\,\text{dB}$
[11]	Microstrip	Linear taper-via	RT/Duroid 6002 (2.94, 0.0012)	$12.4 - 18.0$	$3.11\,\text{mm}$	$32\,\text{dB}$	$0.7\,\text{dB}$
[12]	Microstrip GCPW	Lumped elements	Taconic TLX-8 (2.55, 0.0012)	$4.1 - 5.8$	$2.80\,\text{mm}$	$10\,\text{dB}$ $20\,\text{dB}$	$1.3\,\text{dB}$ $0.8\,\text{dB}$
[13]	Microstrip	Two consecutive tapers	RO4003C (3.55, 0.0027)	$12.0 - 18.0$	$8.17\,\text{mm}$	$20\,\text{dB}$	$1.2\,\text{dB}$
[15]	Microstrip	Aperture-coupled slot	LTCC material	$47.8 - 60.0$	—	$15\,\text{dB}$	$2.0\,\text{dB}$
[23]	GCPW	Tapered V-Slot	$\epsilon_r = 9.8$	$8.0 - 12.5$	$3.70\,\text{mm}$	$15\,\text{dB}$	$0.4\,\text{dB}$
This work	Microstrip GCPW	Cascaded linear tapers	RO4003C (3.55, 0.0027)	$24.25 - 27.5$	$8.90\,\text{mm}$ $6.79\,\text{mm}$	$35\,\text{dB}$ $45\,\text{dB}$	$1.05\,\text{dB}$ $1.3\,\text{dB}$

back-to-back transitions from microstrip and GCPW lines to SIW technology. The use of a cascade of consecutive linear tapers as a multistep transition has been proved to be an effective way to enhance the obtained response in the 5G NR *n258* band. And, because it is based in consecutive linear tapers, the same design procedure can be applied to other frequency bands. With this approach, we have successfully reduced the maximum $|S_{11}|$ values from more than $-20\,\text{dB}$ to $-45\,\text{dB}$ for GCPW lines, and to $-35\,\text{dB}$ for microstrip lines, in the 24.25 GHz to 27.5 GHz band.

In the literature, similar designs to our 1 step microstrip line transitions have obtained maximum $|S_{11}|$ levels in simulations of $-20\,\text{dB}$ in a similar band [7], [11]. Improvements to these transitions, based on additional design elements such as additional vias [11], lowered this value to a maximum of $-30\,\text{dB}$, adding additional design equations to the process. In all these cases, the presented $|S_{21}|$ levels have a difference less than 0.6 dB with our results.

In the case of GCPW transitions, we can find in the literature $|S_{11}|$ levels in simulations inferior to $-20\,\text{dB}$ using probes [4], [5]. Maximum levels of $-25\,\text{dB}$ when using tapers similar to our 1 step GCPW design have been presented [19]. In the case of the $|S_{21}|$ levels, differences with our simulation not greater than 0.8 dB have been observed.

The observed differences in insertion losses between this paper and the works presented in the literature are also affected by the chosen substrate. Better insertion losses can be obtained using more expensive substrates with lower dielectric losses, such as the RT/Duroid 5880 ($\tan\delta = 0.0009$), without changing the presented design methodology. Nevertheless, the RO4003C, with its $\tan\delta = 0.0027$, has been elected as a good compromise between performance

and cost. A more direct comparison between this work and the ones presented in the literature, including differences in terms of substrate, is performed in Table 5, where it can be seen how the presented back-to-back prototypes obtain better insertion losses than some previous works with better substrates for similar frequencies. For this work, we have included the lengths and S-Parameters of the 3 step GCPW and 4 step microstrip enclosed designs in Table 5, as they have the best results in terms of return losses.

We have also seen how adding an additional step to the transition does not always produce the same enhancement in terms of S-Parameters. In some cases, we even have not been able to improve the $|S_{11}|$ levels by using 4 steps, which suggests that even more optimization iterations are needed due to the high number of variables. Therefore, the results seem to indicate that the proposed design methodology, heavily based on an heuristic approach, has a limit in terms of response enhancement per additional computational time. A comparison between the highest obtained $|S_{11}|$ levels of the enclosed and line configurations for each planar line type in the *n258* band, and the number of steps used, is carried out in Table 6. With these obtained levels, the designer can decide how many additional steps should be included, if better $|S_{11}|$ values are needed, while also considering the increase in complexity and optimization time required, and reach a compromise for each application.

As we have seen in this work, two different reference planes have been considered. The reference plane location for the optimization does not take into account the end-launch connectors, since a transition between technologies might be present at an internal position on the board, not necessarily at the edges. In these cases, we have obtained excellent values

TABLE 6. Comparison between the highest $|S_{11}|$ levels obtained with CST Studio Suite 2019 of the enclosed and line configuration for each planar line type in the *n*258 band, and the number of steps used.

Steps used	Max. Microstrip $|S_{11}|$	Max. GCPW $|S_{11}|$
1	$-18.3\,\mathrm{dB}$	$-16.5\,\mathrm{dB}$
2	$-25.0\,\mathrm{dB}$	$-26.9\,\mathrm{dB}$
3	$-33.2\,\mathrm{dB}$	$-38.9\,\mathrm{dB}$
4	$-30.6\,\mathrm{dB}$	$-36.2\,\mathrm{dB}$

in terms of $|S_{11}|$ and $|S_{21}|$. However, experimental characterization of SIW circuits with a network analyzer with coaxial ports requires compatibility to end-launch connectors. To provide a more exhaustive analysis, EM simulations at both reference planes have been presented.

The results presented in the literature can be sufficient for standard real applications, since $-20\,\mathrm{dB}$ in $|S_{11}|$ is usually considered a sufficient value. This value has been lowered in the literature using additional elements such as precisely located vias or lumped elements, which usually require additional design considerations. Nevertheless, our heuristic approach only requires an increase in the number of iterations in order to obtain better $|S_{11}|$ levels. Furthermore, if the distance between feeding points is fixed, the insertion losses do not worsen due to the increase in step number. And, since other alternatives also include an exhaustive optimization process and an increase in fabrication complexity, our design approach can be considered simple enough to obtain a better performance.

V. CONCLUSION

In this work, a novel approach to transition design from microstrip and GCPW to SIW technology has been presented, using cascaded linear tapers as a multistep transition. We have designed several transitions, each one with a different step counter and a different planar technology configuration, comparing its performance and the optimization iterations used for each design. By just increasing the number of geometrical parameters to optimize (with its correspondent increase in optimization time), the obtained $|S_{11}|$ levels have been dropped from more than $-20\,\mathrm{dB}$ to $-45\,\mathrm{dB}$ (using GCPW lines) and to $-35\,\mathrm{dB}$ (using microstrip lines) in the 5G *n*258 band, defined from 24.25 GHz to 27.5 GHz. These transitions have been fabricated, measured, and simulated with an approximation of the measurements conditions. The performed measurements and additional simulations with an in-house FEM full-wave solver validate the usefulness of the presented design process, exhibiting the same behavior as in the simulations. Comparisons of the effect of additional steps both in computational time and performance have been carried out, so a compromise between the two can be decided if a better a performance is needed. Although there are other designs procedures presented in the literature, few of them are comparable in terms of performance or cost, compatible with single-layer standard PCB manufacturing, and they introduce additional elements and complexity to the design process.

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YOLANDA CAMPOS-ROCA was born in Guitiriz, Lugo, Spain, in 1970. She received the M.S. and Ph.D. degrees in telecommunication engineering from the Universidade de Vigo, Vigo, Spain, in 1994 and 2000, respectively.

Her Ph.D. dissertation concerned the design of millimeter-wave frequency multipliers. From 1996 to 2000, she performed research stays that accumulate almost three years at the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany, either as a Guest Researcher from the University of Vigo or as a Staff Member. In 2000, she joined the University of Extremadura, Cáceres, Spain, as an Assistant Professor, and became an Associate Professor, in 2002. Her current research interests include circuit design in the microwave and millimeter-wave range and speech processing for biomedical applications.

RAFAEL GÓMEZ ALCALÁ (Member, IEEE) was born in Córdoba, Spain, in 1965. He received the degree in telecommunication engineering and the Ph.D. degree in telecommunication from the University of Vigo, Pontevedra, Spain, in 1990 and 1996, respectively.

In 1999, he moved to the University of Extremadura, Cáceres, Spain, where he is currently a Faculty Member of the Polytechnic School of Cáceres. His research interests include microwave filters and antenna design.

ALFONSO GÓMEZ GARCÍA was born in Córdoba, Andalusia, Spain, in 1994. He received the B.S. and M.S. degrees (Hons.) in telecommunications engineering from the University of Extremadura, Cáceres, in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree in electromagnetic engineering.

Since 2018, he has been a Professor Assistant with the Departamento de Tecnología de Computadores y Comunicaciones, University of Extremadura. His research interests include applications of a finite element/modal analysis method for microwave circuits and antennas, and the design and characterization of SIW-based microwave antennas and circuits.

JESÚS RUBIO was born in Talavera de la Reina, Toledo, Spain, 1971. He received the M.S. and Ph.D. degrees in telecommunication engineering from the Universidad Politécnica de Madrid, Spain, in 1995 and 1998, respectively.

Since 1994, he has been collaborating with the Departamento de Electromagnetismo y Teoría de Circuitos, Universidad Politécnica de Madrid. He is currently working with the Departamento de Tecnología de Computadores y Comunicaciones, Universidad de Extremadura, as a Professor. His current research interests include application of the finite element method and modal analysis to passive microwave circuits problems and antennas.

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