IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 17, 2021, accepted April 27, 2021, date of publication May 3, 2021, date of current version June 8, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3077090

An Ultra-Low-Voltage Level Shifter With Embedded Re-Configurable Logic and Time-Borrowing Latch Technique

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This work was supported in part by the National Key Research and Development Program of China under Grant 2020YFB2205600.

ABSTRACT The increasing number of voltage domains along with the size of the data bus requires an exponential increase in the number level shifter (LS) circuits for signal interfacing, creating an exploding in silicon area and power consumption. Higher area-efficiency can be attained by further improving the integration density of the LS circuit. In this paper, we present a multi-function ultra-low-voltage LS with re-configurable logic with embedded time-borrowing latch. The proposed circuit is implemented on CMOS 45nm technology. It is capable of converting the input voltage of 0.3 V to an output voltage of 1.8 V with an input frequency of 1 MHz. The proposed architecture has achieved a superior area efficiency with reduced transistors number of 2.4× and reduced power delay product (PDP) of 4.65× compared with its discrete logic block level implementation when the input voltage, output voltage, and the input frequency are 0.3 V, 1.8 V, and 1 MHz, respectively. The average propagation delay and power consumption are 52.7 ns and 34.6 nW, respectively.

INDEX TERMS Level shifter, ultra-low-voltage, embedded re-configurable logic, time-borrowing latch technique.

I. INTRODUCTION

Multiple-supply-voltages technique is widely used in energy-constrained system-on-chips (SoCs), where level shifter (LS) is required to interface logic signal across different supply domains [1]. As the number of LS circuits increases exponentially with the increasing number of power domains and data bus, this leads to extravagant area and power consumption [2]–[6]. Therefore, it is pivotal to propose a multi-functional LS circuit to achieve a significant breakthrough in area and power consumption reduction.

The current state-of-the-art LS circuits are optimized to interface between the ultra-low supply voltage (hundreds of mV) to I/O supply voltage (1.2-to-3.3 V) while minimizing power-delay-product (PDP) [7]–[16]. Although highly optimized PDP LS circuits with a wide supply operating range [12]–[16] have been reported, there is still a lack of LS circuits focusing on functionality integration.

Several state-of-the-art designs [3], [17]–[19] have integrated LS circuits with a latch or flip flop to further reduce the area. However, these LS circuits are unable to handle the timing variation problems under the ultra-low supply voltage situation. Thus, LS circuit with time-borrowing latch capability [20]–[22] seems to be a suitable circuit topology to relax the timing requirement. Therefore, it is worthwhile to further optimized the integration density of LS circuit by incorporating the combinational logic with time-borrowing latch capability, as shown in Fig. 1.

In this paper, we have proposed a multi-input LS embedded with re-configurable logic and time-borrowing latch. As a proof of concept, the proposed structure has incorporated NAND and NOR logic operations. The time-borrowing technique prevents timing error, enabling the design to operate at a higher frequency while improving its tolerance against the process, voltage, and temperature (PVT)

The associate editor coordinating the review of this manuscript and approving it for publication was Vyasa Sai.

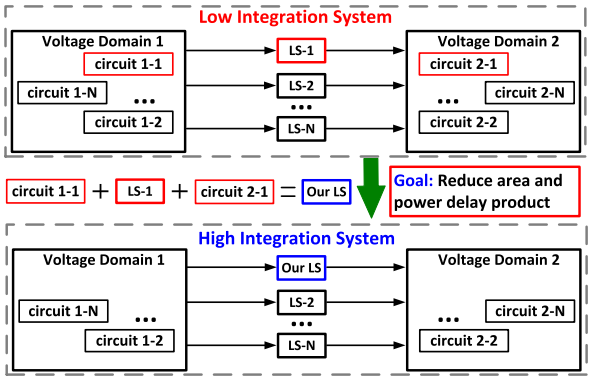

FIGURE 1. Concept of high integration system using LS circuit with embedded logic.

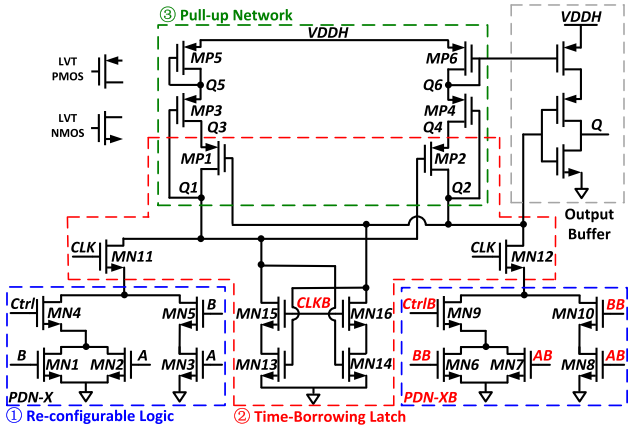

FIGURE 2. Schematic of the proposed level shifter.

variations [23]–[27]. The proposed structure is implemented on CMOS 45nm technology. With a minimum input voltage V_{DDL} of 0.3 V and the maximum output voltage V_{DDH} of 1.8 V at the input frequency of 1 MHz, it achieves a power consumption of 34.6 nW, which is a reduction of 18×, comparing with its discrete logic implementation. Furthermore, its best performing PDP is 1823.4 nW·ns, which is a reduction of 4.65×.

The rest of this paper is organized as follows: Section II presents the architecture of the proposed LS circuit. Section III details the simulation results of the proposed design, followed by a comparison with its discrete implementation. Section IV draws a conclusion of our work.

II. DESIGN OF LS CIRCUIT WITH MULTI-FUNCTIONAL LOGIC AND LATCH

The schematic of the proposed LS circuit with embedded re-configurable logic and time-borrowing latch is illustrated in Fig. 2. Its discrete implementation is illustrated in Fig. 3. Fig. 4 illustrates the behavioral simulation of the proposed LS circuit, demonstrating that its functionality can be configured to perform NAND and NOR logic operations with time borrowing effect. The analysis of the LS circuit can be broken down into four parts, namely (i) re-configurable logic in the pull-down network (PDN), (ii) time-borrowing latch in

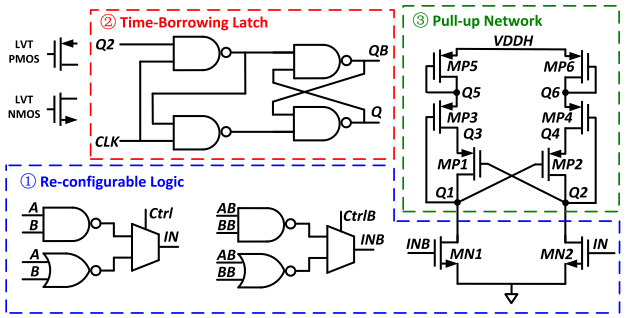

FIGURE 3. Schematic of the discrete implementation for the proposed level shifter.

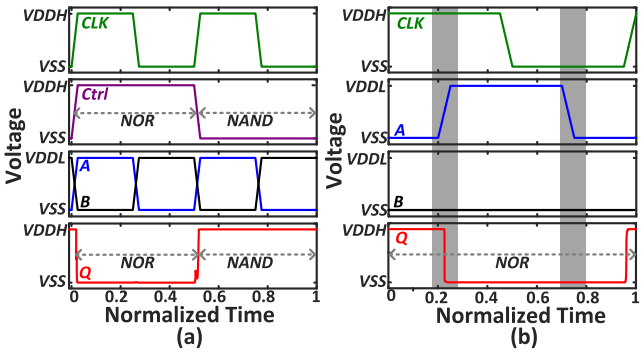

FIGURE 4. Simulation waveforms for the proposed level shifter.

the PDN, (iii) regulated cross-coupled in the pull-up network (PUN), and (iv) device selection.

A. RE-CONFIGURABLE LOGIC PULL-DOWN NETWORK (PDN)

NAND and NOR logic gates are the fundamental building blocks in digital design. Thus, it is important to demonstrate our concept of re-configurable logic LS circuit with these fundamental functionalities. Since LS circuit requires complementary input signals to perform its basic level shifting functionality, these signals are connected to two configurable PDNs, namely *PDN-X* and *PDN-XB*. The implementation of NAND and NOR logic function for *PDN-X* is simply cascaded and parallel *N*-type transistor structures, respectively. Similarly, for the *PDN-XB*, the complementary input signals are connected to parallel and cascaded *N*-type transistor structures, respectively. It is worth noting that the implementation of re-configurable logic would simply require a complementary control signal, *Ctrl*. When *Ctrl* is connected to a logic high signal, MN4 and MN9 are turned "ON" and "OFF", respectively. The *PDN-X* and *PDN-XB* function as a NOR and an OR logic, respectively. Similarly, when *Ctrl* is connected to a logic low signal, the *PDN-X* and *PDN-XB* function as a NAND and an AND logic, respectively. The proposed architecture also allows the implementation of different logic functionality into LS circuit easily.

B. TIME-BORROWING LATCH PDN

When digital logic circuit operates under an ultra-low supply voltage, the variation in delay propagation will often lead

TABLE 1. The types and physical dimensions of the transistors used in the implementation of proposed LS circuit and its discrete logic circuit.

Transistor	Type	W/L
NMOS	LVT	260 nm/45 nm
PMOS	LVT	390 nm/45 nm

to logic error. Thus, time-borrowing latching technique is introduced to eliminate the timing variation across different voltage domains. Moreover, the proposed technique combines the circuit implementation with cross-coupled *N*-type transistors to further improve switching speed and strengthen the PDN to minimize the current contention problem in cross-coupled LS architecture.

As shown in Fig. 2, the time-borrowing latch consists of cross-coupled *N*-type transistors, MN13 and MN14 to latch and store the data at nodes *Q1* and *Q2*. The circuit is latched by the complementary clock signals, *CLK* and *CLKB*, which are connected to MN11, MN12, MN15, and MN16, respectively. When the clock signal, *CLK* transits to a logic high signal (*CLKB* transits to a logic low signal), MN11 and MN12 are turned "ON". The nodes Q1 and Q2 are selectively discharged by *PDN-X* or *PDN-XB*, respectively. When the clock signal, *CLK* transits to a logic low signal, MN11 and MN12 are turned "OFF" while MN15 and MNM16 are turned "ON". The cross-coupled *N*-type transistors amplify the voltage difference between *Q1* and *Q2* to rail-to-rail voltage signals and latch it till the next transition of *CLK* and *CLKB* signals.

C. REGULATED CROSS-COUPLED PULL-UP NETWORK (PUN)

To further reduce the current contention problem while reducing the power consumption of the LS circuit, we have adopted diode-connected transistors MP5 and MP6 in the PUN [13]. Similar to [28], the *P*-type transistors MP3 and MP4 regulate the strength of the PUN, allowing faster output transition while reducing its dynamic power consumption. The cross-coupled *P*-type transistors, MP1 and MP2 amplify and latch the voltage differences between *Q1* and *Q2*.

D. DEVICE SELECTION

To achieve a competitive advantage with its discrete implementation while minimizing the overall area, we have used the smallest device sizes from the standard cell library, i.e., 260 nm (width) / 45 nm (length) and 390 nm(width) / 45 nm (length) for *N*-type transistors and *P*-type transistors, respectively. To further reduce the minimum operating supply voltage, we have selected the low voltage threshold (LVT) transistors to reduce the transistor's threshold voltage, allowing more voltage headroom to enhance the robustness of the circuit and reducing the propagation delay. The type and device dimensions of these transistors are presented in Table 1. The physical design of the proposed LS circuit is shown in Fig. 5.

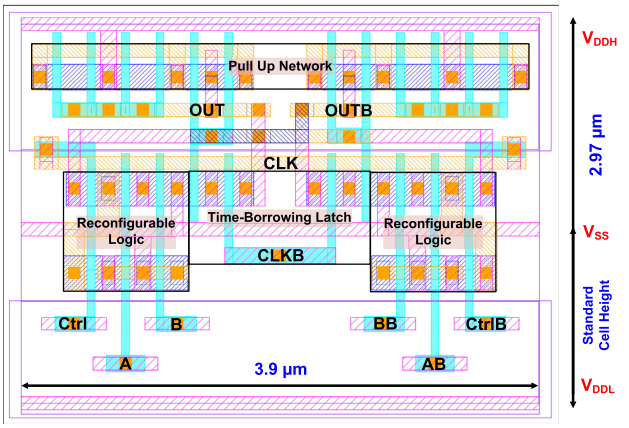

FIGURE 5. Physical Design of the proposed LS circuit.

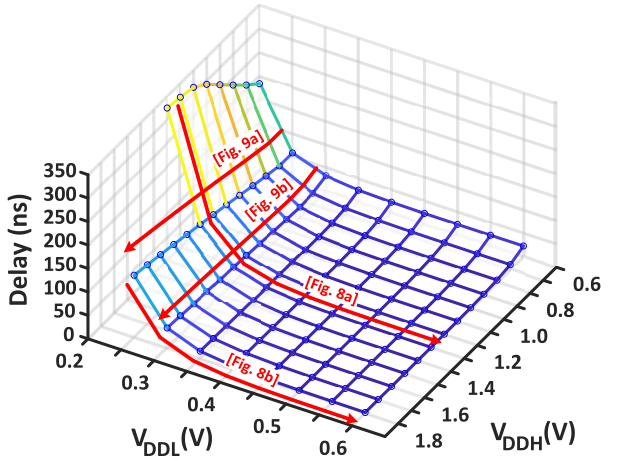

FIGURE 6. Mesh plot of proposed LS circuit's signal propagation delay as a function of supply voltages, V_{DDH} and V_{DDL}.

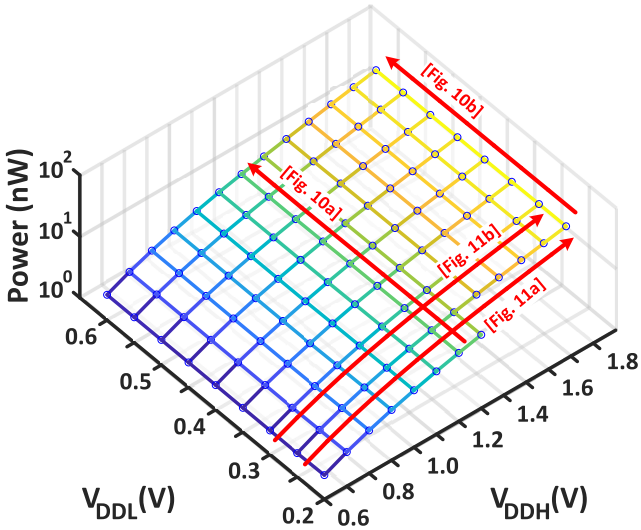

FIGURE 7. Mesh plot of proposed LS circuit's power consumption as a function of supply voltages, V_{DDH} and V_{DDL}.

III. SIMULATION RESULTS AND DISCUSSION

In this work, we have designed and verified the proposed LS circuit and its corresponding discrete circuit implementation on CMOS 45nm technology.

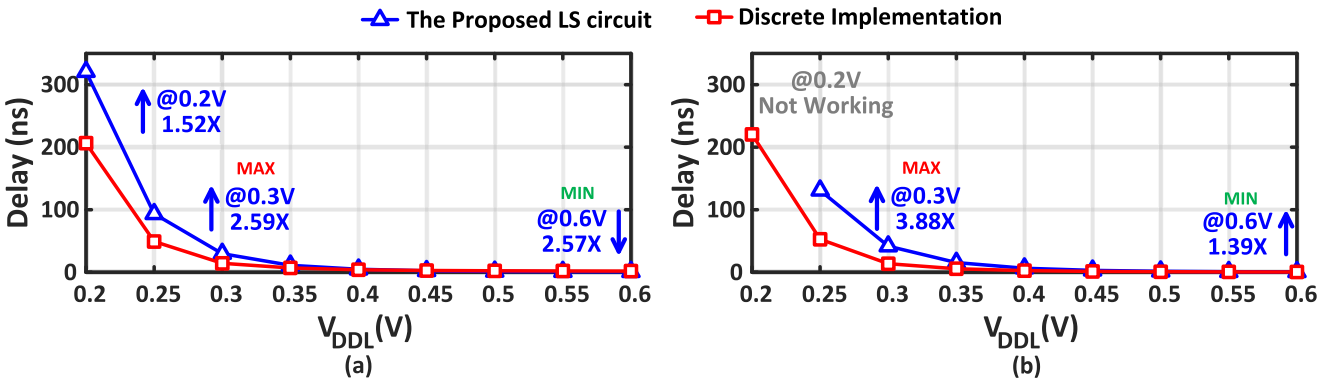

FIGURE 8. Signal propagation delay as a function of V_{DDL} at f_{IN} = 1MHz. (a) V_{DDH} = 1.2 V, (b) V_{DDH} = 1.8 V.

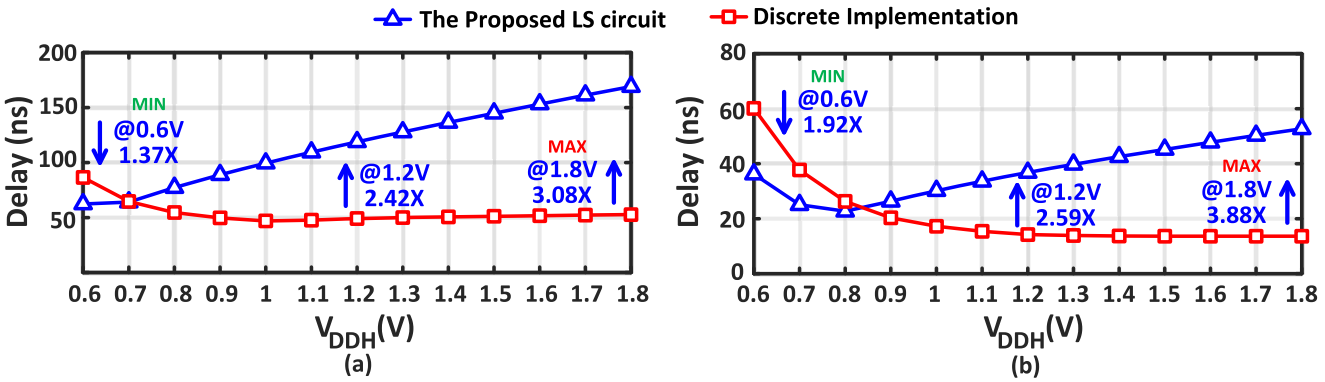

FIGURE 9. Signal propagation delay as a function of V_{DDH} at f_{IN} = 1MHz. (a) V_{DDL} = 0.25 V, (b) V_{DDL} = 0.3 V.

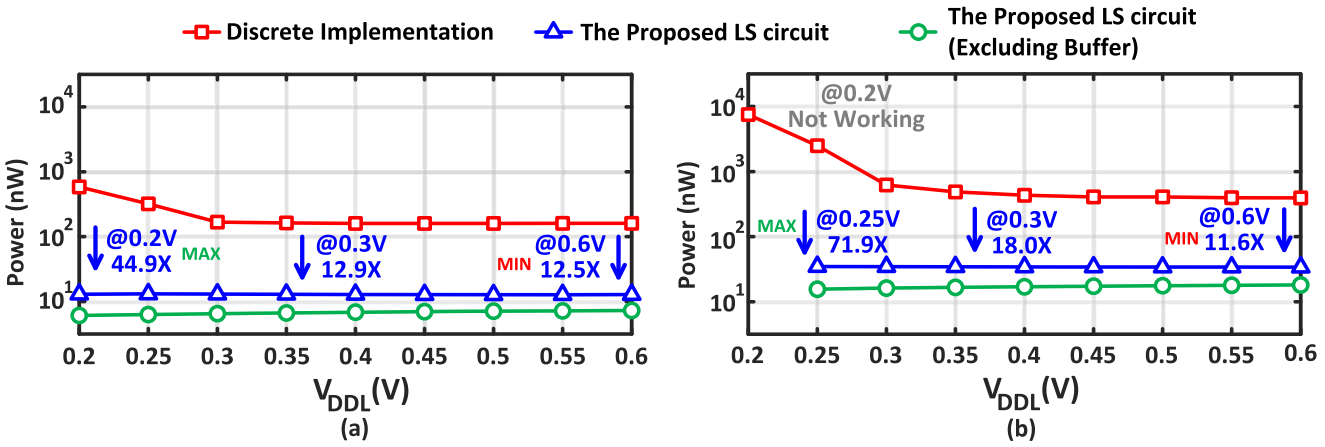

FIGURE 10. The power consumption as a function of V_{DDL} at f_{IN} = 1MHz. (a) V_{DDH} = 1.2 V, (b) V_{DDH} = 1.8 V.

To understand the performance limits of the proposed LS circuit, we perform post-layout circuit simulation and present the average propagation delay (Fig. 6) and power consumption (Fig. 7) as a function of the supply voltages, V_{DDL} and V_{DDH}.

A. PROPAGATION DELAY

The propagation delay is calculated based on the average of rising and falling propagation delays for both NAND and NOR operations. Fig. 6 illustrates the propagation delay of our proposed LS circuit with varying V_{DDL} from 0.2 V to 0.6 V and V_{DDH} from 0.6 V to 1.8 V at an operating frequency, f_{IN} = 1 MHz. Similar to the state-of-the-art designs, the propagation delay increases exponentially when the V_{DDL} or V_{DDH} decreases. Fig. 8 illustrates the propagation delay as a function of V_{DDL} with the supply voltage V_{DDH} of 1.2 V and 1.8 V, respectively. Fig. 9 illustrates the propagation delay as a function of V_{DDH} with V_{DDL}

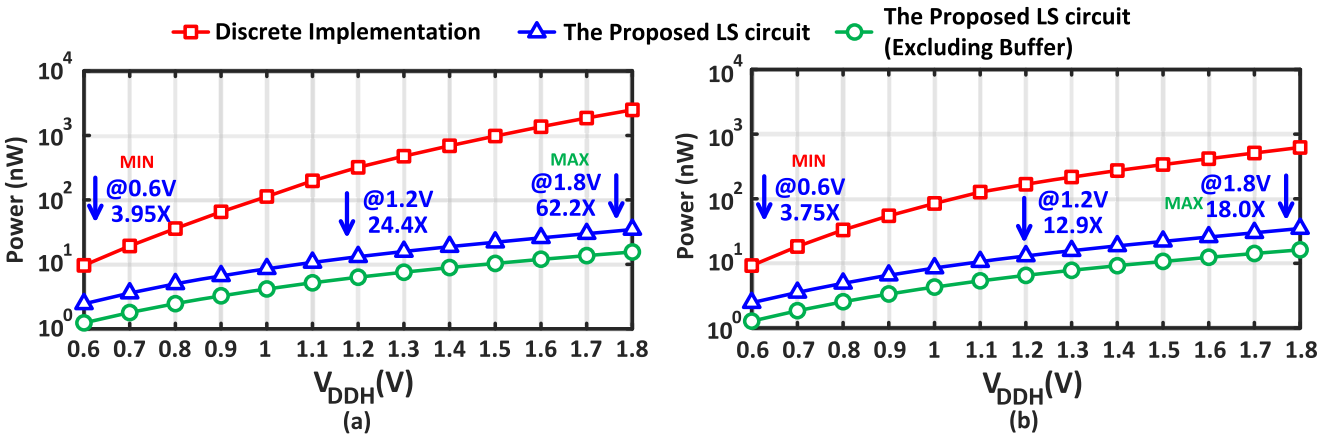

FIGURE 11. The power consumption as a function of V_{DDH} at f_{IN} = 1MHz. (a) V_{DDL} = 0.25 V, (b) V_{DDL} = 0.3 V.

TABLE 2. Comparison of the proposed LS circuit and its discrete implementation (V_{DDL} = 0.3 V, f_{IN} = 1 MHz, process of *tt* and temperature of 27°C.).

Specifications	Discrete Implementation (Fig. 3)			This Work (Fig. 2)		
Technology	CMOS 45nm					
Min. VDDL (V)[1]	0.3@V_{DDH} = 1.8 V			0.3@V_{DDH} = 1.8 V		
Transistors	60			25 (↓ 2.4×)		
Logic Operation	NAND	NOR	AVR	NAND	NOR	AVR
Total Power (nW)[2]	167	168	168	13.0 (↓ 12.8×)	13.0 (↓ 12.9×)	13.0 (↓ 12.9×)
Average Delay (ns)[2]	15.1	13.3	14.2	35.1 (↑ 2.32×)	38.5 (↑ 2.89×)	36.8 (↑ 2.59×)
Power Delay Product (nW · ns)[2]	2521.7	2234.4	2385.6	456.3 (↓ 5.53×)	500.5 (↓ 4.46×)	478.4 (↓ 4.99×)
Total Power (nW)[3]	623	623	623	34.6 (↓ 18.0×)	34.6 (↓ 18.0×)	34.6 (↓ 18.0×)
Average Delay (ns)[3]	14.5	12.7	13.6	48.5 (↑ 3.34×)	56.9 (↑ 4.48×)	52.7 (↑ 3.88×)
Power Delay Product (nW · ns)[3]	9033.5	7912.1	8472.8	1678.1 (↓ 5.38×)	1968.7 (↓ 4.02×)	1823.4 (↓ 4.65×)

[1] PVT post-simulation result. See Fig. 12.
[2] Post-simulation result with V_{DDH} = 1.2 V.
[3] Post-simulation result with V_{DDH} = 1.8 V.

of 0.25 V and 0.3 V, respectively. Even with a total stacking of six transistors in our proposed LS circuit, the propagation delay is comparable or even better than its discrete circuit implementation when V_{DDL} is greater than 0.35 V and V_{DDH} is less than 1.2 V.

B. POWER CONSUMPTION

The power consumption of the circuits are evaluated based on the average of the total power consumption under different input switching activities. Fig. 7 shows the power consumption of proposed LS circuit with varying V_{DDL} from 0.2 V to 0.6 V and varying V_{DDH} from 0.6 V to 1.8 V at f_{IN} = 1 MHz. As the V_{DDH} increased, the power consumption increased exponentially. This trend is similar to the results of its discrete implementation. Fig. 10 illustrates the power consumption as a function of V_{DDL} with V_{DDH} of 1.2 V and 1.8 V, respectively. Fig. 11 illustrates the power consumption as a function of V_{DDH} with V_{DDL} of 0.25 V and 0.3 V, respectively. The power consumption of the proposed LS circuit is significantly reduced by 44.9× for NAND and NOR operations at V_{DDH} = 1.2 V, V_{DDL} = 0.2 V and f_{IN} = 1 MHz.

C. TEMPERATURE AND VARIABILITY ASSESSMENT

To understand the variability performance and determine the minimum supply voltage, V_{DDL} of LS circuit, we have evaluated the PDP of our proposed LS circuit and its discrete implementation at different process and temperature conditions. i.e., five process corners: *ff, fs, sf, ss, tt*, and three temperatures: $-40°C$, $27°C$, $125°C$ with the input frequency of 1 MHz. The simulation results are illustrated in Fig. 12. The proposed LS shows significantly lower PDP at almost all the conditions, reducing PDP by 4.24× (*ff*, $-40°C$), 35.7× (*sf*, $-40°C$), 11.0× (*fs*, $27°C$), 4.65× (*tt*, $27°C$) and 14.2× (*ss*, $125°C$) compared to its discrete implementation when V_{DDH} = 1.8 V and V_{DDL} = 0.3 V.

D. COMPARISON AND DISCUSSION

The performance of our proposed LS circuit and its discrete implementation is summarized in Table 2. The NAND and NOR logic operations are evaluated at V_{DDL} of 0.3 V, V_{DDH} of 1.2V and 1.8 V, input frequency of 1 MHz, *tt* process corner, and temperature of 27°C, respectively. As illustrated in Table 2, the proposed LS circuit requires only 25 transistors (3 transistors for the output inverter) whereas its discrete implementation requires 60 transistors (8 transistors for the differential input LS). By integrating the logic and latch function into our proposed LS circuit, it has reduced the number of transistors by 2.4×, reducing the area significantly. Our proposed LS circuit has reduced the average power consumption by 12.9× and 18× when the input voltage is

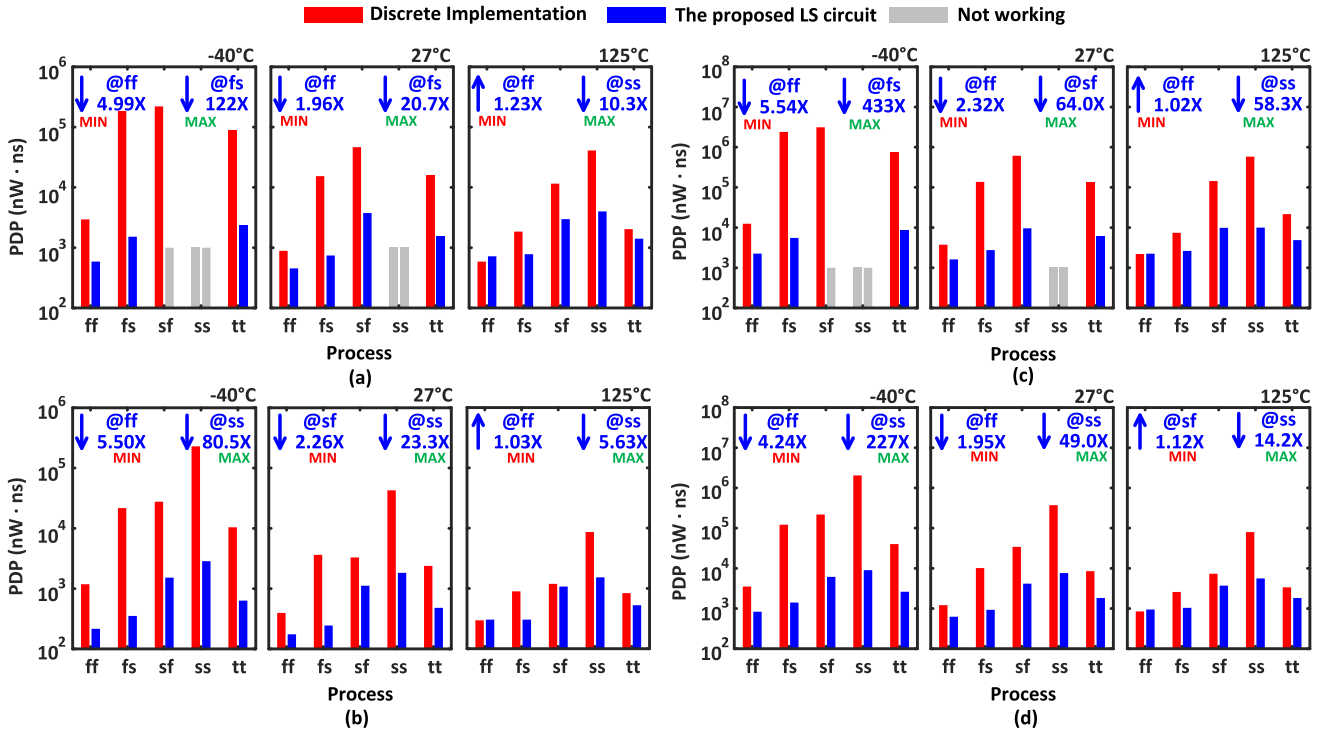

FIGURE 12. Power delay product (PDP) at different process, temperature conditions. i.e., five process corners: *ff, fs, sf, ss, tt*, three temperatures: $-40°C$, $27°C$, $125°C$ with the input frequency of 1 MHz. (a) $V_{DDH} = 1.2$ V, $V_{DDL} = 0.25$ V, (b) $V_{DDH} = 1.2$ V, $V_{DDL} = 0.3$ V, (c) $V_{DDH} = 1.8$ V, $V_{DDL} = 0.25$ V, and (d) $V_{DDH} = 1.8$ V, $V_{DDL} = 0.3$ V.

0.3 V, the output voltage is 1.2 V and 1.8 V, respectively. The average propagation delay is 36.8 ns and 52.7 ns with V_{DDH} of 1.2 V and 1.8 V. Our proposed LS circuit also achieves the lowest PDP of 478.4 nW·ns and 1823.4 nW·ns when the input voltage is 0.3 V, the output voltage is 1.2 V and 1.8 V, respectively, which is a reduction of 4.99× and 4.65× compared to its discrete implementation.

IV. CONCLUSION

In this work, we have designed an ultra-low-voltage LS circuit with embedded re-configurable logic, which is capable of carrying out two NAND and NOR logic operations with the input signals while amplifying the output signals to V_{DDH}. Besides, the timing performance against input signal arrival time variations is improved by incorporating the time-borrowing latch, enabling the design to operate at a higher frequency. Our simulation results prove that our proposed LS circuit is able to convert a minimum input voltage of 0.3 V to an output voltage max to 1.8 V when working under 1 MHz on CMOS 45nm technology. The average propagation delay and power consumption is 52.7 ns and 34.6 nW, respectively. With a reduction in number of transistors of 2.4×, power consumption of 18× and PDP of 4.65× compared to the discrete implementation, our proposed LS has higher integration density and is applicable for energy-constrained SoCs.

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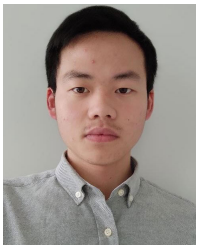

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