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Bandwidth Extension of Three-Way Doherty Power Amplifier With Reactance Compensation Using Parallel Peaking Amplifiers

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ABSTRACT This paper presents a new methodology for designing a broadband three-way Doherty power amplifier (DPA), which utilizes a reactance compensation generated by parallel peaking amplifiers to extend the bandwidth and improve the back-off efficiency. By analyzing the load impedance and efficiency of the reactance-compensated DPA, the optimal reactance at the output of the peaking amplifier required for bandwidth extension can be obtained. Then, a structure using two parallel peaking amplifiers is proposed to reduce the output reactance for the desired distribution. Using a $\lambda_0/4$ transmission line, a sufficiently large output reactance of the peaking branch can be realized at the combining point over a wider frequency band, which can compensate the effective load impedance of the carrier amplifier and improve its efficiency and bandwidth. A wideband three-way DPA is designed and fabricated to verify the proposed method. Measurement results indicate that an efficiency of 50-53% at 10 dB output power back-off and a saturated efficiency of 54-68% can be achieved over the frequency range from 1.6 to 2.7 GHz.

INDEX TERMS Bandwidth extension, Doherty power amplifier, high efficiency, reactance compensation, parallel peaking amplifier, three-way Doherty.

I. INTRODUCTION

In order to improve spectrum utilization and data transmission rate, modern communication systems often adopt complex modulation methods, which leads to modulated signals characterized by large peak to average power ratio (PAPR). Traditional Doherty power amplifiers (DPAs) can only maintain high efficiency at the 6 dB output power back-off (OPBO) [1]–[7], and cannot be applied to modulated signals characterized by large PAPR.

To meet the needs of future wireless communication systems, the DPAs that can improve the efficiency and dynamic range of OPBO are important issues in the research community [8]–[15]. Among them, three-stage and three-way DPAs have garnered significant research attention [16]–[22], which can effectively amplify the signal at larger back-off power. In [18], a broadband three-stage DPA with 40% fractional bandwidth (FBW) at the center frequency of 0.75 GHz has been presented. Then, a three-stage DPA topology based on reactance compensation for bandwidth enhancement has been exploited to achieve up to 48% FBW [21]. Recently, a dual input digitally controlled broadband three-stage DPA with back-off reconfigurability is introduced in [22]. However, the implementation of this DPA is complicated and the bandwidth is still limited. Therefore, to meet the requirements of wireless communication systems, it is of great significance to further extend the DPA bandwidth while maintaining high efficiency at large OPBO. Although the reactance compensation technique proposed in [23] can be used to extend the bandwidth, the excessive output impedance distribution of the peaking amplifier affects further expansion of its bandwidth.

To overcome this major limitation, this paper presents a novel methodology for designing a broadband three-way DPA, which employs the reactance compensation of parallel peaking amplifiers. Different from the conventional reactance compensated DPA [23], the parallel connection of the outputs

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of two peaking amplifiers can reduce the output reactance by half when the peaking amplifiers are in the off-state. After being transformed by a quarter-wavelength transmission line, the compensation reactance can distribute more concentrated at the combining point, which can benefit further bandwidth expansion. For experimental verification, a 1.6–2.7 GHz three-way DPA was designed and measured. The results show that the proposed method can further extend the working bandwidth while achieving high efficiency at OPBO.

II. ANALYSIS OF PROPOSED THREE-WAY DPA

Conventional reactance compensated DPA usually consists of two amplifiers, namely carrier amplifier and peaking amplifier, and a common load R_L, which employs a transmission line ($\lambda_0/4$, Z_T) after the peaking amplifier to compensate the effective load impedance of the carrier amplifier in the low-power region for bandwidth extension, as shown in Fig. 1 [23]. In general, a quarter-wavelength transformer ($\lambda_0/4$, $Z_{0,C}$) is used to achieve the expected load modulation for the carrier amplifier. In order to generate the appropriate compensation reactance (jX'), the output impedance of the peaking amplifier (jX) should be short-circuited or quasi-short in the low-power region [21]. However, in practical designs, with further increase of the operational bandwidth, the above requirements cannot be fully satisfied. This section first analyzes the frequency response of the reactance compensated DPA, and then obtains the optimal reactance at the output of the peaking amplifier for bandwidth extension. At last, a novel matching network topology is proposed to expand the operational bandwidth of the reactance compensated DPA.

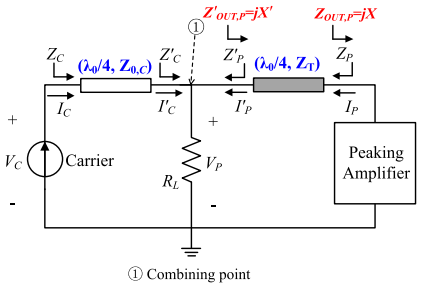

FIGURE 1. Architecture of the reactance compensated DPA.

A. ANALYSIS OF LOAD IMPEDANCE AND EFFICIENCY

Assuming that each transistor is considered as an ideal current source [24], the effective load impedance of the two amplifiers at OPBO can be expressed as the function of the parameters of impedance converter, the output impedance of the peaking amplifier and common load R_L, which can be derived as follows.

Firstly, in the low-power region, assuming that the output impedance of the peaking amplifier at OPBO (i.e., $Z_{OUT,P}$ in Fig. 1) is a reactance distributed near the short-circuit point, given by

$$Z_{OUT,P} = jX. \tag{1}$$

In Fig. 1, the quarter-wavelength transformer ($\lambda_0/4$, Z_T) performs impedance transformation from $Z_{OUT,P}$ to $Z'_{OUT,P}$, which is expressed as jX'. So, the following relationship can be inferred:

$$X' = Z_T \frac{X + Z_T \tan\theta}{Z_T - X \tan\theta}, \tag{2}$$

where Z_T is the characteristic impedance of the quarter-wavelength transformer ($\lambda_0/4$, Z_T), normally, $Z_T = Z_0$ (Z_0 is usually the optimal load impedance). And, θ is the phase delay of the quarter-wavelength transformer ($\lambda_0/4$, Z_T) at a given normalized frequency f, which can be expressed as

$$\theta = \frac{\pi}{2} \cdot f. \tag{3}$$

Then, for the reactance compensated DPA, the load impedance Z'_C can be derived as follows

$$\begin{aligned} Z'_C &= jX' // R_L = \frac{jX' \cdot R_L}{jX' + R_L} \\ &= \frac{jZ_0(X + Z_0 \tan\theta)R_L}{jZ_0(X + Z_0 \tan\theta) + R_L(Z_0 - X \tan\theta)} \\ &= \frac{jaR_L}{ja + bR_L}, \end{aligned} \tag{4}$$

where $a = X + Z_0 \tan\theta$ and $b = Z_0 - X \tan\theta$.

Considering the impedance transformation of the quarter-wavelength transformer ($\lambda_0/4$, $Z_{0,C}$), the output impedance of the carrier amplifier at OPBO is given by

$$Z_{C,OPBO} = \left|Z_{C,OPBO}\right| e^{j\theta_{C,OPBO}} = Z_{0,C} \frac{Z'_C + jZ_{0,C} \tan\theta}{Z_{0,C} + jZ'_C \tan\theta}. \tag{5}$$

Taking into account (4), the following expression arises

$$Z_{C,OPBO} = Z_{0,C} \frac{jZ_0 aR_L + jZ_0 \tan\theta (jZ_0 a + R_L b)}{Z_{0,C}(jZ_0 a + R_L b) - Z_0 aR_L \tan\theta}. \tag{6}$$

Therefore, it is possible to evaluate the drain efficiency (DE) η at OPBO, given by [24]

$$\eta_{OPBO} = \begin{cases} \frac{\pi}{4} \cos\left(\theta_{C,O\,PBO}\right) \frac{\left|Z_{C,O\,PBO}\right|}{2R_{opt}}, & \left|Z_{C,O\,PBO}\right| \le 2R_{opt} \\ \frac{\pi}{4} \cos\left(\theta_{C,O\,PBO}\right) \frac{2R_{opt}}{\left|Z_{C,O\,PBO}\right|}, & \left|Z_{C,O\,PBO}\right| > 2R_{opt}, \end{cases} \tag{7}$$

where R_{opt} is the optimum load impedance of the carrier and peaking amplifiers.

Secondly, at saturation, based on the analysis presented in [23], when the peaking amplifier is on, the quarter-wavelength transformer ($\lambda_0/4$, Z_T) simply acts as a delay line that does not affect the load modulation of the DPA. Thus, desired output power and drain efficiency can be achieved.

From (7), the back-off drain efficiency of the DPA is related to $Z_{C,OPBO}$, which is determined by X, R_L and f. Generally, $R_L = 0.5\,Z_0$ and f is the normalized frequency. So, the output

reactance X has an important influence on the back-off drain efficiency. Therefore, the next section will analyze the influence of X on the drain efficiency of the DPA to determine the optimal reactance value at the output of the peaking amplifier for bandwidth extension.

B. ANALYSIS OF OPTIMAL VALUE RANGE OF COMPENSATION REACTANCE

For anticipated Doherty load modulation over the whole operational bandwidth, the desired value of the compensation reactance X can be determined, as shown as follows.

Firstly, considering X as a degree of freedom, a set of carrier drain efficiency at OPBO can be calculated by using (6) and (7). Fig. 2 illustrates the drain efficiency as a function of normalized f and X when the DPA operates at OPBO. As shown in Fig. 2, for a specific frequency f, the larger $|X|$, the lower the drain efficiency. When X has been determined, as the frequency f deviates from f_0, the drain efficiency decreases. Therefore, the compensation reactance X should be selected appropriately to obtain better DPA performance over the entire frequency band.

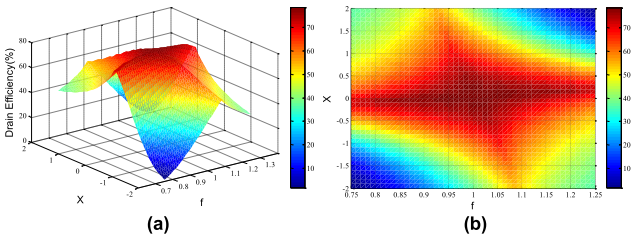

FIGURE 2. Simulated drain efficiency versus the normalized frequency and X at OPBO. (a) Stereogram. (b) Vertical view.

To determine the optimal value of X, the relationship between drain efficiency and X at different frequencies is analyzed, as shown in Fig. 3, where the red dotted line corresponds to a drain efficiency of 70%. For drain efficiency of greater than 70%, the value range of X corresponding to each normalized f can be obtained, as shown in Table 1. The results show that, for the frequency band from 0.75 f_0 to 1.25 f_0 (the relative bandwidth of 50%), the desired value range of normalized X can be determined as (–0.22, 0.22).

TABLE 1. Range of X values corresponding to the normalized frequencies.

f	0.75	0.8	0.9	1.1	1.2	1.25
X(low)	**-0.22**	-0.27	-0.41	-0.31	-0.02	0.08
X(high)	-0.08	0.02	0.32	0.41	0.27	**0.22**

For conventional two-way reactance compensated DPA [23], the output impedance of the peaking amplifier when it is in off-state within 50% relative bandwidth was obtained, as depicted in Fig. 4, where the shaded area is the desired value range (–0.22, 0.22). From this figure, it is

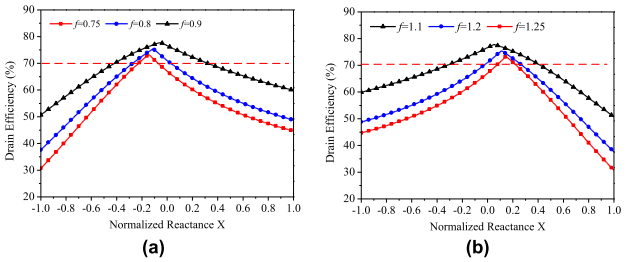

FIGURE 3. Simulated drain efficiency at OPBO as a function of X at normalized frequencies. (a) 0.75, 0.8 and 0.9. (b) 1.1, 1.2 and 1.25.

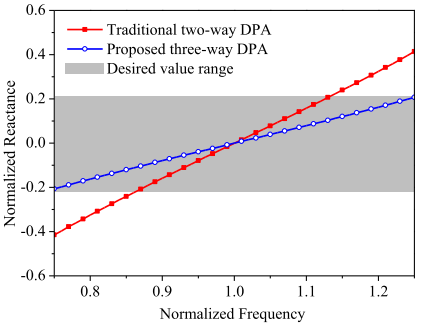

FIGURE 4. Reactance distribution when the peaking amplifier turns off in the traditional two-way DPA and the proposed three-way DPA using parallel peaking amplifiers.

evident that, considering the reactance compensation of the peaking amplifier, the conventional two-way DPA cannot fully meet the optimal value of X.

C. PROPOSED THREE-WAY DPA WITH PARALLEL PEAKING AMPLIFIERS

To obtain the optimal value of X, a novel three-way DPA is proposed, which achieves reactance compensation by using two parallel peaking amplifiers, as shown in Fig. 5. Unlike conventional reactance compensated DPA, a parallel connection of two peaking amplifiers is employed instead of a single peaking amplifier. Although the proposed architecture is similar to traditional three-way DPA, it should be pointed that the outputs of two peaking amplifiers in conventional design are assumed to be open-circuited. Different from it, in the proposed design, the output impedances (i.e. $Z_{OUT,P1}$ and $Z_{OUT,P2}$) are converted to quasi-short when the peaking devices are turned off, assuming the peaking output matching networks (OMN) can be treated as quarter-wavelength transformers ($\lambda_0/4$, $Z_{0,P1}$) and ($\lambda_0/4$, $Z_{0,P2}$). After connecting these two output impedances in parallel, the quarter-wavelength transformer ($\lambda_0/4$, Z_T) can be employed for reactance compensation. Since the parallel connection of two peaking amplifiers can reduce the distribution range of the output reactance, the bandwidth limitation in reactance compensated DPA can be alleviated. In the following, the characteristics of the proposed design approach will be analyzed, then the design parameters will be given.

Firstly, the output impedance of the peaking branch $Z_{OUT,P}$ using parallel peaking amplifiers in the proposed three-way DPA was simulated, as depicted in Fig. 4. It can be seen that the distribution range of the normalized reactance is about (–0.2, 0.2), which proves that the proposed method can make the output reactance of the peaking branch to achieve the optimal impedance range (–0.22, 0.22) obtained by theoretical analysis.

Then, to achieve proper load modulation and quasi-short output impedance, the carrier and peaking OMNs can be treated as three quarter-wavelength transformers with characteristic impedances of $Z_{0,C}$, $Z_{0,P1}$ and $Z_{0,P2}$. Thus, the proposed load combiner can be composed of four quarter-wavelength transmission lines, which combine the output powers of the carrier amplifier with two peaking amplifiers and transmit them to the common load R_L, as demonstrated in Fig. 5.

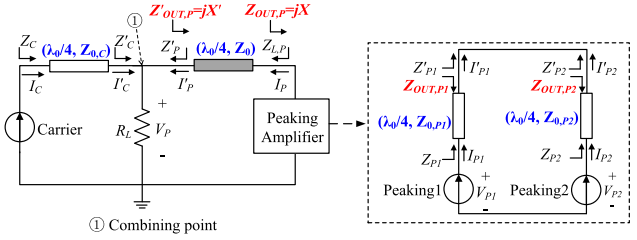

FIGURE 5. Schematic diagram of the proposed three-way DPA with parallel peaking amplifiers.

The proposed three-way DPA has two working states. At OPBO range, two peaking amplifiers are turned off and their output impedances are quasi-short. A compensating reactance can be generated to compensate the load impedance of the carrier amplifier with the help of the quarter-wavelength transformer ($\lambda_0/4$, Z_T). At saturation, the carrier and peaking amplifiers can generate the output currents with the same amplitude, then anticipated load modulation can be obtained.

For proper Doherty operation, the characteristic impedance Z_0, $Z_{0,C}$, $Z_{0,P1}$ and $Z_{0,P2}$ in the load combiner can be expressed as:

$$Z_0 = \sqrt{1.5 R_L Z_{L,P}}, \tag{8}$$

$$Z_{0,C} = \sqrt{3 R_L R_{opt}}, \tag{9}$$

$$Z_{0,P1} = Z_{0,P2} = \sqrt{2 Z_{L,P} R_{opt}}, \tag{10}$$

where R_{opt} is the optimum load impedance of the carrier and peaking amplifiers, which is 24 Ω obtained from the load-pull simulation. For a three-way DPA using symmetrical devices [17], the common load R_L can be chosen as 16.6 Ω to achieve 50 Ω load impedance at the output of the carrier OMN at saturation. $Z_{L,P}$ is the load impedance of the peaking branch, which can be regarded as an independent variable.

Since $Z_{L,P}$ has an impact on the DPA bandwidth, its optimum value will be analyzed in detail below. The design parameters of the load combiners for different $Z_{L,P}$ are determined using (8)–(10), as given in Table 2. Using current source simulations in Keysight Advanced Design System (ADS), the output impedance of the carrier amplifier at OPBO is obtained, as shown in Fig. 6(a). It can be seen that for case II, the output impedance of the carrier amplifier tends to the ideal value at OPBO. Fig. 6(b) gives the performance at saturation. Similar conclusions can be obtained for case II. So, considering both OPBO and saturation conditions, $Z_{L,P}$ is chosen as 30 Ω.

TABLE 2. Design parameters of the load combiner.

Case	$Z_{L,P}$	Z_0	$Z_{0,C}$	$Z_{0,P1}$	$Z_{0,P2}$
I	25 Ω	25 Ω	34.6 Ω	34.6 Ω	34.6 Ω
II	30 Ω	27.4 Ω	34.6 Ω	38 Ω	38 Ω
III	35 Ω	29.5 Ω	34.6 Ω	41 Ω	41 Ω

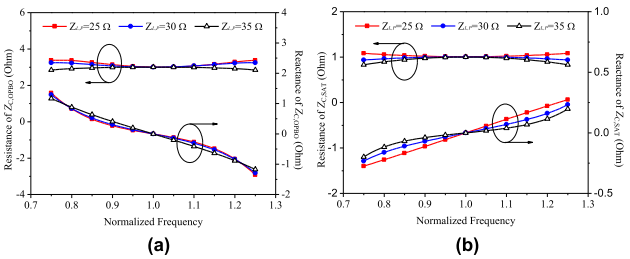

FIGURE 6. Comparison of the normalized carrier load impedance for the case I, II and III. (a) At OPBO. (b) At saturation.

Therefore, in the following design, $Z_{L,P}$ is 30 Ω and the corresponding Z_0, $Z_{0,C}$, $Z_{0,P1}$ and $Z_{0,P2}$ are 27.4, 34.6, 38 and 38 Ω, respectively. These parameters can be employed in the design of the OMNs in the proposed three-way DPA with parallel peaking amplifiers.

III. DESIGN AND SIMULATION OF PROPOSED THREE-WAY DPA

For verification of the proposed design methodology, a wideband three-way DPA was designed using Wolfspeed CGH40010 GaN HEMT device within the frequency band of 1.6–2.7 GHz. Considering the influence of the parasitic parameters of the transistor, the quarter-wavelength transformers ($\lambda_0/4$, $Z_{0,C}$), ($\lambda_0/4$, $Z_{0,P1}$) and ($\lambda_0/4$, $Z_{0,P2}$) in the combining network were implemented by the OMNs designed by using the two-point matching method [23], as described below.

A. DETERMINATION OF CARRIER AND PEAKING IMPEDANCES

For the OMN design, the load-pull simulations in ADS were used to obtain the optimal load impedances of the carrier and peaking amplifiers over the frequency band of 1.6–2.7 GHz. Fig. 7 illustrates the simulated load-pull results of the fundamental impedances for the carrier and peaking amplifiers,

where the carrier amplifier is operated at class AB mode, while the peaking amplifier is biased using class C operating condition. The results show the optimal load impedance regions of the carrier and peaking amplifiers at 1.6, 2.15, and 2.7 GHz at saturation. Meanwhile, the impedance area of the carrier amplifier at OPBO and the peaking device output impedance at class C mode were also given. The peaking and carrier impedances for the OMN designs were shown in Table 3 and 4.

TABLE 3. Design parameters of the peaking OMNs.

Freq. (GHz)	$Z_{P1/2}$	$Z'_{P1/2}$	$Z_{OUT,P1/2}$	$Z'_{OUT,P1/2}$	S_{22}	θ_{21}
1.6	28.7-j11Ω	60Ω	1.6-j53Ω	0.24-j18Ω	-0.25-j0.17Ω	-45°
2.15	18.8-j0.7Ω	60Ω	0.6-j41.7Ω	Quasi short	0.45-j0.02Ω	-65°
2.7	13.9+j11Ω	60Ω	0.87-j37Ω	1+j18Ω	0.52+j0.26Ω	-84°

TABLE 4. Design parameters of the carrier OMN.

Freq. (GHz)	$Z_{C,SAT}$	$Z'_{C,SAT}$	$Z_{C,OPBO}$	$Z'_{C,OPBO}$	S_{11}	θ_{21}
1.6	33-j9Ω	50Ω	19.2+j25.4Ω	13+j6.9Ω	-0.19-j0.13Ω	-36°
2.15	22.3-j3.5Ω	50Ω	19+j20Ω	16.6Ω	-0.28-j0.07Ω	-53°
2.7	16.7+j4.7Ω	50Ω	11.9+j24.8Ω	13-j6.9Ω	-0.4-j0.02Ω	-68°

For the design of input matching network (IMN) with desired gain performance, the optimum source impedances of the carrier and peaking transistors were analyzed. After optimization and adjustment, the source impedances at the high, center and low frequencies were determined to be (6.7–j8.8) Ω, (9.6–j8.3 Ω) and (8.5–j4.7 Ω), respectively.

B. DESIGN OF MATCHING NETWORKS

In this design, a specific OMN design method using two-point matching technique was employed. According to two pairs of impedance transformation required at saturation and OPBO (as shown in Table 3 and 4), the *S* parameters of the OMNs can be obtained. And, the required carrier and peaking amplifier OMNs can be designed, avoiding the use of traditional offset lines, thereby simplifying the DPA design process.

To begin with, the design of peaking OMN is introduced. Because of the symmetry of the peaking amplifiers, their OMNs were designed with the same structure. At the center frequency of 2.15 GHz, the load impedance $Z_{P1/2} = (18.8–j0.7)\Omega$ at saturation can be obtained by using the load-pull results in Fig. 7, while $Z'_{P1/2}$ is chosen as 60 Ω. At the OPBO region, the small-signal output impedance of the peaking transistor $Z_{OUT,P1/2}$ is (0.6–j41.7)Ω. And, the relationship between the output impedance $Z'_{OUT,P1/2}$ and the phase θ_{21} of the peaking OMN at 2.15 GHz can be obtained, as shown

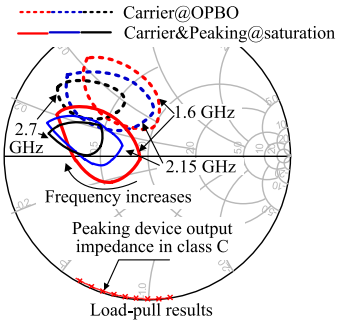

FIGURE 7. Load-pull simulation results and output impedances at 1.6, 2.15, and 2.7 GHz.

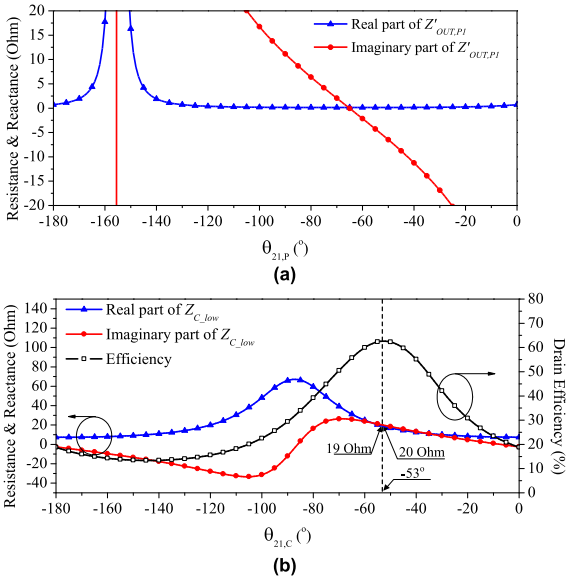

FIGURE 8. Graphical illustration of the calculation of the phase delay θ_{21} at 2.15GHz. (a) Peaking OMN. (b) Carrier OMN.

in Fig. 8(a). According to the results, it can be obtained that when θ_{21} is –65°, $Z'_{OUT,P1/2}$ can achieve short-circuited, which can satisfy the requirement of the integrated compensation reactance.

By employing the similar method, the design parameters of peaking OMNs at 1.6 and 2.7 GHz, including their *S* parameters, can also be determined, as shown in Table 3. Therefore, the OMNs can be designed and optimized according to the obtained design parameters. As can be seen from Table 3, the peaking OMNs can satisfy the impedance matching requirements at saturation, and at the same time provide compensation reactance to increase the carrier effective load impedance at OPBO for low and high frequencies. Moreover, it can be noted that, when only one peaking amplifier is used, the normalized output impedance $Z'_{OUT,P1/2}$ cannot satisfy the requirement of (–0.22, 0.22) obtained in Section II.B. However, the output impedance range can be effectively reduced to half of the original value by using two parallel peaking amplifiers, as the proposed design in Fig. 5.

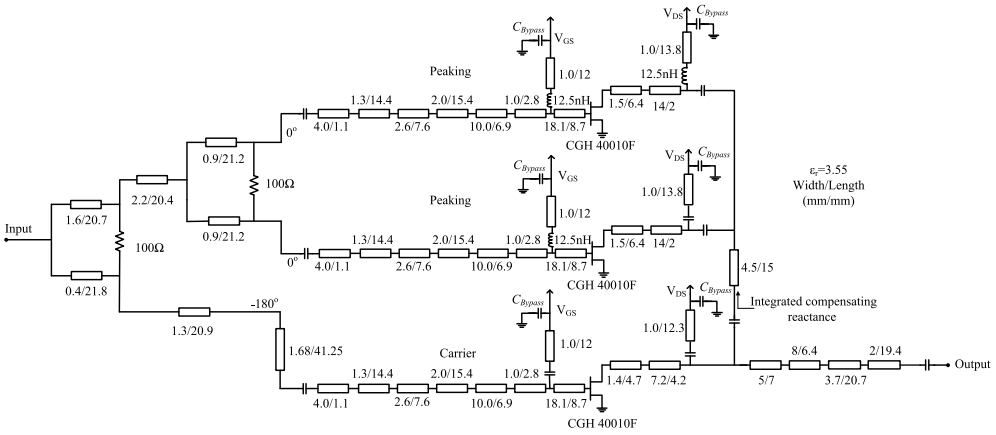

FIGURE 9. Complete schematic of proposed DPA.

Similarly, the carrier OMN can also be designed. The obtained output impedance $Z_{C,OPBO}$ and the relationship between drain efficiency and phase θ_{21} at 2.15 GHz are given in Fig. 8(b). The results show that, when $Z_{C,OPBO}$ is (19 + j20) Ω, the carrier amplifier can obtain the highest drain efficiency with corresponding θ_{21} of –53°. In addition, Table 4 also shows the design parameters of the carrier OMN at 1.6 and 2.7 GHz. Then, the carrier OMN can be designed and optimized.

Using the obtained source impedances in Section III.A, the IMNs can be designed based on the stepped-impedance matching topology to cover the required frequency band of 1.6–2.7 GHz.

C. DPA SIMULATION RESULTS

With the above-designed carrier and peaking amplifiers, a three-way DPA with parallel peaking amplifiers is designed on a Taconic RF35 substrate with $\varepsilon_r = 3.55$ and a thickness of 30 mil, as shown in Fig. 9. In order to accurately convert 50 to 16.6 Ω over a wide frequency band, a four-stage real-to-real matching network was used. Meanwhile, two Wilkinson power dividers were designed as the input dividers to generate equal power splitting ratio for the carrier and peaking amplifiers. And, the length of the input compensation line was adjusted to ensure the proper phase relationship between the output currents.

Fig. 10(a) shows the simulation results of the drain efficiency and saturation output power at different frequencies. With the saturation power of higher than 45 dBm, the proposed DPA can deliver an associated efficiency of higher than 56%, and the drain efficiency is about 51-55% at 10 dB OPBO range. The measured drain efficiency and gain as a function of the output power are depicted in Fig. 10(b). Good Doherty efficiency behavior can be observed. The drain efficiency is almost consistent at low-power region, while the drain efficiency in the OPBO region is slightly degraded at the lowest and highest frequency of 1.6 and 2.7 GHz, respectively.

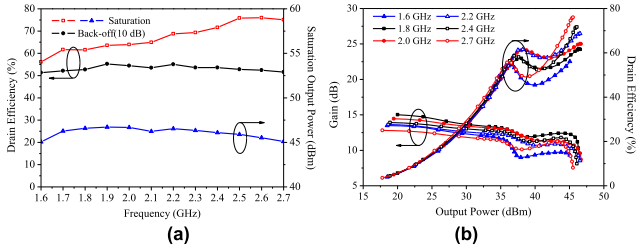

FIGURE 10. Simulation results of the proposed DPA. (a) Drain Efficiency and saturation output power versus frequency. (b) Gain and drain efficiency versus output power.

TABLE 5. Comparisons of the DPD performances at different frequencies.

Frequency (GHz)	Output Power (dBm)	Average Drain Efficiency(%)	ACLR(dBc) Before DPD	ACLR(dBc) After DPD
1.96	35.4	51.6	-31.2/-31.7	-50.3/-51.2
2.14	35.7	50.2	-30.0/-30.7	-50.1/-50.7
2.355	35.4	50.8	-30.3/-30.7	-50.8/-52.1
2.655	35.7	51.8	-28.4/-29.4	-51.3/-52.5

IV. REALIZATION AND EXPERIMENTAL VERIFICATION

To verify the proposed method, a wideband three-way DPA was designed and fabricated using the 10 W GaN HEMT CGH40010F from Wolfspeed, as shown in Fig. 11(a). To achieve desired load modulation, the carrier amplifier was biased with the quiescent current of 0.05 A and $V_{DS} = 26$ V, and two peaking amplifiers were biased in the class C mode with V_{DS} of 30 V, whose V_{GS} were appropriately tuned for on-state at about 10 dB OPBO simultaneously.

For continuous wave measurements, Fig. 11(b) gives the results of measured efficiencies and output powers at OPBO and saturation. Fig. 11(c) and (d) shows the measured gain and drain efficiency performance at different frequencies. The results show that the drain efficiency at saturation ranges from 54% to 68%, and the drain efficiency at 10 dB OPBO

TABLE 6. Performance comparison with recently published high back-off DPAs.

Ref. (Year)	Freq. (GHz)	Configuration	FBW (%)	Pout @ Saturation (dBm)	Drain Efficiency @ Saturation (%)	Drain Efficiency @ Back-Off (%)
[18] 2018	0.6-0.9	three-stage DPA	40	46.1-46.9	51-78	50-62@12 dB
[19] 2018	1.45-2.35	three-stage DPA	46	44.3-46.8	58-70	40-54@9 dB
[20] 2018	2.0-2.6	three-way DPA	26	43.6-45.4	53-76	41-48@8 dB
[21] 2019	1.6-2.6	three-stage DPA	48	45.5-46	53-66	50-53@9.5 dB
[22] 2021	0.55-0.9	three-stage DPA	48.3	41.3-42.9	54-72	50-58@12 dB
This work	**1.6-2.7**	**three-way DPA**	**51**	**44.9-46.3**	**54-68**	**50-53@10 dB**

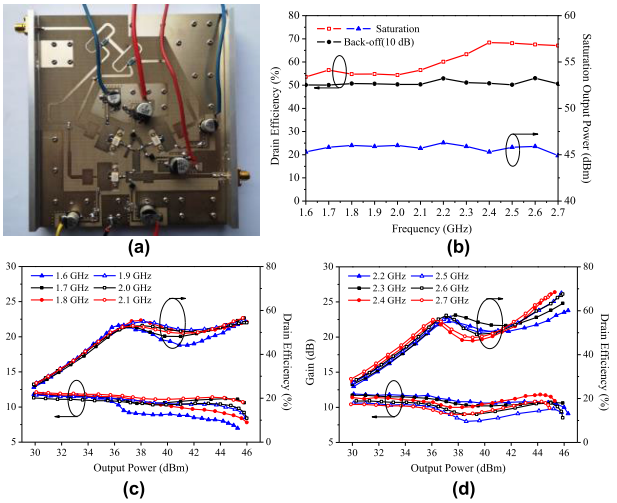

FIGURE 11. Designed three-way DPA. (a) Photograph. (b) Measured gain and drain efficiency versus frequency. (c) Measured gain and drain efficiency at the frequency band of 1.6–2.1 GHz. (d) Measured gain and drain efficiency at the frequency band of 2.2–2.7 GHz.

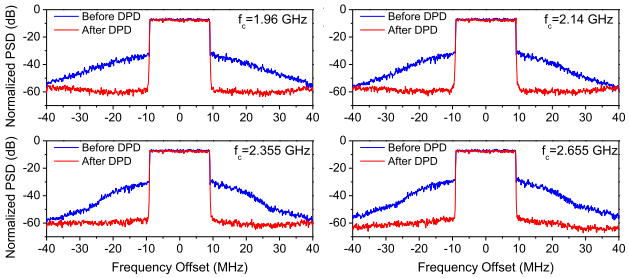

FIGURE 12. Measured spectrum before and after DPD for a 20 MHz LTE signal at 1.96, 2.14, 2.355 and 2.655 GHz.

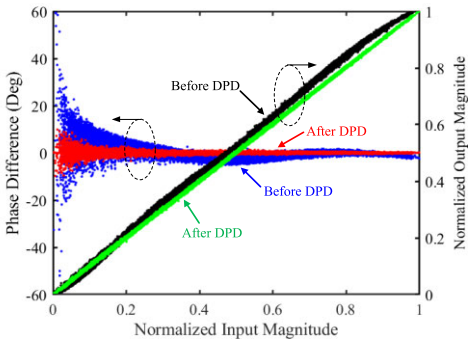

FIGURE 13. AM/AM and AM/PM plots for 20 MHz LTE signal before and after DPD at 2.14 GHz.

is between 50% and 53%, which corresponds to 51% FBW. The saturated output power ranges from 44.9 to 46.3 dBm.

For modulated signal measurements, to validate the linearity improvement of the DPA, the digital pre-distortion (DPD) measurement was conducted at 1.96, 2.14, 2.355 and 2.655 GHz considering the frequency division duplex (FDD) LTE frequency band allocations using a 20 MHz LTE signal with a PAPR of about 9 dB. The linearization results at different frequencies are summarized in Table 5. The proposed DPA can achieve an average drain efficiency of higher than 50% and an adjacent channel leakage ratio (ACLR) of better than –50 dBc at 10 dB back-off power (about 36 dBm) when using DPD linearization. Fig. 12 and 13 show the measured signal spectra of normalized outputs and the time-domain AM/AM and AM/PM characterizations before and after DPD. The results show that the distortion caused by the DPA can be removed effectively. For modulated signal measurements at about 10 dB OPBO power, the proposed DPA can simultaneously achieve good efficiency and high linearity over the entire design frequency band.

The proposed DPA is compared with other published DPAs, as shown in Table 6. It can be noted that, with a drain efficiency of higher than 50% at 10 dB back-off, the proposed DPA can achieve the widest FBW (about 51%), verifying the feasibility of the proposed method for wideband DPA design.

V. CONCLUSION

A wideband three-way DPA with reactance compensation by using parallel peaking amplifiers has been proposed. Parallel amplifiers can reduce the output impedance of the peaking branch, and effectively improve the compensation reactance at the combining point through the quarter-wavelength transformer. With the compensation at high/low frequencies, the effective load impedance and efficiency of the

carrier amplifier can be improved to expand the bandwidth. Both simulation and experimental results have verified the proposed structure at the frequency band between 1.6 and 2.7 GHz.

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