IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received April 12, 2021, accepted April 25, 2021, date of publication April 28, 2021, date of current version May 6, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3076202

Statistical Strategies to Capture Correlation Between Overshooting Effect and Propagation Delay Time in Nano-CMOS Inverters

HAMED JOOYPA[1], DARYOOSH DIDEBAN[1], AND HADI HEIDARI[2], (Senior Member, IEEE)
[1]Electrical and Computer Engineering Department, University of Kashan, Kashan 8731753153, Iran
[2]James Watt School of Engineering, University of Glasgow, Glasgow G12 8QQ, U.K.

Corresponding author: Daryoosh Dideban (dideban@kashanu.ac.ir)

This work was supported by the University of Kashan under grant number 1073372 and by Microelectronics Lab (meLab) through the University of Glasgow, U.K., under Grant EPSRC IAA EP/R511705/1.

ABSTRACT In this paper, we model statistical correlation between overshooting effect and propagation delay time in nano-CMOS technology considering the influence of intrinsic parameter fluctuations caused by discreteness of charge and granularity of matter. The impact of input slew rate, output capacitive load, and supply voltage on this statistical correlation is comprehensively studied. Moreover, we propose two alternative approaches which are capable of reproducing the statistical correlation as well as mean and standard deviation of both propagation delay time and overshoot voltage. We evaluate the accuracy of these alternative approaches against accurate Monte-Carlo simulations. It is shown that the statistical correlations are almost preserved using these alternative approaches.

INDEX TERMS Propagation delay time, statistical variability, nano-CMOS, overshoot voltage, statistical modelling.

I. INTRODUCTION

The impact of Statistical Variability (SV) on the timing of nano-CMOS circuits has attracted much attention in recent years [1]–[8]. SV makes the digital circuits to manifest non deterministic performance rather than having a deterministic behavior in terms of critical path delay or even power consumption. The major sources of SV are comprised of Random Dopant Fluctuations (RDF), Line Edge Roughness (LER) and Metal Grain Granularity (MGG) [9]–[11]. These sources influence the device electrical figures of merit such as threshold voltage (V_{th}), off-state current and Subthreshold Slope (SS) which in turn they will make a significant impact on the circuit behavior. In particular, the impact of process and random variability on the propagation delay time is widely studied in the literature [12]–[20].

In a pioneering work, authors proposed a semi-analytical model to predict delay distribution of logic circuits caused by V_{th} variation [12]. The propagation delay variation due to RDF at different technology nodes is comprehensively studied in [13]. A variation-aware timing model for a two-input NAND gate is proposed in [14] for 65-nm technology node. Authors in [15] have investigated statistical estimation of delay in nano-CMOS circuits using Burr distribution. In our previous work, we have embedded SV into propagation delay time compact models for nano-CMOS technologies considering different number of parameters [16]. In addition, the accuracy of these statistical compact models at different extrinsic and environmental conditions are studied in [17]. Moreover, we have proposed different statistical strategies to reproduce delay variability with taking the full or partial correlation between important parameters of a delay time compact model into account [18].

However, a main component of the propagation delay time is the overshoot time (t_{ov}) which indicates the time when the output exceeds the supply voltage. The overshooting effect in nano-CMOS technology was comprehensively modelled with emphasis on the delay prediction in [19]. This work does not take the effect of SV into account. Nevertheless, other authors recently considered the variability introduced into this overshooting time and they have modelled its impact on timing variation [20]. In this paper, for the first time we model

The associate editor coordinating the review of this manuscript and approving it for publication was Guangdeng Zong.

the statistical correlation between the overshooting effect and the propagation delay time in nano-CMOS inverters with the aid of Monte-Carlo (MC) simulations. Moreover, we study the impact of fan-out, input rise time, and supply voltage on this correlation. Finally, we propose two alternatives for predicting this statistical correlation and compare the accuracy of these approaches against accurate MC results. It is worth noting that in this work we deal with the statistical variability on the device level which arises from discreteness of charge and granularity of matter. The impact of this type of variability on the overshooting effect of a nano-CMOS inverter is emphasized via Monte-Carlo simulations. Therefore, the impacts of RDD, LER and MGG as local effects are taken into account but the global effects such as the variability imposed by fabrication process are not considered.

The main novelty of our work is twofold: first, we capture the hidden statistical correlation between the overshooting effect and propagation delay time caused by statistical variability (SV) under different circumstances. Second, we propose two simplified approaches which can replicate these correlations with enough degree of accuracy. The remaining of this research is divided into three sections. In section II we briefly discuss the statistical modelling of overshooting effect with the aid of MC simulations and show its importance in delay variation. Section III is devoted to evaluate the correlation between overshooting effect and propagation delay time in response to some parameters. In section IV we propose two alternative strategies which are capable of reproducing mean (μ) and Standard Deviation (SD) of overshooting effect in correlation with delay time variability. The paper is concluded in section V.

II. STATISTICAL MODELLING OF OVERSHOOTING EFFECT

In order to highlight the impact of SV on the overshooting effect, we perform a Monte-Carlo simulation for basic CMOS inverter subject to sources of SV. Fig. 1(a) illustrates a chain of inverter with a Device Under Test (DUT) in the middle. Fig. 1(b) depicts the input/output waveforms corresponding to a typical inverter with the inset showing circuit schematic of a CMOS inverter. Overshooting time (t_{ov}), overshoot voltage (V_{ov}) and propagation delay time (t_p) are defined and indicated in this figure. We adjusted the rise time of the input signal (t_r) as shown in the inset of Fig. 1(b) to change the input slew rate of the CMOS inverter. In order to investigate the impact of SV on the DUT behavior, we performed MC simulations to obtain I-V trajectories of the CMOS inverter. Statistical modelcards for 1000 samples of 35nm CMOS technology obtained from University of Glasgow atomistic simulator are utilized in HSPICE as comprehensively discussed in our previous works [16]–[18]. These statistical modelcards are referred to 'atomistic' modelcards in the remaining of this work.

Fig. 2 illustrates this trajectory for the DUT in the case it suffers from SV. It clearly indicates that a range of overshoot voltages are produced by different devices caused by the impact of statistical variability (the region where the voltage exceeds the supply voltage of 1V). The black solid lines in this figure illustrate the I_{ds}-V_{ds} characteristics for a uniform NMOS device in the DUT. It is expected that different overshoot voltages are associated with corresponding overshooting times as well as different propagation delay in the transient time analysis.

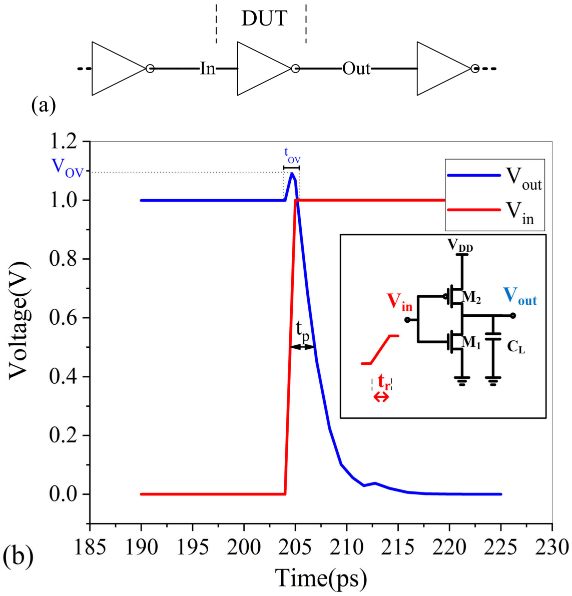

FIGURE 1. (a)-Chain of inverters with a DUT subject to statistical variability, (b)-Output versus input transient response with definition of overshooting parameters.

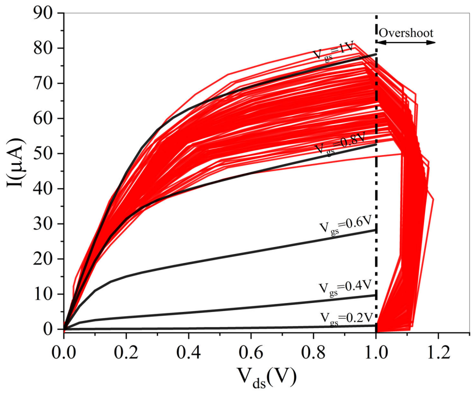

FIGURE 2. Current versus drain-source voltage trajectory for NMOS device in the CMOS inverter shown in the inset of Fig. 1(b) subject to statistical variability.

Fig. 3 illustrates the histogram of overshoot time normalized to propagation delay time. The inset shows the Q-Q plot for this distribution. It clearly indicates the fact that the ratio of t_{ov}/t_p follows a normal distribution with a mean of 0.45 and SD of 0.01.

In order to better understand the statistical correlation between overshoot and propagation delay time, the scatter plot showing the behavior of important variables is shown in Fig. 4.

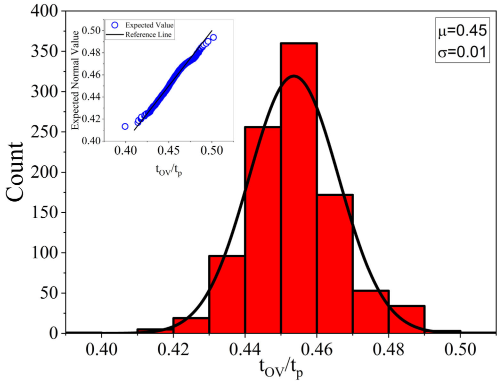

FIGURE 3. Statistical distribution of t_{ov}/t_p for the DUT in Fig. 1(a). The inset shows the Q-Q plot for this variable.

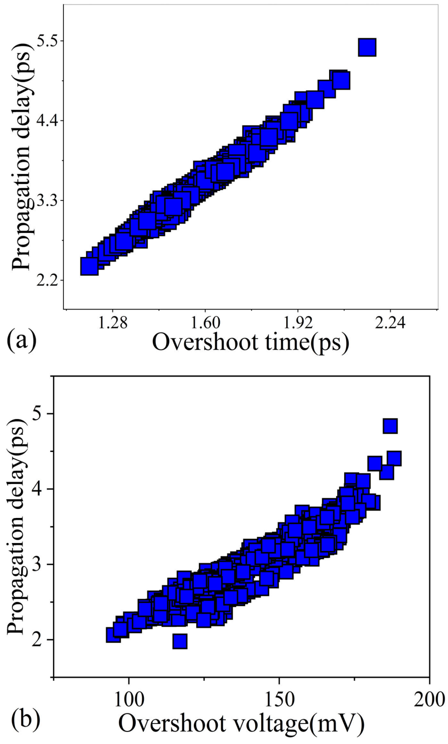

FIGURE 4. The scatter plots between propagation delay time and (a)-overshoot time, (b)-overshoot voltage.

The Correlation Coefficient (CC) between two statistical variables is defined by:

$$\rho(X, Y) = \frac{COV(X, Y)}{\sigma_X . \sigma_Y} \tag{1}$$

where *COV(X,Y)* is the covariance of two variables and σ denotes the standard deviation of each variable. It can be extracted using Origin software [21]. It is an important parameter in variation aware design in CMOS technology because it answers whether two variables are independent or dependent [22]. While a zero value of CC indicates independent variables, a CC close to 1 confirms they are significantly related. A very strong statistical correlation can be seen between propagation delay and overshoot time which results in a Correlation Coefficient (CC) of 0.99 as indicated in Fig. 4(a). In addition, Fig. 4(b) confirms the fact that a strong correlation between propagation delay and overshoot voltage exists while the CC is reduced to a lower value of 0.94.

III. EVALUATING THE STATISTICAL CORRELATION BETWEEN OVERSHOOTING EFFECT AND PROPAGATION DELAY TIME

Since in the last section we studied the impact of SV on the overshooting effect correlated with propagation delay time at a particular point of bias parameters, in this section our study is extended to investigate the impact of parameters such as fan-out, input slew rate, and supply voltage on the statistical correlation between propagation delay time (t_p) and overshoot voltage (V_{ov}) in 1000 simulation. These parameters affect on the statistical behavior of t_p [16]–[18] but here we emphasize to model the range of variations and the correlations between t_p and V_{ov} caused by the change in these parameters. Fig. 5(a) illustrates the scatter plots between t_p and V_{ov} as a result of change in fan- out (FO). Increase of the fan-out causes the overshoot voltage to be decreased while the propagation delay is increased. The overshoot voltage is mainly influenced by the device parasitic capacitances including the miller input-output coupling capacitance. By increase of the fan-out, the contribution of these capacitances compared with the output capacitance is reduced [19]. Therefore, the overshoot voltage will be decreased.

The interesting point is that the CCs between t_p and V_{ov} calculated from these plots are 0.91, 0.82, 0.91, and 0.82 corresponding to output load conditions of FO1, FO4, FO8, and FO12, respectively. It is seen that the strong correlation between t_p and V_{ov} is almost preserved despite the increase in the load capacitance and propagation delay or associated decrease in the overshoot voltage. Fig. 5(b) shows the impact of input slew rate (input rise time) on the correlation between t_p and V_{ov}. As was expected, it is seen that sharp input slew rates gives higher overshoots and lower propagation delay times. Moreover, the statistical correlations are again preserved to a value about 0.8. Fig. 5(c) indicates the impact of supply voltage change on the correlation between t_p and V_{ov}. It is worth noting that since the settling point of the output voltage alters as a result of change in V_{dd}, the overshoots are still calculated considering the definition given in Fig. 1(b). Here, the CCs in all cases are preserved to around 0.8.

IV. PROPOSING ALTERNATIVE APPROACHES

Since modelling statistical correlations based on original Monte-Carlo simulations necessitates use of atomistic model-cards, in this section we propose two alternative approaches in order to simplify these statistical models. Moreover, we evaluate the accuracy of these simplified approaches against original MC simulations.

Since it is widely agreed that the use of V_{th} as a major component of statistical models gives the first order accurate

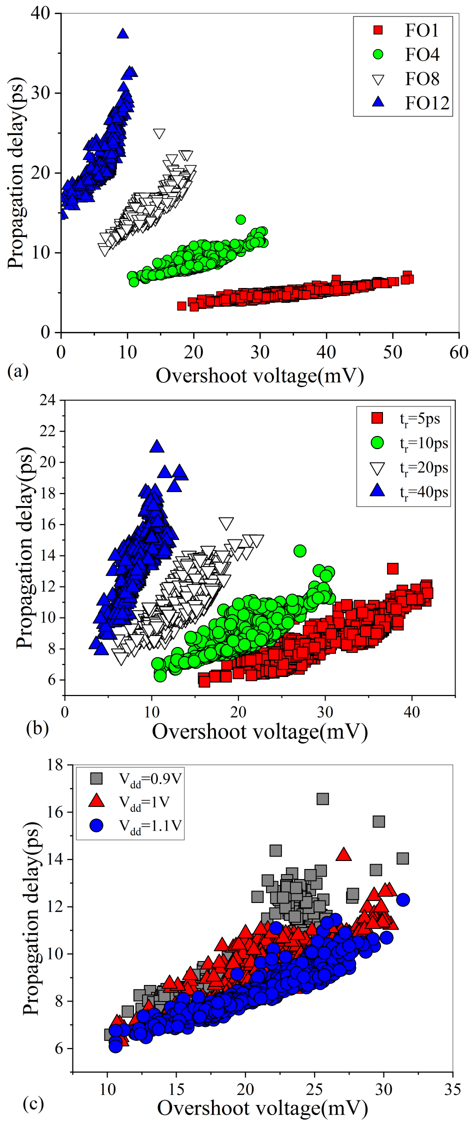

FIGURE 5. Scatter plots between propagation delay time and overshoot voltage in response to different conditions of (a) fan-out, (b) input rise time, (c) supply voltage.

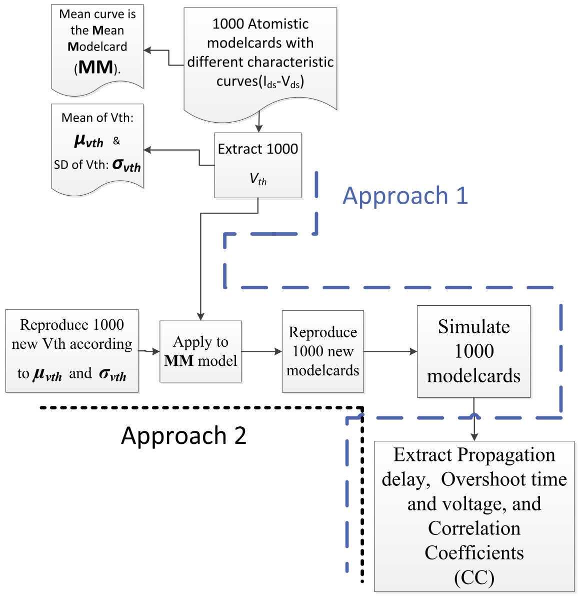

FIGURE 6. Flowchart showing two alternative approaches for statistical modeling of overshooting effect.

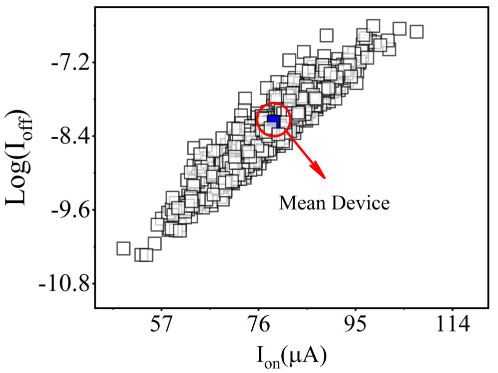

FIGURE 7. Selection of Mean Device from Log (I_{off}) versus I_{on} for 1000 samples.

models, here we focus on introducing models which only use V_{th} to capture the statistical variations in overshooting effect. The reason for selecting V_{th} among other parameters is based on the fact that it is the most efficient parameter as investigated in our previous work [18]. On the other hand, in this work and in order to extract correlations between overshooting and propagation delay time we aim to use simple one-parameter model. Fig. 6 presents a flowchart for these simplified approaches. Approach 1 reproduces statistical modelcards which use one important parameter (V_{th}) as exactly given in the original 'atomistic' modelcards. In other words, among seven important parameters which are varying in statistical BSIM modelcards (V_{th0}, U_0, N_{factor}, V_{off}, M_{inv}, R_{dsw}, D_{sub}) [17], six parameters are preserved as a default value taken from the Mean Modelcard (MM) but V_{th} is replaced with its original values as given in 'atomistic' modelcards. Approach 2 is almost like approach 1 but the V_{th} parameters are taken from a normal distribution which has a mean and standard deviation (SD) equal to its original values from 'atomistic' modelcards. In other words, the V_{th} parameters in approach 2 are a reproduced version of original values with given mean and SD.

It is worth noting that the Mean Modelcard (MM) can be extracted from the Log(I_{off}) versus I_{on} scatter plots of 1000 samples as illustrated in Fig. 7. The mean value of Log(I_{off}) is -8.31 while the corresponding mean value for I_{on} is 78.3 μA. Therefore, among all other samples the device which matches this criteria in the center of the scatter plot is selected as the Mean Device and its associated modelcard in the atomistic library is referred to 'Mean Modelcard' (MM).

Fig. 8 illustrates the scatter plots between propagation delay time and overshoot voltage obtained from two alternative approaches compared with original MC simulations. The simulation conditions of $t_r = 10$ psec, $V_{dd} = 1$ V and Fan-out=4 is utilized. Despite the fact that a main part of the cloud in scatter plots are disappeared as a

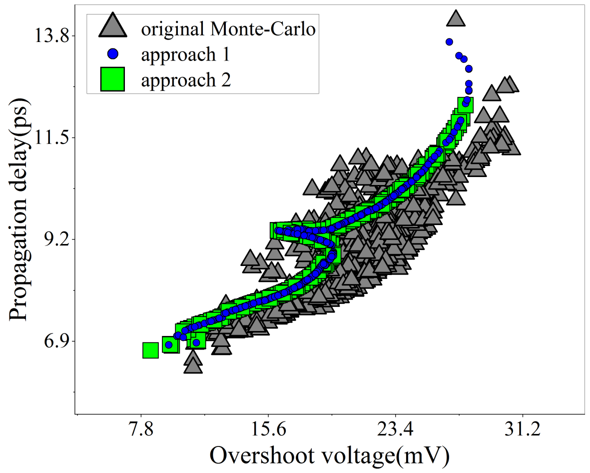

FIGURE 8. Scatter plots between propagation delay time and overshoot voltage obtained from alternative approaches and compared with original MC simulations.

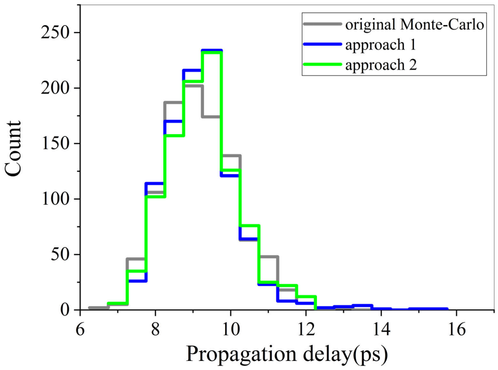

FIGURE 9. Comparison of propagation delay time distribution between original Monte-Carlo simulations and our proposed approaches.

TABLE 1. Mean and standard deviation of the propagation delay time and overshoot voltage and their correlation coefficient.

	Correlation Coefficient	t_p(ps)		V_{ov}(mv)	
		μ	**σ**	**μ**	**σ**
Original M.C	0.82	8.96	1	21	3
Approach 1	0.88	8.98	0.97	18.9	2.9
Approach 2	0.91	9.01	0.93	19	3.1

result of using simplified approaches, Table 1 shows that the correlation coefficients are almost preserved while the mean and SD of both t_p and V_{ov} are close to their reference values while using alternative approaches. On the other hand, approach 1 gives slightly better results or less error in comparison with approach 2. Fig. 9 illustrates a graphical comparison of data shown in Table 1 for the distribution of propagation delay time. It clearly indicates that both approaches produce mean and standard deviation which are close to original data obtained from Monte-Carlo simulations.

V. CONCLUSION

This paper addresses statistical modeling of overshooting effect correlated with propagation delay time variation. We studied the impact of parameters such as supply voltage, input rise time, and output fan-out on the scatter plots using accurate Monte-Carlo simulations. In addition, we proposed two alternative approaches which can reproduce the statistical distribution of propagation delay time and overshoot voltage with a high degree of accuracy. Despite the fact that a large amount of the scatter plots were disappeared, the statistical correlations were almost preserved in these simplified alternative approaches.

ACKNOWLEDGMENT

This research was supported by University of Kashan under supervision of Dr. Daryoosh Dideban. Thanks for the support received from Microelectronics Lab (meLab) through the University of Glasgow, U.K., under Grant EPSRC IAA EP/R511705/1.

REFERENCES

[1] Q. Tang, "Transistor-level statistical timing analysis: Solving random differential equations directly," Ph.D. dissertation, Dept. Microelectron., Fac. Elect. Eng., Math. Comput. Sci., Delft Univ. Technol., Delft, The Netherlands, 2013.

[2] M. Alioto, G. Scotti, and A. Trifiletti, "A novel framework to estimate the path delay variability on the back of an envelope via the fan-out-of-4 metric," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 8, pp. 2073–2085, Aug. 2017, doi: 10.1109/TCSI.2017.2687059.

[3] F.-U. Hassan, W. Vanderbauwhede, and F. Rodriguez-Salazar, "Impact of random dopant fluctuations on the timing characteristics of flip-flops," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 1, pp. 157–161, Jan. 2012, doi: 10.1109/TVLSI.2010.2088409.

[4] C. Forzan and D. Pandini, "Statistical static timing analysis: A survey," *Integration*, vol. 42, no. 3, pp. 409–435, Jun. 2009, doi: 10.1016/j.vlsi.2008.10.002.

[5] S. R. Ramesh and R. Jayaparvathy, "Improved statistical static timing analysis using refactored timing graphs," *J. Comput. Theor. Nanosci.*, vol. 13, no. 11, pp. 8879–8884, Nov. 2016, doi: 10.1166/jctn.2016.6057.

[6] J. H. Kim, W. Kim, and Y. H. Kim, "Efficient statistical timing analysis using deterministic cell delay models," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2709–2713, Nov. 2015, doi: 10.1109/TVLSI.2014.2364736.

[7] Q. Tang, J. Rodriguez, A. Zjajo, M. Berkelaar, and N. van der Meijs, "Statistical transistor-level timing analysis using a direct random differential equation solver," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 2, pp. 210–223, Feb. 2014, doi: 10.1109/TCAD.2013.2287179.

[8] C. C. McAndrew, X. Li, I. Stevanovic, and G. Gildenblat, "Extensions to backward propagation of variance for statistical modeling," *IEEE Des. Test Comput.*, vol. 27, no. 2, pp. 36–43, Mar. 2010, doi: 10.1109/MDT.2010.44.

[9] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr. 2001, doi: 10.1109/16.915703.

[10] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003, doi: 10.1109/TED.2003.813457.

[11] A. Brown, G. Roy, and A. Asenov, "Impact of Fermi level pinning at polysilicon gate grain boundaries on nano-MOSFET variability: A 3-D simulation study," in *Proc. Eur. Solid-State Device Res. Conf.*, Sep. 2006, pp. 451–454, doi: 10.1109/ESSDER.2006.307735.

[12] H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1787–1796, Sep. 2005, doi: 10.1109/JSSC.2005.852164.

[13] K. G. Verma, B. K. Kaushik, and R. Singh, "Propagation delay variation due to process induced threshold voltage variation," in *Proc. Int. Conf. Adv. Inf. Commun. Technol.*, vol. 101, 2010, pp. 520–524.

[14] B. Kaur, A. Sharma, N. Alam, S. K. Manhas, and B. Anand, "A variation aware timing model for a 2-input NAND gate and its use in sub-65 nm CMOS standard cell characterization," *Microelectron. J.*, vol. 53, pp. 45–55, Jul. 2016, doi: 10.1016/j.mejo.2016.03.010.

[15] A. Moshrefi, H. Aghababa, and O. Shoaei, "Statistical estimation of delay in nano-scale CMOS circuits using burr distribution," *Microelectron. J.*, vol. 79, pp. 30–37, Sep. 2018, doi: 10.1016/j.mejo.2018.06.013.

[16] H. Jooypa and D. Dideban, "Embedding statistical variability into propagation delay time compact models using different parameter sets: A comparative study in 35-nm technology," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2714–2720, Jul. 2018, doi: 10.1109/TED.2018.2833879.

[17] H. Jooypa and D. Dideban, "Impact analysis of statistical variability on the accuracy of a propagation delay time compact model in nano-CMOS technology," *J. Comput. Electron.*, vol. 17, no. 1, pp. 192–204, Mar. 2018, doi: 10.1007/s10825-017-1108-2.

[18] H. Jooypa and D. Dideban, "Statistical strategies to reproduce the propagation delay time variability using compact models," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 11, pp. 1880–1884, Nov. 2019, doi: 10.1109/TCSII.2019.2895364.

[19] Z. Huang, A. Kurokawa, M. Hashimoto, T. Sato, M. Jiang, and Y. Inoue, "Modeling the overshooting effect for CMOS inverter delay analysis in nanometer technologies," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 2, pp. 250–260, Feb. 2010, doi: 10.1109/TCAD.2009.2035539.

[20] K. Zhang, Y.-N. Chen, Y. Dong, Z.-Q. Xie, Z.-F. Zhao, P. Si, T.-Y. Yu, L. Dai, and W.-F. Lv, "Effect of random channel dopants on timing variation for nanometer CMOS inverters," in *Proc. IEEE 2nd Int. Conf. Electron. Technol. (ICET)*, May 2019, pp. 208–212.

[21] *Originlab is a Licensed Software Which Can be Accessed From.* Accessed: Apr. 29, 2021. [Online]. Available: https://www.originlab.com

[22] B. Cheng, D. Dideban, N. Moezi, C. Millar, G. Roy, X. Wang, S. Roy, and A. Asenov, "Capturing intrinsic parameter fluctuations using the PSP compact model," in *Proc. Design, Autom. Test Eur. Conf. Exhib. (DATE)*, Mar. 2010, pp. 650–653, doi: 10.1109/DATE.2010.5457123.

HAMED JOOYPA received the M.Sc. degree in electrical engineering and electronics from the University of Kashan, Iran, in 2016. Since 2014, he has been teaching several courses in electronics and logic circuits. His current research interests include nanoelectronic devices, statistical circuit simulations, and statistical variability on circuits and systems.

DARYOOSH DIDEBAN received the M.Sc. degree in electrical engineering and electronics from the Sharif University of Technology, Tehran, Iran, in 2001, and the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 2012.

He was with the Device Modeling Group, University of Glasgow. He is currently an Associate Professor with the University of Kashan, Kashan, Iran, where he has supervised more than 25 M.Sc. students and six Ph.D. students. His current research interests include emerging nanoelectronic devices, 2D semiconductors, and statistical compact models. He has been a recognized reviewer of reputable journals in the field of semiconductor devices and nano-electronics with more than 100 articles reviewed.

HADI HEIDARI (Senior Member, IEEE) received the Ph.D. degree. He is currently an Associate Professor (Senior Lecturer) with the School of Engineering, University of Glasgow, U.K., where he leads the Microelectronics Laboratory. He has authored more than 90 articles in tier-1 journals and conferences. His research interests include developing microelectronics and sensors for neurotechnology devices. He is a member of the IEEE Circuits and Systems Society Board of Governors (BoG) and the IEEE Sensors Council Administrative Committee (AdCom). He was a recipient of a number of awards, including the Best Paper Award from ISCAS 2014, the PRIME 2014, the ISSCC 2016, the IEEE CASS Scholarship (NGCAS 2017), and the Rewards for Excellence Prize from the University of Glasgow, in 2018. He is the General Chair of the 27th IEEE ICECS 2020 in Glasgow. He served on the organizing committee for several conferences, including the U.K.-China Emerging Technologies (UCET), PRIME, in 2015 and 2019, the IEEE SENSORS, in 2016 and 2017, NGCAS 2017, and BioCAS 2018. He is an organizer for several special sessions on the IEEE conferences. He is an Associate Editor of the IEEE Journal of Electromagnetics, *RF and Microwaves in Medicine and Biology*, IEEE Access, and *Microelectronics Journal* (Elsevier). He is a Guest Editor of the IEEE Sensors Journal.

• • •