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Linear Equivalent Model for VHF Class Φ_2 Inverter Based on Spectrum Quantification Method to Reduce GaN Reverse Conduction Loss

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ABSTRACT Reverse conduction loss of GaN high electron mobility transistors (HEMTs) in very high frequency (VHF) converters is non-neglectable due to the absence of body diode. To reduce the reverse conduction time, this paper proposes a linear equivalent model for class Φ_2 inverter to derive optimal duty cycles for different working conditions. The proposed model is derived from frequency-domain perspective, which simplifies the derivation process and provides an intuitive physical insight for class Φ_2 inverter. Firstly, the power switch is modeled as a current source according to time-domain expressions of inductor current, which simplifies the circuit to a linear network. Based on quantitative analysis of the current source spectrum characteristics, the linear network response to the current excitation is derived, which forms the linear equivalent model. Then, drain voltage of the main switch under different working conditions is obtained. With the zero-crossing point of the drain voltage, numerical solutions of the optimal duty cycles are calculated. Finally, the optimal duty cycles are implemented with a high-resolution duty cycle generation circuit in a 27.12MHz prototype, which achieves not only a peak efficiency of 93.6% at full load, but also higher efficiency over the whole load and input voltage range compared to conventional fixed duty cycle.

INDEX TERMS GaN HEMTs, reverse conduction loss, very high frequency, class Φ_2 inverter, linear equivalent model, spectrum quantification.

I. INTRODUCTION

Resonant inverters are widely used in wireless power transfer systems [1], [2], resonant dc-dc power converters [3]–[5] and radio-frequency power amplifiers [6]. To improve the power density and performance of power systems, very high frequency (VHF) resonant power converters are widely explored in recent years [7]–[9]. As the switching frequency increasing to tens of MHz, GaN high electron mobility transistors (HEMTs) are preferred because of their advantages of fast switching speed, low switching loss and low drive power [10], [11]. However, due to the absence of body diode, the reverse conduction voltage of GaN HEMTs is much higher than that of Si MOSFET, as shown in Fig 1, which increases the reverse conduction loss and degrades efficiency [12], [13]. Furthermore, reverse conduction time in VHF resonant power converters is sensitive to working conditions [14], where the drain voltage of main power switch deviates as the load or input voltage varies. Since a fixed driving signal is usually used to control the power switch [15]–[18], the reverse conduction time often increases by the deviated drain voltage, leading to higher losses.

In order to reduce the reverse conduction time of GaN HEMTs, reverse conduction detection circuits implemented in gate driver ICs are proposed [19]–[22]. In [23], a gate side detection circuit is designed according to the transient voltage of gate-to-source capacitor. The power switch turns on at the transient completing moment. However, the minimum resolution of driving signal is 15ns, which is unacceptable for VHF operation. To improve the detection resolution, the reverse conduction duration is directly detected at the switching node [24]. Based on the detected duration, the driving signal

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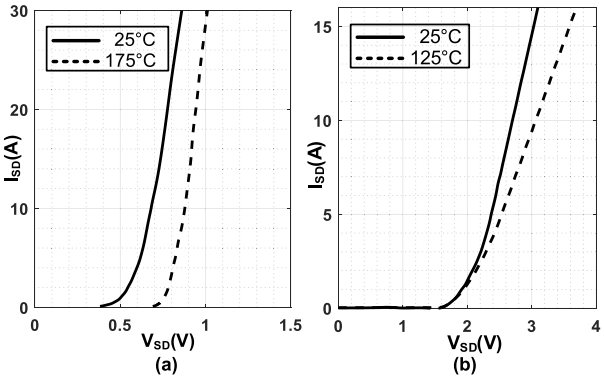

FIGURE 1. Reverse conduction characteristics of (a) Si MOSFET and (b) GaN HEMTs.

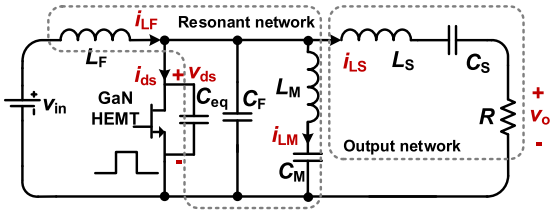

FIGURE 2. Topology of class Φ_2 inverter.

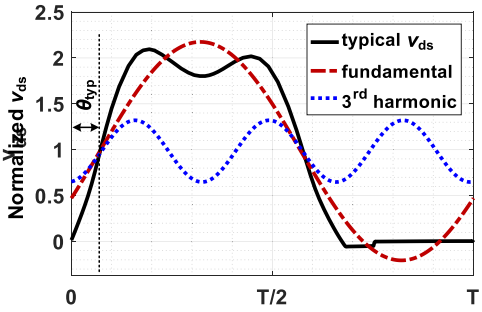

FIGURE 3. Typical drain voltage of class Φ_2 inverter and its harmonics.

is updated by a close loop correction circuit in the next switching cycle. Although the detection circuit can provide a high resolution of 0.66ns, the maximum operation frequency is limited to 10MHz due to the delay of the correction circuit. The detection-based circuits provide a solution to reduce reverse conduction time regardless of input voltage and load, but the switching frequency is constrained by detection circuit delay. Furthermore, the detection circuit is sensitive to parasitic inductance of PCB trace, which may cause difficulties to debug.

Comparatively, model-based method provides a flexible solution to reduce the reverse conduction time. Resistance compression networks are added at the output port of inverter stage to reduce load sensitivity [25]–[27], which reduce reverse conduction loss over a wide load range. But the additional passive components increase the complexity and cost of converters. Without changing the circuit topology, a digital adaptive driving schema based on a state-space model is implemented with a buffer chain [28]. However, output voltage variations are not considered in the derivation process. To improve efficiency of class E converter under a wide input and output range, the optimal driving signals are predicted by solving differential equations of the circuit [29]. Although the working conditions are greatly extended, the maximum working frequency is limited by the performance of commercial digital controllers. Besides, the differential equations for class Φ_2 converter are complicated. In the mentioned models, intuitive physical insight for VHF power converters is not provided. Furthermore, the limited duty cycle resolution constrains the application of the model in higher frequency.

To address above issues, a linear equivalent model for class Φ_2 inverter is proposed to derive the optimal duty cycles over wide input voltage and load range. The basic idea is to model the power switch as a current source, which simplifies the circuit to a linear network. By deriving the network response to the current source excitation, analytical expression of power switch drain voltage is derived. With the zero-crossing point of derived drain voltage, optimal duty cycles under different input voltage and load are calculated. Furthermore, the optimal duty cycles are generated from a high-resolution duty cycle generation circuit. By measuring input voltage and input current, the duty cycle is adjusted to the optimal value accordingly. With the proposed model and derived optimal duty cycles, the reverse conduction loss of GaN HEMT is significantly reduced from 551.7mW to 27.8mW in a class Φ_2 inverter prototype operating at 27.12MHz. This paper expands from our earlier conference publication [30], where initial experimental results are provided. Here, detailed theoretical analysis considering the non-linear characteristics of GaN output capacitor are presented and extended experimental results are provided.

The rest of this paper is organized as follows. In Section II, the influence of input voltage and load on GaN reverse conduction loss is discussed. In Section III, the linear equivalent model of class Φ_2 inverter is proposed to derive the optimal duty cycle under different working conditions. Furthermore, a high-resolution duty cycle generation circuit is proposed to realize the optimal duty cycles. In Section IV, the proposed model and derived optimal duty cycles are verified by experimental results. Finally, a brief conclusion is given in Section V.

II. REVERSE CONDUCTION LOSS OF GAN HEMTS WITH CONVENTIONAL FIXED DUTY CYCLE

The topology of class Φ_2 inverter is shown in Fig 2, which is regarded as three parts: main switch (GaN HEMT), a resonant network and an output network. By carefully designing the resonant network, the drain voltage is shaped as Fig 3, where the second harmonic is absorbed by $L_M - C_M$ branch. Therefore, the drain voltage is dominated by the fundamental and third harmonic, which greatly reduces drain voltage stress compared to class E topology.

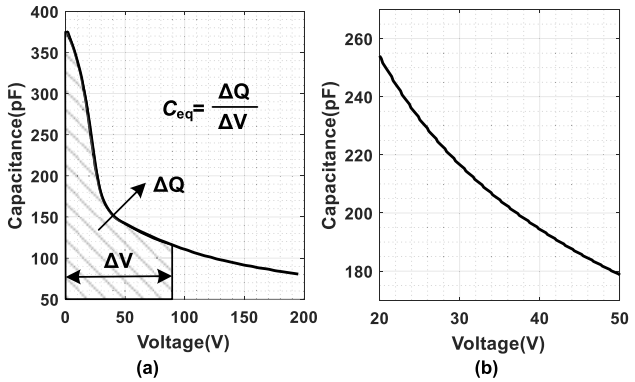

FIGURE 4. Non-linear characteristic of output capacitance of GaN HEMTs. (a) C_{oss} of EPC2019 with respect to junction voltage. (b) equivalent resonant capacitance in class Φ_2 inverter under different input voltage.

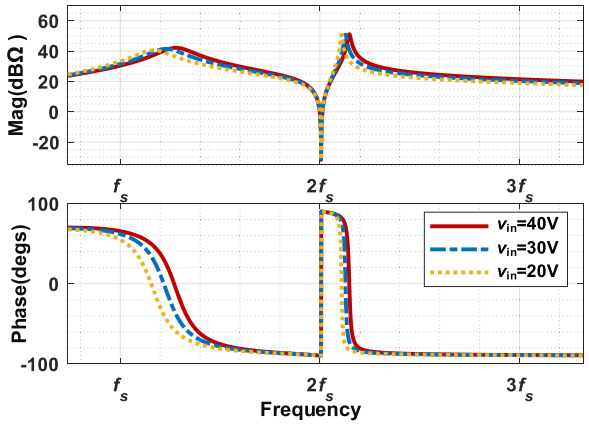

FIGURE 5. Z_{ds} characteristics under different input voltage.

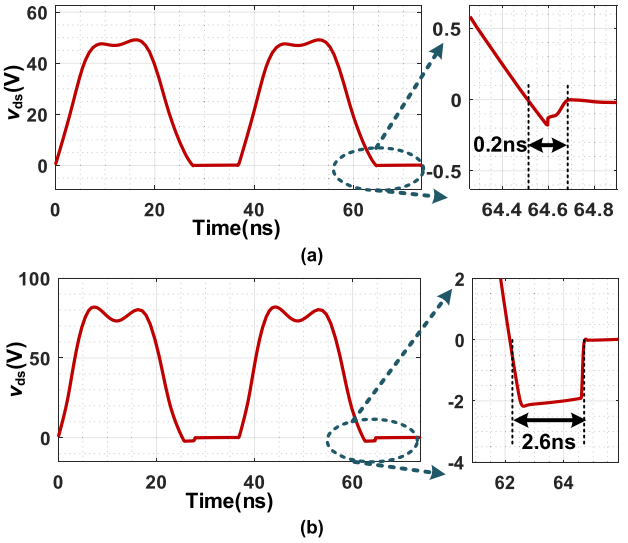

FIGURE 6. Drain voltage of class Φ_2 inverter under different input voltage. (a) $v_{in} = 25V$, $R = 18\Omega$. (b) $v_{in} = 40V$, $R = 18\Omega$.

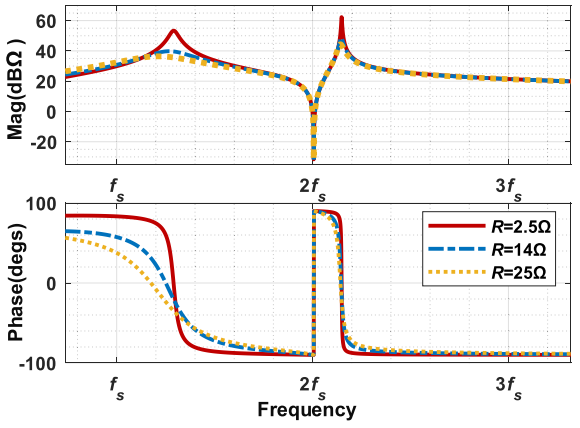

FIGURE 7. Z_{ds} characteristics under different load.

However, the drain voltage is sensitive to working conditions since it is determined by the switching node impedance (Z_{ds}) characteristics. For examples, as load or input voltage varies, the characteristics of Z_{ds} changes, leading to a deviated drain voltage. Nevertheless, the driving signals in conventional VHF power converters remain unchanged, which increases reverse conduction time and loss. The details of the increase in reverse conduction loss are as follows.

A. REVERSE CONDUCTION LOSS WHEN INPUT VOLTAGE VARIES

Due to the non-linear characteristic of the output capacitance (C_{oss}) of GaN HEMTs, the value of resonant capacitor $C_{eq} + C_F$ changes as input voltage varies. As shown in Fig 4, the equivalent capacitance C_{eq} decreases as input voltage increases, which affect the impedance characteristics of Z_{ds} as shown in Fig 5. It shows that the phase of Z_{ds} at switching frequency (f_s) increases as input voltage increases. The increased phase implies that Z_{ds} shows more inductive characteristic at f_s, and the phase of v_{ds} fundamental component increases as input voltage increases. Therefore, the drain voltage waveform is affected. With unchanged driving signal, v_{ds} reduces to zero before the power switch is turned on, and reverse conduction loss of GaN HEMTs is induced which degrades the overall power efficiency.

Simulation results for class Φ_2 inverter under different input voltage is given in Fig 6, where the specifications are the same as those in experiments. As shown in Fig 6(a), when $v_{in} = 25V$, the power switch is turned on immediately when the drain voltage reduces to 0 with no reverse conduction loss produced. Comparatively, when $v_{in} = 40V$, the drain voltage reduces to 0 before the power switch is turned on in Fig 6(b), which induces reverse conduction loss. As input voltage increases from 25V to 40V, the reverse conduction time increases from approximately 0.2ns to 2.6ns, and the reverse conduction loss increases from 3.6mW to 213.1mW.

B. REVERSE CONDUCTION LOSS WHEN LOAD VARIES

When load resistance changes, the switching node impedance characteristics change as shown in Fig 7. The phase of Z_{ds} increases as the load resistance decreases, which implies

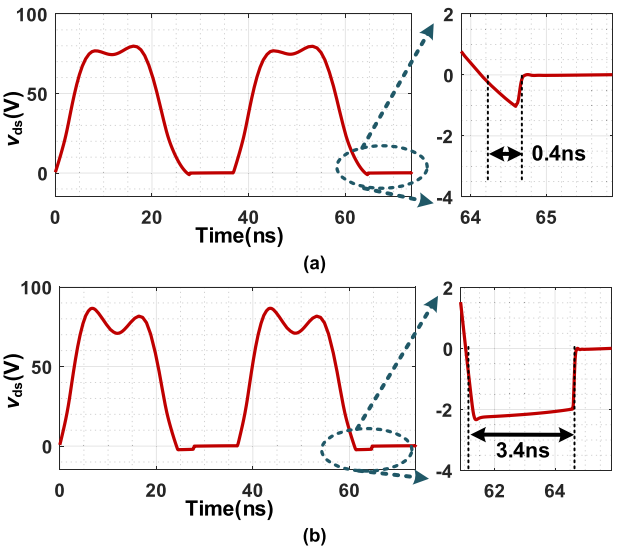

FIGURE 8. Drain voltage of class Φ_2 inverter under different load resistance. (a) $v_{in} = 40V$, $R = 25\Omega$. (b) $v_{in} = 40V$, $R = 10\Omega$.

more inductive impedance characteristic and longer reverse conduction time.

Simulation results for class Φ_2 inverter under different load is given in Fig 8. As load resistance decreases from 25Ω to 10Ω, the reverse conduction time increases from 0.4ns to 3.4ns, and the reverse conduction loss of GaN HEMTs increases from 43.0mW to 551.7mW.

In conclusion, when load or input voltage varies, the reverse conduction loss of GaN HEMTs in VHF class Φ_2 inverter increases significantly, which degrades the overall power efficiency. To reduce reverse conduction loss of GaN HEMT, the power switch should be turned on immediately once v_{ds} reduces to zero. Therefore, the duty cycle of driving signal should be adjusted accordingly under different working conditions.

III. LINEAR EQUIVALENT MODEL AND OPTIMAL DUTY CYCLES

To reduce the reverse conduction time of GaN HEMT in VHF class Φ_2 inverter, the linear equivalent model is proposed. Based on the model, numerical solutions for optimal cycles under different working conditions are calculated. Furthermore, the optimal duty cycles are realized through a high-resolution duty cycle generation circuit, which significantly reduces the reverse conduction time and improves overall efficiency.

A. ANALYTICAL EXPRESSIONS OF INDUCTOR CURRENT

The switch current is derived by solving the analytical expressions of inductor current. As shown in Fig 2, there are three inductors L_F, L_M, L_S in class Φ_2 inverter. By analyzing the current of these inductors, the switch current is derived. To simplify the analysis, reasonable assumptions are made that the on-resistance of power switch is zero and the output capacitance is absorbed in C_F.

Firstly, when the power switch is on, the voltage across L_F is v_{in}, and the current of L_F increases linearly during the switching on time. Besides, the average value of i_{LF} equals to average input current, which is estimated using output power and input voltage. Therefore, the analytical expression of i_{LF} is derived as (1).

$$i_{LF}(t) = i_{in,avg} + \frac{v_{in}}{L_F}(t - \frac{t_{on}}{2}) \quad t \in [0, t_{on}]. \tag{1}$$

Then the current of L_S (i_{LS}) is modeled by analyzing the typical v_{ds} waveform and considering the output network impedance characteristics. Class Φ_2 inverter is developed to reduce drain voltage stress of power switch devices. By carefully choosing the resonant components, Z_{ds} satisfies following constrains:

- The magnitude of Z_{ds} at the second harmonic is zero, so that the second harmonic of drain voltage is absorbed, and the peak drain voltage is reduced.
- The magnitude of Z_{ds} at fundamental frequency is 4-8dB larger than the magnitude at the third harmonic.
- The phase of Z_{ds} at fundamental frequency is between 30 and 60 degrees.

With such a resonant network, the fundamental and third harmonic of v_{ds} dominate, whereas the second harmonic is neglectable. Besides, as shown in Fig 3, the typical waveform of v_{ds} is usually symmetrical, so the phase difference between fundamental component and third harmonic is approximately zero. Therefore, the AC component of a typical v_{ds} is approximated as:

$$v_{ds,ac}(t) = V_1 \sin(\omega_s t + \theta_{typ}) + V_3 \sin(3\omega_s t + 3\theta_{typ}), \tag{2}$$

where ω_s is the switching frequency and θ_{typ} is the typical fundamental component phase of drain voltage in Fig 3. V_1, V_3 are the magnitudes of fundamental component and the third harmonic respectively.

The impedance of output network is calculated by:

$$Z_L(s) = \frac{1 + sRC_S + s^2 L_S C_S}{sC_S}. \tag{3}$$

Therefore, i_{LS} is approximated to:

$$i_{LS}(t) = \frac{V_1}{|Z_L(j\omega_s)|}\sin(\omega_s t + \theta_{typ} - \angle Z_L(j\omega_s)) + \frac{V_3}{|Z_L(3j\omega_s)|}\sin(3\omega_s t + 3\theta_{typ} - \angle Z_L(3j\omega_s)), \tag{4}$$

Subscribing R into (5), the output power is calculated by:

$$P_{out} = \left(\frac{V_1}{|Z_L(j\omega_s)|\sqrt{2}}\right)^2 R + \left(\frac{V_3}{|Z_L(3j\omega_s)|\sqrt{2}}\right)^2 R. \tag{5}$$

With the derived output power and input voltage, the average input current is calculated by:

$$i_{in,avg} \approx \frac{P_{out}}{v_{in}}. \tag{6}$$

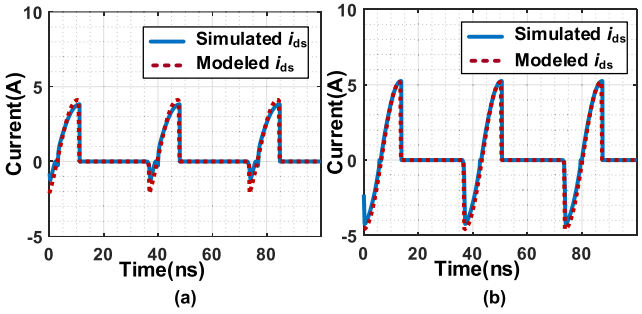

FIGURE 9. Simulated i_{ds} and modeled i_{ds} under different working conditions. (a) $R = 25\Omega$, $v_{in} = 40V$. (b) $R = 2.5\Omega$, $v_{in} = 40V$.

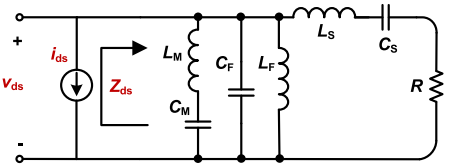

FIGURE 10. Linear equivalent model for class Φ_2 inverter.

The current of L_M (i_{LM}) only contains the second harmonic because the resonant frequency of $L_M - C_M$ branch is exactly $2\omega_s$,

$$i_{LM} = I_{LM} \sin(2\omega_s t + \theta_{2,typ}), \tag{7}$$

where $\theta_{2,typ}$ is the typical phase of i_{LM}. Combining the analyzing result of i_{LF}, i_{LS} and i_{LM}, i_{ds} is derived as:

$$i_{ds} = \begin{cases} i_{LF} - i_{LM} - i_{LS} & t \in [0, t_{on}] \\ 0 & t \in [t_{on}, T], \end{cases} \tag{8}$$

where T is the switching period of the inverter. To verify the accuracy of the i_{ds} model, an example is given in Fig 9, which shows that the model and the simulated waveform highly match under different load.

B. LINEAR EQUIVALENT MODEL AND NUMERICAL SOLUTIONS FOR OPTIMAL DUTY CYCLES

To simplify the analysis, the power switch is modeled as a current source based on the derived i_{ds}, which converts the circuit to a linear network in Fig 10. With the network response under the current source excitation, v_{ds} under different working conditions is derived, and the reverse conduction time is calculated to optimize the duty cycles.

As indicated in Fig 3, v_{ds} mainly composes of DC, fundamental component, and the third harmonic. According to inductor volt-second balance, the DC value of v_{ds} equals v_{in}. The fundamental and third harmonic is determined by i_{ds} and Z_{ds}. As a linear network, the fundamental and third harmonic of i_{ds}, v_{ds} satisfy

$$\begin{aligned} v_{ds,\omega s} &= -|Z_{ds}(j\omega_s)| \cdot |F_{ids}(\omega_s)| \\ &\quad \cdot \sin(\omega_s t + \angle F_{ids}(\omega_s) + \angle Z_{ds}(j\omega_s)) \\ v_{ds,3\omega s} &= -|Z_{ds}(j3\omega_s)| \cdot |F_{ids}(3\omega_s)| \end{aligned}$$

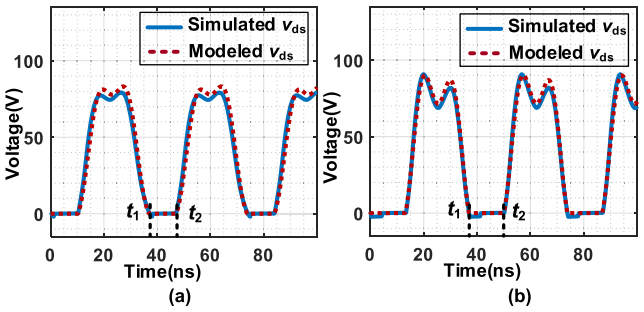

FIGURE 11. Modeled and simulated v_{ds} under different working conditions. (a) $R = 25\Omega$, $v_{in} = 40V$. (b) $R = 2.5\Omega$, $v_{in} = 40V$.

$$\cdot \sin(3\omega_s t + \angle F_{ids}(3\omega_s) + \angle Z_{ds}(j3\omega_s)), \tag{9}$$

where $v_{ds,\omega s}$ is the fundamental component of v_{ds} and $v_{ds,3\omega s}$ is the third harmonic of v_{ds}. The Fourier Series of i_{ds} is calculated by

$$F_{ids}(\omega) = \frac{2}{T} \int_0^T i_{ds}(t) e^{-j\omega t} dt, \tag{10}$$

Furthermore, Z_{ds} is calculated by:

$$Z_{ds}(s) = \frac{sL_F(1 + s^2 L_M C_M)}{1 + s^2(L_M C_M + L_F C_F + L_F C_M) + s^4 L_M C_M L_F C_F} //Z_L(s). \tag{11}$$

Therefore, when power switch is OFF, the analytical expression of v_{ds} is calculated by

$$v_{ds,off} = v_{in} + v_{ds,\omega s} + v_{ds,3\omega s}. \tag{12}$$

Furthermore, by solving the zero-crossing point of v_{ds} according to (12), the end (t_1) and the beginning time (t_2) of resonant process are calculated. Turning on the power switch at t_1 and turning it off at t_2 can effectively reduce the reverse conduction time. During t_1 to t_2, v_{ds} is clamped to zero by the power switch. Therefore, v_{ds} is derived as:

$$v_{ds} = \begin{cases} 0 & t \in [0, t_2\text{-}t_1] \\ v_{in} + v_{ds,\omega s} + v_{ds,3\omega s} & t \in [t_2\text{-}t_1, T] \end{cases} \tag{13}$$

A comparison between the modeled and simulated results is given in Fig 11, where the specifications are the same as those used in experiments. Despite the load varies, there is no big difference between the v_{ds} model and the simulated waveform.

Based on the analysis above, the optimal duty cycles are calculated by (14).

$$D_{opt} = \frac{t_2 - t_1}{T}. \tag{14}$$

The optimal duty cycles under different load resistance and input voltage are calculated in MATLAB and given in Fig 12. It shows that when the load resistance decreases or input voltage increases, adapting the duty cycle to a larger value can effectively reduce the reverse conduction time of GaN HEMT.

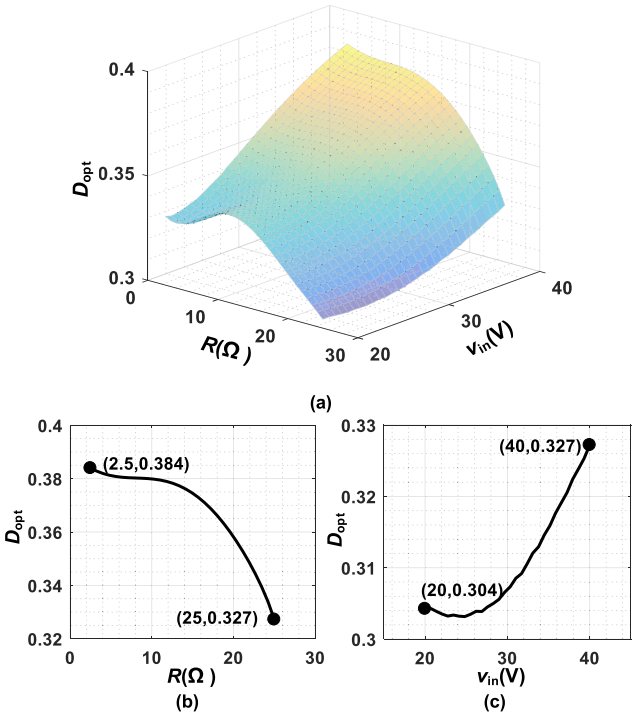

FIGURE 12. Optimal duty cycles for different working conditions (a) optimal duty cycles under different input voltage and load. (b) when $v_{in} = 40V$, optimal duty cycles with respect to load. (c) when $R = 25\Omega$, optimal duty cycles with respect to input voltage.

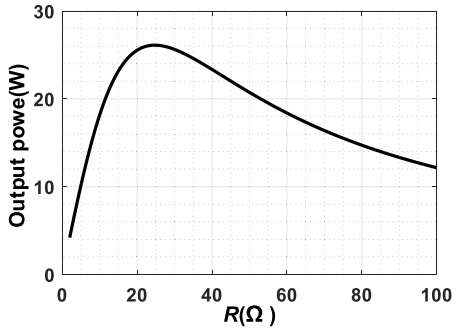

FIGURE 13. Relationship between load resistance and output power.

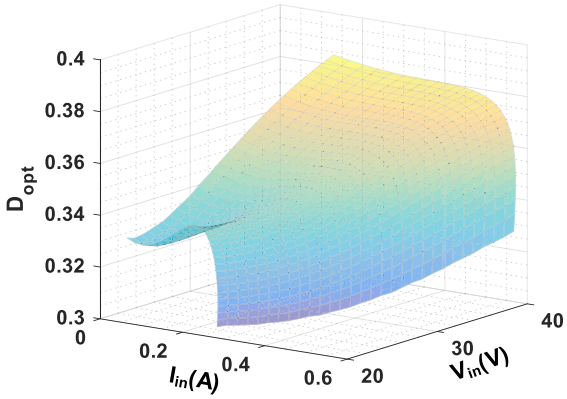

FIGURE 14. Optimal duty cycle with respect to input current and input voltage.

C. LOSS MODEL AND LOAD ESTIMATION

To apply the optimal duty cycles, the working conditions need to be observed. In the followings, input power and losses in VHF class Φ_2 inverter are calculated to estimate load resistance. The input power is calculated by:

$$P_{\text{in}} = v_{\text{in}} i_{\text{in}}. \tag{15}$$

The conduction loss caused by power switch is estimated based on i_{ds} and $R_{\text{ds,on}}$. However, the static $R_{\text{ds,on}}$ value given in datasheet is not accurate for VHF operation, and the dynamic $R_{\text{ds,on}}$ is roughly 4-6 times the value given in datasheet [31]. Therefore, the conduction loss of power switch is calculated by (16).

$$P_{\text{sw, on}} = i^2_{\text{ds, rms}} 5 R_{\text{ds, on}}. \tag{16}$$

In Section III. B, the analytical expression of i_{LM}, i_{LS} is derived. Therefore, the losses caused by L_{M} and L_{S} is calculated by:

$$\begin{aligned} P_{\text{LM}} &= i^2_{\text{LM, rms}} R_{\text{LM, ac}} \\ P_{\text{LS}} &= i^2_{\text{LS, rms}} R_{\text{LS, ac}}. \end{aligned} \tag{17}$$

The loss of L_{F} is approximated to

$$P_{\text{LF}} = 2 \cdot i^2_{\text{LFon, rms}} R_{\text{LM, ac}}, \tag{18}$$

where $i_{\text{LFon,rms}}$ is the root-mean-square (rms) value of i_{LF} during switching-on time. With the derived optimal duty cycles, the reverse conduction loss of GaN HEMTs is neglected. Therefore, the total loss of the inverter is calculated by (19), and the output power is estimated as (20).

$$P_{\text{Loss}} = P_{\text{sw,on}} + P_{\text{LM}} + P_{\text{LS}} + P_{\text{LF}}. \tag{19}$$

$$P_{\text{out}} = P_{\text{in}} - P_{\text{Loss}}. \tag{20}$$

Furthermore, based on FHA (fundamental harmonic approximation), the output power is calculated by:

$$P_{\text{out}} \approx \left| \frac{1}{R_{\text{Load}} + j\omega_s L_s} \right|^2 \frac{V_1^2 R}{2}. \tag{21}$$

The relationship between R and P_{out} is plotted in Fig 13. For a given P_{out}, there are two solutions for R. Discard the invalid solution, the load resistance is calculated by (22).

$$R = \frac{V_1^2 - \sqrt{V_1^4 - 16 L_s^2 P_{\text{out}}^2 \omega_s^2}}{4 P_{\text{out}}}. \tag{22}$$

With the derived load resistance, measured input voltage and average input current, the duty cycles under different working conditions can be adjusted to the optimal value.

D. REALIZATION OF OPTIMAL DUTY CYCLES

Based on the results of Section III. B and C, the optimal duty cycles under different input voltage and input current are given in Fig 14, where the specifications are the same as those in experiments.

The optimal duty cycles are realized using a high-resolution duty cycle generation circuit and a DSP Controller, as shown in Fig 15. The numerical solutions of optimal duty cycles

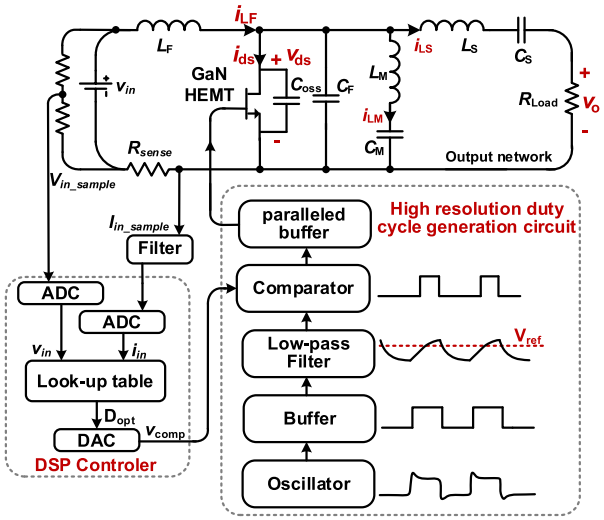

FIGURE 15. Realization of the derived optimal duty cycles.

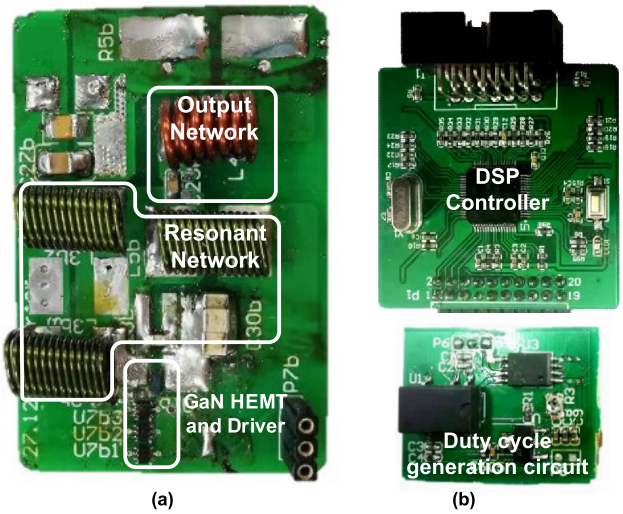

FIGURE 16. Prototype of class Φ_2 inverter. (a)Main power stage. (b) DSP control board and high-resolution duty cycle generation circuit.

under different working conditions are programed in the DSP controller. By measuring the input voltage and input current using 2 ADC modules, the optimal duty cycle D_{opt} is selected accordingly. The selected D_{opt} is then converted to an analog voltage v_{comp} by a DAC module. Finally, the duty cycle of gate driving signal is modulated by the high-resolution duty cycle generation circuit.

The generation circuit is designed delicately, since the resolution of commercial digital controller is low for VHF operation. Working principle of the circuit is explained as follows. Firstly, a square wave with approximately 0.5 duty cycle is generated by commercial MEMS clock oscillator. Then, a RC low pass filter converts the original square wave to a ramp signal. Finally, the signal is compared to a reference voltage v_{comp} using a high-speed comparator to generate a square wave, where the duty cycle can be adjusted by changing the reference voltage v_{comp}. Note that in the latest paper [29], duty cycle and frequency modulations are used to extend the input/output voltage range for HF DC/DC converters. The switching frequency is 2MHz, where commercial digital controller can still provide a square wave with adjustable duty cycle and frequency. However, as the frequency rises up to tens of MHz, full digital approach cannot satisfy the need for high-resolution driving signals. Therefore, the proposed circuit can be used to generate a square wave with adjustable duty cycle and frequency by replacing the clock oscillator with a voltage-controlled oscillator (VCO).

With the derived results and proposed circuit, the optimal duty cycles are implemented, which reduce the reverse conduction time of GaN HENTs and improve overall power efficiency.

IV. EXPERIMENTAL RESULTS

To verify the effectiveness of proposed model and derived optimal duty cycles, a class Φ_2 inverter prototype is built, as shown in Fig 16. The experimental circuit is designed for the inverter stage of a wireless power transfer system.

TABLE 1. Specifications of the prototype.

Components	Proposed method
L_S	150nH (6 turns of 1.3mm diameter copper wire with inner diameter 4.6mm)
C_S	4.7nF
L_F	143nH
C_F	3 2929SQ-431 in parallel
L_M	47pF+C_{OSS} (190pF)
C_M	430nH
C_{IN}	2929SQ-431GEC
R	20pF
Switch	4.7μF
Gate drive	2.5~25Ω
	Thick-film resistor
	EPC2019
	3 NC7WZ17 in parallel

The specifications of the inverter are shown in TABLE 1. The main switching component is a GaN HEMT from EPC (EPC2019). The gate driver is realized through 3 parallel high-speed buffers (NC7WZ17), since commercially available gate driver IC cannot operate properly at such a high frequency. The buffer is placed as close as possible to the main switch to reduce the parasitic inductance of gate driving path. Resonant inductors are realized using Coilcraft air-core inductors, and the resonant capacitor are realized with C0G Multiplayer Ceramic Chip Capacitors (MLCCs). The main DSP controller is TMS320F280049, which selects the optimal duty cycle according to input voltage and input current. The high-resolution duty cycle generation circuit generates the driving signal, which minimizes the reverse conduction time.

Experiments with conventional fixed duty cycle and proposed optimal duty cycles are both carried out to prove the effectiveness of derived optimal duty cycles.

A. DRAIN VOLTAGE WITH DIFFERENT CONTROL METHODS

The measured data is imported and replotted in MATLAB to better present the results. The drain and output voltage

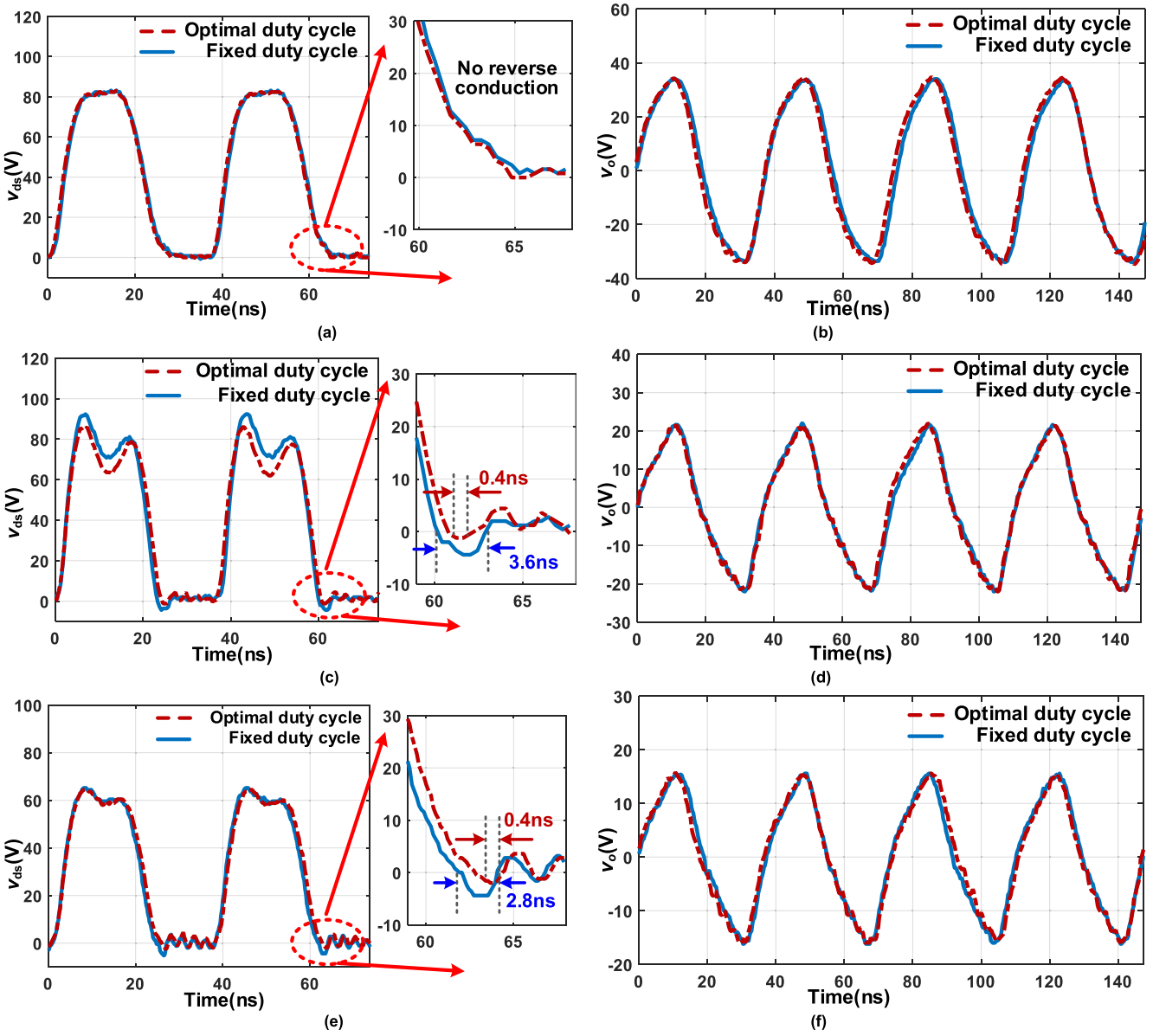

FIGURE 17. Drain and output voltage waveforms under different working conditions with different control. (a) drain voltage when $v_{in} = 40V$, $R = 25\Omega$. (b) output voltage when $v_{in} = 40V$, $R = 25\Omega$. (c) drain voltage when $v_{in} = 40V$, $R = 10\Omega$. (d) output voltage when $v_{in} = 40V$, $R = 10\Omega$. (e) drain voltage when $v_{in} = 30V$, $R = 10\Omega$. (f) output voltage when $v_{in} = 30V$, $R = 10\Omega$.

waveforms under the same working condition with different duty cycles are plotted in the same figure to emphasize the performance comparison.

Fig 17(a) shows the drain voltage when $R = 25\Omega$ and $v_{in} = 40V$. It shows that the drain voltage waveforms with conventional fixed duty cycle and proposed optimal duty cycles are the same. The power switch is turned on immediately when v_{ds} reaches 0 with no reverse conduction loss produced. Fig 17(b) shows the output voltage when $R = 25\Omega$ and $v_{in} = 40V$, which indicates the proposed method does not affect the output voltage of the inverter. Fig 17(c) and Fig 17(d) show the results when $R = 10\Omega$, $v_{in} = 40V$. The output voltage waveforms under fixed and optimal duty cycles are still the same. However, as the load resistance reduces from 25Ω to 10Ω, the drain voltage reduces to zero before the power switch is turned on with conventional fixed duty cycle. The reverse conduction time increases to 3.6ns, which induces reverse conduction loss and degrades power efficiency. Comparatively, the reverse conduction loss is reduced to 0.4ns with proposed optimal duty cycle, which improves the overall power efficiency. Moreover, as shown in Fig 17(e), when the input voltage reduces from 40V to 30V, the reverse conduction time with fixed duty cycle is 2.8ns. With proposed optimal duty cycle, the reverse conduction time is significantly reduced to 0.4ns.

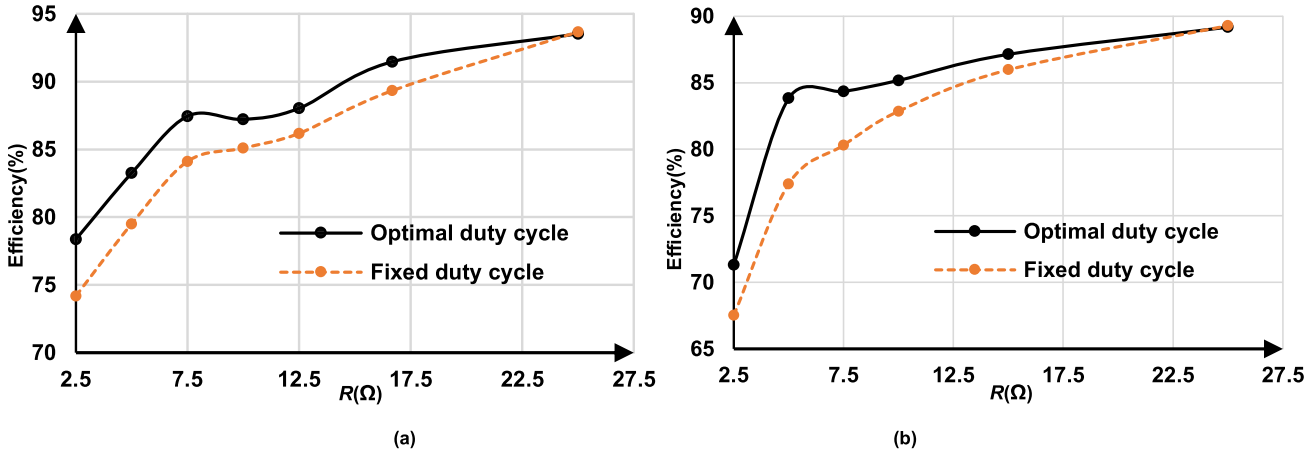

FIGURE 18. Overall efficiency under different load with different control (a)v_{in} = 40V (b)v_{in} = 30V.

TABLE 2. Reverse conduction time under different control.

v_{in}	R_{load}	Reverse conduction time	
		Conventional control	Proposed control
40V	25Ω	0.0ns	0.0ns
40V	16Ω	2.5ns	0.4ns
40V	10Ω	3.6ns	0.5ns
40V	5Ω	4.1ns	0.5ns
30V	25Ω	0.0ns	0.0ns
30V	16Ω	1.8ns	0.3ns
30V	10Ω	2.8ns	0.4ns
30V	5Ω	3.3ns	0.4ns

The reverse conduction time under different working conditions with different control is shown in TABLE 2. It shows that the optimal duty cycles significantly reduce the reverse conduction time over the whole input voltage and load resistance range.

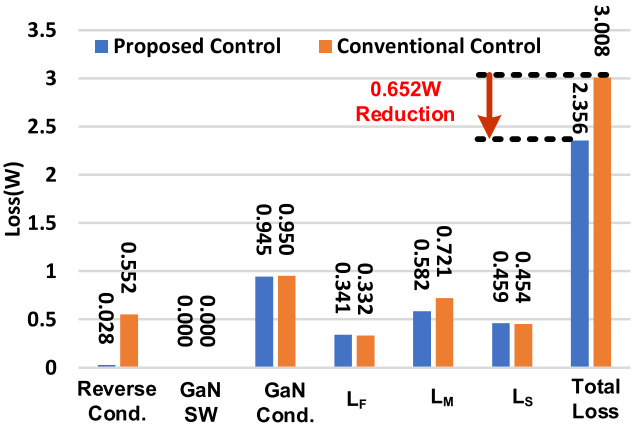

FIGURE 19. Loss breakdown under different control when v_{in} = 40V, R = 10Ω.

B. OVERALL EFFICIENCY AND LOSS BREAKDOWN UNDER DIFFERENT CONTROL METHODS

The efficiency under different working conditions with different control methods is measured and shown in Fig 18. The input power is obtained by measuring dc input voltage and dc input current with multimeter FLUKE 15B+. The output voltage is measured by oscilloscope MDO3054 with a bandwidth of 500MHz and a sample rate of 5GS/s. The root mean square (RMS) value of output voltage is then calculated based on the measured waveform. Furthermore, the output power is obtained by the RMS value of output voltage and the knowledge of load resistance.

Similar efficiency trend is achieved with respect to load resistance when v_{in} = 40V and v_{in} = 30V, as shown respectively in Fig 18(a) and Fig 18(b). When R = 25Ω, the efficiency under both fixed duty cycle and optimal duty cycle is 93.6%, since there is no reverse conduction loss under this working condition. However, as the load resistance reduces, higher efficiency is achieved with proposed optimal duty cycles since the reverse conduction time is significantly reduced. As shown in Fig 18, the proposed optimal duty cycles achieve higher efficiency over the whole load range. At full load when v_{in} = 40V, a peak efficiency of 93.6% is achieved. At light load when v_{in} = 40V, the efficiency with derived optimal duty cycle is 78.4%, while the efficiency with conventional method is 74.2%, an improvement of 4.2% is achieved.

To quantify the changes of each loss, loss breakdown when v_{in} = 40V, R = 10Ω is simulated and given in Fig 19. It shows that the reverse conduction loss of GaN HEMT is significantly reduced from 551.7mW to 27.8mW, an improvement of 523.9mW is achieved. This result indicates that reverse conduction loss of GaN HEMT is greatly reduced with derived optimal duty cycles. As a result, obvious overall efficiency improvement under proposed optimal duty cycles is achieved compared with conventional fixed duty cycle.

V. CONCLUSION

This paper proposes a linear equivalent model for VHF class Φ_2 to derive the optimal duty cycles under different

working conditions, which reduce the reverse conduction time of GaN HEMT and improve the overall efficiency. The non-linear characteristic of GaN HEMT output capacitance is considered to improve the accuracy of the model. Based on the model, comprehensive analysis of v_{ds} waveform under different working conditions are presented, which provide an intuitive physical insight to VHF class Φ_2 inverter. Furthermore, numerical solutions for optimal duty cycles under different working conditions are calculated based on the model. Finally, a high-resolution duty cycle generation circuit is designed to realize the derived duty cycles, which significantly reduce the reverse conduction time of GaN HEMT. A class Φ_2 inverter prototype operating 27.12MHz is built to verify the effectiveness of proposed method. The GaN HEMT is turned on immediately once v_{ds} reduces to zero which significantly reduces the reverse conduction loss. Therefore, higher efficiency is achieved with proposed control method across the whole input voltage and load range.

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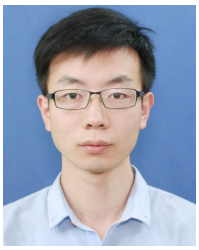

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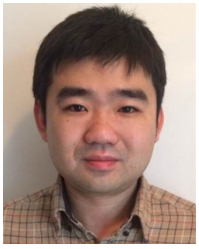

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