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2.4 GHz BLE Receiver With Power-Efficient Quadrature RF-to-Baseband-Current-Reuse Architecture for Low-Power IoT Applications

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ABSTRACT In this paper, a 2.4 GHz Bluetooth low energy receiver employing a power-efficient quadrature RF-to-baseband-current-reuse architecture is presented for low-power low-voltage internet of things applications. The proposed quadrature RF-to-baseband-current-reuse RF front-end consists of a low-noise transconductance amplifier, an active-type polyphase filter-based quadrature generator, transimpedance amplifiers, and double-balanced current-mode passive mixers on a single dc current path. An input matching network is used to perform power-constrained simultaneous noise and input power matching and $1/f$ noise reduction in the RF and baseband domains, respectively. The quadrature RF signals are provided to the single-quadrature mixers through an embedded active-type polyphase filter-based quadrature generator. The implemented Bluetooth low energy receiver is composed of the RF-to-baseband-current-reuse RF front-end, IF amplifiers, two-stage passive-*RC* polyphase filter, and fifth-order Chebyshev-II G_m-C filters. The proposed design was fabricated using a 65-nm CMOS process and characterized primarily in the Bluetooth low energy operating frequency bands. The active die area of the implemented receiver was 0.85 mm^2, and the receiver drew a bias current of 1.41 mA from a nominal supply voltage of 0.8 V. The Bluetooth low energy receiver achieved a noise figure of 13.2 dB, conversion gain of 42 dB, image rejection ratio of more than 30 dB, and input-referred third-order intercept point of −25 dBm.

INDEX TERMS Active-type polyphase filter, bias-current sharing, Bluetooth low energy, current-reuse, image rejection ratio, IoT, I/Q mismatch, low-IF receiver, low-voltage, non-invasive filter, quadrature generator, quadrature transconductor, RF-to-BB-current-reuse.

I. INTRODUCTION

In recent years, smart cities have been envisioned as a solution to problems such as traffic and environment degradation caused by urban concentration and a means to enhance the convenience and quality of life of the citizens and realize sustainable cities. Accordingly, considerable research is being performed on smart cities based on internet of things (IoT) sensor devices. To overcome the associated battery issues, most sensor devices adopt ultra-low-power IoT transceivers. In this regard, a Bluetooth low-energy (BLE) transceiver, which is a representative wireless communication protocol with a low data rate and power consumption, can be implemented in IoT smart sensors.

The BLE transceiver has relatively moderate specifications such as a sensitivity of −70 dBm with 1 MSym/s uncoded data, carrier-to-adjacent (2/3 MHz) interference ratio ($C/I_{2/3MHz}$) of −17 / −27 dB, and carrier-to-image interference ratio (C/I_{Image}) of −9 dB [1]. Based on the sensitivity and interference requirements, the specifications for the noise figure (NF) and input-referred third-order intercept points (IIP3) can be derived as 30 dB and −31 dBm,

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respectively [2]. In general, the interference in the image frequencies can degrade the carrier-to-noise ratio (CNR) and thus must be suitably eliminated. Moreover, the output CNR of the system is related to the image rejection ratio (IRR) and input CNR of the system, and can be expressed as $CNR_{OUT} = CNR_{IN} / (1 + 1 / IRR)$. When the sensitivity degradation caused by the image signals is required to be within 0.3 dB, an IRR of more than 21 dB is required with a C/I_{Image} of -9 dB. A low-power BLE receiver with a simple architecture can be implemented in such scenarios owing to its moderate requirements in terms of specifications, as mentioned previously. To this end, many researchers have attempted to enhance the key performance parameters of BLE receivers, including the sensitivity and linearity, while restricting the power consumption.

The current-reuse (CR) technique is a representative and powerful method to achieve a low-power design. The CR technique has been applied to unit blocks such as low-noise amplifiers (LNAs) and low-noise transconductance amplifiers (LNTAs) [3]. In recent years, CR techniques for sharing bias currents among several blocks have been actively studied. Specifically, an LNA-mixers-VCO (LMV) cell was developed [4] to be used in low-power applications; however, it cannot obtain a low NF, and VCOs with large blockers are generally susceptible to injection locking. Balun-LNA-mixer (BLIXER) cells [5], [6] can be used to reuse the bias currents of the building blocks. However, such cells also exhibit a high NF and insufficient linearity owing to the limited linearity of the active mixer and lack of RF filtering. A receiver architecture employing a function-reuse RF front-end and a CR VCO-filter cell has been proposed [7]; however, the NF of this architecture is also relatively high, and the in-band input 1-dB compression point is -50 dBm because of the low supply voltage of 0.5 V. Low-power receiver architectures in which the dc bias current of an RF LNTA and baseband (BB) stage is shared were also developed [8]–[11]. An RF-to-BB-CR receiver incorporating an RF bandpass filter with an eight-path passive mixer was proposed [8] to improve the linearity of the architecture. Moreover, an active noise-shaping network and linearity-enhancement circuits were proposed [9] to improve the NF and linearity, respectively. In another study [10], an active inductor was adopted to isolate the RF and BB stages. However, these RF-to-BB-CR receivers exhibited relatively high NFs. To reduce the NF, an RF-to-BB-CR receiver employing power-constrained simultaneous noise and input power matching (PCSNIPM) and $1/f$ noise reduction was introduced [11]. Such a receiver allowed the LNTA to implement PCSNIPM with an additional C_{EX} in the RF domain, thereby achieving a reasonably low NF. In previously developed RF-to-BB-CR receivers, quadrature signals for single-quadrature mixing were supplied through additional quadrature generators, such as divide-by-two circuits and passive-*RC* polyphase filters (PPF) in the local oscillator (LO) path. Nevertheless, if the RF LNTA of an RF-to-BB-CR receiver has an inherent quadrature-generation function, the additional circuits for quadrature generation in the LO path can be eliminated. In this regard, the design of a new quadrature RF-to-BB-CR receiver architecture is necessary to develop a power-efficient single-quadrature BLE receiver.

To this end, in this study, a 2.4 GHz BLE receiver with a power-efficient quadrature RF-to-BB-CR architecture was developed to be used in low-power IoT applications. Through the input matching network, the proposed receiver implemented PCSNIPM and $1/f$ noise reduction in the RF and BB domains, respectively. Moreover, an embedded active-type PPF was used to generate the quadrature signals for single-quadrature mixing.

The remainder of the paper is organized as follows. Section II describes the conventional RF-to-BB-CR architecture and proposed quadrature RF-to-BB-CR receiver architecture. Section III elaborates on the circuit implementation of the BLE receiver with the proposed receiver architecture. The experimental results are discussed in Section IV. The concluding remarks are presented in Section V.

II. NEW POWER-EFFICIENT QUADRATURE RF-TO-BB-CR RECEIVER ARCHITECTURE

This section describes the conventional RF-to-BB-CR receiver architectures as well as the novel power-efficient quadrature RF-to-BB-CR receiver architecture employing an active-type PPF-based quadrature generator.

A. CONVENTIONAL RF-TO-BB-CR ARCHITECTURE

Ghosh and Gharpurey [9] proposed an RF-to-BB-CR receiver architecture in which the dc bias current was shared between an LNTA and a transimpedance amplifier (TIA). However, the NF of this architecture was high. To reduce the NF, Kim and Kwon [11] introduced an RF-to-BB-CR receiver architecture that implemented PCSNIPM through an input impedance network, as shown in Fig. 1. The sources of M_{N1} and M_{N2} were degenerated through the impedance network consisting of C_{RFS}, L_S, and R_S. In the RF domain, the I-path of the receiver was simplified as shown in Fig. 1(b) when $1/\omega_{RF}C_{RF} \approx 0$ and $R_S \gg \omega_{RF}L_S$. The impedance network enabled the LNTA to perform PCSNIPM with an additional C_{EX} in the RF domain. The cascode devices improved the isolation and I/Q cross talk. In the BB domain, the I-path of the proposed receiver was simplified as shown in Fig. 1(b) when $1/\omega_{RF}C_{RFS} \approx \infty$. In this domain, the $1/f$ noises of the short-channel devices (M_{N1-6}) at the output were extremely intense and required to be suppressed. The R_S significantly reduced the $1/f$ noises of the devices, which are generated at the BB output owing to the source-degeneration effect. A double-balanced current-mode passive mixer driven by a non-overlapping 25% duty-cycle LO was used to realize the frequency down-conversion, which could increase the conversion gain, reduce the noise, and enhance the linearity of the architecture.

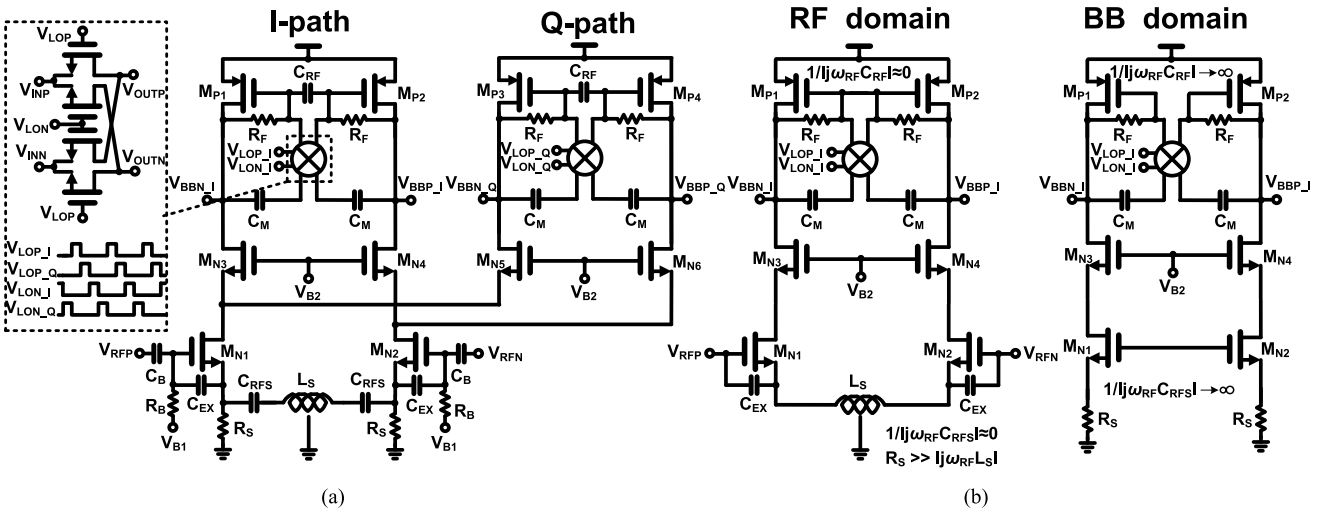

FIGURE 1. RF-to-BB-CR architecture with PCSNIPM and 1/f noise reduction technique [11] (b) Simplified schematics of the I-path in the RF and BB domains.

B. PROPOSED QUADRATURE RF-TO-BB-CR ARCHITECTURE

A quadrature RF-to-BB-CR receiver can be realized by implementing a quadrature LNTA in the RF-to-BB-CR receiver shown in Fig. 1(a). The quadrature RF-to-BB-CR receiver architecture is more power-efficient because the circuitry for quadrature generation in the LO path is eliminated. In recent studies, quadrature LNTAs based on a common-source (CS) amplifier with capacitive degeneration [4], [12], [13] and a quadrature LNTA based on the common-gate amplifier and single-*RC* network [14], [15] were developed, as shown in Fig. 2(a) and (b). When used as the LNA, the main transistors (M_0 and M_1) in the conventional topologies shown in Fig. 2 generated the quadrature output currents and influenced the overall performance in terms of the voltage gain, NF, and linearity. Moreover, two dc current paths existed in this framework. In general, separating the transistors that generate the quadrature output currents from those that influence the key performance parameters of the LNA is desirable to enhance the design degree of freedom. Moreover, it is advantageous to optimize the key performance parameters. Furthermore, to minimize the power consumption, the quadrature LNA must include only one dc current path. Recently, Park and Kwon proposed a quadrature LNTA topology with an active-type PPF-based quadrature generator which developed considering the aforementioned aspects, and it is shown in Fig. 3 [16]. The active-type PPF consisting of M_I, M_Q, R_I, R_Q, C_I and C_Q is shown in Fig. 3(b). The PPF can be placed in the cascode stage of the quadrature transconductor to provide accurate quadrature output currents. Unlike the passive-*RC* PPF, the proposed active- type PPF does not generate excessive loading on the preceding circuit. The small signal model can be analyzed to derive the quadrature output currents through Kirchhoff's current and voltage laws. Herein, to enable an intuitive and simple analysis, the effects of the parasitic capacitances and

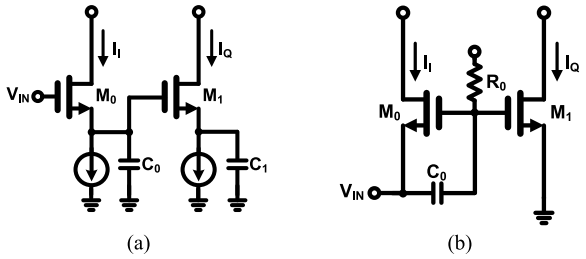

FIGURE 2. Conventional quadrature LNTA: (a) CS-based [12] (b) CG-based [14].

resistances of M_I and M_Q are ignored. The output currents I_I and I_Q can be expressed as follows:

$$I_I = g_{mI}(V_X - V_{IN}) = -\frac{1}{1 + sR_I C_I} g_{mI} V_{IN} \quad (1)$$

$$I_Q = g_{mQ}(V_Y - V_{IN}) = -\frac{sR_Q C_Q}{1 + sR_Q C_Q} g_{mQ} V_{IN} \quad (2)$$

According to (1) and (2), I_I and I_Q exhibit low- and high-pass filter characteristics, respectively. Moreover, I_I and I_Q exhibit a quadrature relationship when $R_I C_I = R_Q C_Q$, $\omega R_Q C_Q = 1$, and $g_{mI} = g_{mQ}$. In practice, because the parasitic capacitances and resistances of the transistors (M_I and M_Q) and layout routing lines considerably influence the quadrature characteristics, R_I, R_Q, C_I, and C_Q must be selected based on an extensive simulation with layout parasitic extraction.

The quadrature RF-to-BB-CR receiver architecture with the proposed quadrature LNTA is shown in Fig. 4. The architecture does not involve any additional circuits to realize quadrature generation in the LO path, and thus, the power consumption of the entire receiver is reduced. When $g_{mn1,2} = g_m$ and $g_{mn3-6} = g_{mC}$, the conversion gain of the proposed quadrature RF-to-BB-CR receiver in the I-path and Q-path

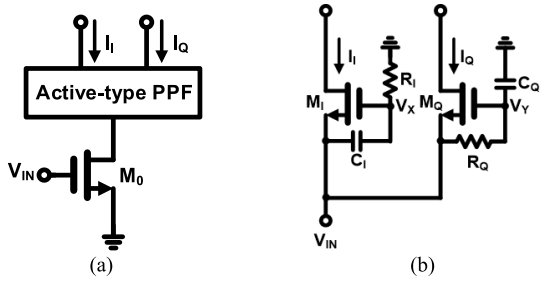

FIGURE 3. (a) Conventional quadrature LNTA with active-type PPF (b) active-type PPF [16].

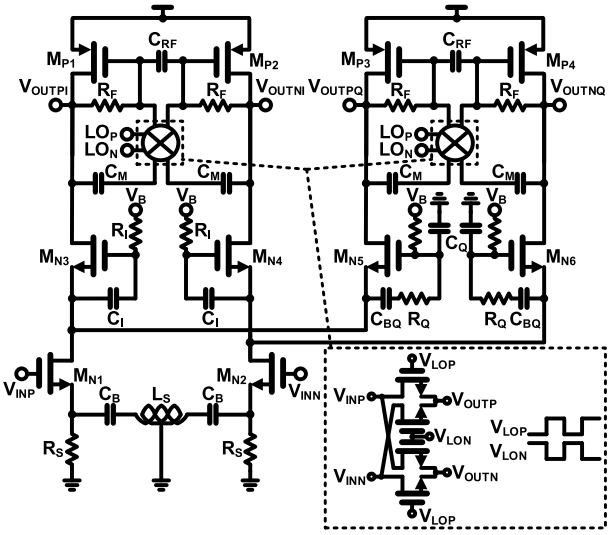

FIGURE 4. Proposed quadrature RF-to-BB-CR receiver architecture.

can be expressed as

$$A_{VI} \approx -\frac{2}{\pi}\frac{g_m g_{mC} R_F}{(1+sR_I C_{I,tot})}\left(\frac{1+sR_I C_I}{g_{mC}+sC_I} \parallel \frac{1+sR_Q C_Q}{sC_Q(R_Q g_{mC}+1)}\right) \tag{3}$$

$$A_{VQ} \approx -\frac{2}{\pi}\frac{g_m g_{mC} R_F C_Q\left(1+sR_Q C_Q\right)}{C_B\left(1+sR_Q C_{Q,tot}\right)} \times\left(\frac{1+sR_I C_I}{g_{mC}+sC_I} \parallel \frac{1+sR_Q C_Q}{sC_Q(R_Q g_{mC}+1)}\right) \tag{4}$$

where R_F is the feedback resistor of the TIA; C_{BQ} is the AC coupling capacitance; C_{gsI} and C_{gsQ} represent the gate-to-source capacitance of M_{N3-4} and M_{N5-6}, respectively. $C_{I,tot}$ is C_I+C_{gsI}; and $C_{Q,tot}$ is C_Q+C_{gsQ}. To facilitate the analysis, the other parasitic capacitances of M_i, such as C_{gdi}, C_{dbi}, and C_{sbi}, are neglected. In addition, assuming $R_I = R_Q = R_0$, $C_I = C_Q = C_0$, and $C_{BQ} \gg C_{Q,tot}$ and ignoring all parasitic effects, (3) and (4) can be expressed as

$$A_{VI} = -\frac{2}{\pi} g_m R_F \frac{g_{mC}}{g_{mC}+sC_0(2+g_{mC}R_0)} \tag{5}$$

$$A_{VQ} = -\frac{2}{\pi} g_m R_F \frac{sg_{mC}R_0C_0}{g_{mC}+sC_0\,(2+g_{mC}R_0)}. \tag{6}$$

Equations (5) and (6) indicate the conversion gains of the I-path and Q-path exhibit the quadrature relationships $|\,V_{OUTPQ}/V_{OUTPI}\,| = 1$ and $\angle(V_{OUTPQ}/V_{OUTPI}) = 90°$ at $\omega = 1/R_0C_0$.

III. PROPOSED BLE RECEIVER WITH THE QUADRATURE RF-TO-BB-CR RECEIVER ARCHITECTURE

This section describes the low-power BLE receiver exploiting the proposed quadrature RF-to-BB-CR receiver architecture along with the corresponding circuit implementation. The proposed BLE receiver adopts a single-quadrature low-IF receiver topology with an IF frequency of 2 MHz to achieve high integrity and low $1/f$ noise performance. As shown in Fig. 5, the BLE receiver is composed of the quadrature RF-to-BB-CR receiver RF front-end, IF amplifiers, two-stage passive PPF, and fifth-order Chebyshev-II filter. Because the quadrature signals are provided by the quadrature LNTA, differential LO signals are required to drive the single-quadrature mixers.

A. RF FRONT-END

The proposed quadrature RF-to-BB-CR receiver architecture shown in Fig. 4 is used to design the RF front-end of the BLE receiver. In particular, the architecture is composed of the LNTA, active-type PPF-based quadrature generator, double-balanced current-mode passive mixers with 50 % duty-cycle differential LO signals, and BB TIAs. Short-channel devices are adopted as $M_{N1}, M_{N2}, M_{N3}, M_{N4}, M_{N5}$, and M_{N6} owing to their influence on the RF characteristics. For M_{P1}, M_{P2}, M_{P3}, and M_{P4}, long-channel devices are adopted to reduce the $1/f$ noise in the BB domain. The impedance network consisting of C_{RFS}, L_S, and R_S performs PCSNIPM with additional C_{EX} in the RF domain and suppresses the $1/f$ noises of the short-channel main transistors in the BB output.

The noise factor of the proposed quadrature RF-to-BB-CR receiver RF front-end can be expressed as

$$F = 1+\frac{2(V_{MN1}^2+V_{MN3}^2+V_{MN5}^2+V_{RI}^2+V_{RQ}^2+V_{MP1}^2+V_{RF}^2)}{4kTR_SA_{Vtot}^2} \tag{7}$$

where k is the Boltzmann constant; T is the absolute temperature; R_S is the source resistance; A_{Vtot} is the conversion gain from the voltage source (V_S) to the output (V_{OUTPI}); and V_{MN1}, V_{MN3}, V_{MN5}, V_{RI}, V_{RQ}, V_{MP1}, and V_{RF} represent the output-referred noise voltages generated by M_{N1}, M_{N3}, M_{N5}, R_I, R_Q, M_{P1}, and R_F, respectively [16]. When the input impedance of the LNTA matches R_S, $\omega R_0C_0 = 1$, $g_{mn1,2} = g_m$, $g_{mn3-6} = g_{mC}$, and $g_{mp1,2} = g_{mp}$, A_{Vtot} is approximately given as

$$A_{Vtot} \approx -\frac{2}{\pi} Q_{IN}\, g_m R_F \frac{1}{\sqrt{1+\left(1+2/g_{mC}R_0\right)^2}} \tag{8}$$

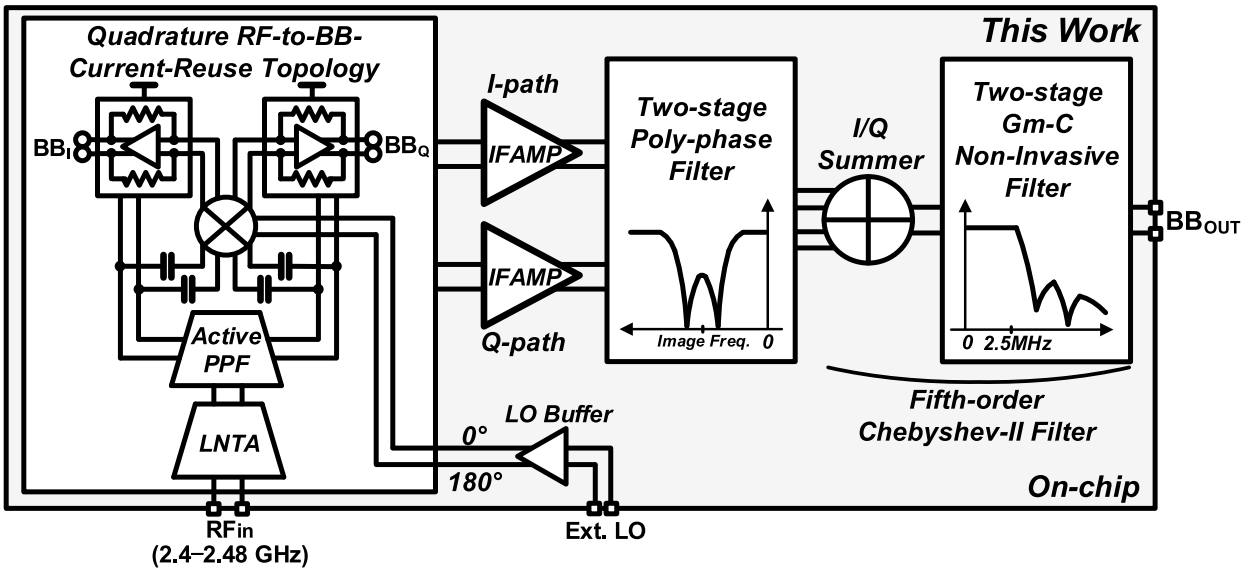

FIGURE 5. Block diagram of the proposed BLE receiver.

where Q_{IN} is the quality factor of the input matching network. The noise factor can be derived to

$$F \approx 1+\frac{2\gamma}{Q_{IN}^2 g_m R_S}\left(1+\frac{g_{mC}}{g_m}\left(1+\frac{2}{g_{mC}R_0}\right)^2+\frac{g_{mC}}{g_m}\right) +\frac{2}{Q_{IN}^2 g_m^2 R_S R_0}\left(\left(2+\sqrt{2}\,g_{mC}R_0\right)^2+1\right) +\frac{\pi^2}{2}\frac{1+\left(1+2/g_{mC}R_0\right)^2}{Q_{IN}^2 g_m^2 R_S}\left(g_{mp}\gamma+\frac{1}{R_F}\right) \quad (9)$$

where γ is a noise parameter and the second, third, and fourth terms represent the thermal noises of M_{N1}, M_{N3}, and M_{N5}; R_I and R_Q; and M_{P1} and R_F, respectively. Based on (9), the main transistor of the quadrature LNTA ($M_{N1,2}$) corresponds to the largest noise contribution. Moreover, the noise contributions of M_{N3} and R_I are significant and depend on the values of g_m, g_{mC}, and R_0. Similar to the conventional CS LNA with inductive degeneration and a cascode device, the proposed quadrature LNTA involves an intrinsic trade-off relationship between the NF and input impedance matching. Specifically, the LNTA is designed to optimize the NF performance. The device parameters of the quadrature RF-to-BB-CR receiver RF front-end are selected such that the BLE receiver corresponds to NF $<$ 15 dB, S11 $<$ -10 dB, and IRR $>$ 21 dB. The target power consumption of the RF-to-BB-CR receiver RF front-end is less than 1 mW under a nominal supply voltage of 0.8 V. These values are established based on a detailed simulation with layout parasitic extraction, as summarized in Table 1.

Assuming that the gain and phase errors are sufficiently small, the IRR of the receiver can be approximately set as $4 / (\varepsilon^2 + \Delta\theta^2)$, where ε and $\Delta\theta$ denote the gain error and phase error of the quadrature signals, respectively [17]. To achieve IRR $>$21 dB, the gain and phase errors of the quadrature signals should be less than 1.4 dB and 4°, respectively. The simulated gain and phase mismatches of the designed quadrature RF-to-BB-CR receiver RF front-end for different RF frequencies are shown in Fig. 6. The RF front-end can provide quadrature signals with gain and phase mismatches of less than 0.3 dB and 0.35° in the BLE band, respectively. The Monte-Carlo simulation results for the gain and phase errors at 2.44 GHz are shown in Fig. 7. In the case of random device mismatches and process variations, the mean values of the gain and phase errors of the proposed quadrature LNTA at 2.44 GHz are 0.29 dB and 0.39°, respectively. The standard deviations of the gain and phase errors are 0.46 dB and 0.55°, respectively. These values are sufficient to achieve an IRR of more than 21 dB.

TABLE 1. Device parameters of quadrature RF-to-BB-CR receiver front-end.

Device parameters	Value
Supply Voltage / I_{dc}	0.8 / 0.8mA
g_m and size of $M_{N1,2}$	6.5 mS, 40 µm / 0.15µm
g_{mC} and size of $M_{N3\text{-}6}$	3.3 mS, 30 µm / 0.24µm
g_{mp} and size of $M_{P1\text{-}4}$	3.7 mS, 100 µm / 0.24µm
C_I, C_Q, and C_B	100 fF, 200 fF, 5 pF
R_I, R_Q, and R_B	370 Ω, 260 Ω, 100 kΩ

B. IF AMPLIFIER

IF amplifiers are primarily used to drive the following two-stage passive-*RC* PPF and amplify the output voltage of the TIA. As shown in Fig. 8, the topology of the IF amplifiers involves a CS amplifier and cross-stacked source-follower [13]. The gain of this combined topology with the buffering function is more than 0 dB; therefore,

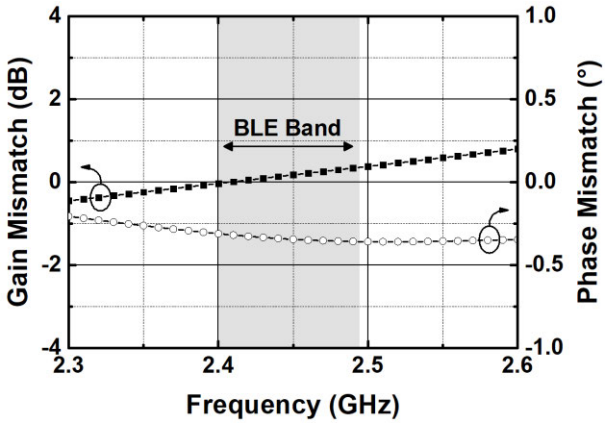

FIGURE 6. Simulated gain and phase mismatches of the designed RF front-end.

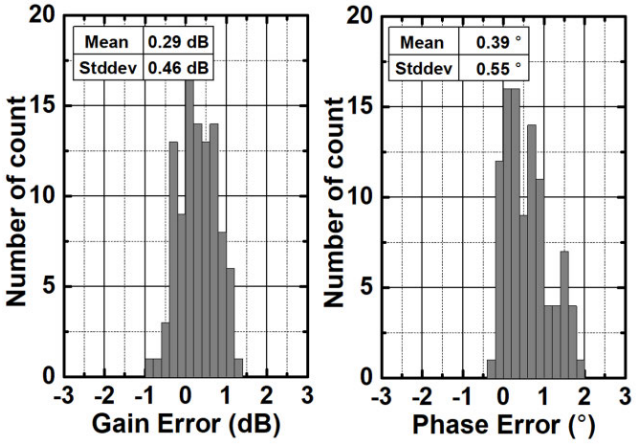

FIGURE 7. Monte-Carlo simulation results at 2.44 GHz with options of device mismatch and process variations (N = 100): (a) gain error and (b) phase error.

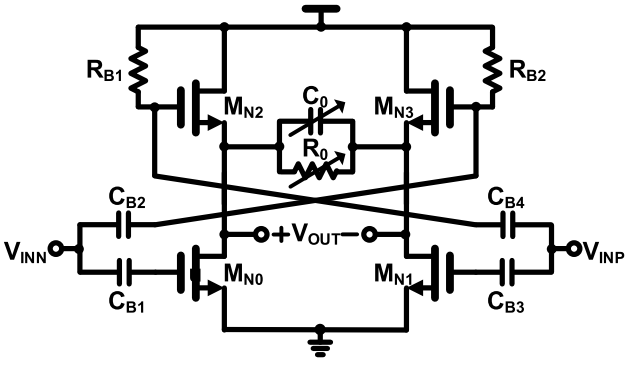

FIGURE 8. IF amplifier.

it can drive the following passive PPF without performance degradation. Furthermore, the IF amplifier performs low-pass filtering with R_0 and C_0. The capacitor array of C_0 can compensate for the variation in the 3-dB cut-off frequency caused by process, voltage, and temperature (PVT) variations. In addition, the resistor array of R_0 can calibrate the I/Q gain mismatch to achieve sufficient IRR performance.

C. TWO-STAGE POLYPHASE FILTER

The two-stage passive-*RC* PPF shown in Fig. 9 is employed to reject the image signals. In particular, the passive topology can enhance the linearity performance. The PPF generates a notch in the frequency response at the positive or negative frequency axis. Although a single notch can be generated only at a single frequency with ideal quadrature signals, the notch depth is degraded owing to the quadrature imbalances caused by the time constant variations [17]. To obtain broad IRR characteristic in the entire image band, two notch frequencies are set as –1.6 and –2.6 MHz. Moreover, considering the trade-off relationship between the device sizes and NF, R_1, R_2, C_1, and C_2 are set as 10 k Ω, 24 kΩ, 6 pF, and 4 pF, respectively, to establish the notch frequencies. C_1 and C_2 can be tuned using 4-bit digitally controlled signals to compensate for the variations in the notch frequencies caused by the PVT variations.

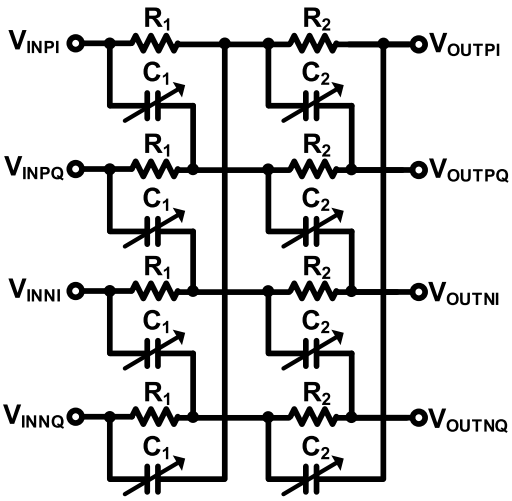

FIGURE 9. Two-stage passive-RC poly-phase filter.

D. FIFTH-ORDER CHEBYSHEV-II FILTER

The BB filter performs channel selection and suppresses out-of-band blockers. According to the BLE standard [1], the carrier-to-adjacent interference ratios ($C/I_{2/3MHz}$) are −17 and −27 dB at the offset frequencies of 2 and 3 MHz, respectively. Therefore, the BB filter should attenuate the interferences at the offset frequencies of 2 and 3MHz by more than 17 and 27 dB, respectively. To satisfy the rejection specification of the adjacent signals, the fifth-order Chebyshev-II topology is selected for channel selection. As shown in Fig. 10, this topology consists of an I/Q summer embedding first-order low-pass filter and two-stage second-order biquad filters based on a non-invasive G_m-C filter topology. As shown in Fig. 10, the I/Q summer includes of I/Q G_m-stages and PMOS load. The G_m-stages realize quadrature voltage-to-current conversion, and the quadrature currents are summed in the PMOS load. Resistive degeneration is applied to enhance the linearity performance. Moreover, the I/Q summer can provide a real pole at $\omega = 1/R_F C_F$.

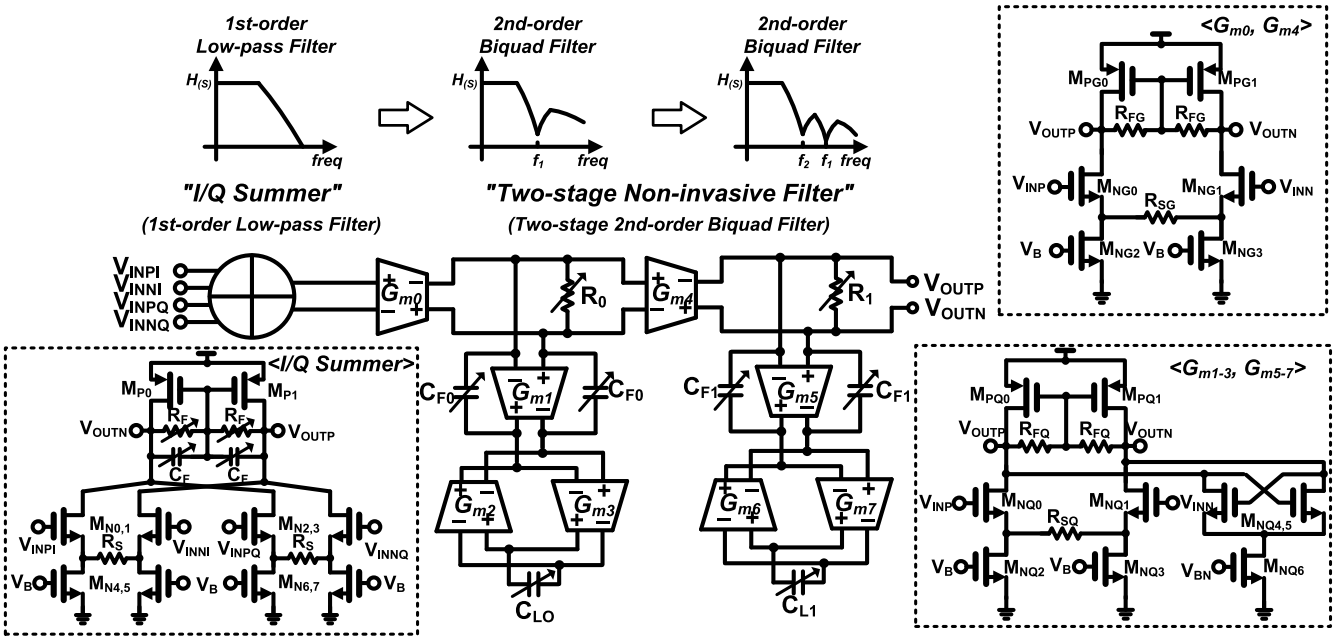

FIGURE 10. Fifth-order Chebyshev-II filter.

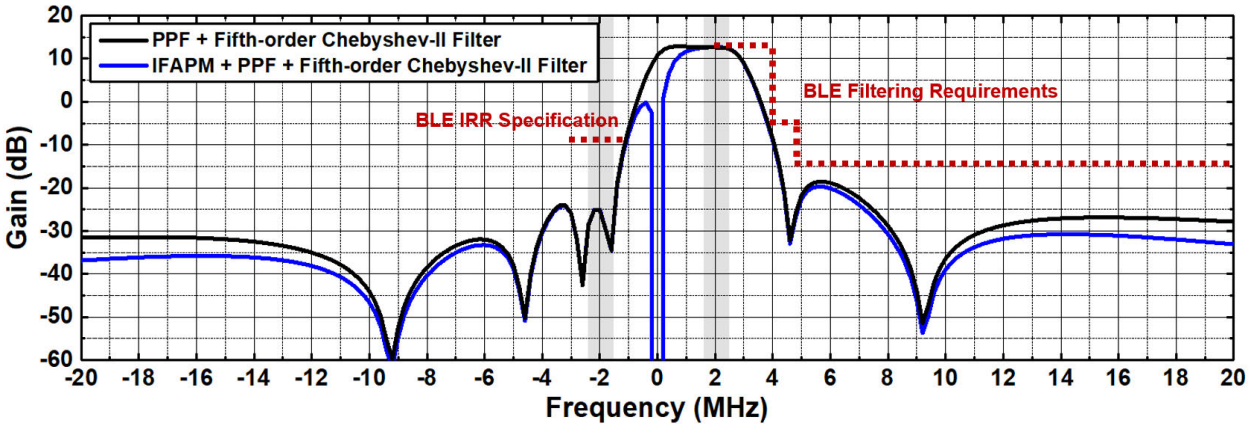

FIGURE 11. Simulated frequency response of the baseband analog circuits.

R_F and C_F can be tuned through 6-bit digitally controlled signals to compensate for the variation in the 3-dB cut-off frequency caused by the PVT variations. The second-order biquad filter adopts a non-invasive G_m-C filter topology, which exhibit a higher linearity and lower noise than the conventional biquad G_m-C topologies [18], [19]. As shown in Fig. 10, the biquad implements notch filtering at the output node with an emulated series LC tank, $Z_N(s)$ placed in parallel with the signal path. $Z_N(s)$ operates as an open and short circuit in the signal and interference bands, respectively. Consequently, $Z_N(s)$ exhibits a certain selectivity with negligible additional noise and generates a small intermodulation current [19]. In the first biquad filter, the gyrator composed of G_{m2} and G_{m3} converts C_{L0} to an emulated inductor $L_{L0} = C_{L0}/\,G_{m2}G_{m3}$. C_{F0} and L_{L0} form the notch impedance $Z_N(s)$ by emulating the series LC tank. The transfer function of the fifth-order Chebyshev-II filter can be expressed as

$$H(s) = -\frac{G_{mIQ}R_F}{1+sR_FC_F}\,\frac{G_{m0}R_0\left(1+\frac{C_{F0}C_{L0}}{G_{m2}G_{m3}}s^2\right)}{1+R_0C_{F0}s+\frac{C_{F0}C_{L0}}{G_{m2}G_{m3}}(G_{m1}R_0+1)s^2} \times\frac{G_{m1}R_1\left(1+\frac{C_{F1}C_{L1}}{G_{m6}G_{m7}}s^2\right)}{1+R_1C_{F1}s+\frac{C_{F1}C_{L1}}{G_{m6}G_{m7}}(G_{m5}R_1+1)s^2} \quad (10)$$

where G_{mIQ} and G_{mi} denote the overall transconductances of the I/Q summer and i-th G_m-cell, respectively. In the design of the G_m-C filter, the G_m-cell is the dominant component influencing the performances of the filter. In particular, all the G_m-cells employ the CS transconductor with resistive degeneration to enhance the filter linearity. The largest noise contribution, which corresponds to G_{m0}, influences the overall noise performance of the filter. The G_m-cells

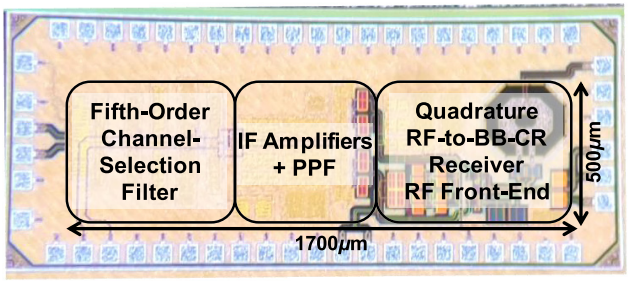

FIGURE 12. Die microphotograph.

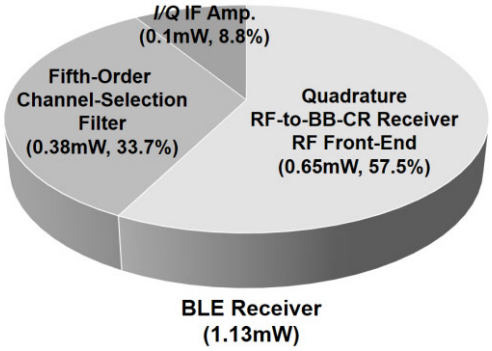

FIGURE 13. Power breakdown of the proposed BLE receiver.

constituting $Z_N(s)$ determine the notch selectivity. Because the finite output impedance of the G_m-cells (G_{m1-3}, G_{m5-7}) can degrade the notch depth and roll-off factor of the filter, negative-resistance is adopted in the G_m-cells to enhance the output impedance [20], [21]. Furthermore, all the resistors and capacitors can be tuned to compensate for the variations in the dc gain, quality factor, and 3-dB cut-off frequency of the filter caused by PVT variations. The simulated frequency response of the BB analog circuits, which consist of the IF amplifiers, two-stage passive *RC* PPF, and fifth-order Chebyshev-II filter, is shown in Fig. 11. The BB analog circuits can satisfy all the specifications for image rejection and channel-selection pertaining to the BLE standard.

IV. EXPERIMENTAL RESULTS

The 2.4 GHz BLE receiver with the proposed power-efficient quadrature RF-to-BB-CR receiver architecture was implemented using a 65-nm CMOS process. The photograph of the chip is shown in Fig. 12. The active area without the bond pads is 1.7 mm × 0.5 mm. The power consumption of the BLE receiver is 1.13 mW with a nominal supply voltage of 0.8 V. The power breakdown is depicted in Fig. 13. The power consumptions of the quadrature RF-to-BB-CR receiver RF front-end, I/Q IF amplifiers, and fifth-order channel-selection filter are 0.65, 0.1, and 0.38 mW, respectively. To perform the measurements, a grounded 50 Ω coplanar waveguide was applied on an assembled printed circuit board. The insertion losses of the input trace, off-chip balun, and matching components were measured at the BLE operating frequencies. The measurement results were compensated considering these losses.

The measured and simulated S11 of the receiver are shown in Fig. 14. The measured S11 is below −10 dB in the BLE band of 2.4–2.4835 GHz. In the measurement, the influence of the PCB input traces and off-chip balun characteristics allowed wider input power matching to be performed. The measured and simulated frequency responses of the implemented BLE receiver are illustrated in Fig. 15. The RF and LO frequencies are 2.442 and 2.44 GHz, respectively. The measured conversion gain of 42 dB is obtained at an IF frequency of 2 MHz. As shown in Fig. 15, the sixth-order channel selection appears on both sides of the LO frequency,

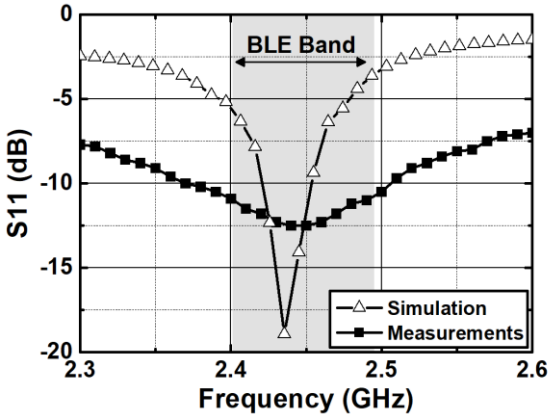

FIGURE 14. Measured and simulated S11.

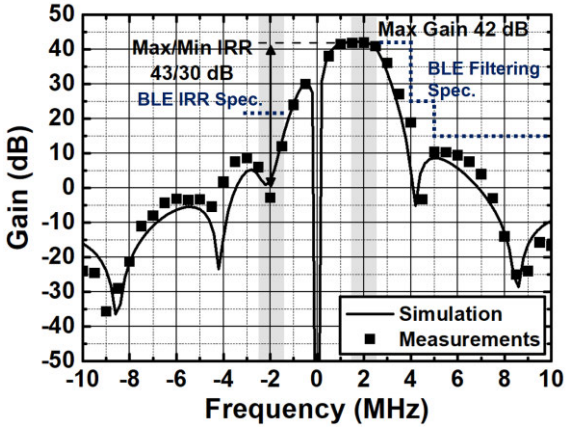

FIGURE 15. Measured and simulated frequency responses.

and two notches appear in the image band owing to the additional image rejection on the left side of the LO frequency. The channel-selection at the offset frequencies of 2 and 3MHz are more than 22 and 31 dB, respectively. With these values, the BLE specification for the rejection of adjacent signals can be satisfied. The maximum and minimum IRRs measured within the BLE channel bandwidth of 1 MHz are 43 dB and 30 dB, respectively. The margin for the IRR specification of 21 dB is adequate. The measured minimum IRR of 30 dB

TABLE 2. Measured performance summaries of the proposed BLE receiver and comparison with previous works.

	Application	Process	Receiver Topology	Current-Reuse Topology	I/Q Generation		Frequency [GHz]	Gain [dB]	NF [dB]	IIP3 [dBm]	IRR [dB]	Pdc [mW]	VDD [V]	Area [mm^2]
JSSC2010 [4]	Zigbee	90nm CMOS	Low-IF	LMV	RF	LNTA / RC PPF	2.4-2.48	76	10	−13	35	3.6	1.2	0.23
JSSC2014 [6]	Zigbee	65nm CMOS	Low-IF	BLIXER	LO	1/2	2.4-2.48	57	8.5	−6	36	1.7	1.2/0.6	0.24
JSSC2014 [7]	IoT	65nm CMOS	Low-IF	CR VCO-Filter	LO	1/2	0.43-0.96	50	8.1	−20.5	20.5	1.15	0.5	0.2
JSSC2014 [8]	TV	65nm CMOS	Zero-IF	RF-to-BB-CR	LO	1/2	0.15-0.85	51	4.6	17.4	No Image	10.6-16.2	1.2/2.5	0.55
JSSC2012 [9]	GPS	180nm CMOS	Low-IF	RF-to-BB-CR	LO	1/2	0.9-0.92	44.5	4.3	−14.5	NR[1)]	8	1.8	0.5
JSSC2017 [10]	Bluetooth	28nm CMOS	Low-IF	RF-to-BB-CR	LO	1/2	2.4-2.48	43.4	7.5	6	31	4.3	1.8	0.4
MWCL2019 [11]	IoT	65nm CMOS	Low-IF	RF-to-BB-CR	LO	1/2	0.9-0.92	40.7	1.94	−25.6	NR[1)]	3.6	1.8	0.559
JSSC2015 [14]	BLE	130nm CMOS	Low-IF	LMV	RF	LNTA	2.4-2.48	56.1	15.1	−15.8	30.5	0.6	0.8	0.25
TMTT2021 [16]	BLE	65nm CMOS	Low-IF	G_m-stage	RF	LNA	2.4-2.48	49.5	8.2	-25.75	> 33	2.16	0.8	1.16
TMTT2018 [22]	BLE Zigbee	28nm CMOS	Sliding-IF	LNA	LO	1/4	2.4-2.48	65	6.5	−20	31	0.64	0.8	0.251
TMTT2019 [23]	BLE	130nm CMOS	Low-IF	LNA	RF	RC PPF	2.4-2.48	42	7.2	−17	40	1.7[2)]	1.2	0.7
JSSC2019 [24]	BLE	40nm CMOS	Zero-IF	LNTA	LO	DCO	2.4-2.48	86	6	−35	No Image	1.55[2)]	0.85	0.3
ISSCC2020 [25]	BLE	22nm FDSOI	Zero-IF	LNTA	LO	1/2	2.4-2.48	61	5.5	−7.5	No Image	0.37	0.7	0.5
JSSC2018 [26]	Zigbee	65nm CMOS	Sliding-IF	CR Balun-LNA Hybrid mixer	LO	1/2	2.4-2.48	57.8	15.7	−18.5	37	1.78	1	0.45
ASSCC2019 [27]	BLE	22nm FDSOI	Low-IF	LNTA	LO	1/2	2.4-2.48	32.3	9.4	-30	27.7	0.33	0.55	0.15
CICC2017 [28]	BLE	40nm CMOS	Zero-IF	LNA	LO	1/2	2.4-2.48	47-72	5.2	-19.7	No Image	0.98	1	0.7
JSSC2013 [29]	Zigbee	65nm CMOS	Low-IF	IF Amplifier	LO	1/8	2.4-2.48	83	6.1	-21.5	NR[1)]	1.6	0.3	2.496
SSLC2019 [30]	BLE	28nm CMOS	Low-IF	LNTA	LO	1/4	2.4-2.48	53.3	6.5	-32	15.3	0.35	0.9	0.1
This Work	BLE	65nm CMOS	Low-IF	Quadrature RF-to-BB-CR	RF	LNTA	2.4-2.48	42	13.2	−25	> 30	1.13	0.8	0.85

1) NR: not reported. 2) It includes power consumption of the demodulator.

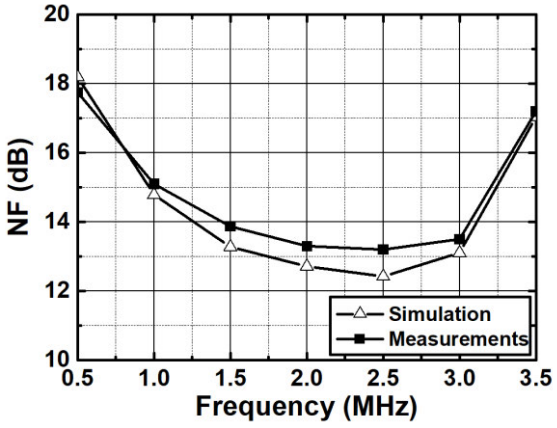

FIGURE 16. Measured and simulated NF.

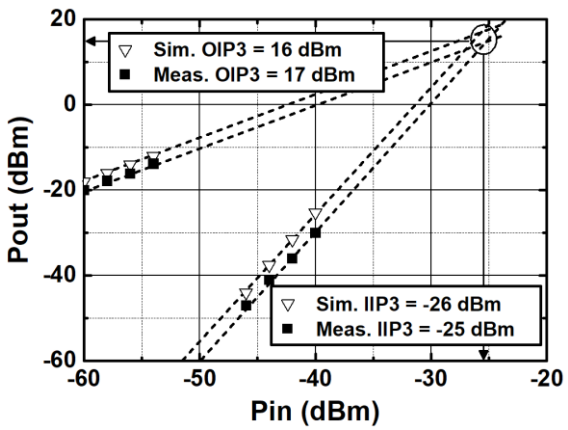

FIGURE 17. Measured and simulated IIP3.

indicates that the gain and phase errors of the implemented BLE receiver are less than 0.4 dB and 2°, respectively. Therefore, the proposed quadrature RF-to-BB-CR RF front-end can generate accurate quadrature signals that can satisfy the IRR specification for the BLE standard. The measured and simulated NFs at the IF frequency of 2 MHz are shown in Fig. 16. The measured NF is 13.2 dB at an RF frequency of 2.44 GHz. The measured and simulated IIP3 and

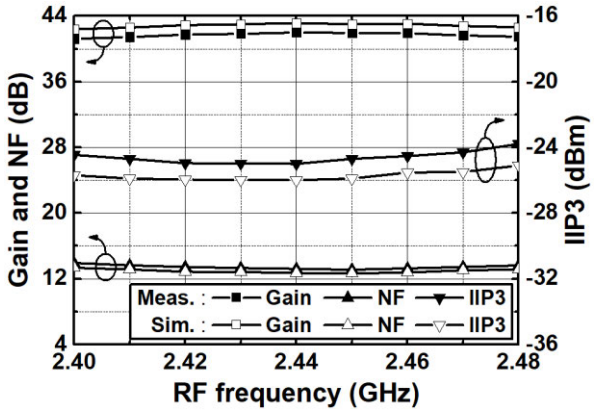

FIGURE 18. Measured and simulated gains, NFs, and IIP3s vs. RF freq.

output-referred third-order intercept points (OIP3) are illustrated in Fig. 17. The two-tone test conditions for IIP3 are $f_1 = f_{LO}+ 5$ MHz, and $f_2 = f_{LO}+ 8$ MHz. The measured IIP3 and OIP3 values are -25 and 17 dBm, respectively. The measured and simulated gains, NFs, and IIP3s across RF frequencies are shown in Fig. 18.

Table 2 presents a comparison of the measured performance values of the BLE receiver with the quadrature RF-to-BB-CR receiver architecture with those reported in previous studies. It can be seen that the implemented BLE receiver is the most power-efficient compared to the previous state-of-the-art RF-to-BB-CR receivers of [8]–[11] while satisfying all the requirements of the BLE standard. Research on the quadrature RF-to-BB-CR receiver architecture using noise-cancelling techniques [31]–[34] could be a future study to realize low-power and low-noise BLE receivers for IoT applications.

V. CONCLUSION

A low-power BLE receiver employing a new quadrature RF-to-BB-CR receiver architecture was implemented for IoT applications through a 65-nm CMOS process. In the proposed architecture, the dc bias current from a single supply voltage was shared among all the sub-blocks in the RF front-end. Furthermore, PCSNIPM and 1/f noise reduction were performed in the RF and BB domains, respectively, through the input impedance network. In addition, quadrature RF signals were generated through the embedded active-type PPF-based quadrature generator. The proposed quadrature RF-to-BB-CR receiver topology is a promising approach to provide quadrature signals to power-efficient single-quadrature low-IF receivers. The implemented BLE receiver achieved a maximum conversion gain of 42 dB, minimum NF of 13.2 dB, maximum IRR of 43 dB, and adjacent blocker rejection of 22 dB.

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