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DDR4 Data Channel Failure Due to DC Offset Caused by Intermittent Solder Ball Fracture in FBGA Package

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ABSTRACT This paper shows that an intermittent AC coupling defect occurring in a DDR4 data channel will cause more intermittent errors in DDR4, compared to such defect in DDR3. The intermittent AC coupling defect occurs due to intermittent fracture in DDR4 package solder ball. The defect causes DC offset in DDR4, which shifts the data signal or data eye and results in DDR4 data channel failure. The DC offset occurs due to the asymmetric nature of pseudo open drain termination scheme. DDR4 data channel response is compared with DDR3 channel. It is shown that pseudo random binary sequence (PRBS) pattern will always cause failure for DDR4, but PRBS will only cause failure in DDR3 if the sequence of consecutive 0's or 1's in PRBS pattern is long enough to cause threshold violation. As a result there will be more intermittent errors in DDR4 compared to DDR3. The defect due to fracture in solder ball is modelled by an AC coupling capacitor. A 1nF AC coupling capacitor corresponding to a solder ball fracture of height about 1nm is used to show the difference between DDR4 and DDR3 response.

INDEX TERMS AC coupling defect, AC coupling capacitor, DC offset, DDR4, DDR3, data channel failure, FBGA solder ball fracture, intermittent defect, pseudo open drain termination.

I. INTRODUCTION

DDR4 introduced a major change in architecture of DDR SDRAM memory by adopting pseudo open drain (POD) I/O standard for data lines [1]. POD has been further adopted for use in DDR5 [2]. In POD the receiver is terminated to V_{dd} voltage [3]. POD standard has weak pull up and strong pull down. This provides power benefits by reducing the power consumption during the logic 1. The logic 1 voltage is fixed to V_{dd}, which is 1.2 V for DDR4. Whereas, the logic 0 voltage depends on the choice of termination resistance and driver impedance. The reference voltage (V_{ref}) is used to determine whether the data signal is logic 1 or logic 0. DDR4 V_{ref} is not fixed and depends on termination resistance and channel characteristics. DDR3 stub series terminated logic (SSTL) I/O standard uses a center taped termination (CTT) scheme [4]. In CTT scheme the receiver is terminated to $V_{dd}/2$. V_{ref} is fixed at $V_{dd}/2$ and there is a symmetrical swing for logic 1 and logic 0 voltage around $V_{dd}/2$ voltage. DDR3 has strong pull up and strong pull down as well. These differences in characteristics of DDR4 POD I/O standard and DDR3 CTT architecture affect how data channel behaves in response to an intermittent AC coupling defect due to fracture in the solder ball of the fine pitch ball grid array (FBGA) package. Intermittent faults occur due to unstable or marginal behavior of hardware. Intermittent faults have following three characteristics- occur repeatedly at same location, have higher error rate and can be removed by replacing the hardware [5].

FBGA packages are used in modern devices for connecting devices to the circuit board. They have better parasitic characteristics and high form factor [6], [7]. FBGA solder balls develop fractures due to difference in thermal expansion coefficients of the FBGA package and printed circuit

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TABLE 1. Capacitance of the fractured solder ball.

	Fracture height (nm)					
	1	2	4	6	8	10
Cap (nF)	1.113	0.556	0.278	0.185	0.139	0.111

TABLE 2. DDR4 V_{ref} depends on termination resistance value.

Termination Resistance (R_t)	V_l	V_h	V_{ref}
40	0.60	1.20	0.90
60	0.48	1.20	0.84
80	0.40	1.20	0.80
120	0.30	1.20	0.75

board material [8]–[10]. The fracture is modelled by an AC coupling capacitor. The value of the AC coupling capacitor depends on the dimensions of the solder ball and the fracture. Table 1 shows capacitance values for fractures with various heights [11].

The fracture divides the solder ball into two pieces. The force of surrounding intact solder balls keep the two faces of fractured solder ball in contact with each other. The fractured solder ball faces get intermittently separated due to board warpage and vibration. The intermittency of the separation of solder ball faces depends on the operating conditions of the system [12].

The solder balls are located under the package and visual inspection of solder balls in working systems is not possible. The analysis of failure mechanism due to intermittent solder ball fractures is helpful in identifying the cause of intermittent errors. The failure mechanism depends on the architecture of the channel and the frequency characteristics of the data.

An AC coupling defect due to fractured solder ball blocks the lower frequencies in the signal and passes the higher frequencies. Data patterns with alternating bits have high frequency content, whereas data patterns consisting of consecutive logic 1's or 0's have low frequency content. There will be voltage variations due to AC coupling defect in the data channel. The voltage variations depend on the value of capacitor and the RC time constant for the data channel. AC coupling capacitor produces DC wander or baseline wander, which depends on the imbalance in the numbers of 1's and 0's in the pattern [13].

This paper analyzes intermittent solder ball fractures in DDR4 data channel from the perspective of data channel architecture and frequency characteristics of the signal. DDR4 data channel response is compared with DDR3 data channel when there is an intermittent solder ball fracture. It is shown that DDR4 will have more intermittent errors in comparison to DDR3, when PRBS data pattern is applied. This is due to asymmetric nature of DDR4 POD termination scheme. The PRBS data pattern will always produce intermittent errors for DDR4. The PRBS data pattern will only cause error in DDR3 if the PRBS signal contains enough consecutive 1's and 0's to cause threshold violation.

Section 2 details DDR4 POD architecture and provides a comparison with the DDR3 CTT architecture. Reference voltage is calculated for various termination resistances. The reference voltage depends on the termination resistance for DDR4, whereas the reference voltage remains fixed for DDR3. This affects how DDR4 and DDR3 data channel respond to solder ball fracture. Section 3 shows that a fracture in the FBGA solder ball changes the electrical model of the interconnection between the solder ball and the printed circuit board. HFSS simulation is done to calculate the S parameters of the fractured solder ball. S parameters show the AC coupling characteristics of the fractured solder ball. Section 4 details the simulation setup for DDR4 and DDR3 data channel when there is an AC coupling defect due to fractured solder ball. Section 5 shows DDR4 data channel response when a long sequence of consecutive 1's and 0's is applied in presence of an AC coupling defect. DDR4 channel response is compared with DDR3. This section shows the asymmetric response of DDR4 data channel to consecutive 1's and 0's data pattern. Section 6 shows DDR4 data channel response when a PRBS data pattern is applied in presence of an intermittent solder ball fracture. There is DC offset which results in DDR4 data channel failure. For DDR3 data channel, there is DC wander but no DC offset. DDR3 data channel will only fail if PRBS pattern contains enough consecutive 1's or 0's to cause voltage to drop below voltage high threshold or increase above voltage low threshold. Section 7 gives the conclusion of the paper.

II. DDR4 AND DDR3 DATA CHANNEL COMPARISON

DDR4 POD I/O standard has the termination resistance (R_t) tied to voltage V_{dd}, as shown in Fig. 1. When driver is driving logic 1, the driver impedance (Z_d) is connected to V_{dd}. There is no power consumption as both ends of the channel are tied to V_{dd} voltage. When logic 0 is being maintained on the data channel, Z_d is connected to ground. The power consumption for logic 0 depends on the choice of termination resistance and the driver impedance. Logic 1 voltage (V_h) and Logic 0 voltage (V_l) values are calculated for DDR4 in this section.

When logic 0 is being driven by the driver, V_l at the DDR4 receiver is found by applying voltage divider rule across R_t and Z_d. V_l is given by equation (1). There is current whose amplitude depends on the value of termination resistance and the driver impedance.

$$V_l = V_{dd} * [Z_d / (R_t + Z_d)] \tag{1}$$

V_h is equal to V_{dd} when logic 1 is being driven by the driver, as both ends of the channel are tied to V_{dd} voltage. There is no current when logic 1 is being maintained on the

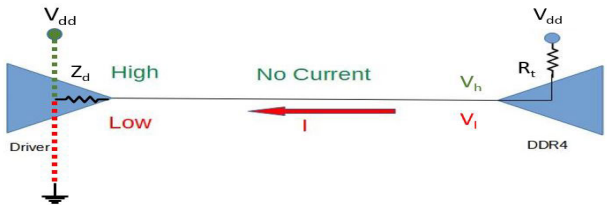

FIGURE 1. DDR4 POD I/O standard showing the data line terminated to V_{dd}. When driver is driving logic 1, Z_d is connected to V_{dd}. When driver is driving logic 0, Z_d is connected to ground.

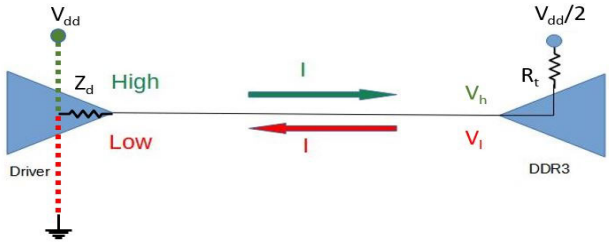

FIGURE 2. DDR3 Centre taped termination, the termination resistance (R_t) is tied to $V_{dd}/2$. When driver is driving logic 1, Z_d is connected to V_{dd}. When driver is driving logic 0, Z_d is connected to ground.

channel and V_h is given by equation (2).

$$V_h = V_{dd} \tag{2}$$

The reference voltage (V_{ref}) is chosen to be at equal distances from V_h and V_l. V_{ref} is equal to the average of V_h and V_l. V_{ref} is given by equation (3) and (4).

$$V_{ref} = (V_l + V_h)/2 \tag{3}$$

$$V_{ref} = [V_{dd} + V_{dd}\,(Z_d/\,(R_t + Z_d))]/2 \tag{4}$$

Table 2 shows V_l, V_h and V_{ref} values calculated using equations (1), (2) and (4) respectively. The driver impedance (Z_d) is 40 Ohm and V_{dd} is 1.2 V. As R_t increases V_l decreases. V_h is fixed at V_{dd} voltage, which is 1.2 V for DDR4. V_{ref} depends on R_t, as R_t increases V_{ref} becomes lower.

DDR4 POD standard is compared with the DDR3 CTT architecture to show the asymmetric nature of POD standard. In CTT architecture, R_t is terminated to $V_{dd}/2$ voltage. There is current flow for both V_h and V_l. Fig. 2 shows CTT architecture used for DDR3.V_l and V_h values are calculated in this section.

Z_d is connected to ground when logic 0 is being driven on DDR3 data channel. V_l is obtained by applying voltage divider rule across Z_d and R_t. V_l is given by equation (5).

$$V_l = V_{dd}/2 * [Z_d/\,(R_t + Z_d)] \tag{5}$$

Z_d is connected to V_{dd} when logic 1 is being driven on the DDR3 data channel. V_h is obtained by applying voltage divider rule across R_t and Z_d. V_h is given by equation (6).

$$V_h = V_{dd} * [R_t/(R_t + Z_d)] + V_{dd}/2 * [Z_d/(R_t + Z_d)] \tag{6}$$

TABLE 3. DDR3 has fixed V_{ref} for various termination resistances.

Termination Resistance (R_t)	V_l	V_h	V_{ref}
40	0.375	1.125	0.750
60	0.300	1.200	0.750
80	0.250	1.250	0.750
120	0.187	1.312	0.750

V_{ref} is chosen to be equidistant from V_l and V_h. V_{ref} is given by the average of V_l and V_h, as shown by equation (7).

$$V_{ref} = (V_l + V_h)/2 \tag{7}$$

Equation (8) is obtained by using equations (5), (6) and (7).

$$V_{ref} = V_{dd}/2 \tag{8}$$

Table 3 shows V_l, V_h and V_{ref} values calculated using equations (5), (6) and (8). The driver impedance (Z_d) is 40 Ohm and V_{dd} is 1.5 V. V_l decreases as R_t increases and V_h increases as R_t increases. V_{ref} remains fixed at $V_{dd}/2$, which is 0.75 V for 1.5 V DDR3.

DDR4 data channel has no current when logic 1 is being driven and has only current when logic 0 is being driven. V_l, V_{ref} depend on channel characteristics and V_h is fixed for DDR4. DDR3 data channel has current for both logic 1 and logic 0. V_h, V_l depend on channel characteristics and V_{ref} is fixed for DDR3.

III. INTERMITTENT FRACTURE IN FBGA SOLDER BALL

FBGA Packages are used in DDR4 memory for their high I/O pin density, low parasitic values and lower package dimensions. These packages have solder balls under the package. For proper operation of the memory device these solder balls must provide a reliable connection.

FBGA devices are connected to the PCB by soldering the solder balls. The soldering process causes voids in the solder balls [14]. During the operation of FBGA devices the thermal cycles cause fractures. The thermal co-efficient difference between the FBGA package device and the printed circuit board causes cracks in the solder ball and these cracks grow into fractures over time [10]. If the solder balls surrounding the fractured solder ball have intact connection, the force of surrounding solder balls will keep the fractured solder ball faces in contact with each other. The vibrations or warpage of PCB board during the operation causes intermittent opens in fractured solder ball [12]. The intermittency means that the effects due to such an intermittent open are hard to detect or analyze in working systems.

The fracture in a solder ball represents a discontinuity in the channel. The fracture can occur at FBGA device package

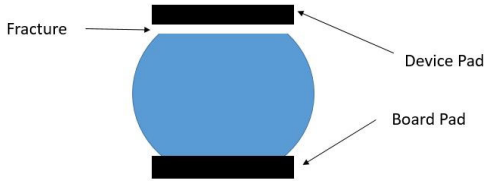

FIGURE 3. Fracture at the device pad and solder ball interface.

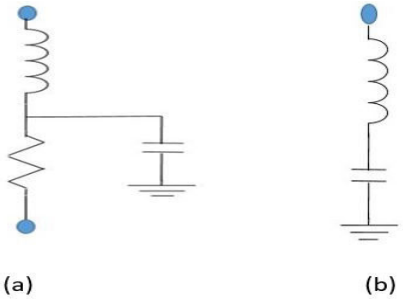

FIGURE 4. (a) Solder ball electrical model (b) fractured solder ball electrical model.

to solder ball interface, in the solder ball, solder ball to pad interface or build up layer on the board. A fracture occurring at the solder ball interface with the FBGA device package is shown in Fig. 3. The fracture changes the electrical model of the interconnection between the device and the printed circuit board.

Fig. 4(a) shows the equivalent electrical model of a solder ball. The electrical model consists of resistance due to the solder ball, the inductance due to the length of the solder ball and the parasitic capacitance between the solder ball and the ground. The resistance when the whole solder ball cross section is carrying current is DC resistance. At higher frequencies due to skin depth, the resistance increases as the available cross section for current flow decreases.

A fracture occurring in the solder ball changes the electrical model of the interconnection between the device and the printed circuit board [11]. The electrical model of such a fracture is shown in Fig. 4(b). There is an AC coupling capacitor due to fracture. The value of capacitance depends on the dimensions of the fracture.

HFSS field solver simulation is done to see the effects of a fracture in the solder ball. The HFSS design consists of a standard FPGA 16 layer board. The traces have 50 ohm characteristic impedance. The layers below and above the traces are ground planes. The fracture happens at the interface of FBGA device pad and the solder ball. The fracture causes an open to form between the FBGA device pad and the solder ball. Fig. 5 shows fracture occurring at the interface between the FBGA device pad and the solder ball and it also shows the HFSS simulation setup. Port 1 is the FBGA device side and port 2 is the board side.

The S parameters are measured for two cases. First case, where the solder ball has no fracture. The second case, where

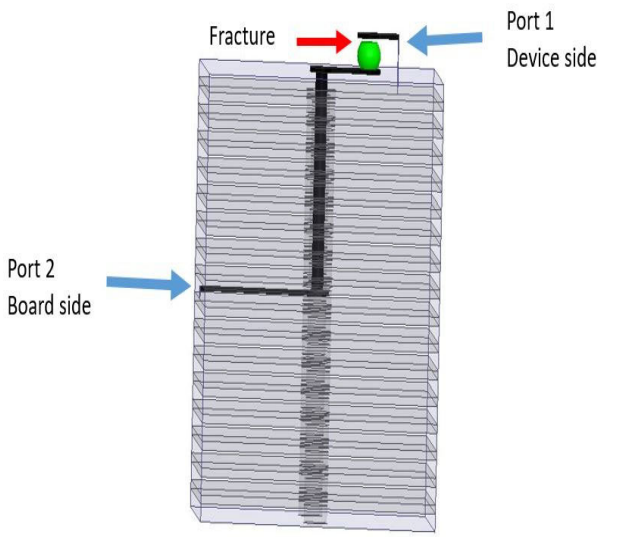

FIGURE 5. HFSS structure showing fractured solder ball.

the solder ball has a fracture at the device package and the solder ball interface.

Fig. 6 shows S_{11} parameter of the fractured solder ball case and the S_{11} parameter of intact solder ball (no fracture) case. The intact solder ball (no fracture) case S_{11} parameter shows very small reflection at lower frequencies and as the frequency increases the reflection increases. For the fractured solder ball case, the S_{11} parameter shows AC coupling characteristic. At lower frequencies all the signal is reflected and as the frequency increases the reflected signal decreases. At higher frequencies both the fractured solder ball and intact solder ball have similar S_{11} parameter characteristics.

Fig. 7 shows S_{21} parameter of the fractured solder ball case and the S_{21} parameter of the intact solder ball (no fracture case). The intact solder ball (no fracture) case S_{21} parameter shows that the transmitted signal has maximum value at lower frequencies and the signal value decreases as the frequency increases. Whereas, the fractured solder ball S_{21} parameter shows AC coupling characteristics. At lower frequencies there is no signal transmission and as the frequency increases the S_{21} parameter value increases. At high frequencies both the intact solder ball (no fracture) case and the fractured solder ball case have same S_{21} parameter characteristics.

IV. SIMULATION SETUP

The intermittent fracture occurs in the solder ball of the DDR4 FBGA package and it changes the behaviour of DDR4 data channel. The AC coupling effect due to fracture is modelled by an AC coupling capacitor. Simulation setup for simulating the effect of an AC coupling defect due to solder ball fracture in a DDR4 data channel is shown in Fig. 8. There is on die termination for DDR4 and the termination resistance is tied to V_{dd}. A 1nF AC coupling capacitor corresponding

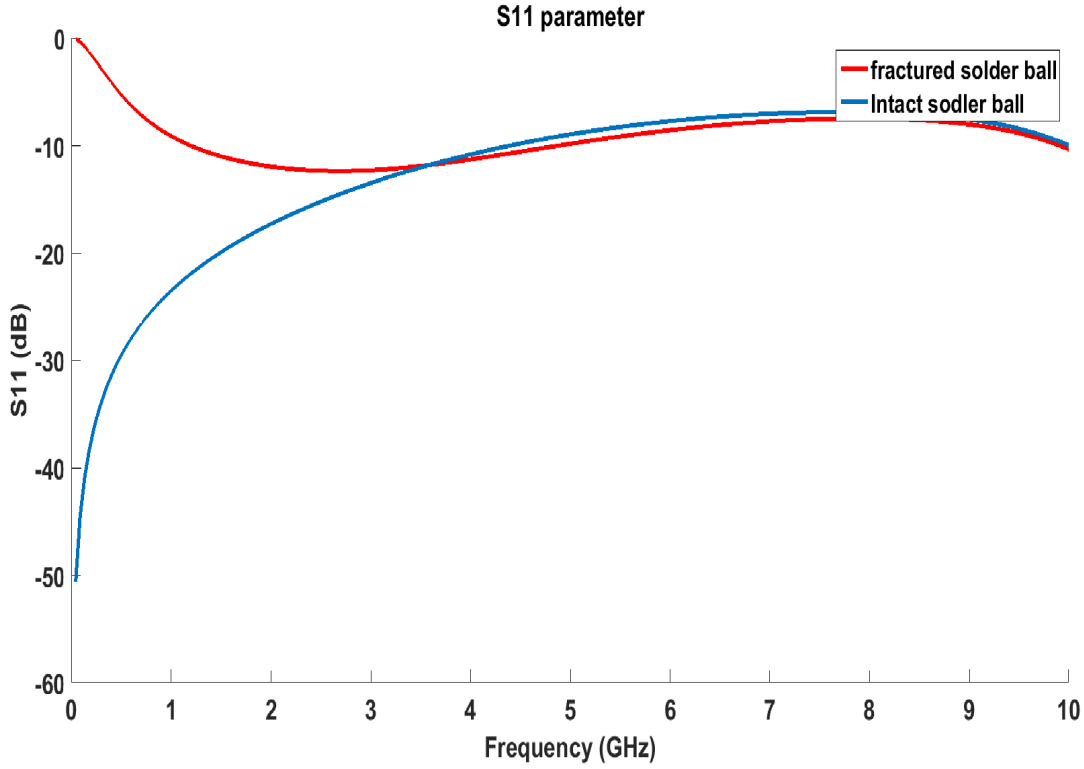

FIGURE 6. S_{11} parameter of fractured solder ball (red) compared with intact solder ball (no fracture) (blue).

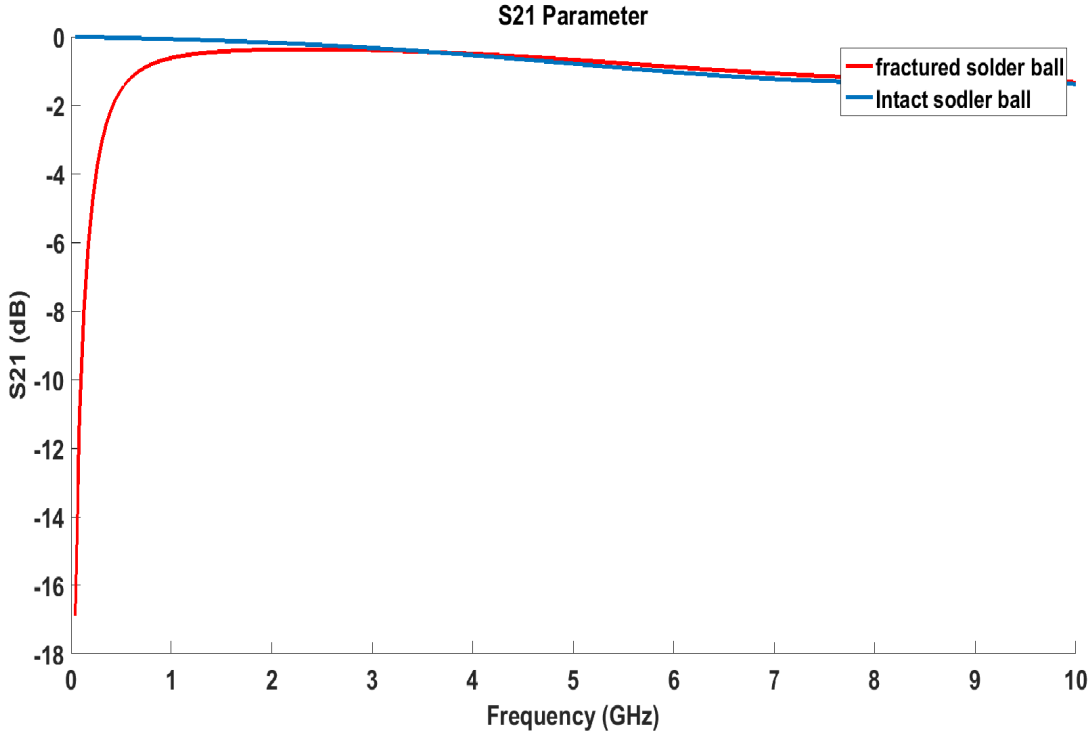

FIGURE 7. S_{21} parameter of fractured solder ball (red) compared with intact solder ball (no fracture) (blue).

to a fracture of height about 1nm is chosen for simulation. FPGA based memory controller is used for generating data patterns. The IBIS model of the driver I/O buffer is used for simulation [15]. DDR4 memory IBIS model with a

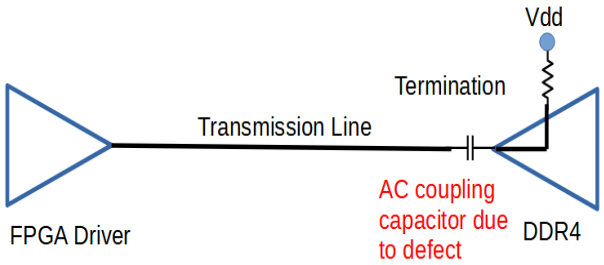

FIGURE 8. Simulation setup for an AC coupling defect in a DDR4 data channel, the AC coupling capacitor has a value of 1nF.

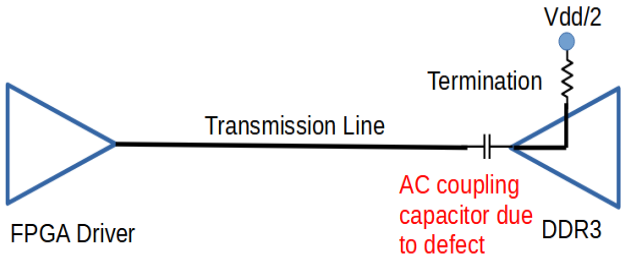

FIGURE 9. Simulation setup for an AC coupling defect in a DDR3 data channel, the AC coupling capacitor has a value of 1nF.

termination resistance of 40 Ohms is used [16]. The data rate for simulation is 2133 Mbps. The reference voltage (V_{ref}) is 0.84 V. $V_{l-threshold}$ and $V_{h-threshold}$ are 0.772 V and 0.908 V respectively for DDR4. Logic 0 voltage must remain below $V_{l-threshold}$ for no bit error and logic 1 voltage must remain above $V_{h-threshold}$ for no bit error.

DDR4 data channel is compared with DDR3 data channel to show the asymmetric response of DDR4 POD architecture to intermittent solder ball fracture. Simulation setup for an intermittent solder ball fracture in DDR3 data channel is shown in Fig. 9. There is on die termination for DDR3 and the termination resistor is tied to $V_{dd}/2$. The termination resistance for DDR3 is 40 Ohms. The data rate for simulations is 2133 Mbps. The reference voltage (V_{ref}) is 0.75 V. $V_{l-threshold}$ and $V_{h-threshold}$ are 0.615 V and 0.885 V respectively for DDR3.

V. DATA PATTERN CONSISTING OF LONG SEQUENCE OF 1'S AND 0'S

Long sequences of identical bits have lower frequency content. To see the effect of an AC coupling defect data patterns consisting of consecutive 0's and 1's are used.

Fig. 10(a) shows DDR4 data channel response when there is long sequence of 0's in presence of an AC coupling capacitor. The data pattern starts with a few alternating bits to show DDR4 logic 1 and logic 0 voltage levels. The voltage is measured at the DDR4 receiver. The data waveform shows that the voltage increases due to AC coupling defect, as it blocks the DC voltage. The voltage increases to V_{dd} because the termination resistance is tied to V_{dd}. The bit error occurs when voltage increases above $V_{l-threshold}$. The number of 0's required for bit error to happen depend on time constant. The RC time constant is given by equation 9. Where R_d is driver impedance, R_t is the termination resistance and C is the capacitance due to solder ball fracture.

$$T = (R_d + R_t) * C \tag{9}$$

Fig. 10(b) shows the measured voltage when there is long sequence of 1's in DDR4 data channel with AC coupling defect. The voltage remains at 1.2 V and there is no AC coupling effect. There is no bit error because $V_{h-threshold}$ is never violated. This is due to POD architecture, as during logic 1 state there is no current and both ends of the channel are tied to 1.2 V.

Fig. 11(a) shows DDR3 data channel response when the driver maintains a long sequence of 0's. The voltage increases to the reference voltage, which is $V_{dd}/2$. The bit error occurs when voltage increases above $V_{l-threshold}$.

Figure 11(b) shows the DDR3 channel response when there is long sequence of 1's in the presence of an AC coupling capacitor. The voltage drops to reference voltage due to DC blocking characteristics of the AC coupling defect. The bit error occurs when voltage decreases below $V_{h-threshold}$.

A long sequence of 0's in DDR4 data channel causes the voltage to rise to V_{dd} and in DDR3 the voltage rises to $V_{dd}/2$. There is bit error for both DDR4 and DDR3 if number of consecutive 0's are large enough to cause $V_{l-threshold}$ violation. This can be seen by comparison of Fig. 10(a) and Fig. 11(a). A long sequence of 1's in DDR4 data channel causes no bit error, but in DDR3 data channel there is $V_{h-threshold}$ violation. This can be seen by comparison of Fig. 10(b) and Fig. 11(b).

DDR3 data channel responds symmetrically to sequence of consecutive 0's and 1's in presence of an intermittent solder ball fracture. DDR4 data channel has an asymmetric response to sequence of consecutive 1's compared to sequence of 0's. This asymmetric response causes DC offset when PRBS signal is applied.

VI. PRBS DATA PATTERN

This section details effect of intermittent solder ball fracture on DDR4 when a PRBS signal is applied to the data channel. DDR4 data channel response is compared with DDR3 data channel response, to show how DDR4 has more intermittent errors.

Fig. 12(a) shows DDR4 data channel response to PRBS when there is no defect. The data channel behaves normally with V_l and V_h levels showing no voltage variations at envelops. Fig. 12(b) shows DDR4 data channel response in presence of a 1nF AC coupling capacitor. There is data waveform distortion due to charging and discharging behavior of AC coupling capacitor and it can be seen on the envelope of waveform. As for POD standard the data pattern consisting of consecutive 0's causes the voltage to increase towards V_{dd}, but for data pattern consisting of consecutive 1's there is no voltage change. This asymmetric behaviour of the pseudo

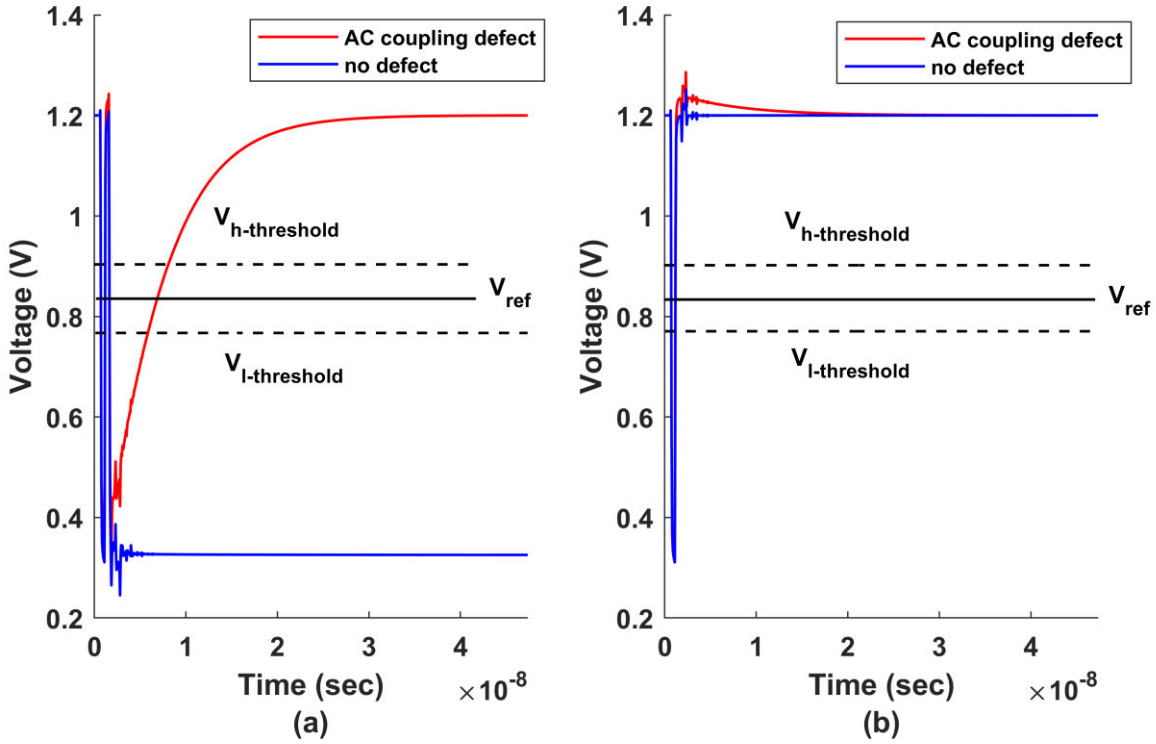

FIGURE 10. (a) Long sequence of 0's for a DDR4 data channel with a 1nF AC coupling capacitor due to solder ball fracture (b) Long sequence of 1's for DDR4 data channel in presence of a solder ball fracture.

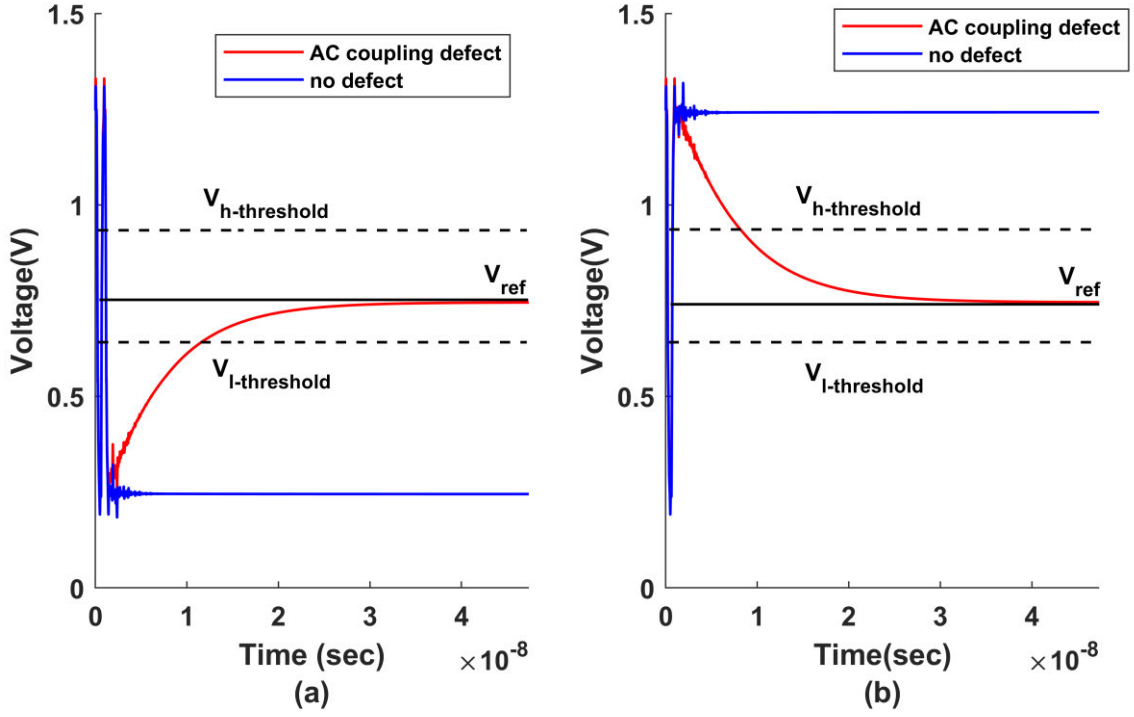

FIGURE 11. (a) Long sequence of 0's for a DDR3 data channel with a 1nF AC coupling capacitor due to solder ball fracture (b) Long sequence of 1's for a DDR3 data channel with an AC coupling defect.

open drain standard causes DC offset. The shifting of data waveform causes channel failure due to $V_{l-threshold}$ violation as shown in Fig. 12(b). Fig. 13 shows channel PRBS response without AC coupling capacitor (red) overlaid on channel

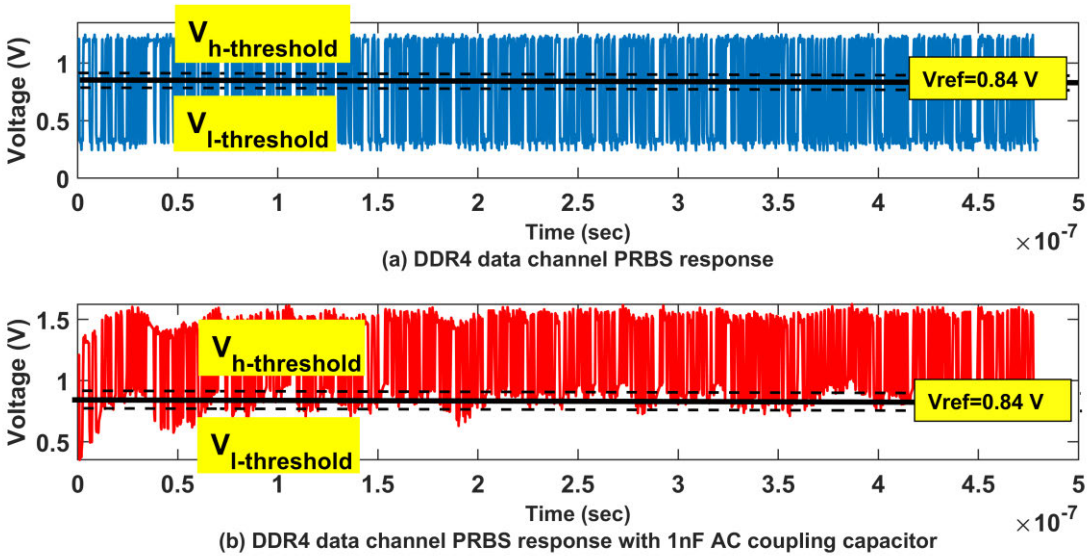

FIGURE 12. (a) PRBS response of DDR4 data channel, (b) PRBS response of DDR4 data channel in presence of a 1nF AC coupling capacitor.

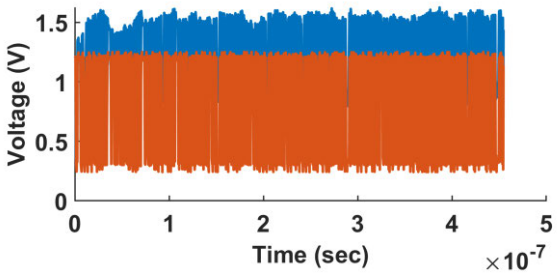

FIGURE 13. (Blue) PRBS data with a DC offset due to a 1 nF AC coupling capacitor, (red) PRBS data without AC coupling capacitor.

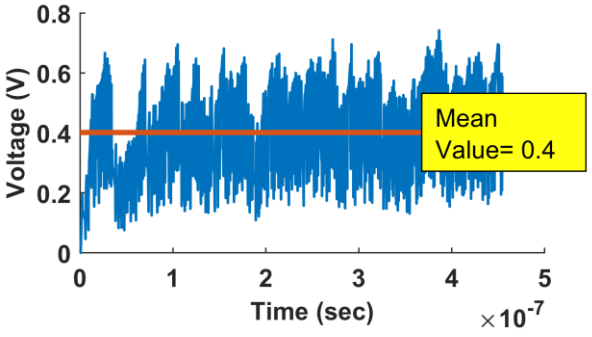

FIGURE 14. DC wander and DC offset due to a 1nF AC coupling capacitor in DDR4.

PRBS response with a 1nF AC coupling capacitor (blue). The overlaid waveforms show the DC offset and this will cause the channel to fail.

AC coupling capacitor removes lower frequencies. This removal of low frequency content will cause DC or baseline wander. The DC wander depends on the difference of 1's and 0's in the data pattern. The DC wander is shown in Fig. 14. The DC wander is measured by calculating the difference between the DDR4 data channel response to PRBS without an AC coupling capacitor and with a 1nF AC coupling capacitor. The mean value of the DC wander shows the DC offset in DDR4 data channel due to solder ball defect.

DDR3 data channel response to PRBS signal without an AC coupling capacitor and with a 1nF AC coupling capacitor is shown in Fig. 15(a) and Fig. 15(b) respectively. For bit patterns consisting of consecutive 0's the voltage increases towards reference voltage. For data patterns consisting of consecutive 1's the voltage on data channel drops towards reference voltage. There are voltage variations at the envelope of the waveform as shown in Fig. 15(b), but there is no shifting of data waveform. There is no bit error as neither $V_{h-threshold}$ nor $V_{l-threshold}$ is violated. There will be errors only if there are enough consecutive 0's or 1's in PRBS data pattern to cause threshold violations. The data on channel is still centered at reference voltage, which is $V_{dd}/2$ for center taped termination. Fig. 16 shows DDR3 data channel PRBS response without an AC coupling defect (red) overlaid on DDR3 PRBS response with a 1 nF AC coupling capacitor (blue). There is no DC offset.

The DC wander is shown in Fig. 17. The DC wander is calculated by finding the difference between the DDR3 data channel response without an AC coupling capacitor and with a 1nF AC coupling capacitor. The DC wander shows variations due to removal of low frequency content from the data waveform. The mean value of the DC wander is 0, which shows that there is no DC offset due to AC coupling capacitor for PRBS signal.

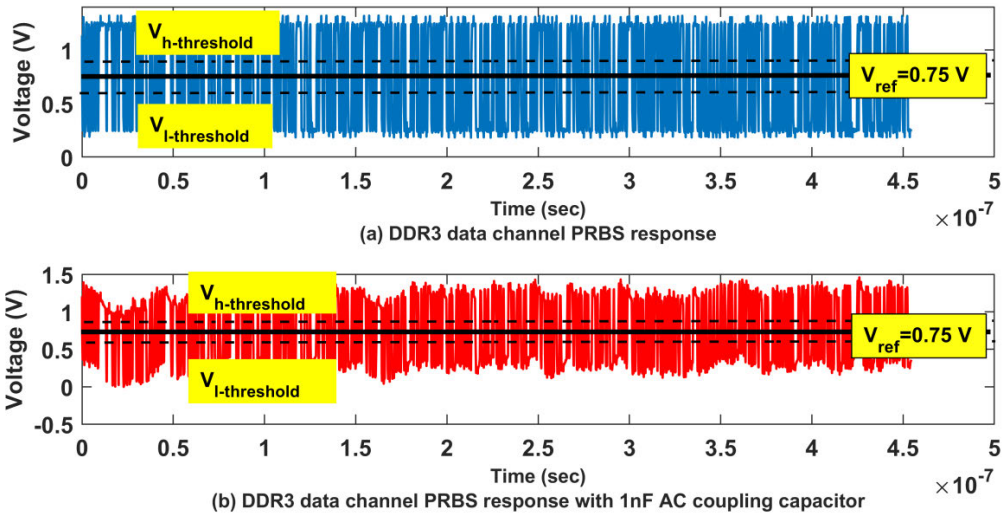

FIGURE 15. (a) PRBS response of DDR3 data channel, (b) PRBS response of DDR3 data channel in presence of a 1nF AC coupling capacitor.

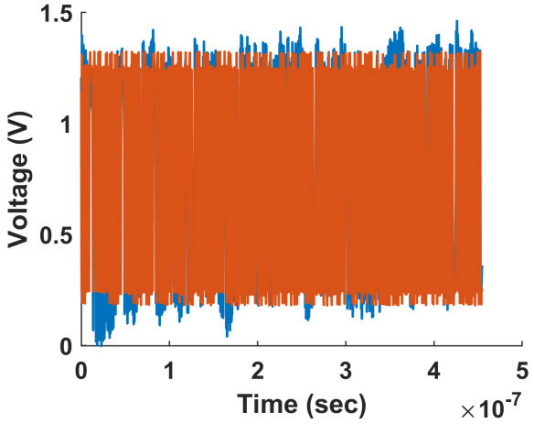

FIGURE 16. (Blue) PRBS data with a 1nF AC coupling capacitor in DDR3, (Red) PRBS data without AC coupling capacitor.

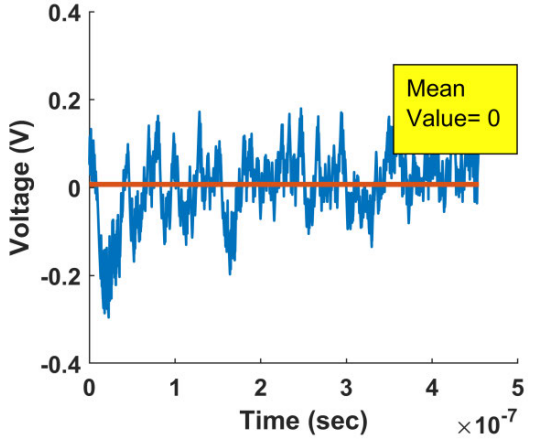

FIGURE 17. DC wander but no DC offset due to a 1 nF AC coupling capacitor in DDR3.

VII. CONCLUSION

An intermittent AC coupling defect can occur in a DDR4 data channel due to intermittent fracture in the solder ball of fine pitch ball grid array package. Such a defect is modelled by an AC coupling capacitor. The behaviour of data channel becomes dependent on the charging and discharging behaviour of the AC coupling capacitor. POD I/O standard is used in DDR4 data channel. In POD standard there is no current during logic 1 and logic 1 is tied to 1.2 V for DDR4. The reference voltage is not fixed and depends on choice of termination resistance and other channel characteristics. These characteristics of POD standard affect how the data channel behaves in presence of an AC coupling defect due to solder ball fracture.

DDR4 data channel for PRBS data pattern has a DC offset due to an intermittent AC coupling defect. This DC offset causes the data on the channel to shift and results in channel failure. Intermittent fractures in solder balls will always result in data channel failure for DDR4. This contrasts to DDR3, where an AC coupling defect for PRBS signal causes no DC offset. In DDR3, intermittent solder ball fractures will only cause failure if the sequence of consecutive 0's or 1's is long enough to cause threshold violations. There will be more intermittent errors in DDR4 due to intermittent solder ball fracture, compared to DDR3.

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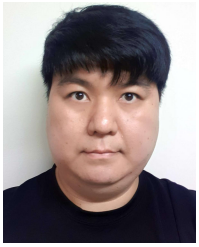

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