IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received March 1, 2021, accepted April 10, 2021, date of publication April 20, 2021, date of current version May 3, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3074464

Comparative Analysis of Ultra-Low Current Measurement Topologies With Implementation in 130 nm Technology

SARATH KUNDUMATTATHIL MOHANAN[1,2], HAMZA BOUKABACHE[1], (Member, IEEE), DANIEL PERRIN[1], AND ULLRICH R. PFEIFFER[2], (Fellow, IEEE)

[1]HSE-RP-IL, CERN, 1211 Geneva, Switzerland
[2]IHCT, University of Wuppertal, 42119 Wuppertal, Germany

Corresponding author: Sarath Kundumattathil Mohanan (sarath.mohanan@cern.ch)

ABSTRACT Radiation detectors need front-end electronics capable of measuring currents over a large dynamic range with femtoampere sensitivity. The goal of this work is to find an alternative to the legacy systems implemented using discrete components or technology nodes of 350 nm or higher. The 130 nm technology is evaluated on its leakage current performance to assess its employability in such applications. A comparative analysis of three low current measurement topologies, namely the charge balancing, reset counting, and direct slope measurement methods, is carried out and their performance in different current ranges is evaluated. The charge balancing method was found to provide a better dynamic range with greater accuracy. However, in the lower current range, the direct slope measurement method was found to give faster results than the other two methods with comparable accuracy. Also, an application-specific integrated circuit implementing the charge balancing method was found to be linear throughout the dynamic range of -1 fA to -1 μA and could measure currents with an accuracy of $\pm 7\%$. This achievement in the 130 nm technology opens the way to using the high-speed digital cells offered by this technology in conjunction with the low-leakage transistors to design a high-speed accurate current measurement system.

INDEX TERMS Femtoampere measurement, radiation detector, low current measurement.

I. INTRODUCTION

Femtoampere current measurements face numerous challenges owing to the very minuscule nature of the signal that needs to be sieved out from the vast sea of noise sources. In most current measurement applications, currents below picoamperes are considered to be leakage currents [1], [2]. However, for specific applications, such as biomedical signal processing [3] and environmental radiation monitoring [4], accurate measurements in the femtoampere range are often required. The bottleneck in such applications is elimination of the intrinsic leakage currents associated with the technology being used and the measurement environment. These leakage currents depend on many factors and are not easily compensated for by calibration. To attain the goal of femtoampere sensitivity, it is important to choose a technology for which the intrinsic leakages are in this range or lower. As the technologies scale down, shrinking the channel length and the gate oxide thickness will negatively affect the leakage currents [5], rendering the advanced nodes unusable for low current measurements. It is unfortunate that the numerous processing capabilities often required in making fast computations for real-time current monitoring systems appear elusive for these applications because of the high leakage current. A solution in this scenario is to use a two-chip system that has the leakage-critical analog part in a higher technology node and the high-speed digital section in a lower technology node or a modern field-programmable gate array (FPGA). To avoid the complexities associated with a two-chip solution and to bring the overall cost down, a technique of using the IO transistors for the entire analog section and core transistors for the digital section is proposed here.

A femtoampere-sensitive current digitizer was designed at European Organization for Nuclear Research (CERN), in AMS 350 nm technology [6]. The leakage current of this technology node is low enough to attain the required sensitivity. Much work has been done in the technology

The associate editor coordinating the review of this manuscript and approving it for publication was Cihun-Siyong Gong.

node of 350 nm or higher for ultra-low current measurements [2], [7]–[10]. An implementation in 180 nm technology [11] reports a current resolution of 314 fA, and another in 130 nm [12] attains a sensitivity of 135 fA. However, no work has been reported in 130 nm or lower that measures current with 1 fA sensitivity and with a dynamic range extending up to microamperes. Therefore, for low current measurement applications, as an alternative to the popular 350 nm node, TSMC 130 nm technology is evaluated in this study. The core transistors were found in simulations to have leakage currents on the order of picoamperes and are not the most suitable candidates for this application. The IO transistors operating with a supply voltage of 3.3 V have thick gate oxides and leakage currents in the femtoampere range. This work aims to characterize the leakage currents associated with the IO transistors of the TSMC 130 nm technology and to evaluate the employability of this technology in low current applications. In the course of designing current measurement circuits, three basic circuit topologies were evaluated to differentiate their capabilities. The limitations associated with each approach and the performance over different current ranges are extensively studied and demonstrated.

II. LOW CURRENT MEASUREMENT TOPOLOGIES

Current-to-frequency conversion (CFC) is the most commonly used technique to measure very low currents [13], [14]. A CFC circuit consists of an operational transconductance amplifier (OTA) with a feedback capacitor and a reset switch. The current to be measured charges the capacitor and thereby produces an output with a slope of integration proportional to the input current. Measurement of this slope enables one to calculate the input current. The slope measurement can be accomplished in multiple ways. Three basic approaches are explained in the following.

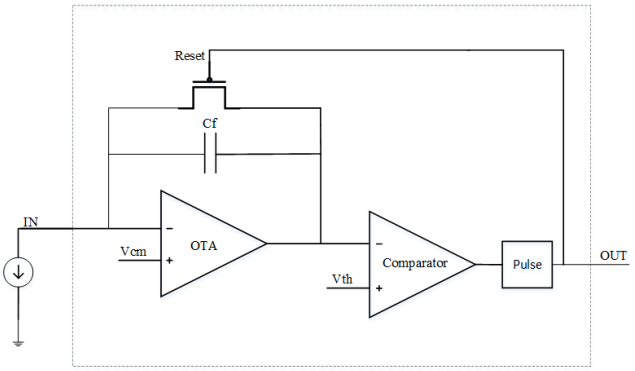

FIGURE 1. Reset counting method.

A. RESET COUNTING METHOD

The circuitry for this method [15] is shown in Fig. 1. A comparator produces an output each time the CFC output crosses a threshold. When the comparator output is high, a pulse generator produces a pulse of fixed length. This pulse

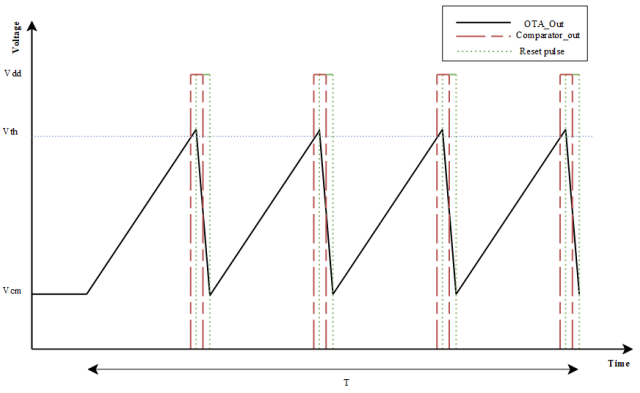

FIGURE 2. Current-to-frequency converter output.

then resets the feedback capacitor of the CFC. An external circuit counts the number of pulses.

The output of the circuit in Fig. 1 is shown in Fig. 2. The number of pulses in a fixed amount of time is proportional to the input current. The measured current I_{in} is given by

$$I_{in} = \frac{NC_f(V_{th} - V_{cm})}{T}, \tag{1}$$

where N is the number of resets in the measurement time T, C_f is the feedback capacitor, V_{cm} is the initial voltage at the output of the integrator and equals the common mode voltage of the OTA, and V_{th} is the threshold voltage of the comparator.

B. DIRECT SLOPE MEASUREMENT

In this method, the output of the CFC is fed to two comparators with different threshold voltages, as shown in Fig. 3. The measurement of the time difference between the two threshold crossings enables calculation of the slope of the CFC output, which is proportional to the input current.

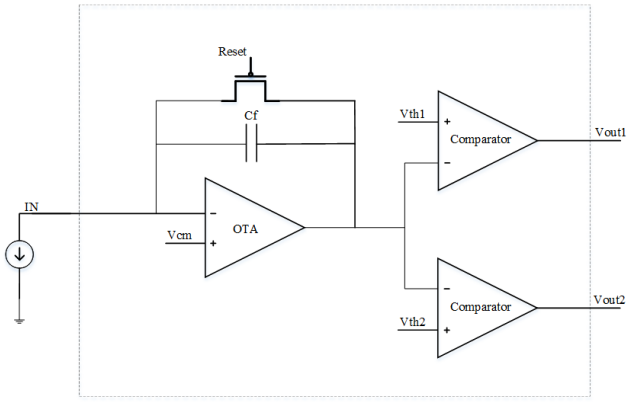

FIGURE 3. Direct slope measurement.

The input current can be calculated from

$$I_{in} = \frac{C_f(V_{th2} - V_{th1})}{t_2 - t_1}, \tag{2}$$

where V_{th2} and V_{th1} are the threshold voltages of the comparators, with $V_{th2} > V_{th1}$, and t_2 and t_1 are the respective times

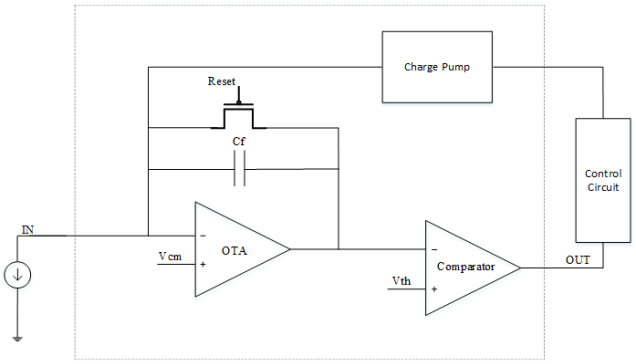

FIGURE 4. Charge balancing method.

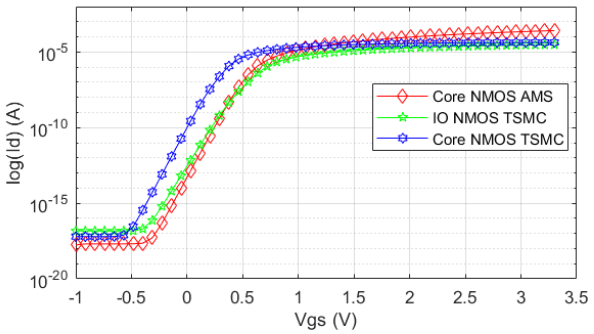

FIGURE 5. Transistor characteristics for TSMC 130 nm and AMS 350 nm NMOS transistors with $W/L = 1\ \mu$m/1 μm, Vds = 0.1 V.

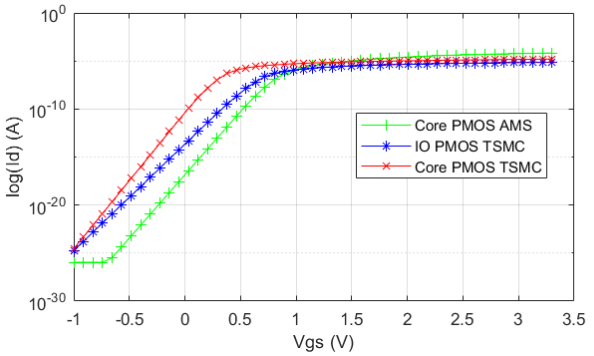

FIGURE 6. Transistor characteristics for TSMC 130 nm and AMS 350 nm PMOS transistors with $W/L = 1\ \mu$m/1 μm, Vds = 0.1 V.

of arrival of the falling edges of the comparator outputs V_{out2} and V_{out1} in the measurement system. The output V_{out2} may be used to generate the reset pulse for the feedback capacitor to start the next measurement cycle.

C. CHARGE BALANCING METHOD

In the charge balancing method [16], shown in Fig. 4, a reference charge is added to or subtracted from the feedback capacitor each time the CFC output crosses the threshold. The number of charge injections is proportional to the input current and can thus be calculated. The input current in this topology is calculated as

$$I_{in} = \frac{NQ_{ref}}{T}, \tag{3}$$

where Q_{ref} is the reference charge generated by the charge pump, N is the number of charge injections, and T is the measurement time interval.

Besides the three methods described above, other techniques, such as ADC sampling of the integrator slope or use of a transimpedance amplifier for current conversion, are available [1], [11], [12], [17], [18], but these methods are not considered in the present study. Other novel solutions for ultra-low current measurement employ technologies such as single-electron pumps or ultra-low noise current amplifiers [19].

III. TECHNOLOGY EVALUATION

The technology of interest, the TSMC 130 nm node, was evaluated in terms of the leakage currents. A comparison of the drain-to-source current variation with the gate-to-source voltage for the NMOS transistors of the AMS 350 nm and TSMC 130 nm technologies is shown in Fig. 5. The spectre simulations were carried out by varying the gate voltage and tying the source and bulk terminals to the ground. The drain terminal was held at a voltage of 0.1 V, which was found to be the maximum voltage that could appear across the drain and source terminals (Vds) of the switches in their off state in the circuit implementations considered here.

The off current observed for the AMS 350 nm NMOS core transistor was 40 fA, that of the TSMC 130 nm core transistor was 178 pA, and that of the corresponding IO transistor was 460 fA. The analogous characteristics for PMOS transistors are shown in Fig. 6.

The off currents associated with the PMOS transistors were simulated to be 22 aA for the AMS core transistor, 33 fA for the TSMC IO transistor, and 74 pA for the TSMC core transistor. The core transistors of the TSMC 130 nm node showed leakages on the order of picoamperes and hence could not be directly used in femtoampere measuring systems. As an alternative to AMS 350 nm transistors, the IO transistors of the TSMC 130 nm node looked promising in terms of offering comparable leakage performance. Another main candidate was the gate leakage current, which at lower technologies such as 130 nm could be significant for low current applications. However, the unavailability of accurate gate leakage models for simulation make estimation of this leakage current difficult, necessitating the use of test structures to quantify it. With the thick gate IO transistors rated for 3.3 V, their leakage current was expected to be comparable to that of the core AMS 350 nm transistors.

IV. SYSTEM DESIGN

To evaluate different topologies, four test chips were designed in TSMC 130 nm technology. Chip 1 is made of two channels, with the first channel having electrostatic discharge (ESD) diodes in its input path and the second one without any

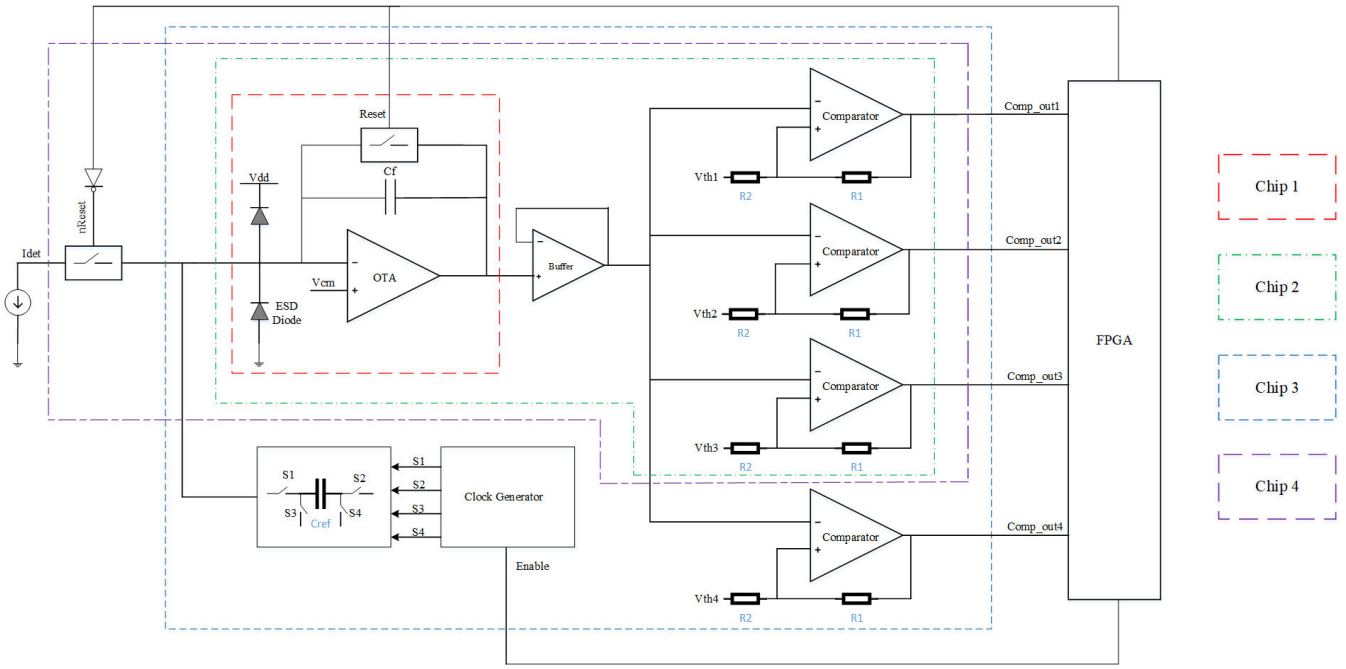

FIGURE 7. System architecture.

ESD structures. The two channels are identical and each consists of an integrating amplifier with a reset switch. The purpose of the chip is to determine whether the integrator can distinguish currents with femtoampere sensitivity by integrating them with various slopes.

Given that ESD diodes have been identified as the main sources of leakage in femtoampere measurements [20], the chip also aims to identify the leakage currents associated with the ESD diodes in this technology.

Chip 2 also has two channels, which, in addition to the integrator in Chip 1, have three comparators with different threshold voltages for performing current measurement with the direct slope or reset counting method. The second channel has floating input and its purpose is to identify all the leakages in the system.

Chip 3 incorporates the charge balancing method and has dedicated blocks for charge generation using switched capacitors and a clock generator to generate the clocks for the switched capacitor.

Chip 4 is similar to Chip 2 but has an additional switch in the input path. This switch is closed during the integrating phase and opens when the integrator is in reset. This helps to eliminate the charge loss during the reset period. Chip 4 aids in understanding the effects of inclusion of such a switch in the input path.

The system architecture, with details of the four chips, is displayed in Fig. 7. For Chips 1, 2, and 4 the depicted section shows the first channel. These chips also have an identical second channel for leakage current measurement. At the heart of all the topologies is an integrator. An operational amplifier or OTA may be used to realize the integrator. The folded cascode OTA topology of the UTOPIA 2 application-specific integrated circuit (ASIC) [21] designed in AMS 350 nm was adopted for the integrator realization. The input stage of the OTA was realized using PMOS transistors because of their intrinsic low-noise behavior and lower leakage compared with the NMOS transistors, as observed from the simulations.

A voltage follower isolates the OTA section from the comparators. To minimize the effect of noise on comparator switching, resistors R_1 and R_2 are used to provide hysteresis. The threshold points of switching are calculated as

$$\text{UTP} = V_{\text{th}} + (V_{\text{satp}} - V_{\text{th}})\frac{R_2}{R_1 + R_2}, \tag{4}$$

$$\text{LTP} = V_{\text{th}} + (V_{\text{satn}} - V_{\text{th}})\frac{R_2}{R_1 + R_2}, \tag{5}$$

where UTP is the upper threshold point, LTP is the lower threshold point, V_{satp} is the positive saturation voltage of the comparator, V_{satn} is the negative saturation voltage, V_{th} is the threshold voltage, and R_1 and R_2 are the feedback resistors. Values of 20 kΩ and 3 kΩ were used for R_1 and R_2, respectively. The threshold voltages for the comparators were generated externally using programmable precision digital-to-analog convertors (DACs).

For direct slope measurement, three sets of values can be calculated by measuring the time difference between the falling edges of the three comparators. The output from the third comparator is used to generate the reset signal. The charge balancing method has a charge generation block where a switched capacitor C_{ref} is charged to a reference

voltage V_{ref}, thereby generating a charge

$$Q_{\text{ref}} = C_{\text{ref}} V_{\text{ref}}. \tag{6}$$

The reference charge is then subtracted from the charge stored in the feedback capacitor. The reference charge generation and subsequent discharge are controlled by the switches S1–S4 of the switched capacitor. S3 and S4 are used to remove any residual charge in C_{ref}. S2 connects C_{ref} to V_{ref}, and later S1 connects C_{ref} to the input path. The generation of the control signals is carried out by the clock generator block according to the enable signal, which is a pulse generated based on the output of the fourth comparator. An FPGA is responsible for generating the reset and enable signals and receiving the comparator outputs to perform the current calculation.

V. EFFECT OF NONIDEALITIES ON CURRENT MEASUREMENT

Current calculation in all three methods using (1)–(3) assumes ideal components and conditions. However, there are many factors that can affect each term in the current calculation and lead to erroneous results.

A. RESET DURATION

In the reset counting method, the capacitor terminals are shorted through a reset switch each time the integrator output reaches a threshold voltage. The time t required to reset the integrator by discharging the capacitor C_{f} is proportional to the on resistance of the transistor switch, R_{on}:

$$t = R_{\text{on}}\, C_{\text{f}}\, \ln\left(\frac{V_{\text{init}}}{V_t}\right). \tag{7}$$

In (7), V_{init} is the initial voltage across the capacitor and V_t is the final voltage. A transistor with $W/L = 4\ \mu$m/350 nm was simulated to have an on resistance of 600 Ω. There are two transistors in series in the reset path, making an on resistance of 1.2 kΩ for the switch. The time to discharge a 1 pF capacitor completely through this resistance is around 6 ns. This reset time results in fewer resets in the measurement time T_{m} compared to the ideal case. The current calculation in (1) can be modified to include the reset time T_{rst}:

$$I_{\text{in}} = \frac{NC_{\text{f}}(V_{\text{th}} - V_{\text{cm}})}{T - NT_{\text{rst}}}. \tag{8}$$

The correction factor helps to minimize the error. A plot of the error in current measurement for an input current of 10 μA with and without correction for a range of reset times is shown in Fig. 8.

The measurement time T was chosen as 100 ms, C_{f} was set to 1 pF, and ΔV was taken to be 0.5 V. From the graph it is clear that the effect of the reset time can be compensated for with minimal impact on accuracy. The residual error is mainly due to the quantization effect arising from the fact that N is an integer. The correction works when the total measurement time $T \gg T_{\text{rst}}$. Thus, the effect of the reset time on measurement accuracy in the reset counting method can be minimized. The reset time does not have any effect on the threshold crossing method and the charge balancing method, since this time does not come into play in the regular measurement interval.

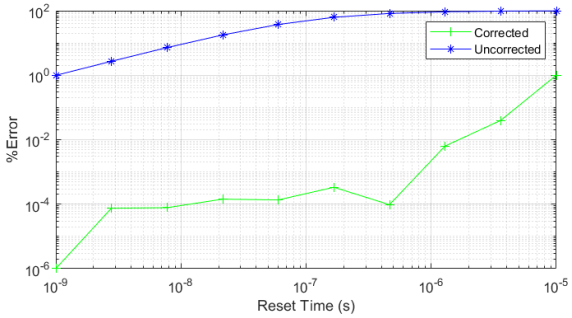

FIGURE 8. Percentage error in current measurement versus the reset duration for an input current of 10 μA with and without correction.

B. COMPARATOR DELAY

The rise and fall times of the comparator directly manifest as its propagation delay. This delay of the comparator also affects the current measurement in the reset counting method. The comparator delay in turn appears as a shift in the threshold voltage, and the integrator output overshoots the threshold. If this delay could be accurately determined, it could be compensated for in the same way as in (8), with T_{rst} replaced by T_{c}, the delay associated with the comparator. The delay should be limited so that the integrator output does not reach saturation. In the direct slope method, the matching between two comparator delays affects the accuracy. Since the threshold voltages of the comparators are different, the associated propagation delays also differ. The comparator delay thus acts as the main source of error in this method for currents of tens of nanoamperes and above. The comparator delay has almost no impact on measurement in the charge balancing method, since the quantum of charge being subtracted is determined by a separate charge generation circuit that is independent of the comparator parameters.

C. COMPARATOR THRESHOLD

The comparator threshold affects the charge that is built up in the feedback capacitor in each reset cycle. In the reset counting method, the comparator threshold is proportional to the gain of conversion, so the current calculation gets modified to

$$I_{\text{in}} = \frac{NC_{\text{f}}(V_{\text{th}} - V_{\text{cm}} + \Delta V_{\text{th}})}{T}, \tag{9}$$

where ΔV_{th} is the change in the threshold voltage. The direct slope method is heavily dependent on the matching between the threshold voltages of the comparators. By using more than two comparators, a better estimate of the slope can be obtained and the deviation in the threshold voltages can be averaged out. From (3), the comparator parameters do not affect the conversion gain in the charge balancing method,

and hence this method is immune to changes in the threshold voltages of the comparators.

D. OTA OFFSET

The finite input offset voltage of the OTA affects the calculation in the reset counting method in the same way as the comparator threshold voltage. This is because, instead of starting the integration from V_{cm}, it starts from $V_{cm} + V_{os}$:

$$I_{in} = \frac{NC_f(V_{th} - V_{cm} - V_{os})}{T}, \tag{10}$$

where V_{os} is the offset voltage of the OTA. The OTA offset does not have any effect on the direct slope method since it gets cancelled out in the calculation. The charge generation in the charge balancing method depends on the voltage to which the switched capacitor is connected. Thus (3) gets modified to

$$I_{in} = \frac{NC_{ref}(V_{ref} - V_{os})}{T}. \tag{11}$$

E. RESISTOR VALUES

The accuracy of the feedback resistors determines the threshold voltage, and a change in the resistor values by process variation affects the current calculation in the same way as a change in comparator threshold. For the direct slope method, the effective voltage difference in threshold voltages is

$$\Delta V = (V_{th2} - V_{th1})\frac{R_1}{R_1 + R_2}. \tag{12}$$

The accuracy of the resistors therefore affects the accuracy of measurement. By measuring the UTPs using (4) for the two different threshold voltages, the resistor values can be calibrated. In the charge balancing method, like the other comparator parameters, resistor values have minimal impact.

F. CAPACITOR VALUES

The values of the feedback and charge balancing capacitors can affect the measurement and need to be calibrated.

G. SWITCHED CAPACITOR NONIDEALITIES

Effects such as charge injection and clock feed-through can have an impact on the charge generation and discharge in the charge balancing method. Proper sizing of the switches of the switched capacitor and accurate timing of the clocks can reduce these effects [21].

VI. CURRENT MEASUREMENT LIMITS

A. LOWER LIMIT

The lowest measurable current is strictly a limitation imposed by numerous factors, the most prominent among them being the leakage current in the system itself. It is a cumulative contribution linked to the technology, the circuit topology, and the measurement setup. The accuracy of the current generating source and the means by which it is transported to the measurement circuitry also limits the magnitude of the minimum current that can be accurately measured.

Different sources of leakage for a current measurement ASIC have been studied and characterized for the AMS 350 nm technology in [22]. The sources of leakages from the circuit point of view are the drain-to-source leakage of the reset switch, the gate leakage current of the input transistors, and the leakage current of the ESD diodes. The charge balancing method has additional switches for charge injection, which contribute extra leakage currents. Chip 4 with the input series switch also has also an additional leakage current.

Consider a system with a leakage current I_{leak}. Let ΔV be the difference between the initial voltage of the integrator output and the threshold voltage, and let C_f be the feedback capacitor. To distinguish a signal of magnitude I_{min}, the minimum measurable current, the minimum time resolution Δt that must be measured with precision is

$$\Delta t = \frac{C_f \cdot \Delta V \cdot I_{min}}{I_{leak}(I_{leak} + I_{min})}, \tag{13}$$

or

$$\Delta t \cong \frac{C_f \cdot \Delta V \cdot I_{min}}{I_{leak}^2}. \tag{14}$$

The challenge is accurately measuring this time difference. For a system with a leakage of 1 pA, assuming C_f to be 1 pF and ΔV to be 0.1 V, the Δt required to measure 1 aA is 100 ns, which is theoretically possible. However, the leakage current does not remain constant and is heavily dependent on temperature, voltage, and process variations. This variation makes it even more challenging to calibrate out the leakage current. Even though, theoretically, measurement down to attoamperes is possible with all the measurement topologies, 1 fA is a reasonably observed limit in standard laboratory conditions.

B. UPPER LIMIT

There are many circuit elements limiting the maximum current that can be measured by the different topologies. The nonidealities described in Section V are the major factors that limit the maximum current measurable with the required accuracy. Calibration helps to minimize the nonidealities to a certain extent, beyond which the error in measurement increases. Apart from the aforementioned factors, the main limiting factor in the measurement is the OTA.

The OTA remains stable until an input measured current is comparable to the bias current that flows through the output stage of the OTA. In the present design, this bias current is around 140 μA. For input currents above the bias current, the operating point of the OTA shifts, which results in the output shifting from the common mode voltage. The OTA loses its linearity in this region of operation.

The sizing of the transistors forming the reset switch is another factor that can result in a shift of the OTA output from the initial value. For higher currents, the drain terminal of the transistor that is connected to the OTA output moves to increase the drain-to-source voltage. This in turn shifts the output voltage. When a minimum-sized transistor is used

as the reset switch, as the input current is increased from 1 μA to 10 μA, the initial output voltage of the OTA shifts by 300 mV, which reduces the effective voltage headroom for slope measurement before the OTA output saturates. This issue can be minimized by increasing the width of the transistor switch, thereby increasing the drain current for smaller drain-to-source voltage. The transistor sizing is thus a tradeoff between the leakage current and the maximum current to be measured. A T-switch having three transistors with $W/L = 4\,\mu$m/350 nm can attain the required leakage below femtoampere level and support the maximum current until the limitation of 140 μA of the OTA is reached.

Each topology has dedicated additional circuitry that further imposes limits on the maximum measurable current.

1) RESET COUNTING METHOD

Considering the effects of all the nonidealities, the current calculation can be modified to

$$I_{\text{in}} = \frac{N\alpha\, C_{\text{f}}(V_{\text{th}} - V_{\text{cm}} - V_{\text{os}} - \Delta V_{\text{th}})}{T - NT_{\text{rst}} - \beta NT_{\text{c}} - T_{\text{d}}}, \tag{15}$$

where α is the correction factor from the calibration of the capacitor value, T_{c} is the comparator delay, T_{d} is the delay due to the digital logic in the FPGA that generates the reset signal, ΔV_{th} is the mismatch in the comparator threshold, and β is the proportionality factor for the delay associated with the comparator and takes into account its dependency on the input current; hence this factor was formulated as a ratio with the reset count N which is the best estimate of the input current.

Most of the nonidealities identified in (15) are constants and can be corrected by calibration. The main limiting factors are the comparator delay and finding a constant value for β for a wide range of input currents. This limits the maximum current that can be accurately measured with this method. Consider a 3.3 V system with a 1 pF feedback capacitor. Assuming a total delay of 50 ns for the comparator and digital section, for an input current of 15 μA and above the OTA output approaches saturation and loses linearity.

Increasing the feedback capacitor makes the system slower and reduces the impact of the comparator delay on the measurement for higher currents. Thus there is a tradeoff between the frequency of operation of the CFC and the desired upper current limit.

2) DIRECT SLOPE METHOD

The limitation in this method arises from the precise measurement of the time between two comparator outputs. For a system in the above example with an input current of 5 μA and a threshold voltage difference of 0.1 V, the time to measure is 20 ns. Given the nonconstant delay associated with the comparator, measurement in this range is greatly error prone.

3) CHARGE BALANCING METHOD

The maximum measurable current in this method is determined by the charging and discharging time of the capacitor that generates the reference charge:

$$I_{\text{max}} = \frac{V_{\text{ref}}}{5(R_{\text{on1}} + R_{\text{on2}})}, \tag{16}$$

where R_{on1} and R_{on2} are the on resistances corresponding to the transistor switches that connect the capacitor to the reference voltage and the OTA input, respectively. For a reference voltage of 1 V and simulated on resistances, I_{max} is calculated as 2.6 μA.

VII. MEASUREMENT SETUP

The test chips were directly wire-bonded onto an FR4 printed circuit board as shown in Fig. 9. Packaging was avoided to eliminate unwarranted leakage from the package. The test board generates the power supplies and houses the DACs to generate precise bias and threshold voltages for the chip. An FPGA board receives the comparator outputs of the chip, generates the control signals, and programs the DACs.

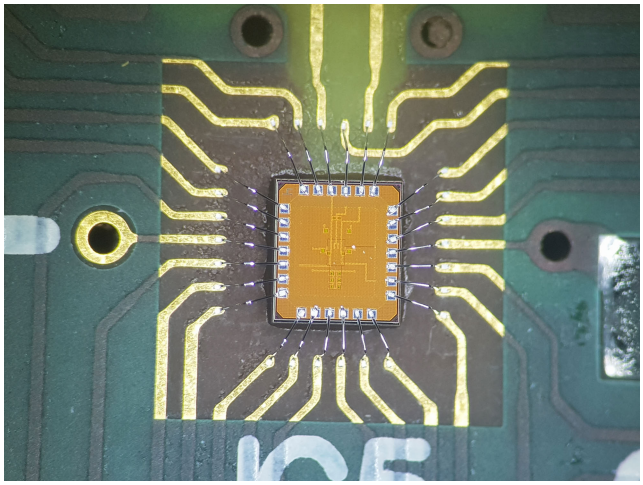

FIGURE 9. Bonded chip.

The current was injected from a Keithley 6430 current source. The outputs captured from the chip on an oscilloscope were transferred to a computer through Ethernet. The current calculations were carried out in the FPGA. The whole data capture was controlled from a MATLAB environment interfaced to the FPGA board through an universal asynchronous receiver-transmitter. The experiment was carried out under standard laboratory conditions, and the chip was shielded in a metallic enclosure for protection against perturbations for Electromagnetic Compatibility.

VIII. MEASUREMENT RESULTS

The current generated by the ionization chambers, which is the target application, is typically negative. The slope of the integrator output is positive for negative current and vice versa.

The output of the OTA obtained from the first channel of Chip 1 is shown in Fig. 10. The measurement was carried out in a controlled environment at 25°C. The slope of the

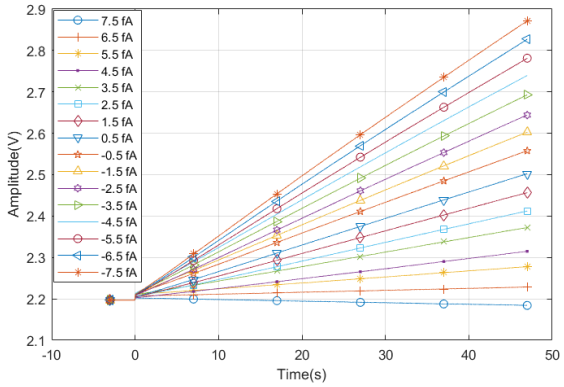

FIGURE 10. OTA output of Chip 1 with input current swept from 7.5 fA to −7.5 fA.

output is close to zero for an input current of 7.5 fA. This represents the cumulative leakage currents at the input. Apart from the leakages associated with the printed circuit board and the cable, the leakage of the ESD diodes, the gate leakage of the input transistors of the OTA, and the leakage current of the transistor in the reset switch are all included in this input bias current. From Fig. 10 it can be seen that the chip distinguishes current with 1 fA sensitivity. A common mode voltage of 2.2 V was chosen for the OTA and so it integrates from this value.

The second channel, without the ESD diodes, produced a similar response but the bias current was found to be 2 fA. A total of five chips were evaluated for leakage currents and the results are summarized in Table 1.

TABLE 1. Measured input leakage currents.

Chip number	Channel 1	Channel 2
Chip1 (Only OTA)	7 fA	2 fA
Chip2 (OTA and comparators)	7 fA	7 fA
Chip3 (Charge balancing)	10 fA	N/A
Chip4 (With input switch)	10 fA	10 fA
Chip5 (OTA and comparators)	7 fA	7 fA

All the chips with ESD diodes in the input reported leakage currents of 7 fA. The second channel in Chip 1 had no ESD diodes and hence reported a leakage current of only 2 fA. The additional input switch of Chip 4 added 3 fA to the leakage. Similarly, the three switches for charge injection in Chip 3 contributed an additional 3 fA, making a total leakage current of 10 fA.

A. MEASUREMENT RESULTS IN THE FEMTOAMPERE RANGE

All three methods produced linear results when injected with an input current ranging from −1 fA to −25 fA. The results from the reset counting method are displayed in Fig. 11. The current values shown are absolute values without taking the polarity into consideration.

The input leakage current was measured and compensated for while plotting the graph for better visualization. Since all

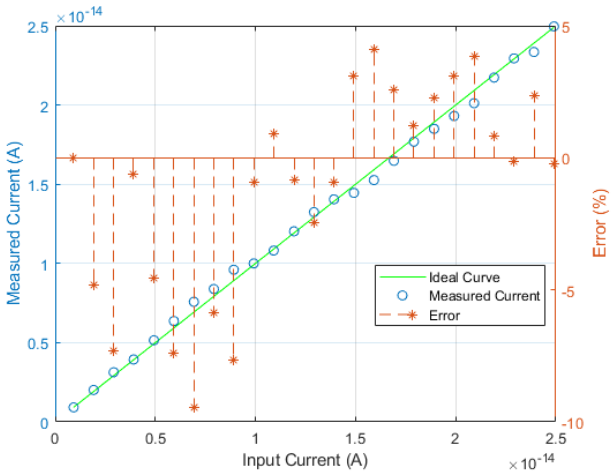

FIGURE 11. The measured current and corresponding percentage error with input current swept from −1 fA to −25 fA with the reset counting method.

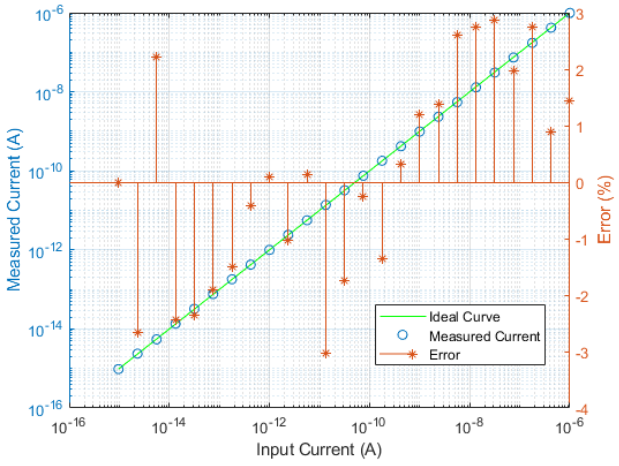

FIGURE 12. The measured current and corresponding percentage error with input current swept from −1 fA to −1 μA with the charge balancing method.

the methods exhibited similar behavior, only the result of the reset counting method, which had the highest maximum error (−9.4%), is shown here. The maximum error reported by the charge balancing method in the −1 fA to −25 fA band was −7.2 %. Of the three methods, direct slope measurement was found to have the smallest errors, with the maximum error reported as −7%.

B. MEASUREMENT RESULTS IN THE FEMTOAMPERE TO MICROAMPERE RANGE

As the input current was increased, the charge balancing method was found to perform better than the other two methods. Fig. 12 shows the linearity and error plot for currents of up to −1 μA for the charge balancing method. The output of the chip was found to be linear over the entire measurement range, and the percentage error in the considered dataset remained within ±3%. The leakage current was compensated

for in post-processing for this plot as well. With the other two methods, for an input current above −10 nA, the comparator delay resulting in the threshold shift and the subsequent overshoot of the integrator output before it was reset led to errors above 10%.

IX. DISCUSSION

A detailed comparison of different low current measurement topologies has revealed the vulnerabilities and advantages associated with each of them. It was found that the three methods performed equally well in the femtoampere measurement range. The charge balancing method was found to have the highest dynamic range and better immunity to nonidealities. The main limiting factor in the reset counting and direct slope measurement methods consisted of the delays associated with the comparator and other circuits, which were variable with respect to the input current, making the proper compensation of such delays in post-processing infeasible. For the reset counting method, the delay resulted in an overshoot of the integrator output, affecting the conversion gain. By using additional circuitry to measure the exact voltage at which the integrator output resets, the conversion gain can be corrected. An ADC that measures the output of the integrator at the start and end of the reset will give an exact value for the quantum of charge that is made to reset in each cycle. In the case of direct slope measurement, increasing the feedback capacitor value is the easiest way of increasing the dynamic range. It represents a tradeoff against the measurement time and hence should be meticulously calculated. Increasing the feedback capacitor value is beneficial for all the methods in facilitating a higher amount of charge collection and thus increasing the overall dynamic range.

X. CONCLUSION

The limits of different low current measurement topologies arising primarily from various nonidealities have been studied and measured. The technique of using the IO transistors with thick gate oxides, as demonstrated in [23], has been used to establish the employability of a 130 nm technology for applications targeting femtoampere current measurement. The measurement capability, which spans nine decades, opens doors to numerous application scenarios for this technology node. The high-speed core transistors can be used to realize the digital section currently implemented in FPGA to make a single-chip solution for a high-speed accurate ultra-low current measurement system.

REFERENCES

[1] R. T. Heitz, D. B. Barkin, T. D. O'Sullivan, N. Parashurama, S. S. Gambhir, and B. A. Wooley, "A low noise current readout architecture for fluorescence detection in living subjects," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 308–309, doi: 10.1109/ISSCC.2011.5746331.

[2] M. H. Nazari, H. Mazhab-Jafari, L. Leng, A. Guenther, and R. Genov, "CMOS neurotransmitter microarray: 96-channel integrated potentiostat with on-die microsensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 338–348, Jun. 2013, doi: 10.1109/TBCAS.2012.2203597.

[3] A. Gore, S. Chakrabartty, S. Pal, and E. Alocilja, "A multi-channel femtoampere-sensitivity conductometric array for biosensing applications," in *Proc. IEEE Eng. Med. Biol. Soc. Int. Conf.*, Aug. 2006, pp. 6489–6492, doi: 10.1109/IEMBS.2006.260865.

[4] H. Boukabache, M. Pangallo, G. Ducos, N. Cardines, A. Bellotta, C. Toner, D. Perrin, and D. Forkel-Wirth, "Towards a novel modular architecture for CERN radiation monitoring," *Radiat. Protection Dosimetry*, vol. 173, nos. 1–3, pp. 240–244, Apr. 2017, doi: 10.1093/rpd/ncw308.

[5] P. M. Zeitzoff and H. R. Huff, "MOSFET scaling trends, challenges, and key associated metrology issues through the end of the roadmap," *AIP Conf. Proc.*, vol. 788, pp. 203–213, Sep. 2005, doi: 10.1063/1.2062964.

[6] E. Voulgari, M. Noy, F. Anghinolfi, F. Krummenacher, and M. Kayal, "Design and measurement methodology for a sub-picoampere current digitiser," in *Proc. 22nd Int. Conf. Mixed Design Integr. Circuits Syst. (MIXDES)*, Jun. 2015, pp. 525–529, doi: 10.1109/MIXDES.2015.7208578.

[7] M. Zhang, N. Llaser, and H. Mathias, "A low noise CMOS preamplifier for femtoampere current detection," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 2094–2097, doi: 10.1109/ISCAS.2008.4541862.

[8] M. Carminati, G. Ferrari, F. Guagliardo, M. Farina, and M. Sampietro, "Low-noise single-chip potentiostat for nano-bio-electrochemistry over a 1MHz bandwidth," in *Proc. 16th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2009, pp. 952–955, doi: 10.1109/ICECS.2009.5410819.

[9] M. Carminati, G. Ferrari, D. Bianchi, and M. Sampietro, "Femtoampere integrated current preamplifier for low noise and wide bandwidth electrochemistry with nanoelectrodes," *Electrochim. Acta*, vol. 112, pp. 950–956, Dec. 2013, doi: 10.1016/j.electacta.2013.03.093.

[10] G. Ferrari, M. Farina, F. Guagliardo, M. Carminati, and M. Sampietro, "Ultra-low-noise CMOS current preamplifier from DC to 1 MHz," *Electron. Lett.*, vol. 45, no. 25, pp. 1278–1280, Dec. 2009, doi: 10.1049/el.2009.2353.

[11] K. J. Pol, H. Hegt, A. van Roermund, and S. Ouzounov, "A femto-ampere sensitive direct-interface current-input sigma delta ADC for amperometric bio-sensor signal acquisition," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 2015, pp. 1–3, doi: 10.1109/BioCAS.2015.7348403.

[12] H. M. Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1149–1157, May 2013, doi: 10.1109/TCSI.2013.2248771.

[13] D. J. Taylor, "A current-to-frequency converter for astronomical photometry," *Rev. Sci. Instrum.*, vol. 40, no. 4, pp. 559–562, Apr. 1969, doi: 10.1063/1.1684005.

[14] E. G. Shapiro, "Linear seven-decade current/voltage-to-frequency converter," *IEEE Trans. Nucl. Sci.*, vol. IT-17, no. 1, pp. 335–344, Feb. 1970.

[15] G. C. Bonazzola, R. Cirio, M. Donetti, F. Marchetto, G. Mazza, C. Peroni, and A. Zampieri, "Performances of a VLSI wide dynamic range current-to-frequency converter for strip ionization chambers," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 405, no. 1, pp. 111–120, 1998, doi: 10.1016/S0168-9002(97)01209-6.

[16] B. Gottschalk, "Charge-balancing current integrator with large dynamic range," *Nucl. Instrum. Methods Phys. Res.*, vol. 207, no. 3, pp. 417–421, Apr. 1983, doi: 10.1016/0167-5087(83)90652-x.

[17] H. Li, C. S. Boling, and A. J. Mason, "CMOS amperometric ADC with high sensitivity, dynamic range and power efficiency for air quality monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 4, pp. 817–827, Aug. 2016, doi: 10.1109/TBCAS.2016.2571306.

[18] S. S. Ghoreishizadeh, I. Taurino, G. De Micheli, S. Carrara, and P. Georgiou, "A differential electrochemical readout ASIC with heterogeneous integration of bio-nano sensors for amperometric sensing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 5, pp. 1148–1159, Oct. 2017, doi: 10.1109/TBCAS.2017.2733624.

[19] R. Fitzgerald, D. E. Bergeron, S. P. Giblin, D. G. Jarrett, S. M. Judge, C. Michotte, H. Scherer, and N. M. Zimmerman, "The next generation of current measurement for ionization chambers," *Appl. Radiat. Isot.*, vol. 163, Sep. 2020, Art. no. 109216, doi: 10.1016/j.apradiso.2020.109216.

[20] E. Voulgari, M. Noy, F. Anghinolfi, D. Perrin, F. Krummenacher, and M. Kayal, "Design considerations for an 8-decade current-to-digital converter with fA sensitivity," *Int. J. Microelectron. Comp. Sci.*, vol. 6, no. 3, pp. 79–85, 2015.

[21] E. Voulgari, "A nine decade femtoampere current to frequency converter," Ph.D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2017.

[22] E. Voulgari, M. Noy, F. Anghinolfi, F. Krummenacher, and M. Kayal, "Sub-picoampere, 7-decade current to frequency converter for current sensing," in *Proc. IEEE 13th Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2015, pp. 1–4, doi: 10.1109/NEWCAS.2015.7182071.
[23] S. K. Mohanan, H. Boukabache, D. Perrin, and U. Pfeiffer, "Femtoampere sensitive current measurement ASIC in 22 nm technology," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2019, pp. 1–3, doi: 10.1109/S3S46989.2019.9320710.

SARATH KUNDUMATTATHIL MOHANAN received the bachelor's degree in applied electronics and instrumentation engineering from the College of Engineering, Trivandrum, India, in 2009, and the master's degree in microsystems engineering from the University of Freiburg, Germany, in 2015. He is currently pursuing the Ph.D. degree with CERN, with a focus on the design of an ASIC for next-generation radiation monitoring.

He has worked with General Electric Healthcare, Cypress Semiconductors, the Defense Research and Development Organization of India, the Fraunhofer Institute for Applied Solid State Physics, and the Technical University of Darmstadt. He is also affiliated with the University of Wuppertal, Germany.

HAMZA BOUKABACHE (Member, IEEE) received the master's degree in electronic and automatic control from the French Institute of Applied Science at Toulouse, and in microtechnology from the University of Toulouse, France, in 2009, and the Ph.D. degree in micro- and nanosystems from the National Institute of Applied Sciences, Toulouse, France, in 2013.

He is currently a Project Leader with the Radiation Protection Group, CERN, leading a team in charge of the development and manufacturing of a new-generation ionizing radiation monitoring system. His research interests include system-on-chip development, ultra-low current measurement techniques, and hardening methods for safety critical systems.

Dr. Boukabache has received many awards for his research work in heterogeneous aerospace structural health monitoring within the French National Center for Scientific Research (CNRS). He was a recipient of the Engineering Sciences Prize from the Toulouse Academy of Science, in 2014, the GEET Prize, in 2013, for the best Ph.D. research work among five Universities and nominated the same year for the 6th top innovations in French aerospace cluster.

DANIEL PERRIN was born in France, in 1963. He received the Diploma degree in electronics from the University Institute of Technology, St-Etienne, in 1983.

After his Diploma, he worked with CERN, as an Electronics Technical Engineer, in developing the control units of the electrostatic separators for the large electron-positron (LEP) collider. In 1992, he joined the CERN Radiation Protection Group, for which he designed and developed instrumentation for ionizing radiation measurement. Since 2001, he has been the Head of the CERN Radiation Protection Group, Instrumentation and Logistics Section. He has led projects on the design and supply of the radiation monitoring system for the large hadron collider (LHC) and the injector chain. Since 2013, he has also been managing the Radiation Monitoring System for the Environment and Safety (RAMSES) Program at CERN.

ULLRICH R. PFEIFFER (Fellow, IEEE) received the Diploma and Ph.D. degrees in physics from the University of Heidelberg, Germany, in 1996 and 1999, respectively.

In 1997, he was a Research Fellow with the Rutherford Appleton Laboratory, Oxfordshire, U.K. From 1999 to 2001, he worked as a Postdoctoral Researcher with the University of Heidelberg on real-time electronics for particle physics experiments at the European Organization for Nuclear Research (CERN), Meyrin, Switzerland. From 2001 to 2006, his research with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, involved RF circuit design, power amplifier design at 60 and 77 GHz, and high-frequency modeling, and packaging for millimeter-wave communication systems. In 2007, he led the Terahertz Electronics Group at the Institute of High-Frequency and Quantum Electronics, University of Siegen, Germany. Since 2008, he has been holding the High-Frequency and Communication Technology Chair at the University of Wuppertal, Germany. His research interests include silicon RFICs for millimeter-wave/terahertz communication, radar, and imaging systems.

Dr. Pfeiffer has been the President of the German Association for Electrical Engineering and Information Technology e.V. (FTEI). He was a co-recipient of the 2004 and 2006 Lewis Winner Award for Outstanding Paper from the IEEE International Solid-State Circuit Conference, the 2006 IBM Pat Goldberg Memorial Best Paper Award, the 2008 EuMIC Best Paper Award, the 2010 EuMC Microwave Prize, the 2014 EuCAP Best Paper Award, the 2017 Microwave Prize, and the 2012 and 2018 Jan Van Vessem Award for Outstanding European Paper from the IEEE International Solid-State Circuit Conference. In 2007, he received the European Young Investigator Award. He has been a Distinguished Lecturer of the IEEE Solid-State Circuits Society.