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A New Hybrid Dual Active Bridge Modular Multilevel Based DC–DC Converter for HVDC Networks

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ABSTRACT Multi-terminal high voltage DC transmission currently represents a leading technology in long-distance power transmission systems. Among the main technical challenges facing such technology, DC fault isolation, permitting different grounding schemes, providing interoperability, and high DC voltage stepping between different HVDC networks, and allowing high-speed power reversal without power interruption especially when connecting the pre-existing voltage source converters (VSC) and line commutated converters (LCC)-based HVDC networks. This paper introduces a new modular multilevel converter (MMC) based front-to-front DC-DC converter to interconnect two different types (LCC/VSC) of HVDC networks. The proposed topology comprises a voltage source MMC (VS-MMC) and a current source MMC (CS-MMC), while both are coupled via an AC link including the isolating transformer. The proposed topology can successfully provide an uninterruptible bi-directional power flow, high DC voltage stepping with a DC fault blocking capability, and low number of semiconductors due to the usage of only half-bridge SMs. The system design is provided with a detailed mathematical analysis. Furthermore, two active power control methodologies are proposed and compared. The first control technique is simpler and entails lower passive elements, while the second technique ensures a zero reactive power over the full range of active power flow. Furthermore, Losses analysis and comparison are provided between the two proposed control techniques. Finally, Control-Hardware-in-the-Loop (CHiL) test validation is employed to confirm the validity of the proposed system under healthy as well as different fault scenarios.

INDEX TERMS Modular multilevel converter, dc-dc power converters, HVDC, power control, bidirectional power flow, control-hardware-in-the-loop (CHiL).

I. INTRODUCTION

RECENT literature has witnessed an extensive investigation to voltage source converters (VSCs) based high voltage direct current (HVDC) transmission networks as a promising technology in long-distance power transmission systems [1]–[3]. This has been geared up especially with the parallel advent of modular multilevel converter (MMC) topology in recent industrial applications [4], [5]. Nevertheless, most of current HVDC transmission networks are still based on line commutated converters (LCC) using thyristor valves [6], which operate as current source converters (CSC). In this context, both technologies offer some advantages, while experience other technical drawbacks. For example, LCC-based HVDC systems needs large amounts of reactive power to deliver active power in addition to the commutation failure problems. However, VSC-based systems provide independent control of active and reactive power in addition to easier power reversal capability. On the other hand, VSC-based HVDC systems are less efficient than LCC-HVDC based counterparts and have much higher cost.

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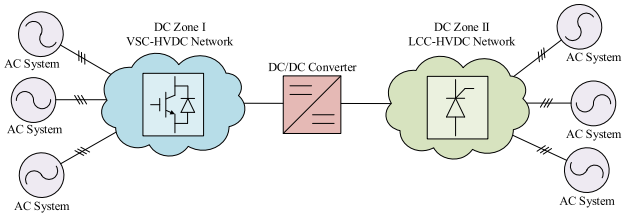

FIGURE 1. Block diagram of generalized DC-DC converter-based hybrid HVDC networks.

In literature, Hybrid HVDC transmission using LCC converter and VSC converter is presented [7], [8], where both LCC-based and VSC-based HVDC networks are directly connected to each other, combining the advantages of both ones. However, for an uninterruptible power reversal capability, MMC with full-bridge submodules (SMs) should be used in the VSC-based side, which increase the cost dramatically. Therefore, most of the existed VSC-based converters are MMC with half-bridge SMs. Moreover, different power reversal strategies are proposed in literature regarding the hybrid LCC/MMC HVDC systems [9]. However, they include the utilization of mechanical switches and slow sequence of power flow reversal in case half-bridge SMs-based MMC.

Establishing a large-scale multi-terminal hybrid HVDC network in the future is technically facing many main obstacles that hinder its progress in practical grounds, where the required solutions can be summarized as follows:

- Providing interoperability (the ability of interconnecting different pre-existing HVDC networks built by different manufacturers and have different control schemes).
- Providing the ability of multiterminal connections instead of just point to point connection.
- Achieving protection zone isolation between the HVDC networks to prevent blackout spreading. (DC circuit breaker functionality).
- Permitting the connection of different grounding HVDC schemes.
- Allowing high-speed power reversal without power flow interruption for hybrid HVDC networks.
- Providing the capability of high DC voltage stepping for different voltage HVDC-networks connection.

DC-DC converters have recently emerged as a key solution to these challenges [10]–[12] especially that they can be used in connecting HVDC hybrid networks instead of only a point-to-point connection as depicted in Fig. 1.

In general, DC-DC converters can be classified into two categories. The first category is the isolated DC-DC converters, which rely on DC/AC/DC conversion stages. The isolation is included by using an AC transformer [10], [11], [13]–[16]. The conventional type is the two-level DAB converter [17], which relies on series connection of IGBTs to withstand the operation at high DC voltage.

Moreover, it was used for interconnection between LCC and VSC HVDC network as it was introduced in [6], where the H-bridge at LCC HVDC side consists of IGCTs instead of the IGBTs. However, it leads to significant stresses at the transformer side with the increase of the DC voltage level in addition to the need for complex snubber circuits to achieve dynamic voltage sharing due to series connection of the switches. Moreover, there is the MMC-DAB technology, which is capable of handling high power and high DC voltage [10], [18]–[20]. It mainly involves two different stages each one converts the DC voltage into AC voltage via DC-AC MMC. However, there is a trade-off between the size reduction of the transformer and conduction losses of switches, which is mainly depending on the operating frequency. They can be operated in two modes namely: sinusoidal mode or quasi-two level (Q2L) mode [15]. Low power density due to lower RMS voltage is a major drawback in sinusoidal mode. On the other hand, Q2L mode offers smaller loading time of the MMC cells as discussed in [21], [22]. Hence, cell requirements are reduced drastically. Furthermore, Multi-module DC-DC converters were introduced in [14], [15] which offer bidirectional power flow. However, each bridge suffers from significant amount of recovery current at high frequency and the main drawback is the usage of multiple transformers when employed in high voltage application. Moreover, some recent works have been carried out to propose the concept of flyback or forward converters using MMC sub-modules instead of series connected IGBTs to withstand the high voltage, bidirectional power flow and avoid voltage sharing mechanisms as in [23]. Additionally, different cell structures can be used as in [24] but it is only used in unidirectional power flow as in offshore windfarms. However, high voltage insulation and rating is a must for the coupled inductor in the isolating transformer due to high voltages and currents.

The second category is the non-isolated DC-DC converters [10], [11]. For example, resonant based DC-DC converters are found in literature which offer soft switching capability. They are divided into two subcategories: single and multiple stages of resonant tanks [25]–[27]. For single stage resonance, as proposed in [27], it uses parallel LC tank and LCL network as in [26]. Mainly, their downsides are low efficiency due to the existence of circulating reactive power and stresses applied on central resonant tank, which restricts this type of converters to medium power range. Moreover, the subfamily, which uses a number of low power resonance tanks [28], [29], uses parallel capacitors in low voltage side and series connection on high voltage side. Moreover, the subfamily, which includes transformer-less DC modular topologies, is categorized into two subgroups namely: transformer-less DC MMC and DC modular based on choppers. Moreover, a two stage modular multilevel DC-DC converter was proposed in [30], which consists of a half-bridge MMC followed by an H-bridge MMC, where the first stage produces an AC square wave while the second stage rectifies the AC square wave into the required DC output voltage, but it has DC link capacitors which limits the converter to medium power applications. Also, a transformer-less DC MMC based converter has been introduced in [31]. It uses branches and

arms of submodules (SMs) to provide power transfer between primary and secondary sides. An AC component is circulating between SMs due to power imbalance between primary and secondary SMs. The major drawback is the requirement to reduce the AC component; thus, bulky passive filters introduced in [32]. Two versions were presented in [33] known as tuned filter and push-pull modular multilevel converter. Another solution introduced in [34] to exchange bulky filters with extra submodules but an increase in conduction losses is inevitable.

In addition, a transformer-less hybrid modular multilevel DC-DC converter has been proposed [35], where another version was proposed in [36] with DC fault blocking capability but they cannot be used for connecting LCC-HVDC and VSC-HVDC networks. On the other hand, the DC modular choppers, which utilize lower number of SMs as introduced in [37], employ capacitive or inductive energy storing elements but these converters exhibit AC circulating current due to the hard switching of SMs, which increase conduction losses [38]. Another autotransformer based DC-DC converter has been proposed in [39], which leads to partial conversion of total DC interchange between both DC sides [39], [40]. However, it employs full-bridge (FB) cells to block DC fault, which reduces the overall efficiency, and the asymmetric ratio leads to increasing DC voltage stresses.

In this paper, a new modular multilevel based DC-DC converter is proposed to interconnect different types of HVDC system networks (LCC and VSC). The main concept of adopting VSC based DC-DC converters is their fully controlled capabilities. On the other hand, the rapid development of insulated gate commutated thyristors (IGCT) technology has promoted IGCTs as promising switching devices in either VSC-HVDC or LCC-HVDC networks [41]. The proposed converter can provide a bidirectional power flow without operation stoppage as well as a DC fault blocking capability. Two control methods of active power flow are also proposed. The proposed system is investigated under healthy as well as different fault scenarios. The main contributions of this paper are summarized as follows:

- Proposing a new modular multilevel DC-DC converter to interconnect LCC-based and VSC-based HVDC transmission systems.
- Two new control methodologies are proposed along with the required system design corresponding to each controller.

This paper is organized as follows. Section II introduces the proposed topology description and principle of operation. Section III addresses the detailed system analysis of voltage source modular multilevel converter (VS-MMC) and current source modular multilevel converter (CS-MMC) in addition to sub-module parameter design. Section IV introduces an equivalent circuit of the proposed DC-DC converter with different control methodologies with the required modifications. Section V discusses and compares between the losses of the proposed control techniques. Section VI shows the experimental results of the Control-Hardware-in-the-Loop (CHiL) for the proposed converter under different healthy and fault scenarios.

II. PROPOSED DC-DC CONVERTER TOPOLOGY STRUCTURE

The proposed DC-DC converter topology, as shown in Fig. 2, comprises two MMCs, namely CS-MMC connected to LCC-HVDC system and VS-MMC connected to VSC-HVDC system. Both MMCs are coupled through an isolating transformer and an LC filter.

A. VOLTAGE SOURCE SIDE MMC

The VS-MMC is constructed by 2 legs, each leg has two arms containing series connection of half-bridge voltage source sub-modules (VS-SM) to withstand the applied high DC voltage, as shown in Fig. 2.

Each VS-SM consists of a capacitor and 2 IGBT switches along with anti-parallel diodes to provide a bidirectional current flow. The VS-MMC provides the desired output AC voltage waveform as will be discussed later. Balancing algorithm is applied on the SMs to limit the voltage ripples among the capacitors in the same arm, where the capacitors' voltages are measured and sorted in both orders. The capacitors with the highest voltages are inserted to be discharged when $I_{arm_{2i}} < 0$. On the other hand, the capacitors with the least voltages are inserted when $I_{arm_{2i}} > 0$, as shown in Fig. 3.

B. CURRENT SOURCE SIDE MMC

The CS-MMC is constructed by 2 legs, each leg consists of two arms containing parallel connection of half bridge current source sub-modules (CS-SM) to withstand the applied high DC current, as shown in Fig. 2. Each sub-module consists of an inductor as a storage element with 2 IGCT switches. As previously mentioned in VS-MMC, same principle of operation is applied, however the CS-MMC generates the required output AC current waveform instead of the voltage waveform. Therefore, by applying the duality, the inductors currents exhibit current ripple, and a balancing current algorithm is therefore required. Currents of the inductors are measured and sorted in both orders similar to VS-MMC case. Also, the arm voltage is measured to detect whether the inductors are charging or discharging, upon which the insertion of the CS-SMs is determined, as explained by the flowchart given in Fig. 4.

III. POWER CONVERTER CIRCUIT ANALYSIS

In this section, a detailed analysis is provided for a proper system design and control.

A. VS-MMC ANALYSIS

To analyze the behavior of the VS-MMC, all VS-SMs per arm are replaced by an equivalent variable capacitor as shown in Fig. 5, whose capacitance depends on the number of connected VS-SMs as in (1).

$$C_{2i} = \frac{C_{SM}}{n_{2i}} \tag{1}$$

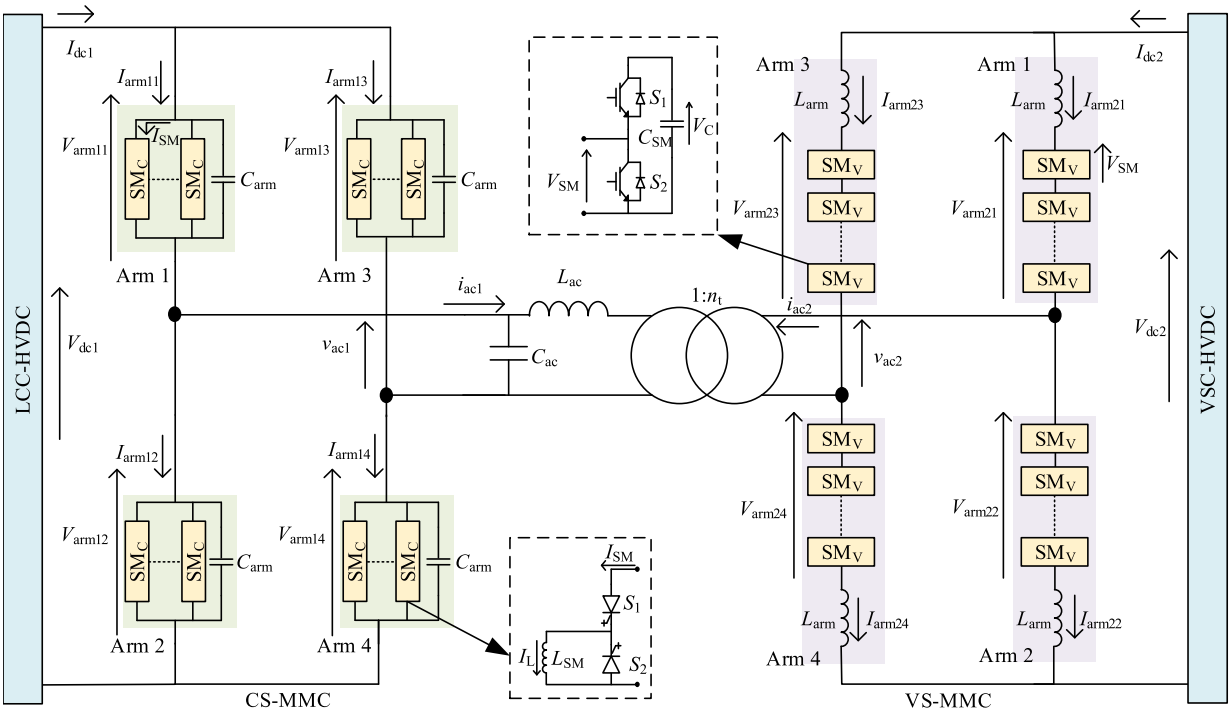

FIGURE 2. Detailed diagram of DC-DC converter.

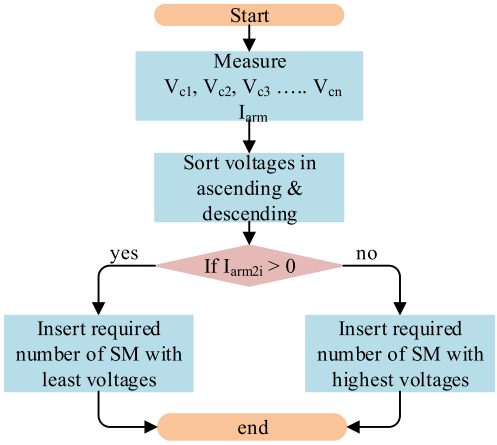

FIGURE 3. Voltage balancing algorithm in the VS-MMC.

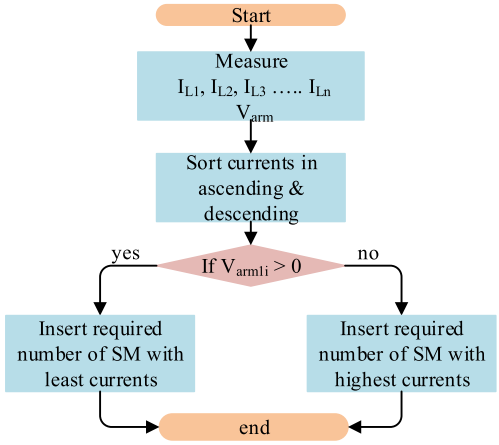

FIGURE 4. Current balancing algorithm in the CS-MMC.

where, C_{2i}, n_{2i} are the equivalent arm capacitance and the number of inserted SMs of the i^{th} arm, respectively, and C_{SM} is the capacitance of each SM. The arms are numbered from 1 to 4 as shown in Fig. 5. The nominal voltage value across each capacitor in the VS-SMs (V_c) is determined by (2).

$$V_C = \frac{V_{dc_2}}{N_2} \tag{2}$$

where, V_{dc_2} is the DC voltage of the VSC-HVDC side and N_2 is the total number of SMs in each arm of the VS-MMC. Besides, the arm voltages ($V_{arm_{2i}}$) can be calculated using (3).

$$V_{arm_{2i}} = n_{2i}\frac{V_{dc_2}}{N_2} \tag{3}$$

To get the equations of the DC and AC voltages of the VS-MMC, apply KVL on loops 1 and 2 as in (4) and (5), respectively.

$$V_{dc_2} = V_{arm_{21}} + V_{arm_{22}} \tag{4}$$

$$v_{ac_2} = V_{arm_{21}} - V_{arm_{23}} \tag{5}$$

Using equations (3), (4) and (5) with taking into consideration that $V_{arm_{22}} = V_{arm_{23}}$, the number of inserted SMs in each arm can be represented as a function of the reference AC voltage signal as in (6) and (7);

$$n_{21} = n_{24} = N_2\frac{1 - v^*_{ac_2}}{2} \tag{6}$$

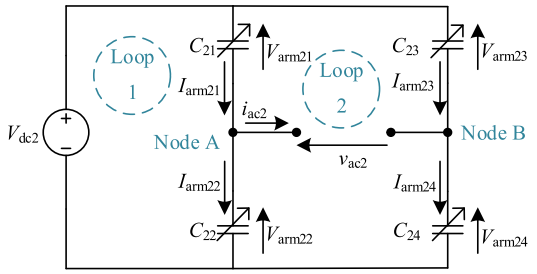

FIGURE 5. VS-MMC equivalent circuit.

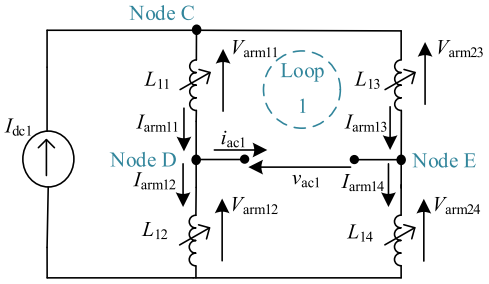

FIGURE 6. CS-MMC equivalent circuit.

$$n_{22} = n_{23} = N_2 \frac{1 + v^*_{ac_2}}{2} \tag{7}$$

where, $v^*_{ac_2} \in \{-1, 1\}$ is the per-unit reference signal of the AC voltage of the VS-MMC. By applying KCL at node A in Fig. 5, the AC current of VS-MMC (i_{ac_2}) is deduced from (8).

$$i_{ac_2} = I_{arm_{21}} - I_{arm_{22}} \tag{8}$$

Assuming a negligible arm inductance and resistance ($L_{arm} = 0$ and $R_{arm_2} = 0$) and using (4) and (8) with taking into consideration that the arm currents can be defined as a function of the arm voltages using the equivalent capacitance model $\left(I_{arm_{2i}} = C_{2i}\frac{dV_{arm_{2i}}}{dt}\right)$, the AC current is divided among the arms depending on the equivalent capacitance of each arm as in (9) and (10).

$$I_{arm_{21}} = I_{arm_{24}} = \frac{i_{ac_2}C_{21}}{C_{21} + C_{22}} = i_{ac_2}\frac{1 + v^*_{ac_2}}{2} \tag{9}$$

$$I_{arm_{22}} = I_{arm_{23}} = \frac{-i_{ac_2}C_{22}}{C_{21} + C_{22}} = -i_{ac_2}\frac{1 - v^*_{ac_2}}{2} \tag{10}$$

B. CS-MMC ANALYSIS

By applying the duality principle in CS-MMC, all CS-SMs per arm are replaced by an equivalent variable inductor (L_{1i}), as described in Fig. 6, whose inductance depends on the number of inserted CS-SMs as in (11);

$$L_{1i} = \frac{L_{SM}}{n_{1i}} \tag{11}$$

where L_{1i}, n_{1i} are defined as the equivalent arm inductor and the number of inserted CS-SMs in the i^{th} arm, and L_{SM} is the inductance of each CS-SM. The letter i represents the number of the arm in the CS-MMC from 1 to 4. The nominal current inside each inductor in the CS-SM (I_L) can be determined by (12).

$$I_L = \frac{I_{dc_1}}{N_1} \tag{12}$$

where I_{dc_1} is the DC current of the LCC-HVDC side and N_1 is the total number of SMs in each arm of the CS-MMC. The arm currents ($I_{arm_{1i}}$) can be calculated ideally as shown in (13).

$$I_{arm_{1i}} = n_{1i}\frac{I_{dc_1}}{N_1} \tag{13}$$

Applying KCL on node C and D, to get the equations of the DC and AC currents of the CS-MMC as in (14) and (15), respectively.

$$I_{dc_1} = I_{arm_{11}} + I_{arm_{13}} \tag{14}$$

$$i_{ac_1} = I_{arm_{11}} - I_{arm_{12}} \tag{15}$$

Assuming that $I_{arm_{12}} = I_{arm_{13}}$ and by using equations (13), (14), and (15), the number of inserted SMs in each arm can be represented by (16) and (17).

$$n_{11} = n_{14} = N_1\frac{1 - i^*_{ac_1}}{2} \tag{16}$$

$$n_{12} = n_{13} = N_1\frac{1 + i^*_{ac_1}}{2} \tag{17}$$

where, $i^*_{ac_1} \in \{-1, 1\}$ is the per-unit reference signal of the AC current of the CS-MMC. The AC voltage of the CS-MMC (v_{ac_1}) is calculated by applying KVL on loop 1 in Fig. 6 as in (18).

$$v_{ac_1} = V_{arm_{11}} - V_{arm_{13}} \tag{18}$$

Similarly, assuming a negligible arm capacitance and resistance ($C_{arm} = 0$ *and* $R_{arm_1} = 0$), using (15) and (18), and taking into consideration that the arm voltages can be defined as a function of the arm currents using the equivalent inductance model $\left(V_{arm_{1i}} = L_{1i}\frac{dI_{arm_{1i}}}{dt}\right)$, the AC voltage is divided among the arms depending on the equivalent inductances of each arm as in (19) and (20).

$$V_{arm_{11}} = V_{arm_{14}} = \frac{v_{ac_1}L_{11}}{L_{11} + L_{12}} = v_{ac_1}\frac{1 + i^*_{ac_1}}{2} \tag{19}$$

$$V_{arm_{12}} = V_{arm_{13}} = \frac{-v_{ac_1}L_{12}}{L_{11} + L_{12}} = -v_{ac_1}\frac{1 - i^*_{ac_1}}{2} \tag{20}$$

C. SUB-MODULE PARAMETERS DESIGN

This sub-section is devoted to design C_{SM} in VS-MMC and L_{SM} in CS-MMC while taking into account that the reference AC signal is trapezoidal as shown in Fig. 7, with variable modulation index $m_{i_{ac_1}}$ for the CS-MMC and $m_{v_{ac_2}}$ for the VS-MMC.

The main selection criteria are to reduce voltage ripple across the C_{SM} and current ripple in the L_{SM}. The control

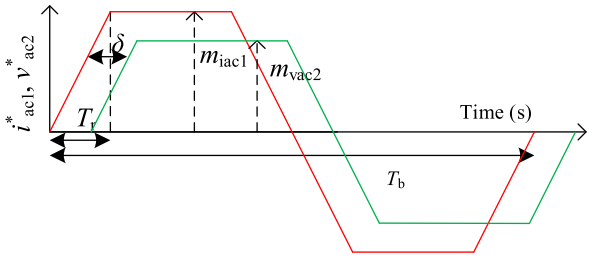

FIGURE 7. Reference AC waveforms.

parameters of the waveform are the rise time T_r, modulation indices $m_{i_{ac_1}}$, $m_{v_{ac_2}}$ and the periodic time T_b.

$$v^*_{ac_2}(t) = m_{v_{ac_2}} \begin{cases} \dfrac{t}{T_r}, & 0 < t < T_r \\ 1, & T_r < t < 0.5T_b - T_r \\ -\dfrac{(t-0.5T_b)}{T_r}, & 0.5T_b - T_r < t < 0.5T_b + T_r \\ -1, & 0.5T_b + T_r < t < T_b - T_r \\ \dfrac{(t-T_b)}{T_r}, & T_b - T_r < t < T_b \end{cases} \tag{21}$$

1) CAPACITANCE DESIGN OF THE VS-MMC

The reference AC voltage of the VS-MMC ($v^*_{ac_2}$) is a trapezoidal wave form and can be described by (21). The change in the voltage across each SM capacitor in the 1st arm of VS-MMC is given by (22).

$$\Delta V_C = \frac{1}{C_{SM}} \int_{t_0}^{t} I_{arm_{21}} \left(\frac{n_{21}}{N_2}\right) dt \tag{22}$$

By substituting (6) and (9) in (22), the change in the voltage across each VS-SM in 1st arm can be expressed by (23).

$$\Delta V_C = \frac{1}{C_{SM}} \int_{t_0}^{t} i_{ac_2} \frac{1 - v^{*2}_{ac_2}}{4} dt \tag{23}$$

Assuming a unity power factor, the VS-MMC AC current can be expressed by (24), where I_{dc_2} is the DC current at the DC side of the VS-MMC at rated power. The change in the capacitor voltage can be deduced by substituting (21) and (24) in (23). Capacitor voltage ripple can be calculated by studying the first half cycle and are given by (25) and (26).

$$i_{ac_2}(t) = m_{v_{ac_2}} I_{dc_2} \begin{cases} \dfrac{t}{T_r}, & 0 < t < T_r \\ 1, & T_r < t < 0.5T_b - T_r \\ -\dfrac{(t-0.5T_b)}{T_r}, & 0.5T_b - T_r < t < 0.5T_b + T_r \\ -1, & 0.5T_b + T_r < t < T_b - T_r \\ \dfrac{(t-T_b)}{T_r}, & T_b - T_r < t < T_b \end{cases} \tag{24}$$

$$V_{ripple} = \Delta V_C(0.5T_b) - \Delta V_C(0) \tag{25}$$

$$V_{ripple} = \frac{m_{v_{ac_2}} I_{dc_2}}{4C_{SM}} \left(T_r \left(\frac{3}{2} m^2_{v_{ac_2}} - 1\right) + \frac{T_b}{2}\left(1 - m^2_{v_{ac_2}}\right)\right) \tag{26}$$

The voltage ripples percentage can be calculated as (27).

$$V_{ripple\%} = \frac{N_2 V_{ripple}}{V_{dc_2}} \tag{27}$$

Then, the SM capacitance for a given voltage ripple percentage can be calculated as in (28).

$$C_{\mathrm{SM}} = \frac{m_{v_{ac_2}} P_{rated} N_2}{4 V_{ripple\%} V^2_{dc_2}} \left(T_r \left(\frac{3}{2} m^2_{v_{ac_2}} - 1\right) + \frac{T_b}{2}\left(1 - m^2_{v_{ac_2}}\right)\right) \tag{28}$$

where, $P_{rated} = V_{dc_2} I_{dc_2}$.

Regarding the 2^{nd} order harmonic current inherited in the VS-MMC, the arm inductance is chosen large enough to reduce its magnitude. Additionally, a number of circulating current elimination techniques can be used as in [42], [43].

$$i^*_{ac_1}(t) = m_{i_{ac_1}} \begin{cases} \dfrac{t}{T_r}, & 0 < t < T_r \\ 1, & T_r < t < 0.5T_b - T_r \\ -\dfrac{(t-0.5T_b)}{T_r}, & 0.5\,T_b - T_r < t < 0.5T_b + T_r \\ -1, & 0.5\,T_b + T_r < t < T_b - T_r \\ \dfrac{(t-T_b)}{T_r}, & T_b - T_r < t < T_b \end{cases} \tag{29}$$

2) INDUCTANCE DESIGN OF THE CS-MMC

Using the duality, the reference AC current signal for the CS-MMC can be expressed by (29). The change in the currents in each SM inductor in the 1st arm of CS-MMC is given by (30).

$$\Delta I_L = \frac{1}{L_{SM}} \int V_{arm_{11}} \left(\frac{n_{11}}{N_1}\right) dt \tag{30}$$

By substituting (16) and (19) in (30), the change in the inductor current for each SM in the 1st arm is given by (31).

$$\Delta I_L = \frac{1}{L_{SM}} \int v_{ac_2} \frac{1 - i_{ac_1}^{*2}}{4} dt \tag{31}$$

$$v_{ac_1}(t) = m_{i_{ac_1}} V_{dc_1} \begin{cases} \dfrac{t}{T_r}, & 0 < t < T_r \\ 1, & T_r < t < 0.5T_b - T_r \\ -\dfrac{(t - 0.5T_b)}{T_r}, & 0.5T_b - T_r < t < 0.5T_b + T_r \\ -1, & 0.5T_b + T_r < t < T_b - T_r \\ \dfrac{(t - T_b)}{T_r}, & T_b - T_r < t < T_b \end{cases} \tag{32}$$

Assuming unity power factor, the output voltage from CS-MMC can be expressed by (32), where V_{dc1} is DC voltage of the CS-MMC at rated power, then by substituting (29) and (32) in (31), the inductor ripple current can be expressed by (33) and (34).

$$I_{ripple} = \Delta I_L\,(0.5T_b) - \Delta I_L\,(0) \tag{33}$$

$$I_{ripple} = \frac{m_{i_{ac_1}} V_{dc_1}}{4L_{SM}} \left(T_r \left(\frac{3}{2} m_{i_{ac_1}}^2 - 1\right) + \frac{T_b}{2}\left(1 - m_{i_{ac_1}}^2\right)\right) \tag{34}$$

The current ripple percentage is given by (35).

$$I_{ripple\%} = \frac{N_1 I_{ripple}}{I_{dc_1}} \tag{35}$$

Then, by substituting (35) in (34), the value of SM inductor can be computed by (36).

$$L_{SM} = \frac{m_{i_{ac_1}} P_{rated} N_1}{4 I_{ripple\%} I_{dc_1}^2} \left(T_r \left(\frac{3}{2} m_{i_{ac_1}}^2 - 1\right) + \frac{T_b}{2}\left(1 - m_{i_{ac_1}}^2\right)\right) \tag{36}$$

where, $P_{rated} = V_{dc_1} I_{dc_1}$.

IV. DC-DC CONVERTER CONTROL METHODOLOGIES

In this section, two control methods are proposed. Each of them has its own advantages and disadvantages from the point of view of reactive power and sizing of L_{SM} and C_{SM}.

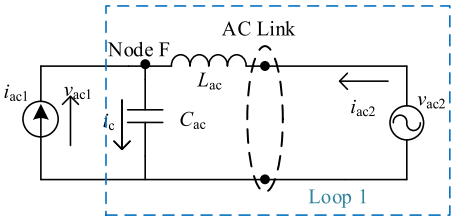

FIGURE 8. Proposed DC-DC converter simplified equivalent circuit.

A. POWER EQUATIONS

Both VS-MMC and CS-MMC are connected through an isolating transformer and an LC filter (L_{ac} and C_{ac}) to eliminate the reactive power at rated power flow. The CS-MMC is replaced by an equivalent current source with variable magnitude. While the VS-MMC is replaced by an equivalent variable voltage source as shown in Fig. 8. Assuming a lossless system, a fundamental harmonic analysis is applied in the analysis of the DC-DC converter in this section, where the AC current fundamental component phasor produced by CS-MMC can be denoted by $\bar{i}_{ac_{1_f}}$.

Similarly, the fundamental component phasor of AC voltage produced by VS-MMC can be denoted by $\bar{v}_{ac_{2_f}}$ and it lags $\bar{i}_{ac_{1_f}}$ by an angle δ. The phasor form of circuit variables can be represented by (37) and (38).

$$\bar{i}_{ac_{1_f}} = m_{i_{ac_1}} \hat{I}_{ac_{1_f}} \angle 0 = m_{i_{ac_1}} \hat{I}_{ac_{1_f}} + j0 \tag{37}$$

$$\bar{v}_{ac_{2_f}} = m_{v_{ac_2}} \hat{V}_{ac_{2_f}} \angle -\delta = m_{v_{ac_2}} \hat{V}_{ac_{2_f}} \cos(\delta) - jm_{v_{ac_2}} \hat{V}_{ac_{2_f}} \sin(\delta) \tag{38}$$

where, $\hat{I}_{ac_{1_f}}$ and $\hat{V}_{ac_{2_f}}$ are the peak values of the fundamental components at unity modulation indices of the AC current of CS-MMC and AC voltage of VS-MMC, respectively. By applying KCL at node F in Fig. 8, the following can be deduced:

$$\bar{i}_{ac_{1_f}} = \bar{i}_{c_f} + \bar{i}_{ac_{2_f}} \tag{39}$$

$$\bar{i}_{c_f} = j\omega C_{ac} \bar{v}_{ac_{1_f}} \tag{40}$$

$$\bar{i}_{ac_{2_f}} = \bar{i}_{ac_{1_f}} - j\omega C_{ac} \bar{v}_{ac_{1_f}} \tag{41}$$

where, ω is the fundamental frequency at the AC link, $\bar{i}_{c_f}$ is the fundamental phasor of the current passing through C_{ac}, $\bar{i}_{ac_{2_f}}$ is the fundamental phasor of AC current of VS-MMC and $\bar{v}_{ac_{1_f}}$ is the fundamental phasor of AC voltage at CS-MMC. By applying KVL in loop (1) in Fig. 8, the following equation is deduced that describes the relation between AC voltage produced by VS-MMC and LC filter:

$$\bar{v}_{ac_{1_f}} = \bar{v}_{ac_{2_f}} + j\omega L_{ac} \bar{i}_{ac_{2_f}} \tag{42}$$

Using (41) and (42), the following can be deduced:

$$\bar{v}_{ac_{1_f}} = \frac{\bar{v}_{ac_{2_f}} + j\omega L_{ac} \bar{i}_{ac_{1_f}}}{1 - \omega^2 L_{ac} C_{ac}} \tag{43}$$

The apparent power S_{ac_1} for CS-MMC can be calculated as follows:

$$S_{ac_1} = \bar{v}_{ac_{1_f}} \bar{i}^*_{ac_{1_f}} \tag{44}$$

$$S_{ac_1} = \frac{m_{i_{ac_1}} \hat{I}_{ac_{1_f}}}{\left(1-\omega^2 L_{ac} C_{ac}\right)} \left(m_{v_{ac_2}} \hat{V}_{ac_{2_f}} \cos(\delta) + j\left(m_{i_{ac_1}} \hat{I}_{ac_{1_f}} \omega L_{ac} - m_{v_{ac_2}} \hat{V}_{ac_{2_f}} \sin(\delta)\right)\right) \tag{45}$$

The active powers of the CS-MMC (P_{ac_1}) and VS-MMC (P_{ac_2}) are given by:

$$P_{ac_1} = \frac{8 m_{v_{ac_2}} m_{i_{ac_1}} I_{dc_1} V_{dc_2} cos\ \delta}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} = -P_{ac_2} \tag{46}$$

where, $\hat{I}_{ac_{1_f}} = \frac{2\sqrt{2}}{\pi} I_{dc_1}$ and $\hat{V}_{ac_{2_f}} = \frac{2\sqrt{2}}{\pi} V_{dc_2}$ assuming that the rise time of the trapezoidal is neglected so the voltage and current waveforms can be considered as square-waveforms for the sake of simplicity in the analysis. Also, the reactive power at CS-MMC can be described as in (47).

$$Q_{ac_1} = \frac{8 m_{i_{ac_1}} I_{dc_1} \left(\omega L_{ac} m_{i_{ac_1}} I_{dc_1} - m_{v_{ac_2}} V_{dc_2} sin\ \delta\right)}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} \tag{47}$$

The DC-DC converter is assumed to be lossless in addition to neglecting the loss in the isolating transformer and LC filter. As a result, the DC-DC converter power is exchanged equally between both DC terminals.

$$\left|P_{dc_1}\right| = \left|P_{ac_1}\right| = \left|P_{ac_2}\right| = \left|P_{dc_2}\right| \tag{48}$$

Thus, the apparent power S_{ac_2} at VS-MMC can be calculated as follows:

$$S_{ac_2} = \bar{v}_{ac_{2_f}} \bar{i}^*_{ac_{2_f}} \tag{49}$$

From (37), (38), (41), and (42), $\bar{i}_{ac_{2_f}}$ can be expressed as follows:

$$\bar{i}_{ac_{2_f}} = \left(\frac{1}{1-\omega^2 L_{ac} C_{ac}}\right) \times \left(m_{i_{ac_1}} \hat{I}_{ac_{1_f}} - \omega C_{ac} m_{v_{ac_2}} \hat{V}_{ac_{2_f}} (\sin(\delta) + j\cos(\delta))\right) \tag{50}$$

Considering the formula of $\hat{I}_{ac_{2_f}}$, the reactive power Q_2 of VS-MMC can be described as follows:

$$Q_{ac_2} = \frac{8 m_{v_{ac_2}} V_{dc_2} \left(\omega C_{ac} m_{v_{ac_2}} V_{dc_2} - m_{i_{ac_1}} I_{dc_1} sin\ \delta\right)}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} \tag{51}$$

From (46) and (48), it is noted that the active power transferred in the proposed DC-DC converter can be controlled via three control variables namely phase shift δ between $i_{ac_{1_f}}$ and $v_{ac_{2_f}}$, modulation indices $m_{v_{ac_2}}$ and $m_{i_{ac_1}}$, and the fundamental frequency ω. The LC filter parameters are chosen to nullify the reactive power in (47) and (51) at rated power transfer. Then, the following sizing equations can be deduced:

$$L_{ac} = \frac{V_{dc_2} sin\ \delta_r}{\omega I_{dc_1}} \tag{52}$$

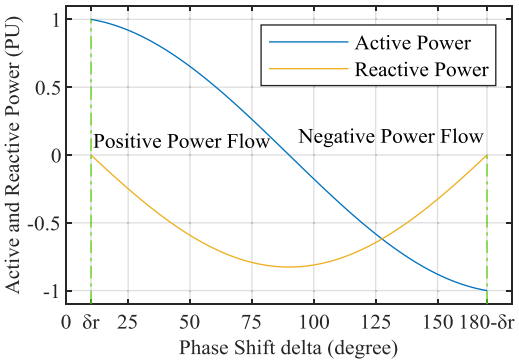

FIGURE 9. Active and reactive powers range under phase shift control.

$$C_{ac} = \frac{I_{dc_1} sin\ \delta_r}{\omega V_{dc_2}} \tag{53}$$

where, δ_r is the phase shift value at rated active power.

The δ_r is designed such that the resonant frequency ω_r of the LC filter at the AC link is higher than 5 times the fundamental frequency to decrease the oscillations produced by the LC filter in the AC link. Therefore, the δ_r should be less than 11.5°.

B. FIRST CONTROL METHOD: PHASE SHIFT CONTROL

The main control variable in this method is the phase shift δ between i_{ac_1} and v_{ac_2} at unity modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$). Hence, the active power is proportional with cos(δ) and governed by the following formula:

$$P_{ac_1} = \frac{8 I_{dc_1} V_{dc_2} cos\ \delta}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} = -P_{ac_2} \tag{54}$$

It is worth mentioning that equations (55) and (56) show that the reactive power component is inevitable when the phase shift deviates from the rated (δ_r).

$$Q_{ac_1} = \frac{8 I_{dc_1} \left(\omega L_{ac} I_{dc_1} - V_{dc_2} sin\ \delta\right)}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} \tag{55}$$

$$Q_{ac_2} = \frac{8 V_{dc_2} \left(\omega C_{ac} V_{dc_2} - I_{dc_1} sin\ \delta\right)}{\pi^2 (1-\omega^2 L_{ac} C_{ac})} \tag{56}$$

On the other hand, by substituting in the SM capacitor and inductor sizing equations (28) and (36), then the following is deduced:

$$C_{\mathrm{SM}} = \frac{N T_r P_{rated}}{8 V_{ripple\%} V_{dc_2}^2} \tag{57}$$

$$L_{\mathrm{SM}} = \frac{N T_r P_{rated}}{8 I_{ripple\%} I_{dc_1}^2} \tag{58}$$

Fig. 9 shows the full control range of phase shift δ with respect to active and reactive powers. While the phase shift deviates from the rated value, the active power decreases, and reactive power increases. Additionally, when the phase shift increases beyond 90° the active power flow is reversed. The block diagram of the closed loop control of this method can be described as shown in Fig. 10, where the PI controller outputs a phase shift, which is fed to a function generator to synthesis

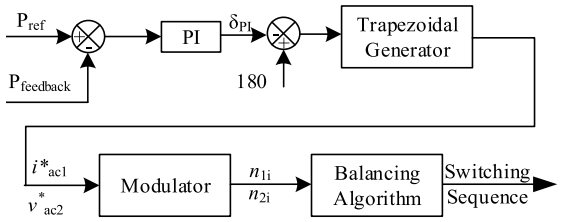

FIGURE 10. Phase shift control method block diagram.

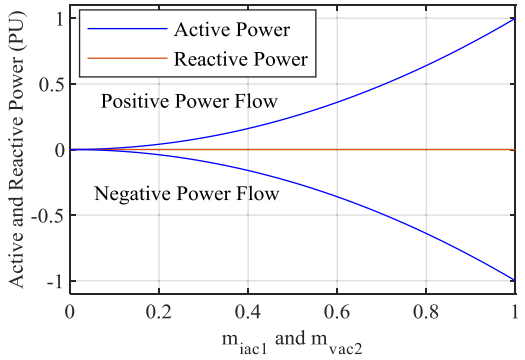

FIGURE 11. Active and reactive powers range under V/I control.

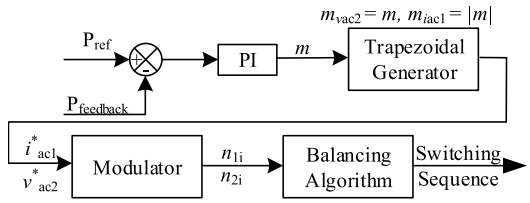

FIGURE 12. V/I control block diagram.

the reference signals $i^*_{ac_1}$ and $v^*_{ac_2}$ with the calculated δ from the PI controller at unity modulation indices. The reference signals are modulated and routed to the balancing algorithm to generate the required SMs to be inserted in each MMC.

C. SECOND CONTROL METHOD: V/I CONTROL FOR ZERO REACTIVE POWER

In this control method, the control variables are the modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$).

The magnitude of active power is controlled by changing the modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$) as shown in (46). Hence, the active power is proportional to the product of modulation indices ($m_{i_{ac_1}} \times m_{v_{ac_2}}$). However, the direction of power flow is controlled by the sign of VS-MMC modulation index ($m_{v_{ac_2}}$), where the positive sign indicates forward power flow and negative sign for reverse power flow. According to (47) and (51), a zero reactive power is maintained for the full range of active power control as shown in Fig. 11 at the same LC filter by keeping the ratio between $m_{i_{ac_1}}$ and $m_{v_{ac_2}}$ constant. The closed loop control block diagram is shown in Fig. 12, where it is based on evaluating the required modulation indices from the PI controller that ranges from -1 to 1 and are used to generate the required reference waveforms in which the modulation index ($m_{i_{ac_1}}$) is maintained positive

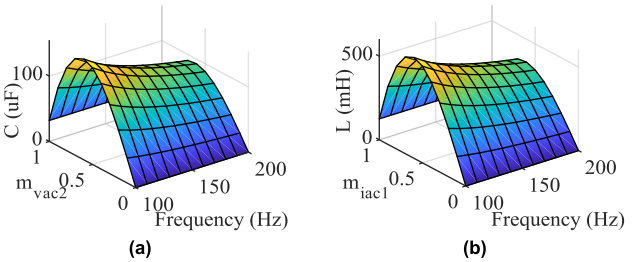

FIGURE 13. SM sizing vs modulation index and frequency in a system with P_{rated} = 400 MW, I_{dc1} = 4 kA, V_{dc2} = 500 kV, Rise time = 1 ms, No. of submodules per arm = 16 for VS-MMC and No. of submodules per arm = 4 for CS-MMC. (a) VS-SM and (b) CS-SM.

and modulation index ($m_{v_{ac_2}}$) sign depends on direction of power flow. The reference signals are modulated then passed to a balancing algorithm to generate the required SMs to be inserted in each MMC. The phase shift is maintained at its rated value (δ_r) while the modulation indices can be positive value for forward power or negative value for the reverse power. The main major consideration for MMC operation with trapezoidal waveform when using modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$) < 1 is that the capacitors used in VS-SMs and inductors in CS-SMs will exhibit a higher loading (larger charging or discharging period of voltage/current). Hence, the selection of L_{SM} and C_{SM} should be at the modulation index that corresponds to the maximum loading on the SM capacitors and inductors. The variation of L_{SM} and C_{SM} size that correspond to 10% ripples in the SM current and voltage with respect to modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$) and operating frequency is shown in Fig. 13. The designed sizing of SM energy storing element is computed according to the modulation index that matches the highest loading as shown in (59) that are calculated by differentiating (28) or (36) with respect to modulation index and equating it to zero.

$$m_{i_{ac_1}\max loading} = m_{v_{ac_2}\max loading} = \sqrt{\frac{2T_r - T_b}{9T_r - 3T_b}} \tag{59}$$

V. LOSSES ESTIMATION

In this section, a mathematical loss analysis and a case study are introduced for the losses' comparison between the two proposed control techniques.

A. MATHEMATICAL ANALYSIS

The losses of the proposed DC-DC converter can be classified into conduction and switching losses. Each SM is composed of two groups of series connected switches. n_{s_1} and n_{s_2} are the number of series connected switches in CS-SM and VS-SM, respectively. Regarding the VS-MMC, the conduction losses are divided into IGBTs and diodes conduction losses. If the arm current is positive, the arm current passes through the IGBTs in case of the bypassed SMs, while passes through the diodes in case of the inserted SMs. On the other hand, if the current is negative, the arm current passes through the IGBTs in case of the inserted SMs while passes through the diodes in case of the bypassed SMs. Therefore, IGBTs

and diodes conduction losses per arm are calculated as in (60) and (61), respectively. I_{igbt} and I_d represent the current of IGBT and diode, respectively, which can be calculated as the absolute value of arm current during their conduction. Moreover, V_{igbt} and R_{igbt} are the on-state voltage and resistance of IGBT, respectively, while V_d and R_d are the on-state voltage and resistance of diode, respectively. Furthermore, $(N_2-n_{21_p})$ and $(N_2-n_{21_n})$ represent the number of SMs in the 1st arm that have their capacitor bypassed in the positive and the negative half-cycles, respectively, while (n_{21_p}) and (n_{21_n}) represent the number of SMs that have their capacitor inserted in the positive and negative half-cycles, respectively.

$$P_{C_{VS_{IGBT/arm}}} = \frac{n_{s_2}}{T_b} \times \int_0^{\frac{T_b}{2}} (N_2-n_{21_p}) \left(I_{igbt}V_{igbt}+I_{igbt}^2R_{igbt}\right)dt + \int_{\frac{T_b}{2}}^{T_b} n_{21_n} \left(I_{igbt}V_{igbt}+I_{igbt}^2R_{igbt}\right)dt \quad (60)$$

$$P_{C_{VS_{Diode/arm}}} = \frac{n_{s_2}}{T_b} \times \int_0^{\frac{T_b}{2}} n_{21_p} \left(I_dV_d + I_d^2R_d\right)dt + \int_{\frac{T_b}{2}}^{T_b} (N_2 - n_{21_n}) \left(I_dV_d+I_d^2R_d\right)dt \quad (61)$$

The total conduction losses per VS-MMC can be calculated as follows:

$$P_{C_{VS}} = 4\left(P_{C_{VS_{IGBT/arm}}} + P_{C_{VS_{Diode/arm}}}\right) \quad (62)$$

On the other hand, since the switching losses are produced due to only the IGBTs in VS-MMC, then the switching losses per VS-SM is calculated as follows:

$$P_{s_{VS-SM}} = 0.5n_{s_2}V_{sw}I_{sw}f_s(t_{on_2} + t_{off_2}) \quad (63)$$

where, V_{sw} is the nominal switch voltage which can be calculated as $V_{dc_2}/(N_2n_{s_2})$ and I_{sw} is the average of the absolute arm current at the switching instants through the periodic time (T_b). Moreover, t_{on_2} and t_{off_2} are the turn-on and turn-off time of IGBT, respectively. Assuming $m_{i_{ac_1}} = m_{v_{ac_2}} = m$, the switching losses are calculated as follows:

$$P_{s_{VS}} = V_{dc_2}I_{dc_2}f_sm\left(t_{on_2} + t_{off_2}\right)\left(1 - \frac{2T_r}{T_b}\right) \quad (64)$$

Regarding the conduction losses calculations of the CS-MMC, it can be assumed that one IGCT per SM is conducting for the whole period. Then the conduction losses of the CS-MMC are calculated as follows:

$$P_{C_{CS}} = 4n_{s_1}\left(V_{igct}I_{dc_1} + R_{igct}\frac{I_{dc_1}^2}{N_1}\right) \quad (65)$$

where V_{igct} and R_{igct} are the on-state voltage and resistance of IGCT, respectively. Besides, the switching losses of the CS-MMC are due to the switching of the IGCTs. Also, by duality to VS-MMC, then the switching losses of the CS-MMC are calculated as in (66), where t_{on_1} and t_{off_1} are the turn-on and turn-off time of IGCT, respectively.

$$P_{s_{CS}} = 2V_{dc_1}I_{dc_1}f_sm(t_{on_1} + t_{off_1})\left(1 - \frac{2T_r}{T_b}\right) \quad (66)$$

TABLE 1. Control-hardware-in-the-loop system parameters.

Symbol		Quantity	Value
P_r		Rated power	400 MW
I_{dc1}		LCC-HVDC DC link current	4000 A
V_{dc2}		VSC-HVDC DC link voltage	500 kV
f		Fundamental Frequency	100 Hz
δ_r		Phase shift angle at rated forward power	10°
$1/n_t$		Transformer turns ratio	1/4
L_{ac}		AC link inductance	8.64 mH
C_{ac}		AC link capacitance	8.84 µF
T_r		Rise Time	1 ms
N_2		Number of SMs per arm in VS-MMC	16
N_1		Number of SMs per arm in CS-MMC	4
DC Filter at LCC/VSC Phase Shift design	L	Filter Inductance	50 mH
	C	Filter Capacitance	22.5 µF
	C_{SM}	Sub-module capacitance	50 µF
	L_{SM}	Sub-module inductance	200 mH
V/I design	C_{SM}	Sub-module capacitance	160 µF
	L_{SM}	Sub-module inductance	600 mH
f_s		Switching frequency	1000 Hz

B. CASE STUDY

The switching devices used for loss calculations are ABB 4000V, 1290A IGCT (5SHY 42L6500) in case of the CS-MMC and ABB 4500V, 2000A StakPak IGBT module (5SNA2000K451300) in case of VS-MMC. The AC inductor is selected empirically to be 0.01 pu. However, the AC capacitor is selected to be 0.001 pu. The system parameters used in losses calculation are shown in Table 1.

The comparison between the total losses of both control techniques is shown in Fig. 14 (a), where both of them yield equal losses at the rated power flow. However, the losses in the V/I control method decreases with the power flow while the losses for the phase shift control method remains constant in the whole power flow region due to the increase in reactive power. Also, the breakdown of the proposed converter losses at rated power flow is shown in Fig. 14 (b), where the AC inductor losses are the dominant item.

VI. EXPERIMENTAL VALIDATION BASED ON CONTROL-HARDWARE-IN-THE-LOOP

The proposed DC-DC topology is designed and tested based on Control-Hardware-in-the-loop (CHiL) system. The hardware platform of CHiL validation is shown in Fig. 15. The main circuit of the DC-DC converter is emulated on OPAL-RT platform, which is operating on 4 cores based on Intel Core Xeon processor at 3 GHz and RAM 2 × 8 GB. The communication port is based on Gigabit Ethernet LAN.

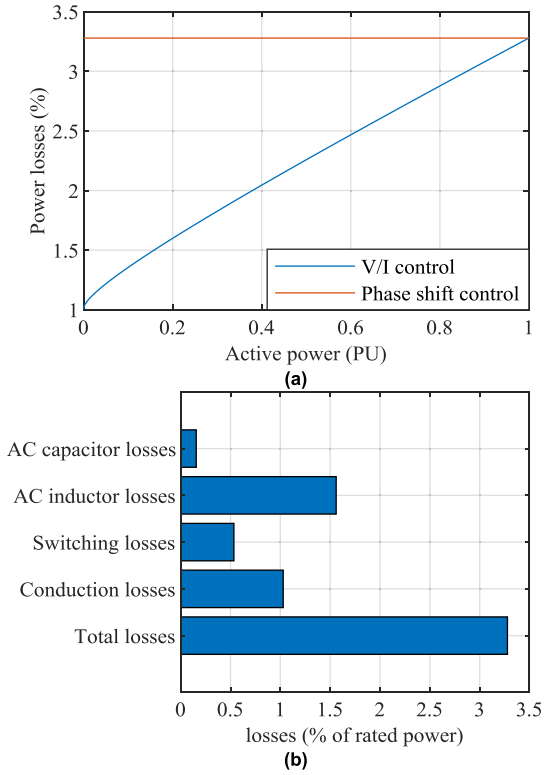

FIGURE 14. (a) Comparison between power losses of both control methods and (b) losses breakdown of the proposed DC-DC converter at rated power.

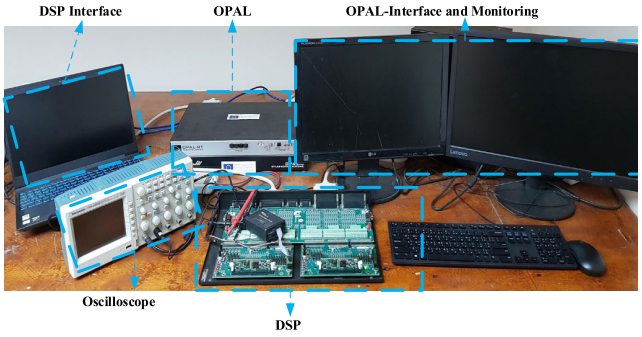

FIGURE 15. Control-hardware-in-the-loop platform.

Alternatively, the system controller is uploaded on a 150 MHz DSP (Digital Signal Processor) control board labeled as (TMS320F28335ZJZA). The DSP is responsible for handling the control and feedback signals of the exact DC-DC converter setup built on OPAL-RT platform.

The DSP receives the active power reference and feedback power and based on these values it generates the required signals to operate the proposed DC-DC converter on OPAL-RT platform. The system parameters are given in Table 1.

The LC filter parameters are designed based on (52) and (53). A 17-level VS-MMC is utilized, while for the CS-MMC (due to the usage of IGCT technology, which can withstand high current), a 5-level CS-MMC can sufficiently be used. A DC filter of 2nd order nature (LC filter) is used at both DC sides of the converter to filter the voltage at LCC and the current at VSC by reducing the even harmonics where DC filter parameters are presented in Table 1.

The CHiL has been implemented for three cases, the first case includes the proposed phase shift control with the corresponding SM parameters design. Whereas in the second case, the proposed V/I control approach is tested after updating the SM parameters design. Finally, the third case simulates some fault scenarios at both VS-MMC and CS-MMC DC sides.

A. PHASE SHIFT CONTROL

The simplest form of power flow control is dependent on the phase shift angle between AC voltage of VS-MMC (v_{ac_2}) and AC current of CS-MMC (i_{ac_1}). The active power is controlled through a closed loop by changing the value of the phase shift δ at unity modulation indices as shown in Fig. 10. Thus, the active power can be controlled over the entire power range. The direction of flow can be controlled either forward or reverse based on the phase shift value.

Fig. 16 describes the behavior of the proposed DC-DC converter during the forward and reverse power flow at rated conditions as well as partial flow of power. From Fig. 16 parts (a) and (b), it is obvious that the active power can be transferred in both directions at zero reactive power but only at rated value. On the other hand, the reactive power increases as the active power deviates from its rated value.

Furthermore, the value of the DC-link currents and voltages at MMCs input terminals are shown in Fig. 16 parts (c) and (d) for CS-MMC and VS-MMC, respectively. CS-MMC input current is always constant, which is the typical case for current source-based converters, while the VS-MMC DC-link voltage is also constant and its current is varying according to loading. Voltages and currents at the AC side of CS-MMC and VS-MMC are shown in Fig. 16 parts (e) and (f), where the oscillations in the AC currents and voltages are produced due to the LC filter resonance at the AC link. It can be observed that the power flow is in the forward direction (from the CS-MMC to the VS-MMC). Fig. 17 parts (a) and (b) show the SM inductor currents during rated and partial power flow, respectively, in two arms of one leg. Also, Fig. 17 parts (c) and (d) illustrate the SM capacitor voltages during rated and partial power flow, respectively, in two arms of one leg. The SMs inductors' current and capacitors' voltages exhibit ripple less than 10%, which matches the required design. In addition, Fig. 17 parts (e) and (f) show the phase shift between i_{ac_1} and v_{ac_2} during forward and reverse power flow at rated power.

B. V/I CONTROL

In order to control the active power without generating any reactive power at the DC-DC converter AC terminals, the modulation indices ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$) should be varied. Therefore, a new design for SMs capacitors and inductors that depends on (28) and (36) is required to withstand a proper operation when ($m_{i_{ac_1}}$ and $m_{v_{ac_2}}$) < 1. The SMs parameters should be designed at the maximum loading condition therefore, equation (59) is substituted in

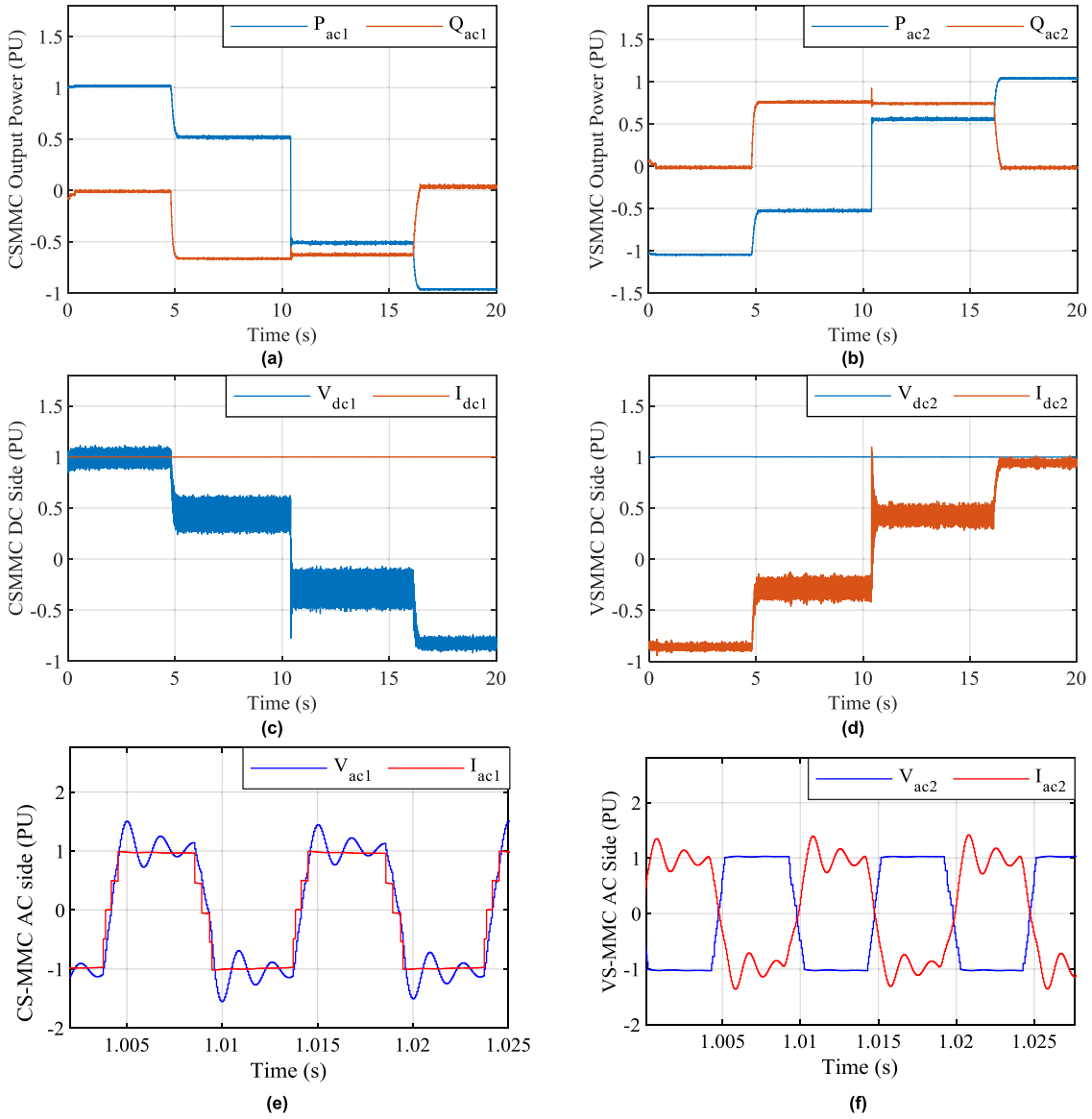

FIGURE 16. OPAL-RT results under phase shift control: (a) Active and reactive powers at CS-MMC, (b) active and reactive powers at VS-MMC, (c) DC link voltage and current at CS-MMC, (d) DC link voltage and current at VS-MMC, (e) AC side of CS-MMC at P_{rated}, and (f) AC side of VS-MMC at P_{rated}.

(28) and (36), then the passive elements parameters are calculated. Fig. 18 parts (a) and (b) show the forward and reverse power flow and the corresponding reactive power of the CS-MMC and VS-MMC, respectively. The reactive power is successfully nullified for the full range of power flow by keeping a constant ratio between $m_{i_{ac_1}}$ and $m_{v_{ac_2}}$. Also, the DC-link voltages and currents at the LCC and VSC based HVDC network terminal are shown in Fig. 18 parts (c) and (d), respectively. The AC voltages and currents of the VS-MMC and CS-MMC are depicted in Fig. 18 parts (e) and (f), respectively, at positive power flow. Oscillations exist in the AC currents and voltages due to the LC filter resonance at the AC link. Moreover, Figs. 19 parts (a) and (b) show the SM inductors currents at full rated and partial power flow, respectively. Additionally, Fig. 19 parts (c) and (d) show the SM capacitors voltages at full rated and partial power flow, respectively. It is evident that the ripple magnitudes are less than 10% due to the new design of L_{SM} and C_{SM} that guarantee small ripple under different power levels. In addition, Fig. 19 parts (e) and (f) show i_{ac_1} and v_{ac_2} at the rated forward and reverse power flow, respectively.

C. FAULT RESULTS

In this subsection, the proposed DC-DC converter response under DC-link pole-to-pole faults is studied under different scenarios. As shown in Fig. 20, fault either occurs at CS-MMC or VS-MMC DC links while receiving rated active power from the other MMC. It is worth to clarify that in case of a fault at the DC side of CS-MMC, the fault detection is based on the increase of the DC current above 120% of

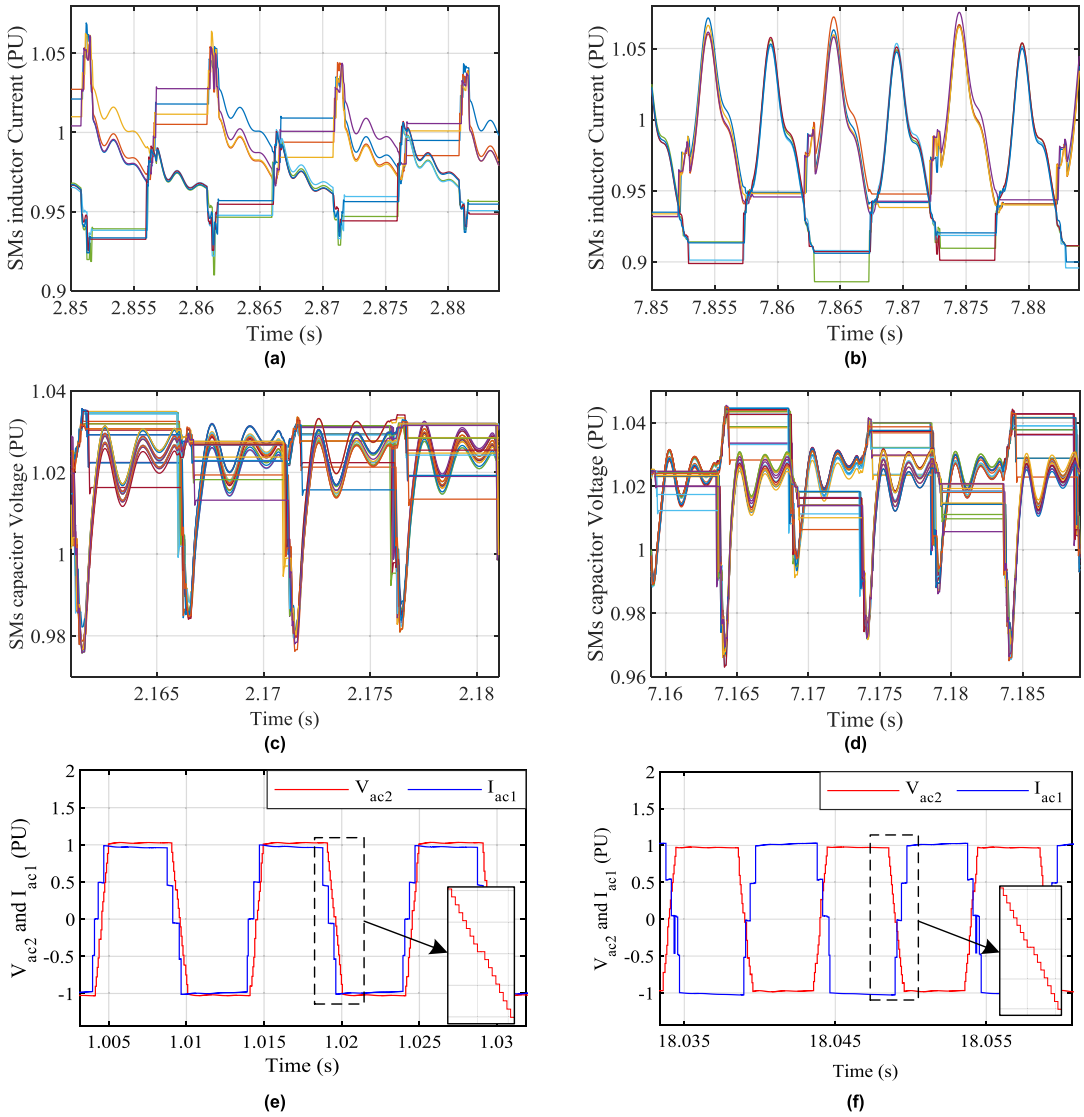

FIGURE 17. OPAL-RT results under phase shift control (Cont.): (a) SM inductor current at P_{rated}, (b) SM inductor current at 0.5 P_{rated}, (c) SM capacitor voltage at P_{rated}, (d) SM capacitor voltage at 0.5 P_{rated}, (e) V_{ac2} and I_{ac1} at forward P_{rated}, and (f) V_{ac2} and I_{ac1} at reverse P_{rated}.

the nominal value. The controller action in that case is to block the CS-MMC. The CS-MMC is blocked by turning off S1 and turning on S2 in each CS-SM to isolate CS-SM inductors from each leg and prevent them from charging from the VS-MMC side, while maintaining a closed path for inductors' currents.

On the other hand, for a fault at the DC side of VS-MMC, the fault detection is based on the increase of the DC current above 120% of the nominal value and the decrease of the DC voltage below 70% of the nominal value. The controller action in this case is to block the VS-MMC. Blocking the VS-MMC is done by turning off all the involved IGBTs to avoid the discharge of VS-SM capacitors in the fault.

1) FAULT AT DC SIDE OF THE CS-MMC

In the first case, the rated active power is delivered to the CS-MMC during the pre-fault period, where the fault occurs at the CS-MMC DC-side at t = 0.5 s. The DC-link voltages and currents of the CS-MMC and VS-MMC are shown in Fig. 21 parts (a) and (b), respectively. The CS-MMC DC-link voltage collapses to zero at the instant of the fault. The fault is detected after 1 ms delay of sensing devices, where after the fault detection, the DC-link current of the CS-MMC drops to zero due to the controller action of blocking the CS-MMC. Accordingly, the received active power becomes zero at the CS-MMC side, as shown in Fig. 21(c). However, there is small reactive power delivered at the terminals of VS-MMC as shown in Fig. 21(d). Therefore, it can be deduced that during fault, an inevitable small reactive power component will be delivered to the proposed DC-DC converter passive elements. Also, the fault is assumed temporary as it persists for small period of time (about 150 ms). As the pre-fault operation is restored, the reactive power is again nullified. Besides, Fig. 21(e) shows the CS-SM inductors'

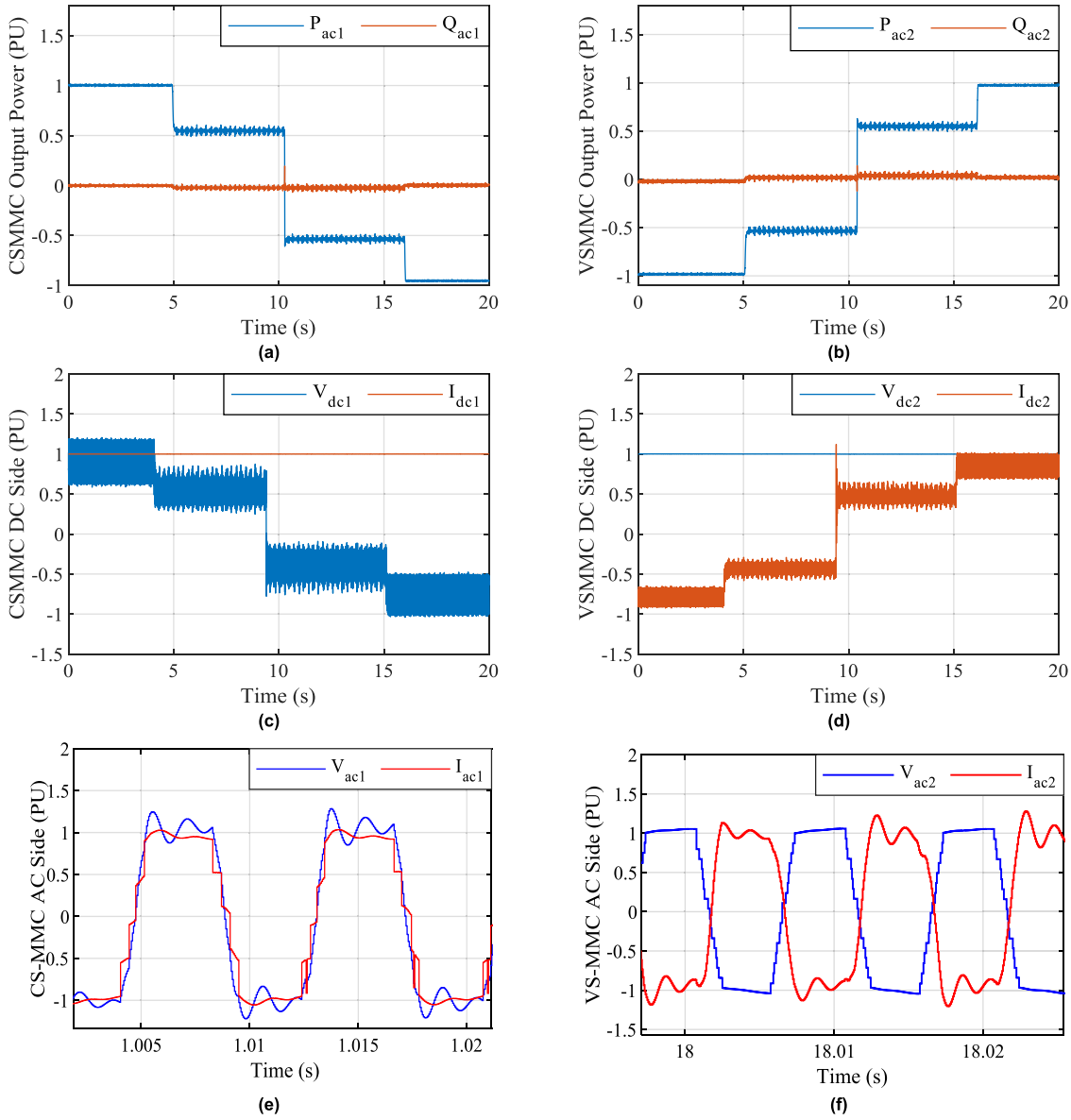

FIGURE 18. OPAL-RT results under V/I control: (a) Active and reactive powers at CS-MMC, (b) active and reactive powers at VS-MMC, (c) DC link voltage and current at CS-MMC, (d) DC link voltage and current at VS-MMC, (e) CS-MMC AC side at P_{rated}, and (f) VS-MMC AC side at P_{rated}.

currents, where the inductors have been charged to higher value from the VS-MMC before being bypassed after the fault detection while Fig. 21(f) shows the VS-SM capacitors' voltages that have minor disturbances during fault occurrence and clearance.

In the case of a less controversial scenario assuming the fault location at the midpoint of an overhead transmission line (OHTL) connecting the terminals of LCC-HVDC network with CS-MMC DC terminals. The fault is a pole to ground fault through a resistance of 2 Ω, where the system behaves with the same scenario except the detection technique will take longer time to pick up the fault as the increase in DC link current will be slower. Moreover, Fig. 22a shows DC link voltage and current at CS-MMC where the fault occurs at t = 0.5 s. The DC link voltage collapses to zero and after a period of t = 1 ms, the fault is detected and current falls to zero. Fig. 22b shows the DC link voltage and current at VS-MMC side, where the DC link current increases at t = 0.5 s due to fault occurrence then after fault detection, the current falls to zero; due to blocking of CS-MMC. On the other hand, the DC link voltage is maintained constant due to nature of VSC.

2) FAULT AT DC SIDE OF THE VS-MMC

Fig. 23 shows the results for the second fault case, where the VS-MMC receives the rated power from the CS-MMC in the pre-fault period. The VS-MMC DC-link experiences a DC pole-to-pole fault at t = 0.5s, where instantly, the DC voltage dropped to zero at both the CS-MMC and VS-MMC sides. Then after fault detection (1 ms), the VS-MMC is blocked to avoid the discharge of VS-SM capacitors in the fault.

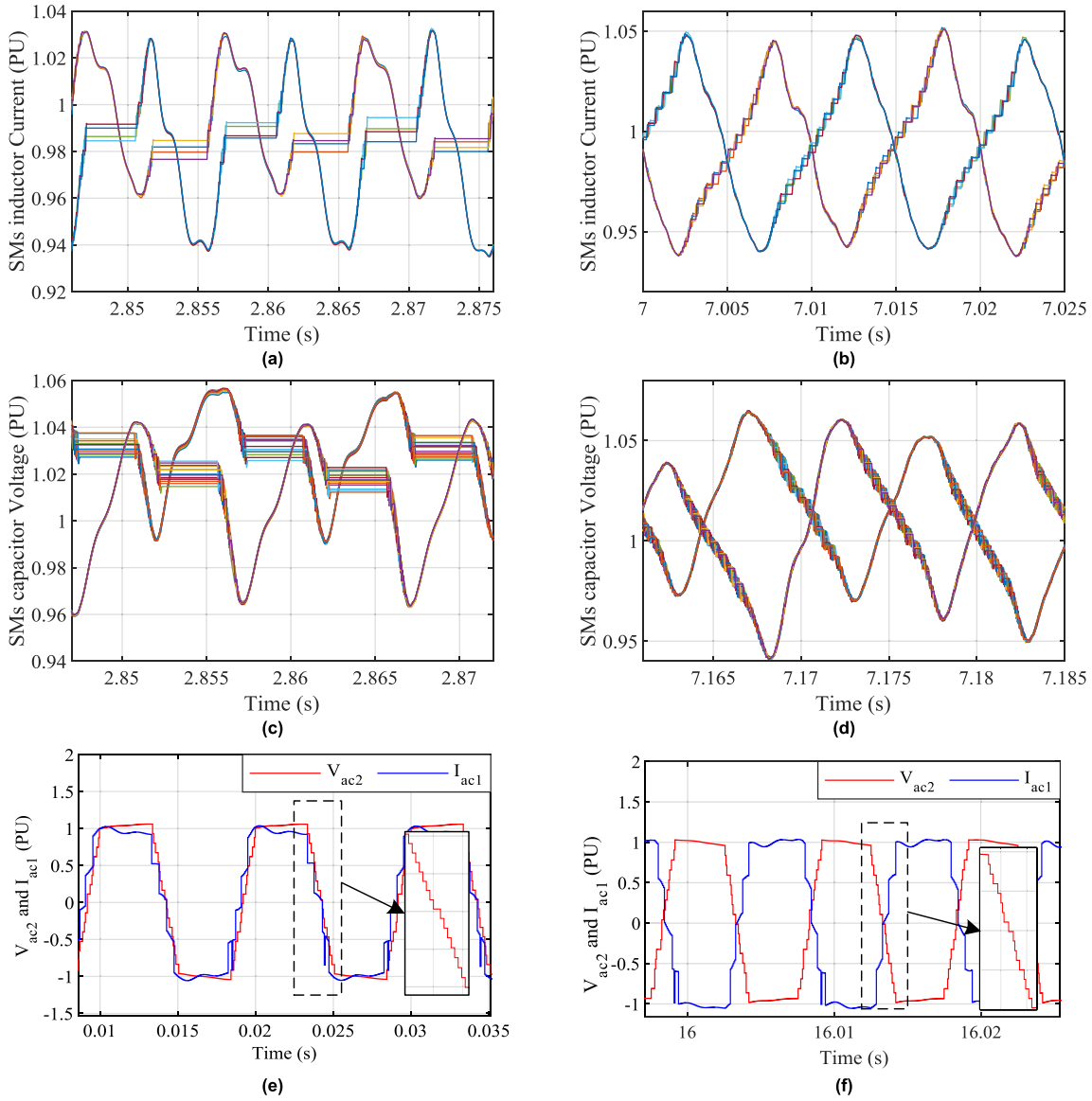

FIGURE 19. OPAL-RT results under V/I control (Cont.): (a) Inductor current in CS-SM at Prated, (b) inductor current in CS-SM at 0.5 P_{rated}, (c) capacitor voltage in VS-SM at P_{rated}, (d) capacitor voltage in VS-SM at 0.5 P_{rated}, (e) I_{ac1} and V_{ac2} at rated forward power flow, and (f) I_{ac1} and V_{ac2} at rated reverse power flow.

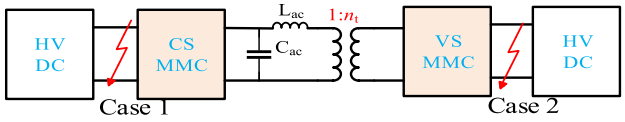

FIGURE 20. Applied fault cases to study topology response.

Therefore, the current of the VS-MMC SMs increases to almost triple of the rated value until the fault is detected. Then, the current decays to almost the rated value until fault clearance, while the DC current at the CS-MMC side remains constant during the whole period. The DC voltages and currents of both CS-MMC and VS-MMC are depicted in Fig. 23 parts (a) and (b), respectively. On the other hand, the active and reactive powers of the CS-MMC and VS-MMC are shown in Fig. 23 parts (c) and (d), respectively, where the active powers of both MMCs dropped to zero at the instant of the fault. Also, it is evident that the CS-MMC is responsible to deliver reactive power during fault to feed passive elements. Furthermore, as seen from Fig. 23 parts (e) and (f), the SM capacitor voltage slightly dropped to a smaller value due to the capacitor discharge through the fault then it remains constant when fault is detected. Whereas, the SM inductor current of the CS-MMC remains constant with small disturbances. Upon fault clearance, the VS-SM capacitors recharge to the nominal value and normal operation is restored.

Similarly, in case of a fault through a resistance of 2 Ω at the midpoint of the OHTL connecting the VSC-HVDC

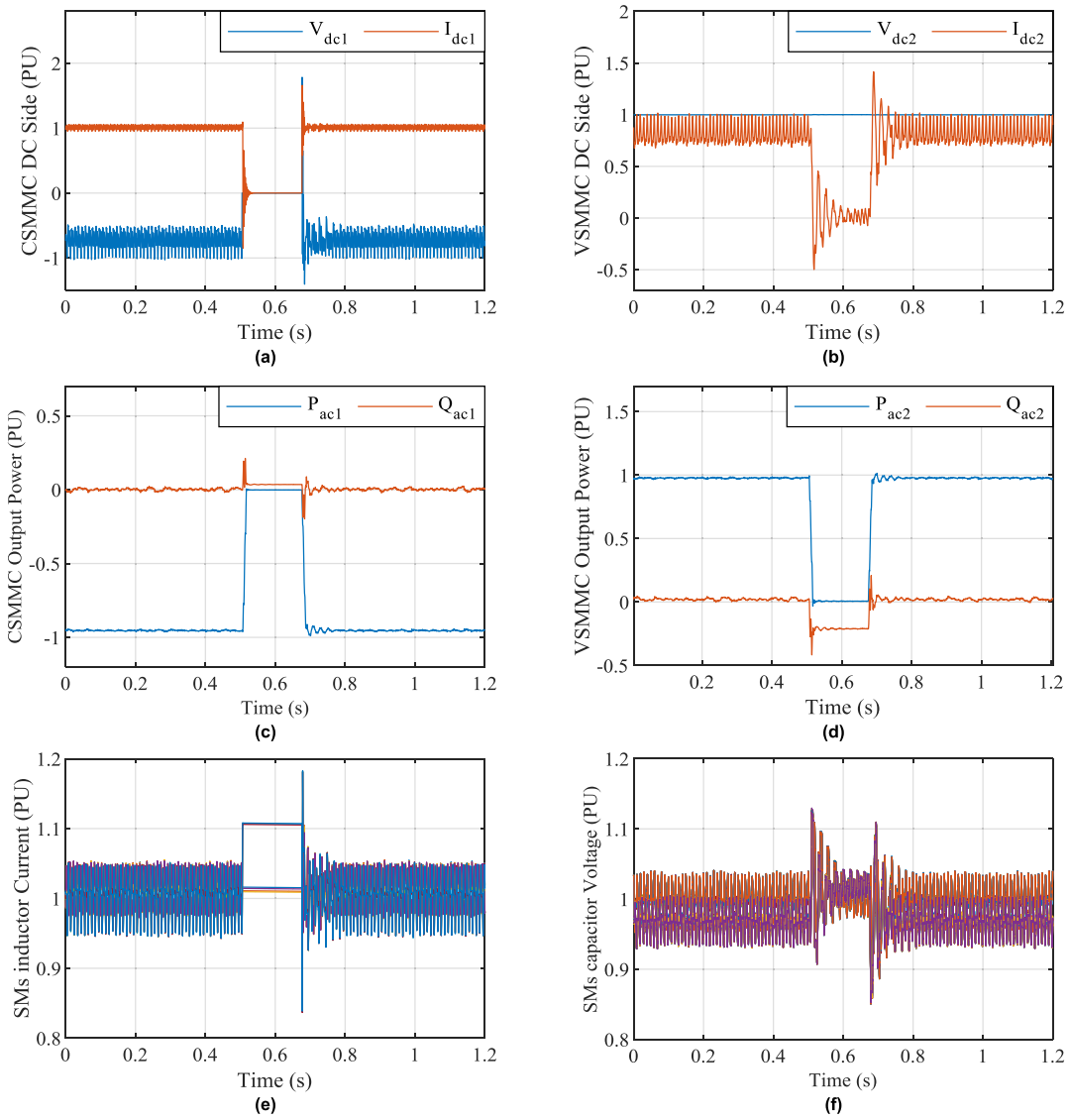

FIGURE 21. Performance of the proposed DC-DC converter during DC pole to pole fault at LCC network at t = 0.5s: (a) Power flow in CS-MMC, (b) Power flow in VS-MMC, (c) DC side of VS-MMC, (d) DC side of CS-MMC, (e) SM inductor current in one leg, and (f) SM capacitor voltage in one leg.

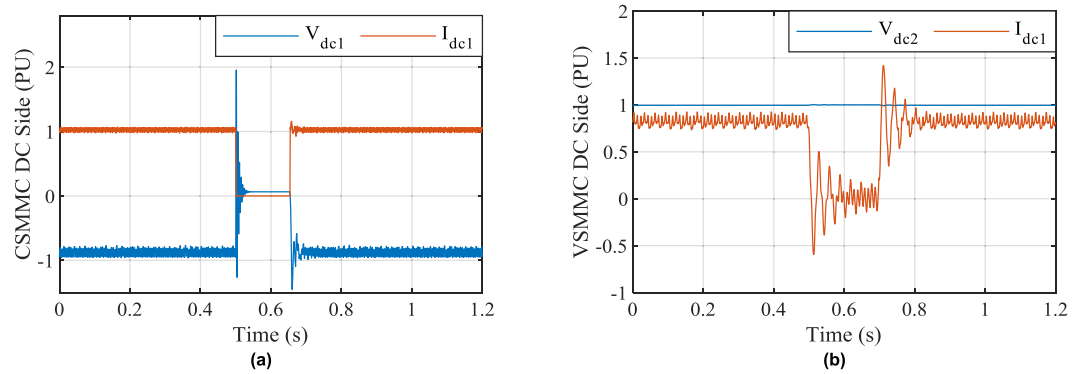

FIGURE 22. Performance of the proposed DC-DC converter during DC fault through resistance at LCC network at t = 0.5s: (a) DC side of CS-MMC and (b) DC side of VS-MMC.

network with the DC link of VS-MMC, the fault detection algorithm succeeds in detecting the fault. Fig. 24 parts (a) and (b) show the DC link voltages and currents of CS-MMC and VS-MMC, respectively. The fault occurs at t = 0.5s. After

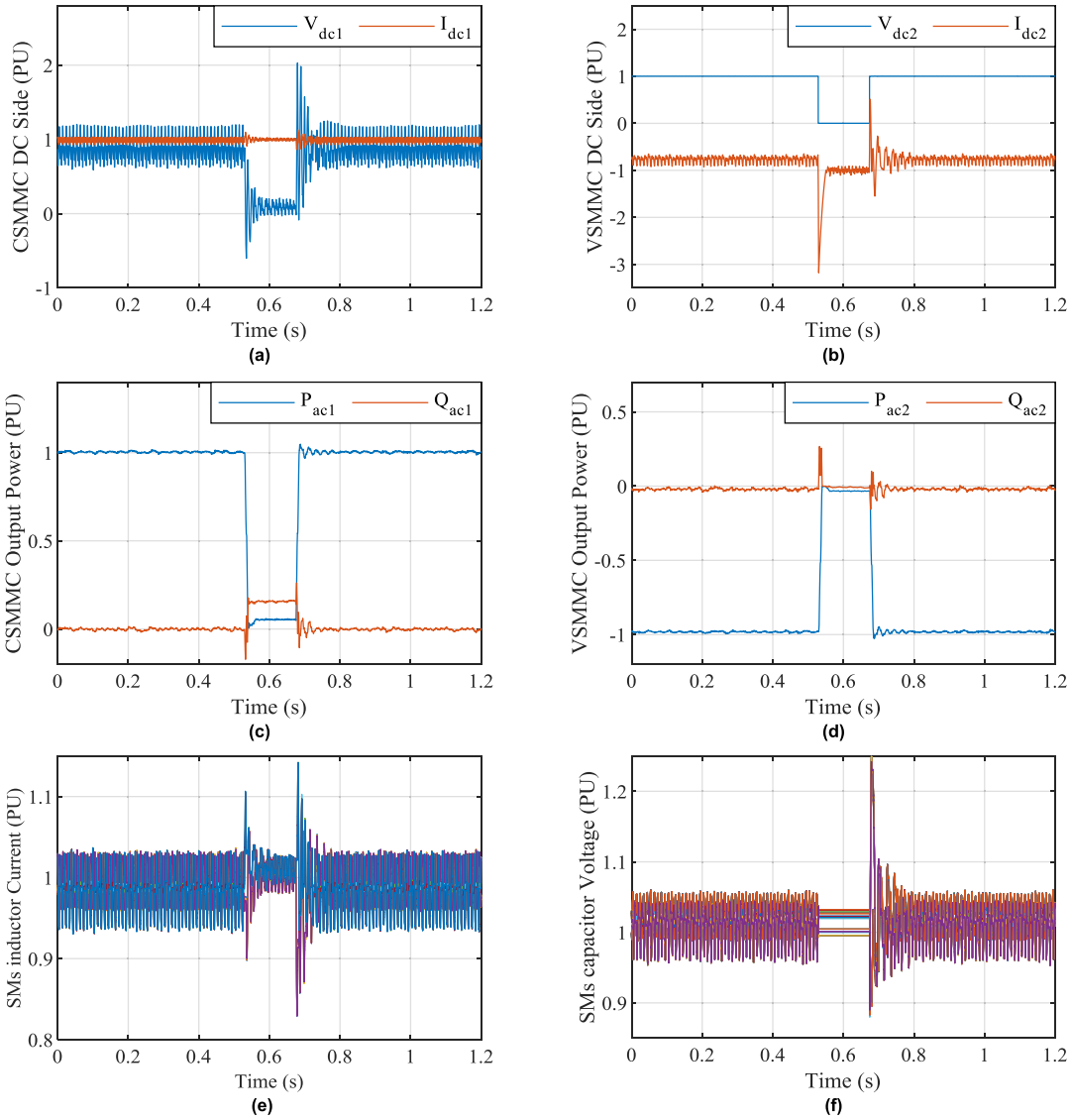

FIGURE 23. Performance of the proposed DC-DC converter during DC pole to pole fault at VSC network at t = 0.5s: (a) Power flow in CS-MMC, (b) Power flow in VS-MMC, (c) DC side of VS-MMC, (d) DC side of CS-MMC, (e) SM inductor current in one leg, and (f) SM capacitor voltage in one leg.

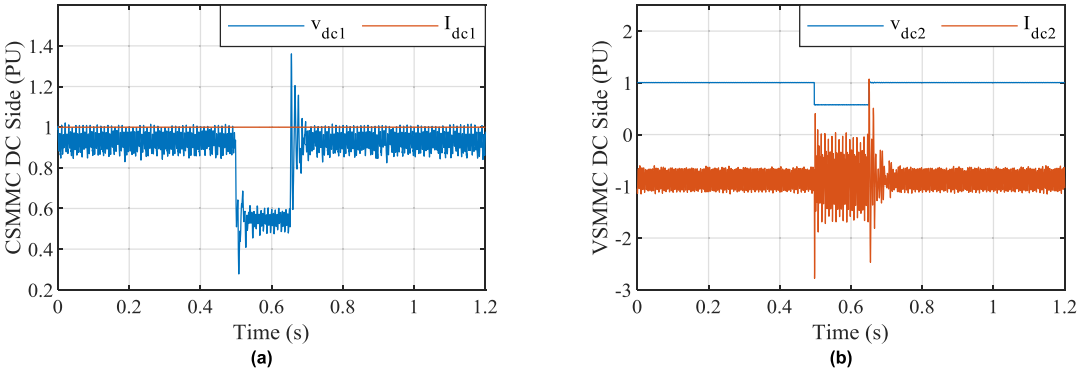

FIGURE 24. Performance of the proposed DC-DC converter during DC fault through resistance at VSC network at t = 0.5s: (a) DC side of CS-MMC and (b) DC side of VS-MMC.

fault detection, the DC link at CS-MMC exhibits reduction in voltage due to control action of blocking the VS-MMC and the same can be observed at the DC link voltage of VS-MMC. Based on obtained results, the proposed DC-DC converter

topology is fault tolerant during the fault at both converter sides.

VII. CONCLUSION

A new modular multilevel-based DC-DC converter has been proposed which provides the capability of connecting two different types of DC networks (LCC/VSC-based HVDC networks) operating at different voltage levels with full bidirectional power flow controllability. The detailed mathematical analysis of SM parameters selection has been discussed to provide a full system design with an acceptable range of SM voltage/current ripple. The active power flow between two different networks is controlled through two new control techniques. The first control technique provides simplicity and lower passive elements with zero reactive power at the rated active power. However, its major obstruction is the reactive power escalation during the active power deviation from the rated value; leading to higher losses and running cost. The second control technique ensures zero reactive power throughout the full active power flow range and guarantees lower losses as the power deviates from the rated power in comparison with the first control technique. However, the parameter size has to be increased up to at least three times compared to that of the first control technique. Control-Hardware-in-the-Loop (CHiL) has been used to validate the proposed hypothesis by studying both control techniques and different fault cases. Moreover, the proposed topology has been validated its capability to tolerate faults and providing DC protection zone isolation at both DC sides without the need to DC circuit breakers.

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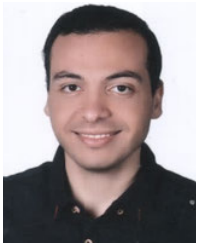

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