IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 22, 2021, accepted April 5, 2021, date of publication April 15, 2021, date of current version May 7, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3073416

A Family of High Step–Up DC–DC Converters With N_c Step-Up Cells and M–Source Clamped Circuits

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This work was supported in part by the Postgraduate Research and Practice Innovation Program of Jiangsu Province, under Grant KYCX18_0095, and in part by the Scientific Research Foundation of Graduate School of Southeast University, under Grant YBPY1877.

ABSTRACT In this paper, in order to study the relationship among different converters, a novel concept—modular high step-up converter—is proposed, which is composed of one basic converter, one N_c step-up cell (N_c-SUC), and one M-source passive lossless clamped circuit (PLCC). N_c means the number of capacitors in step-up cell and M-source represents the number of capacitors in PLCC. N_c-SUCs composed of many voltage lift cells (VLCs) and many constant voltage lift cells (CVLCs) are proposed and their general voltage gain formula is deduced. Each type of N_c-SUCs has N_c+1 different structures and the same voltage gain formula. Different N_c-SUCs can converse each other by adding or removing VLC and CVLC. Then, the general voltage gain formula of the proposed converters with N_c-SUCs is deduced, which is an additive combination of the voltage gain of N_c-SUCs and basic converter. Besides, a novel clamp circuit called M-source PLCC which is consisted of $M+1$ capacitors and one diode is presented. M capacitors of the M-source PLCC come from the N_c-SUC of converter, so only one capacitor and one diode are added. In comparison with classical PLCC, it makes the converters with N_c-SUCs not only possible to recycle the energy stored in the leakage inductor, but also further reduce the voltage stresses of the switch and the output capacitor, further improve the voltage gain, and even realize a three-level converter. Compared with the classical PLCC, the cost in M-source PLCC is unchanged. As M increases, the number and the variety of M-source PLCCs will also increase. Therefore, different M-source PLCCs can be chosen for the same converter to recycle the energy stored in the leakage inductor. If adopting converse thinking, based on the general voltage gain formula, removing basic converter and M-source PLCC, then, the number and the combination way of VLC and CVLC of different N_c-SUCs will expose the relationship among different high step-up converter to researcher. Finally, an improved converter based on 3-SUC as a representative of the deduced converters is proposed and analyzed in detail in the laboratory to verify performances.

INDEX TERMS Coupled inductor, asymmetric voltage multiplier cell, clamped circuit, dc-dc converters.

I. INTRODUCTION

Recently, owing to the shortage of fossil fuels and seriously environment pollution, the renewable energy sources, such as photovoltaic systems and fuel cell, have become increasingly popular [1]. Unfortunately, the low output voltage at the end of those applications limits their developing speed. In general, step-up converters have the ability to convert low voltage into high voltage. In theory, conventional Boost converter can achieve an infinitely voltage conversion ratio with extremely duty cycle, but the extremely duty cycle results in fearful conduction losses, serious diode reverse recovery problems and severe EMI [2], [3]. Besides, the voltage stresses of switch and diode are equal to output voltage so that the switch and the diode with large R_{ON} and high forward voltage drop are employed. In practice, the step-up voltage gain is limited by those factors.

The associate editor coordinating the review of this manuscript and approving it for publication was Chi-Seng Lam.

In order to overcome the defects above, various step-up converters have been widely studied [4]–[11]. Switched capacitor (SC) and switched inductor (SI) technologies have been researched and integrated into classical Boost converter to upgrade voltage conversion gain and efficiency [4]–[8]. As the number of SC cell increases, the voltage gain can be rapidly enhanced, but the active switch attacks from a big surge current so that its losses are added and the efficiency of the converters is decreased [5]–[7]. The converter can employ the inductor in SI cell to avoid serious current spike [8]–[11]. The voltage lift cell (VLC) transfers the energy of inductor to the intermediate capacitor to attain a high conversion ratio. Unfortunately, the volume is increased and the power density is decreased owing to the magnetic cores [8]. Nevertheless, the voltage and current stresses on the capacitor are high [9]–[11].

Flyback converter should be considered as a qualified candidate by adjusting the turns ratio for high voltage gain. But, active switch suffers from a severe voltage spike as the effect of leakage inductor, so that there is fearful switching dissipation. The converter with coupled inductor technique is similar to flyback converter. It can also increase voltage gain by modulating the turns ratio. Therefore, various converters successfully integrate that technique to achieve a high voltage conversion gain, including Boost converter, buck-boost converter, forward converter, flyback converter, and so on. In order to further increase voltage gain, VLC and coupled inductor technique are melded together [12], [13]. Compared with the converter in [12], there is a higher voltage gain in the converter in [13].

Furthermore, symmetric voltage multiplier cell (SVMC) can efficiently improve high voltage gain. Many converters with SVMC and coupled inductor are presented to further upgrade voltage gain [14]–[18] The SVMC is embedded directly in classical Boost converter [14], [15]. The only difference is that both of the converters adopted different passive lossless clamped circuits (PLCCs). Although the SVMC is also employed in [16], the location of the dotted terminal on the secondary side of coupled inductor is changed. In order to further increase voltage conversion ratio of converter, voltage multiplier cell (VMC) which fused SVMC with SC technique is employed by the two converters [17], [18]. The only difference is just the connection way of the clamped circuits. In order to improve efficiency, the energy stored in the leakage inductor must be absorbed to limit its effect on switch of the converter based on both coupled inductor and step-up cells. Usually, various step-up cells are combined with coupled inductor together to improve the voltage conversion ratio of converter. However, none of literature studied the relationship among different step-up cells.

In order to limit voltage spike on main switch because of leakage inductor, active clamped technique is introduced to absorb the energy stored in leakage inductor [12], [19], [20]. Zero voltage switching (ZVS) is realized by employing the technique, which improves the efficiency [19]. However, there is a discontinuous input current in this converter. In [12] and [20], that technique not only effectively imposes the voltage spike of main switch, but also realizes ZVS. The converter in [12] has the lower voltage gain, but there is the higher voltage gain in the converter in [20]. However, these converters even allow the input current to flow back to input source and their auxiliary switch is operated in hard switching. It is important that the technique results in increasing cost and complex control system.

PLCC can effectively restrict the effect of leakage inductor [13]–[18], [21]–[29]. Normally, PLCC is composed of one diode and one capacitor, and it is directly connected to both sides of the main switch or both sides of the primary side winding. The single switch Boost converters employed PLCC to connect directly to two sides of primary-side winding in [14], [16]–[18]. Although the voltage spike is restricted, there is a discontinuous input current and it can not help the converters to improve voltage gain. In another connection, switch realized soft-switching at turn-on, but there is still a discontinuous input current and it still can not improve their voltage gain [13], [15]. In [21]–[25], the sepic converters tried to integrate PLCC and VL cell to suppress voltage spike. Not only did those converters get to a continuous input current, but also PLCC improved their voltage gain. The converter in [21] adopts three-winding coupled inductor to realize bipolar outputs. The converters in [22] and [23] realize a small current ripple by the interleaved structure of inductors. In the dual switches converter, PLCC is integrated with SVMC and connected with the two sides of the primary-side winding for recycling the energy stored in leakage inductor [26]–[29]. Although the voltage conversion ratio is further increased in these converters, extra inductor must be added to realize continuous input current.

Compared to active clamped technique, the converters based on PLCC have an easier control system and the cost is reduced. However, the classical PLCC is difficult to accomplish a continuous input current and further improve voltage gain in the single switch Boost converter. Regardless of the selected type of PLCC to clamp the main switch, the most obvious feature is that the clamp capacitor is used to absorb the energy stored in the leakage inductor and must directly connect with the both sides of primary inductor or switch. It will restrict seriously the using PLCC for converter. Although clamped capacitor can be connected in series with output capacitor to reduce the voltage of output capacitor, the voltage of the clamped capacitor is far lower than the output voltage of step-up converter, so that the voltage of output capacitor is close to the output voltage and there is need for converter to choose the bulk power high-voltage rated electrolytic capacitor to reduce the voltage ripple. As output voltage increases, the power density of converter will severely be influenced by increasing volume of electrolytic capacitor [30].

In this paper, a modular combination concept is proposed for high-up converter, which is composed one basic converter, one N_c step-up cell (N_c-SUC), and one M-source PLCC. Then, N_c step-up cells consisted of many voltage lift

cells (VLCs) and many constant voltage lift cells (CVLCs) are proposed, and the relationship among different N_c-SUCs is revealed by the deduced general formula of the voltage gain. Then, N_c-SUCs are integrated into the basic Boost converter and the deduced general formula of their voltage gain is to show the relationship among the different converters. Moreover, a named M-source PLCC which is consisted of $M + 1$ capacitors and a diode is presented in order to recycle the energy stored in leakage inductor. If a converter employs M-source PLCC, M capacitors in this M-source PLCC are belong to its step-up cell so that only one extra capacitor is added. Therefore, the cost is same in comparison with the classical PLCC. If there are M capacitors in series in any converter, this converter may employ a variety of PLCCs from 0-source PLCC to M-source PLCC. Except for the 0-source PLCC, the other M-source PLCCs can be mixed into the converter by using different connection ways. As the number of series capacitors increases, the proposed converters will have more PLCCs. Besides, PLCC can further improve the voltage conversion ratio of the proposed converter and reduce the voltage stress of main switch. In addition, PLCC plays a major role in reducing the voltage and volume of output capacitor to improve the power density of converter and it make some proposed converters possible to become three-level converter. Finally, a novel converter as a representative of the deduced converters is analyzed to verify its performances.

II. FAMILY OF HIGH-GAIN DC–DC CONVERTERS STEMS

Usually, each step-up converter with coupled inductor is studied as an individual. Therefore, the relationship among different converters is ignored. A new concept named by modular combination of step-up converter with coupled inductor is proposed as shown in Fig.1. The picture shows that a step-up converter is consisted of one basic step-up converter, one N_c step-up cell (N_c-SUC), and one M-source PLCC. It is important to note that the three parts are independent individuals but they can reveal the relationship among different converters. For the basic step-up converters have been extensively studied, they will be not discussed here. Then, only the N_c-SUC and the M-source PLCC will be studied to show the relationship among different converters or different step-up cells.

A. STEP-UP CELLS

High Step-up cells are one of the most important components in the high conversion ratio converters to improve the voltage gain. Wherever in photovoltaic system or in fuel cell system, all kind of step-up cells can be found and used to improve voltage gain and other performances in [9]–[20]. Since the VLC in Fig.2 (a) and the SVMC in Fig.2 (c) are respectively presented in 2001 in [11] and 2011 in [14], the two cells or their improved cells are employed in various converters to further upgrade the performance of the converters in [9]–[20]. With the development of converter, asymmetric voltage multiplier cell (AVMC) is proposed in 2018, as shown

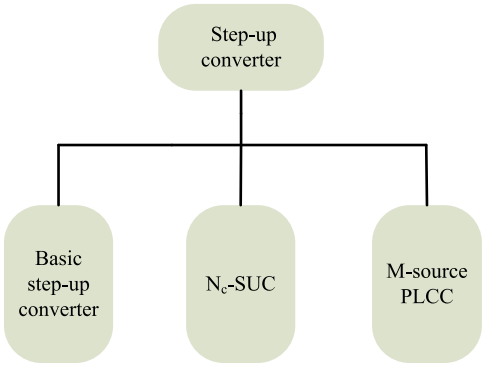

FIGURE 1. Modular combination diagram of step-up converter with coupled inductor.

in Fig.2 (d), which adopts two voltage asymmetry capacitors to realize high voltage gain [32]. However, until very recently, the relationship among different step-up cells is still unrevealed. In this section, the novel N_c-SUCs are proposed to reveal the relationship among different step-up cells.

According to the number of capacitor in step-up cell, all of the step-up cells are called by N_c step-up cell (N_c-SUC), as shown in Fig.2. N_c means the number of capacitor or the number of the transferring voltage of inductor L_2. The two principles are that one capacitor only charges one capacitor, and all capacitors in N_c-SUCs must improve the voltage gain of the step-up cell. In N_c-SUCs, the published step-up cells (Figs.2 (a), (c), (d), and (n)) and the novel step-up cells (the other cells) are composed of VLC and CVLC as shown in Fig.2, and the relationship among each cell will be descripted here. Fig.2 shows the derivation process of the different N_c-SUCs and the number of N_c-SUCs of the same type.

In the VL cell (VLC) as shown in Fig.2 (a), its capacitor connected in series with inductor L_2 directly improves the voltage gain of converter, and the voltage of this cell is not a constant (0 or $V_{L2}^{on} + V_{L2}^{off}$). A novel step-up cell called constant voltage lift cell (CVLC) is proposed as shown in Fig.2 (b). Compared with VLC, the voltage across this cell is a constant ($V_{L_2}^{off}$), and its capacitor indirectly increases the voltage gain of converter. Essentially, they are the same step-up cell, but try to improve the voltage gain in different ways. The other N_c-SUCs can be composed of many VLCs and many CVLCs by different series connection ways.

In Fig.2 (a), the number of capacitor is equal to 1, and when diode D_1 is turned on, the voltage $V_{L_2}^{on}$ of inductor L_2 is transferred into C_1 (that is $N_c = 1$). In Fig.2 (b), when diode D_1 is turned on the voltage $V_{L_2}^{off}$ of inductor L_2 is transferred into C_1, and N_c is also equal to 1. Usually, two different cells (Figs.2 (a) and (b)) have four different series connection ways by sharing an inductor, which respectively are a-a, a-b, b-a, and b-b. In 2-SUCs, Fig.2 (c) is SVMC [14], which is composed of two VLCs (a-a); Fig.2 (d) [32] and Fig.2 (e) are two AVMCs, which are composed of one VLC and one CVLC (a-b and b-a). Then, the combination b-b is in existence. Therefore, there are three different 2-SUCs.

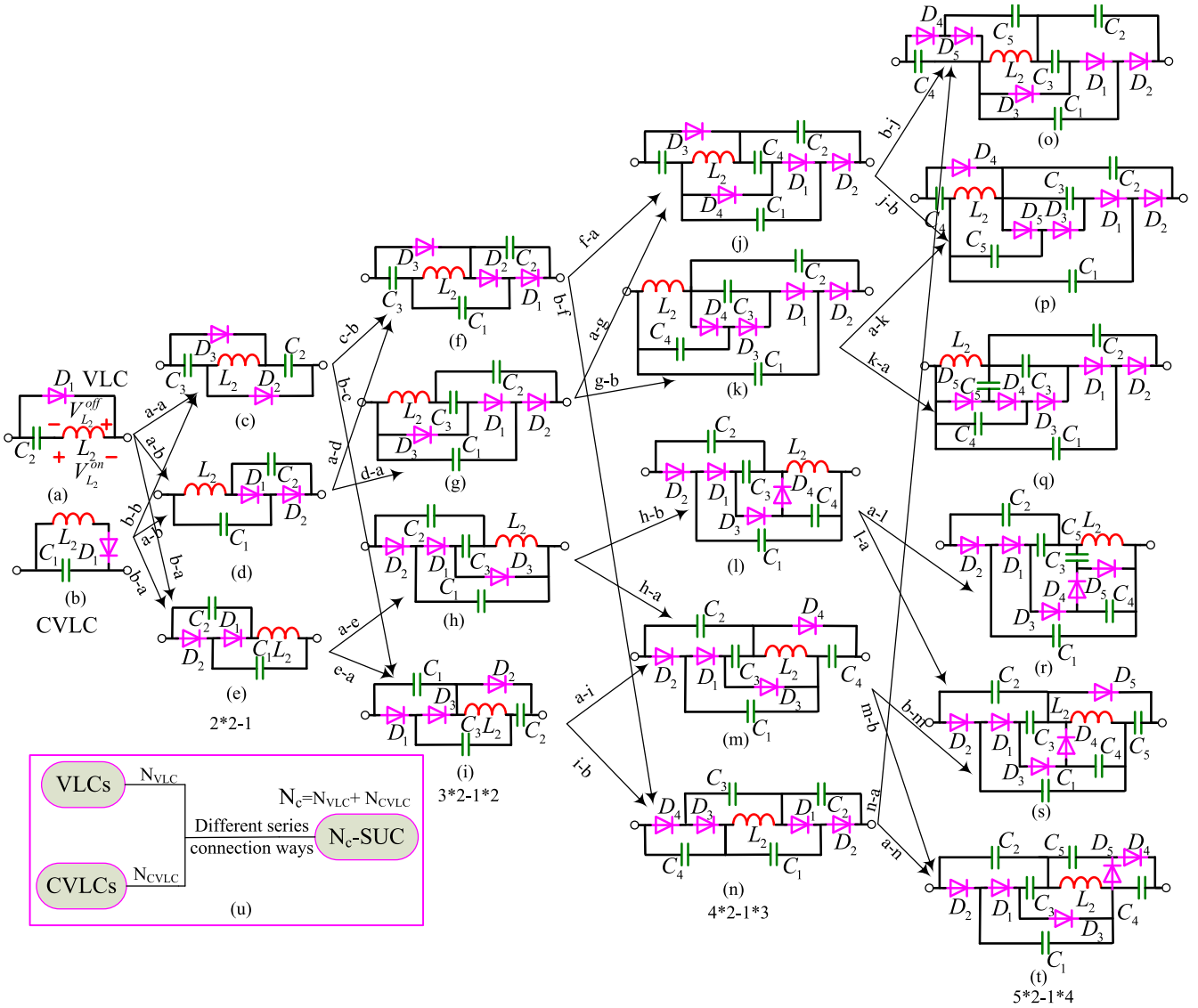

FIGURE 2. Relationship among different step-up cells. (a)-(t) Different Nc-SUCs (u) Modular combination diagram of Nc-SUCs.

Similarly, one 3-SUC is composed of one 2-SUC and one VLC or one 2-SUC and one CVLC by sharing an inductor as shown in Figs.2 (f)-(i). The 2-SUC as shown in Fig.2 (c) and the CVLC as shown in Fig.2 (b) only can structure two different 3-SUCs by two different series connection ways, as shown in Figs.2 (f) and (i), respectively. In Fig.2 (f), the capacitor C_1 of the CVLC charges C_2 of Fig.2 (c). Besides, in Fig.2 (i), the capacitor C_1 of the CVLC charges another capacitor C_3 of Fig.2 (c). Then, Fig.2 (c) can not combine with the VLC to structure 3-SUC. Fig.2 (d) and the VLC can form the 3-SUCs by two different series connection ways as shown in Figs.2 (f) and (g), respectively. Similarly, Fig.2 (e) in combination with the VLC can form two different 3-SUCs as shown in Figs.2 (h) and (i), respectively. Each 2-SUC in series with one CVLC or one VLC can structure two different 3-SUCs (3*2), and the two 3-SUCs as shown in Figs.2 (f) and (i) seem to appear twice. Therefore, the total number of 3-SUCs is the number of 2-SUCs (3) multiplies by the number of 1-SUCs (2) minus the number of the repeated 3-SUCs ($3*2-2=4$). Besides, one 3-SUC is also composed of one CVLC and two VLCs by sharing an inductor as shown in Table 1. Fig.2 (u) shows the modular combination diagram of Nc-SUCs, in which any of Nc-SUC can be composed of N_{VLC} VLCs in series with N_{CVLC} CVLCs. Where N_{VLC} and N_{CVLC} mean the number of VLC and CVLC, respectively. In N-SUCs, the total number of each type of N_c-SUCs is equal to N_c+1 ($N_c^*2-(N_c\text{-}1)$, $N_c=1,2,3\ldots$), where N_c means the number of capacitor in N_c -SUC. Besides, when $N_c=2$, the repeated 2-SUC which is composed of two CVLC (b-b) is defined as in Fig.2 (c). Therefore, based on the combination between VLC and CVLC, the relationship among different N_c-SUCs can be established by this formula.

Based on Fig.2 and Table 1, as a gross generalization, the following conclusions are obtained:

1) When $N_c \geq 2$, the number of VLC is greater than or equal to the number of CVLC. In N_c-SUCs ($N_c \geq 2$), their voltage gain are equal to $N_{VLC}V_{L2}^{on}+(N_{CVLC}+1)V_{L2}^{off}$. Where N_{VLC} and N_{CVLC} respectively mean the number of VLC and CVLC, and V_{L2}^{on} and V_{L2}^{off} respectively denote the voltage of L_2 when the inductor L_2 stores energy or releases energy.

2) Any of N_c-SUCs can be composed of 1-SUC to (N_c-1)-SUC by different combination modes. For example, take the case of the 5-SUC, it can be composed of three VLCs and two CVLCs, or two 2-SUCs and one 1-SUC, or one 3-SUC and one 2-SUC, or one 3-SUC and two 1-SUCs, or one 4-SUC and one 1-SUC. Besides, when N_c is an odd number under $N_c > 1$, the same type of N_c-SUCs have the same voltage gain and different structures. When $N_c$is an even number, the same type of N_c-SUCs have different voltage gain and different structures. The number of each type of N_c-SUCs is equal to $N_{VLC}+N_{CVLC}+1$ (N_c+1). Besides, the number of the capacitors of N_c-SUC is equal to N_c.

B. ALL KIND OF STEP-UP cONVERTERS

The step-up converters can be composed of the basic converters (Boost, Buck-Boost, Sepic and so on) and the Nc-SUCs as shown in Fig.1. Some of these converters, namely the converters in Figs.3 (a), (c), (d), (n), have been respectively published in [33], [34], [32], [17]. Besides, the other converters in Fig.3 are firstly proposed. Similarly, this ideal can be applied to other type of the basic converters in [35], [36], and [37]. Table 2 shows the relationship among different the converters with Nc-SUCs under continuous conduction mode (*CCM*) operation.

Based on Fig.3 and Table 2, Figs.3 (d) and (e) are the same type of different converters, they have the same voltage gain, as shown in Table 2, even the voltage stress of switch, operation mode and so on. Besides, other converters, such as Figs.3 (f)-(i), Figs.3 (j) and (m), Figs.3 (k) and (l), and so on, can be respectively seen as the same converter to be studied, because their voltage gain are the same. Therefore, for the different type of converters with the same type of N_c-SUCs, the only difference in their voltage gains is that the voltage gain of the basic converters is different. For different type of converters with different type of N_c-SUCs, the difference is merely that the voltage gains of the basic converters and the number of VLC and CVLC are different. In order to save space, the other type of step-up converters composed of the other basic converters and the Nc-SUCs are not shown here.

One common feature of the converters in Fig.3 is that the N_c-SUCs are inserted between switch S and output diode D_o. Based on Table 2, when $N_c \geq 2$ the general output voltage formula is $V_{basic}+N_{VLC}V_{L2}^{on}+(N_{CVLC}+1)V_{L2}^{off}$ under *CCM*. Where V_{basic} means the output voltage of the basic converters. Based on the general formula, it can be seen that the output voltage of N_c-SUCs is directly superimposed on that

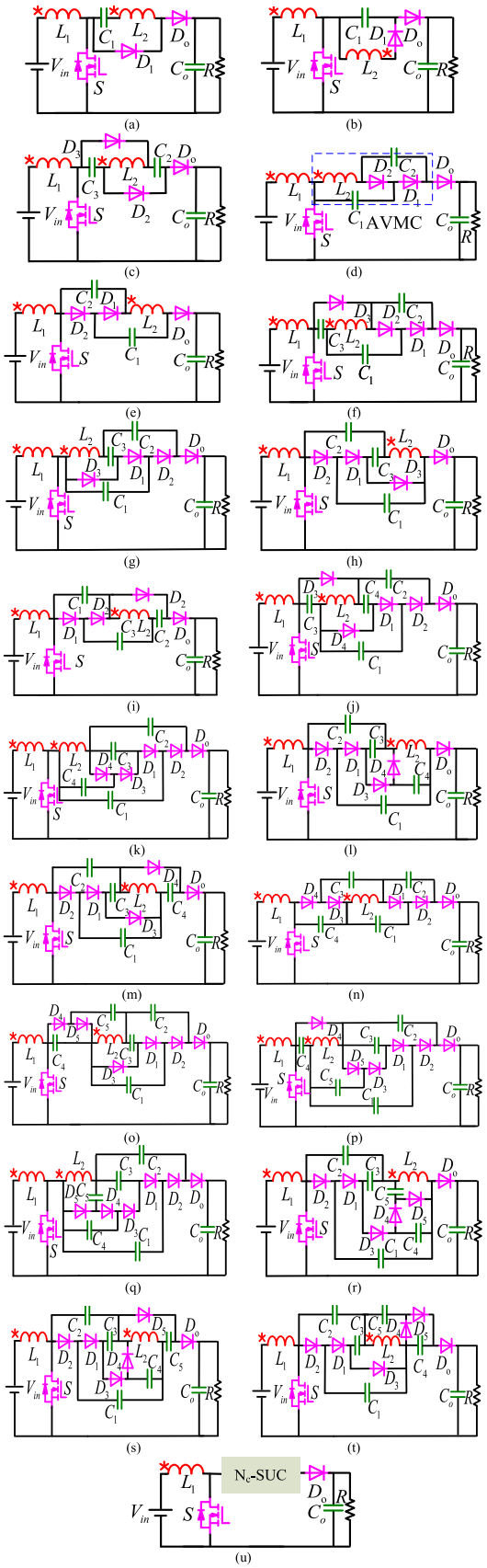

FIGURE 3. Boost topologies.

TABLE 1. Relationship among different sep-up cells.

	Topology	No. of VLCs	No. of CVLCs	No. of 2-SUCs	No. of 3-SUCs	No. of 4-SUCs	Output Voltage	N_c
1-SUC	Fig.2(a)	1	0				$V_{L2}^{on}+V_{L2}^{off}$	1
	Fig.2(b)	0	1				V_{L2}^{off}	1
2-SUC	Fig.2(c)	2	0				$2V_{L2}^{on}+V_{L2}^{off}$	2
	Figs.2 (d) and (e)	1	1				$V_{L2}^{on}+2V_{L2}^{off}$	2
3-SUC	Figs.2 (f), (g), (h) and (i)	2	1	1(1)			$2V_{L2}^{on}+2V_{L2}^{off}$	3
4-SUC	Figs.2 (j) and (m)	3	1	2	1(1)		$3V_{L2}^{on}+2V_{L2}^{off}$	4
	Figs.2 (k), (l) and (n)	2	2	2	1(1)		$2V_{L2}^{on}+3V_{L2}^{off}$	4
5-SUC	Figs.2(o), (p), (q), (r), (s) and (t)	3	2	2(1)	1(2/1)	1(1)	$3V_{L2}^{on}+3V_{L2}^{off}$	5
N_c-SUC (N_c>1)	Fig.2	N_{VLC}	N_{CVLC}				$N_{VLC}V_{L2}^{on}+(N_{CVLC}+1)V_{L2}^{off}$	N_{VLC}+ N_{CVLC}

TABLE 2. Relationship among different the converters with Nc-SUCs under CCM.

Topology	No. of VLs	No. of CLCs	Voltage gain of Boost converters	Nc
Fig.3 (a)	1	0	$V_{in}/(1-D)+V_{L2}^{on}+V_{L2}^{off}=V_{in}/(1-D)+NV_{in}+NDV_{in}/(1-D)$	1
Fig.3 (b)	0	1	$V_{in}/(1-D)+V_{L2}^{off}=V_{in}/(1-D)+NDV_{in}/(1-D)$	1
Fig.3 (c)	2	0	$V_{in}/(1-D)+2V_{L2}^{on}+V_{L2}^{off}=V_{in}/(1-D)+2NV_{in}+NDV_{in}/(1-D)$	2
Figs.3 (d) and (e)	1	1	$V_{in}/(1-D)+V_{L2}^{on}+2V_{L2}^{off}=V_{in}/(1-D)+NV_{in}+2NDV_{in}/(1-D)$	2
Figs.3 (f), (g), (h), and (i)	2	1	$V_{in}/(1-D)+2V_{L2}^{on}+2V_{L2}^{off}=V_{in}/(1-D)+2NV_{in}+2NDV_{in}/(1-D)$	3
Figs.3 (j) and (m)	3	1	$V_{in}/(1-D)+3V_{L2}^{on}+2V_{L2}^{off}=V_{in}/(1-D)+3NV_{in}+2NDV_{in}/(1-D)$	4
Figs.3 (k), (l), and (n)	2	2	$V_{in}/(1-D)+2V_{L2}^{on}+3V_{L2}^{off}=V_{in}/(1-D)+2NV_{in}+3NDV_{in}/(1-D)$	4
Figs.3 (o), (p), (q), (r), (s) and (t)	3	2	$V_{in}/(1-D)+3V_{L2}^{on}+3V_{L2}^{off}=V_{in}/(1-D)+3NV_{in}+3NDV_{in}/(1-D)$	5
Converters with N_c-SUC (N_c>1)	N_{VLC}	N_{CVLC}	$V_{basic}+N_{VLC}V_{L2}^{on}+(N_{CVLC}+1)V_{L2}^{off}$	N_{VLC}+ N_{CVLC}

Where D and N mean duty cycle and turns ratio, respectively.

of the basic converters. Therefore, their voltage gain can be expressed as $[V_{basic}+N_{VLC}V_{L2}^{on}+(N_{CVLC}+1)V_{L2}^{off}]/V_o$. It means that one high step-up converter can be structured by superimposition of one basic converter and one Nc-SUC and the relationship among different converters depend on the type of basic converter and the number of VLC and CVLC. So, the deduction process and the relationship among different converters can be established by increasing or decreasing the number of the VLC and CVLC, and replacing the basic converter.

C. M-SOURCE PASSIVE lOSSLESS CLAMPED CIRCUIT

The leakage inductor results in high voltage spike on the switch in converters based on coupled inductor so that the efficiency is seriously decreased. Therefore, the clamped circuit must be integrated into these converters to suppress the voltage spike on switch. The characteristic of the classical passive lossless clamped circuit in [30] is that there is a capacitor and a diode, which are directly connected either on the both sides of the switch or on the both sides of the primary winding of the coupled inductor. Unfortunately, the use of classic passive lossless clamp circuit is limited by its connection way. This point will be illustrated behind.

To expand its applicable scope to meet the requirement of any converter based on coupled inductor, three novel clamp ways called M-source PLCC which is consisted of M + 1 capacitors and one diode are proposed to suppress voltage spike and reduce voltage stress on devices as shown in Fig.4. M means the number of voltage sources, which can be considered as a fixed voltage network, such as single capacitor network or multiple capacitor network.

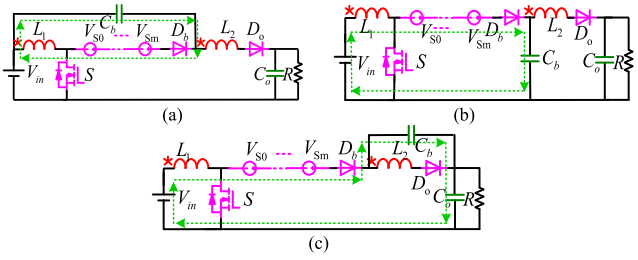

FIGURE 4. M-source passive lossless clamped circuit.

In the M-source passive lossless clamped circuit, only one extra capacitor and one extra diode are added and its essence is that the voltage sources are connected in series

with the classical passive lossless clamped circuit, and then the M-source passive lossless clamped circuit is connected in parallel with the switch to clamp the voltage of this switch. Compared with the traditional PLCC, the major difference of the M-source PLCC is that there are many voltage sources between the primary-side of the coupled inductor and the clamped diode. So its clamped capacitors are more than one. Another distinction is that the classical clamped capacitor is only used to absorb energy of leakage inductor; however, the clamped capacitors in M-source PLCC not only absorb energy from leakage inductor but also create a flowing way to transfer the energy. Furthermore, as one of the key parts of the modular step-up converter with coupled inductor, M-source PLCC is a general construction.

D. FAMILIES OF BOOST CONVERTERS WITH M-SOURCE PASSIVE LOSSLESS CLAMPED CIRCUIT

In this part, some of the aforementioned Boost converters with N_c-SUCs integrate with M-source PLCC as examples to show how these converters combine with M-source PLCC to suppress the voltage spike on the switch and reduce the voltage stress on output capacitor and switch, as shown in Figs. 5, 6, and 7.

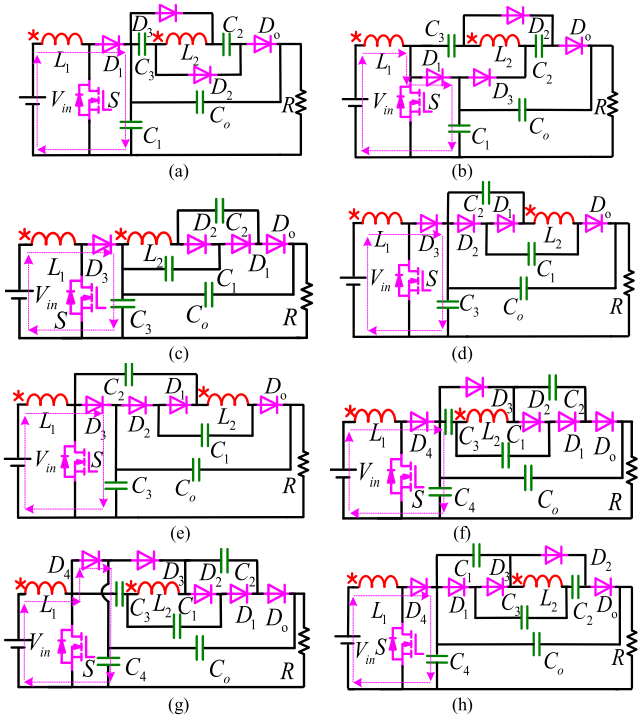

FIGURE 5. A family of boost converters with 0-source PLCC.

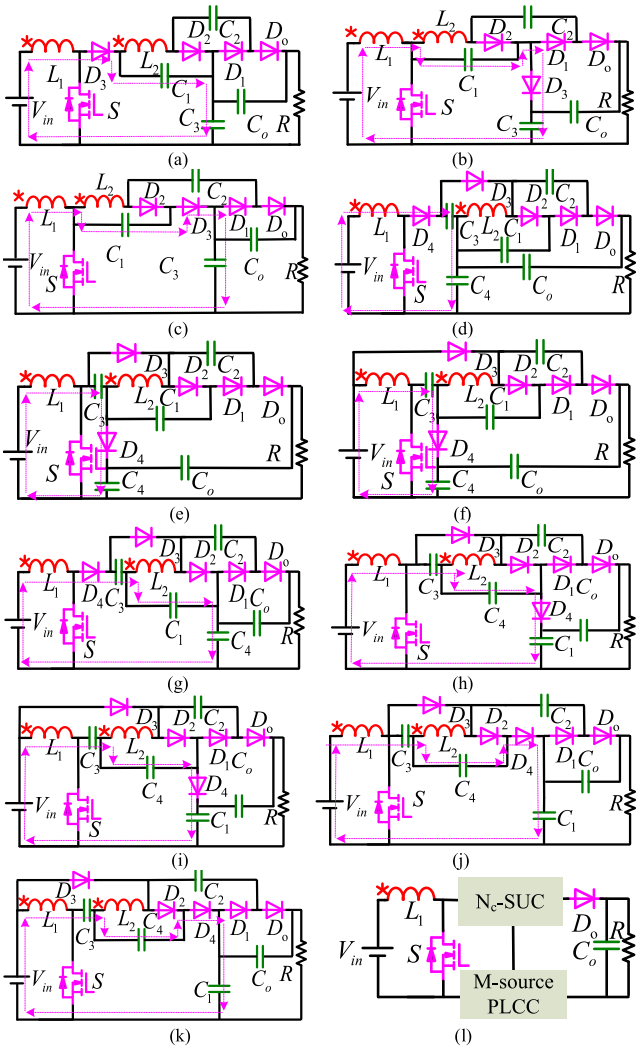

FIGURE 6. A family of boost converters with 1 or 2-source PLCCs.

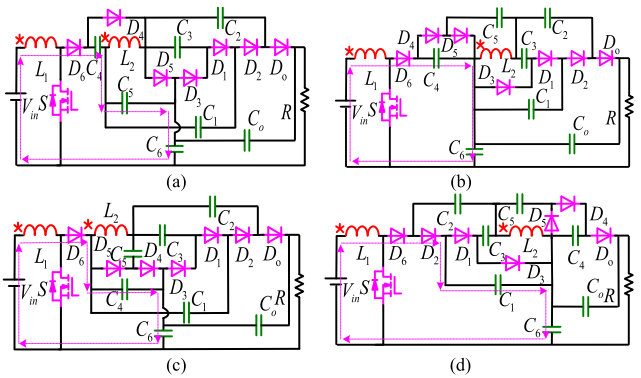

FIGURE 7. A family of three-level boost converters with 1 or 2-source PLCCs under N = 1.

When M = 0, Fig.5 shows how to employ 0-Source PLCC (classical PLCC) and improve voltage gain in the Boost converters based on N_c-SUCs. Then their output capacitor C_o is connected in series with the clamped capacitor of 0-source PLCC to reduce the voltage stress on the output capacitor C_o. Then, a family of Boost converters with 1-source or 2-source PLCC is shown in Fig.6 to further decrease the voltage stress on the output capacitor and increase the voltage gain. Finally, based on 5-SUCs, a family of Boost converters achieves the three-level voltage between output capacitor and clamped capacitor as shown in Fig.7.

Based on Figs.4, 5, 6, and 7, in M-Source PLCCs, there are M + 1 capacitors in series, which are connected in parallel

TABLE 3. Comparison among the converters based on Nc-SUCs under CCM.

Topology	Voltage stress of active switch (clamped diode)	No. of clamped capacitors	No. of clamped diodes	No. of diodes (capacitors)	Output capacitor voltage	Voltage gain
Fig.5(a)	V_o/A_1	1	1	4	$(A_1-1)V_o/A_1$	$A_1/(1-D)$
Fig.5(b)	$V_o/(1+A_1)$	1	1	4	$A_1V_o/(1+A_1)$	$(1+A_1)/(1-D)$
Fig.5(c) and (d)	V_o/A_2	1	1	4	$(A_2-1)V_o/A_2$	$A_2/(1-D)$
Fig.5 (e)	$V_o/(1+A_2)$	1	1	4	$V_oA_2/(1+A_2)$	$(1+A_2)/(1-D)$
Fig.5 (f) and (h)	$V_o/(2N+1)$	1	1	5	$2NV_o/(2N+1)$	$(2N+1)/(1-D)$
Fig. 5 (g)	$V_o/(2N+2)$	1	1	5	$(2N+1)V_o/(2N+2)$	$(2N+2)/(1-D)$
Fig.6(a) and (b)	V_o/A_2	1	1	4	NV_o/A_2	$A_2/(1-D)$
Fig.6 (c)	$V_o/(1+A_2)$	1	1	4	$(1+N)/(1+A_2)$	$(1+A_2)/(1-D)$
Fig.6 (d) and (e)	$V_o/(2N+1)$	1	1	5	$N(D+1)V_o/(2N+1)$	$(2N+1)/(1-D)$
Fig.6 (f)	V_o/A_5	1	1	5	$(A_2-1)V_o/A_5$	$A_5/(1-D)$
Fig.6 (i)	V_o/A_5	1	1	5	NV_o/A_5	$A_5/(1-D)$
Fig.6 (g),and (h)	$V_o/(2N+1)$	1	1	5	$NV_o/(2N+1)$	$(2N+1)/(1-D)$
Fig.6 (j)	$V_o/(2N+2)$	1	1	5	$V_o/2$	$(2N+2)/(1-D)$
Fig.6 (k)	$V_o/(A_5+1)$	3	1	5	$(N+1)V_o/(A_5+1)$	$(A_5+1)/(1-D)$
Fig.7 (a)-(d)	$V_o/(3N+1)$	1	1	7	$2NV_o/(3N+1)$	$(3N+1)/(1-D)$

where $A_1=2N+1-ND$, $A_2=N+1+ND$, $A_3=3N+1-ND$, $A_4=1+ND+2N$, $A_5=2+2N-D$, $A_6=2+3N-ND-D$, and D and N mean duty cycle and turns ratio, respectively

with the both sides of the switch or the both sides of the primary-side of the coupled inductor. M capacitors are used to establish a branch to release the energy stored in leakage inductor, and only one capacitor is used to store the energy. Only one extra capacitor is added so the cost is the same under different M-Source PLCCs, and the other capacitors belong to N_c-SUCs. M-Source PLCCs can be divided into two types: directly passive lossless clamped circuit (DPLCC) and indirectly passive lossless clamped circuit (IPLCC).

Fig.5 shows the Boost converters based on 0-Source PLCC. The converters in Figs.5 (a), (b), and (c) have been respectively published in [34], [38], [32], and the other converters are firstly proposed in order to employ 0-Source PLCC. The pink dashed line indicates the loop direction of releasing the leakage energy in Figs. 5, 6 and 7. The converters in Figs. 5 (a), (c), (d), (f), and (h) employ the DPLCC, and the others employ the IPLCC. For example, in the Boost based on SVMC in Fig.5 (a), the DPLCC is composed of D_1 and C_1, and it has no effect on the voltage gain; although the IPLCC is also consisted of D_1 and C_1 in Fig.5 (b), it can further improve the voltage gain of the converter, as shown in Fig.8 (a). In 0-Source PLCC, the precondition of existing the IPLCC is that there must be a capacitor between the switch and the secondary-side of the coupled inductor. Therefore, the Boost converter based on AVMC can not employ the IPLCC to increase its voltage gain, because there is no capacitor between the switch and the secondary-side of the coupled inductor. The Similar problem also happens in the Boost converters based on the step-up cells as shown in Figs.3 (g), (k), and (q). Therefore, 0-Source PLCC may limit the converters to further improve the voltage gain, for the clamped capacitor in 0-Source PLCC is must directly connected either on the sides of the switch or on the sides of the primary winding of the coupled inductor. To summarize, the difference between the DPLCC and the IPLCC in 0-Source PLCC in the same topology circuit is that the DPLCC can not improve the voltage gain of converter but the IPLCC may improve the voltage gain of converter. Unfortunately, the application of the IPLCC is limited by that precondition. Besides, based on Fig.5 and Table 3, compared with the DPLCC, the IPLCC can not reduce the voltage stress of the output capacitor for the same converter, but increase its voltage stress.

Based on Figs. 5, 6, and 7, compared with 0-Source PLCC, in the M-Source PLCCs under M > 0, the clamped capacitor used to absorb the energy is far away from the switch or the primary-side of the coupled inductor. Besides, whether in 0-Source PLCC or in the other M-Source PLCCs, the number of the additional components of them is the same so the cost is the same. The main advantages of the M-Source PLCCs under M > 0 are shown as follows:

1) The 1-Source DPLCC is employed in Figs.6 (a) and (d). In the converter with AVMC in Fig.6 (c), the 1-Source IPLCC is employed, which is consisted of two capacitors (C_1 and C_3) and one diode (D_3). Based on Table 3 and Fig.8, they realize a continuous input current and further reduce the voltage stress on switch and output capacitor as shown in Figs.8 (a) and (c) in comparison with those of the corresponding converters with 0-Source PLCC. Besides, Fig.6 (b) shows that the 1-Source IPLCC can further increase the voltage gain as shown in Fig.8 (a) and in the M-Source PLCCs M > 0 the restricted condition of the IPLCC is eliminated.

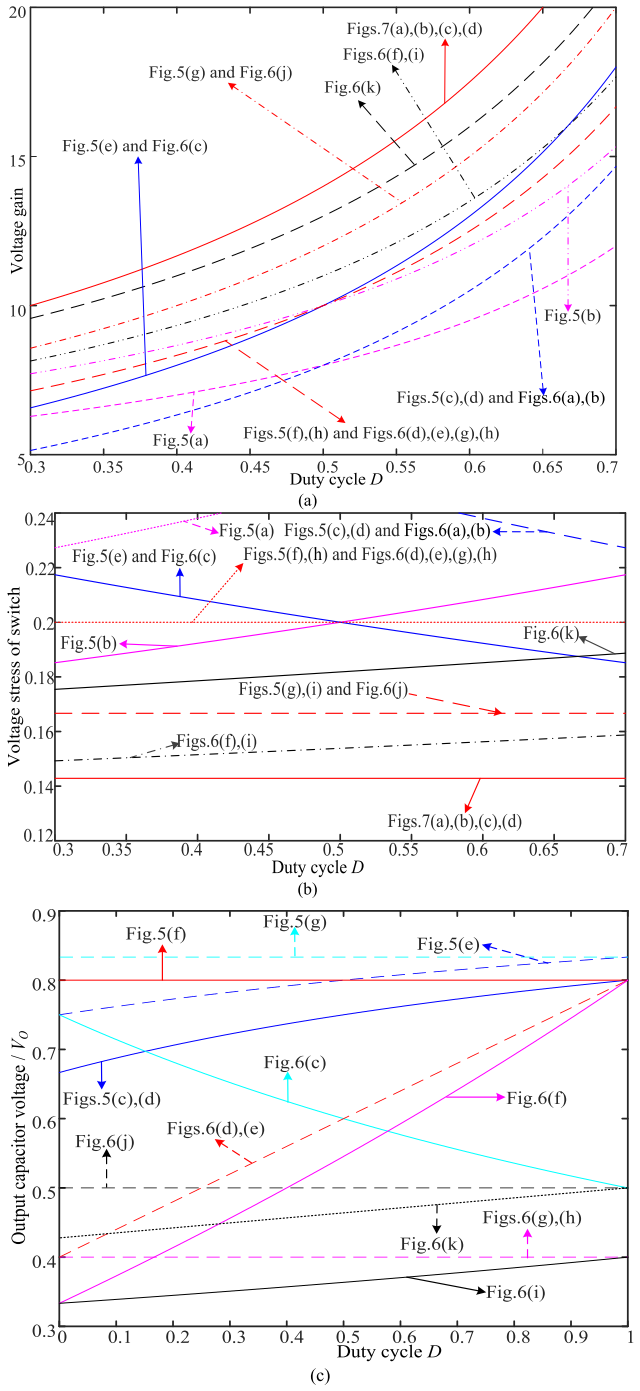

FIGURE 8. Comparative analysis among converters under N = 2.

Therefore, the 1-Source IPLCC can eliminate the restriction of improving voltage gain caused by the connection way in 0-Source PLCC.

2) In the M-Source PLCCs, as M increases, the voltage stress of output capacitor and switch of these converters is more effectively decreased, and the voltage conversion ratio and the number of the converters and the connection ways of M-source PLCCs are further increased. The converters in Figs.5 (f) and (g) and Figs.6 (d)-(k) are taken as an example to further reveal how the deduction process improves their performances. In Fig.6, the converters in Figs.6 (d)-(f) employ 1-Source PLCC, and the others employ 2-Source PLCC. In the converters based on 0-Source PLCC, 1-Source PLCC, and 2-Source PLCC, their voltage gains are gradually increased as shown in Fig.8 (a). And their 1 or 2-Source PLCCs have three or five connection ways respectively, so that they are more flexible. In the converters based on 0-Source PLCC, 1-Source PLCC, 2-Source PLCC, the voltage stress on the output capacitor is decreased gradually as shown in Fig.8 (c). And the voltage stresses of the clamped capacitor (C_1) and the output capacitor (C_o) of the converter in Fig.6 (j) are equal to half of the output voltage so that it is a three-level converter as shown in Table 3. Besides, in Fig.7, a family of Boost converters with 1 or 2-Source PLCCs integrated with 5-SUCs is proposed. Based on Table 3, the voltage stress on the output capacitor of the converters in Fig.7 is the same and equal to $2NV_o/(3N+1)$. When $N=1$, the voltage stress is exactly equal to half of the output voltage so that these converters belong to three-level converter.

Based on Table 3 and Figs. 5, 6, 7, and 8, some conclusions can be summarized as follows:

1) As M increases, the voltage of output capacitor in these converters is more effectively decreased so that the volume of this capacitor can be effectively downgraded.

2) As M increases, the number of the converters and the connection ways of M-source PLCCs are increased, so that the converters have more different structures to employ PLCC to recycle the energy stored in leakage inductor.

3) As M increases, M-source PLCC may further upgrade voltage conversion ratio and reduce the voltage stress on the switch.

4) For the same converters with N_c-SUCs, M-source PLCCs may help them realize three-level voltage between output capacitor and clamped capacitor.

5) A continuous input current can be realized.

Fig.6 (l) shows the generalized high step-up converter based on N_c-SUC and M-Source PLCC. With converse thinking, the clamped circuit is removed in high step-up converter, then, the using general voltage gain formula can reveal the similarity and difference among the converters. In summary, a high step-up converter with coupled inductor can be composed of one basic converter, one Nc-SUC composed of VLC and CVLC, and M-source PLCC. As a representative, the converter in Fig.6 (k) is analyzed in detail, because compared with that of the others, it has better performances, including the higher voltage gain, lower voltage stresses of switch and output capacitor, and so on.

III. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

Usually, the output voltage at the end of the PV panel is less than 50V, therefore, step-up converter is required to convert the low voltage to high voltage (400V) to DC bus. However, the lifetime of PV system is seriously affected by the grid-connected invert. Unfortunately, the lifetime of the

grid-connected invert is determined by the output capacitor of step-up converter. In step-up converter, electrolytic capacitor is selected as output capacitor, but its lifetime is short. For the proposed converters based on N_c-SUCs and M-source PLCCs can efficiently reduce the voltage across the output capacitor, the proposed converters can be used to improve the lifetime of PV system.

The circuit configuration of the proposed converter is shown in Fig.6 (k). This presented converter adopts 2-source PLCC, which is composed of capacitors C_1, C_3, C_4 and diode D_4. The equivalent circuit of the proposed converter is shown in Fig. 11. The coupled inductor is modeled as a magnetizing inductor L_M, a primary leakage inductor L_{K_1}, a secondary leakage inductor L_{K_2} and an ideal transformer whose turns ratio is $N = N_2 : N_1$. In order to simplify the circuit analysis of the converter, some assumptions are considered as follows:

1) All capacitors are sufficiently large so that the voltages on them are considered to be constant in one switching period.

2) The voltage drops across switch and diodes are all zero when they are turned ON, and the parasitic components of the switch and diodes are neglected.

3) The coupling coefficient K of the coupled inductor is equal to $L_M / (L_M + L_{K_1})$.

Based on the aforementioned assumptions, there are seven intervals in the proposed converter in one switching period under the continuous conduction mode (*CCM*) operation. Some typical waveforms of the proposed converter are illustrated in Fig.10. The current-flow path for each stage is depicted in Fig.11. The operating principle is described below in more detail.

$[t_0, t_1]$: As shown in Fig.11 (a), the switch S is turned ON at $t = t_0$. The diodes D_2 and D_o are turned ON, while the other diodes are turned OFF. The currents of the magnetizing inductor and the leakage inductor of the primary-side are increased almost linearly by the input voltage source V_{in}. The capacitor C_4 in 2-source PLCC is charged by the secondary-side winding because of the freewheeling current flowing through the leakage inductor of the secondary-side. As the current of the leakage inductor of the secondary winding decreases to zero, the diodes D_2 and D_o are turned OFF and this operation ends.

$[t_1, t_2]$: During this interval, the switch S keeps on. The diode D_1 is turned ON at $t = t_1$. The other diodes are turned OFF. The current-flow path is shown in Fig.11 (b). The primary-side winding is still charged by the input voltage source V_{in}. The capacitors C_2 and C_3 in series are charged by the secondary winding and the capacitor C_1. Therefore, the capacitor C_1 as the member of 2-source PLCC needs to involve not only the improving voltage gain when switch S is turned on, but also recycle of the leakage energy of the primary winding when switch S is turned off. Besides, the energy needed by the load is supplied by the capacitor C_o in series with the capacitor C_1 as output capacitor. The diode D_3 is turned ON at $t = t_2$, and this mode is ended.

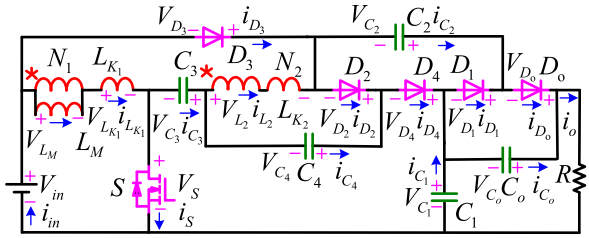

FIGURE 9. The equivalent circuit of the proposed converter.

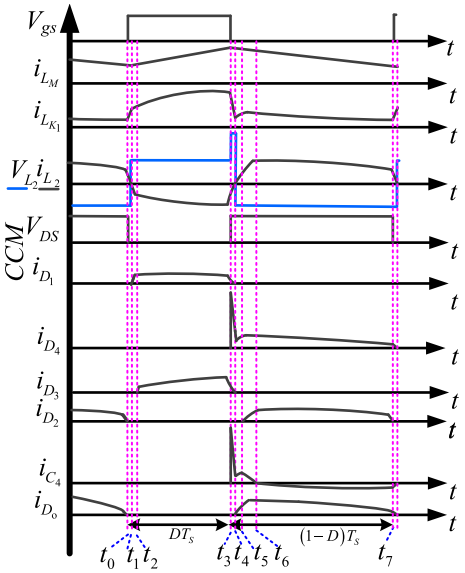

FIGURE 10. Some theoretical waveforms diagram of the presented converter at CCM operation. Where "DTs" means the on-state time of the main switch.

$[t_2, t_3]$: The diode D_3 is turned ON at $t = t_2$, while the diode D_1 and the switch S keep ON. The current-flow path is shown in Fig.11 (c). The only difference between this mode and the last mode is that the input source also provides its energy for the capacitor C_3 in this mode. Moreover, the output capacitors C_o and C_1 continue to provide their energy for the load R. When switch S is turned OFF at $t = t_3$, and this mode is ended.

$[t_3, t_4]$: During this interval, the switch S is turned OFF and the clamped diode D_4 is turned ON. The current-flow path is shown in Fig.11 (d). The leakage inductor of the primary-side is connected in series with the capacitors C_3 and C_4 to transfer their energy to the capacitor C_1. In 2-source PLCC, the capacitor C_1 is used to store the energy stored in the leakage inductor of the primary-side, but the capacitors C_3 and C_4 are used to construct a flowing branch for this energy. Therefore, the active switch is clamped by the 2-source clamped circuit consisted of the three capacitors and the one diode. Moreover, the voltage of the capacitor C_1 is increased so that the voltage of the output capacitor C_o can be significantly reduced by employing the serial connection. Besides, the current flowing through the secondary winding is in a freewheeling state and when the current decreases to zero, this operation ends.

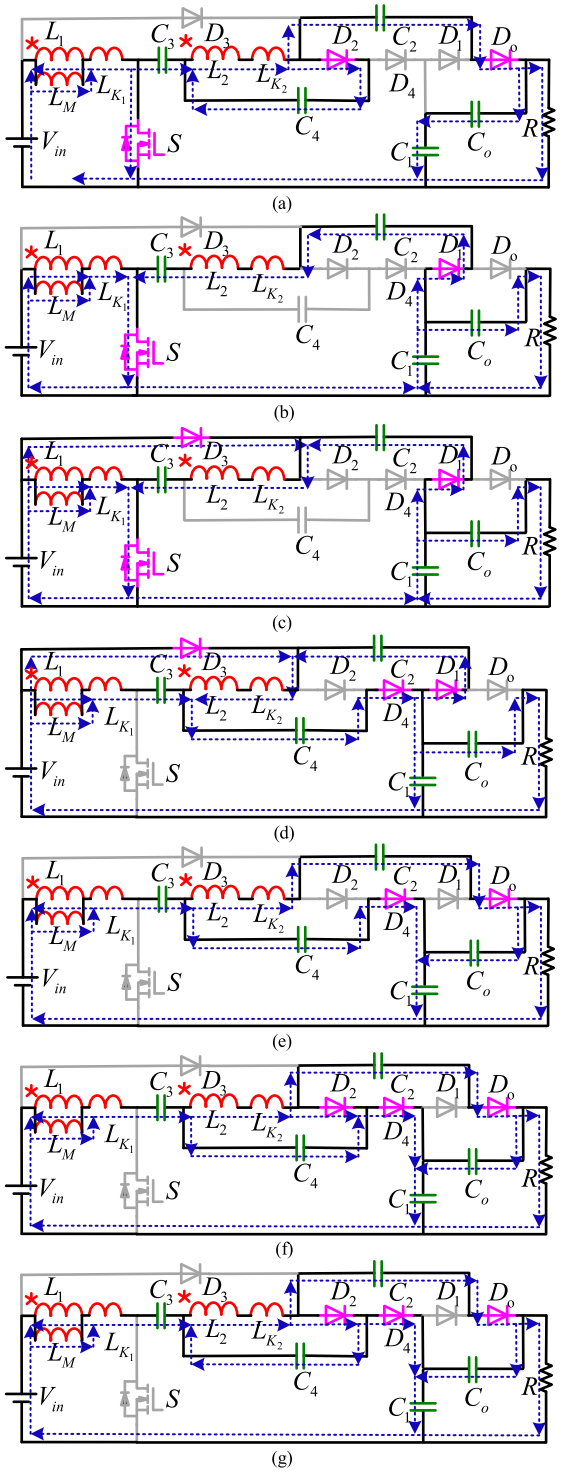

FIGURE 11. Current flow paths of operating modes during one switching period at CCM operation: (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII.

$[t_4, t_5]$: As shown in Fig.11 (e), the switch S is turned OFF and the diodes D_1 and D_3 are turned OFF naturally at $t = t_4$. Besides, the diode D_o is turned ON naturally. The energy stored in the leakage inductor of the primary-side is still released into the 2-source clamped circuit. Therefore, the capacitor C_1 is still charged by the input source, the primary-side winding, and the capacitors C_3 and C_4. Besides, the input source is connected in series with the primary-side winding, the capacitor C_3, the secondary-side winding and the capacitor C_2 to charge the load and the output capacitor C_o. When the diode D_2 is turned ON naturally this mode ends.

$[t_5, t_6]$: During this interval, the switch S and the diodes D_1 and D_3 are turned OFF, and the diodes D_2, D_o and D_4 are turned ON. The current-flow path is shown in Fig.11 (f). The secondary winding is connected in parallel with the capacitor C_4 to transfer their energy to the capacitor C_1. As the current of the capacitor C_4 decreases to zero, the current of the diode D_2 is equal to the current flowing through the clamed diode D_4, then, this mode ends.

$[t_6, t_7]$: At $t = t_6$, the capacitor C_4 is charged by the secondary winding through the diode D_2. The current-flow path is shown in Fig.11 (g). The capacitor C_1 is charged by the input voltage, the primary winding, and the capacitors C_3 and C_4. This mode ends when the switch S is turned on at the beginning of the next switching period.

IV. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. STEADY-STATE ANALYSIS

As the duration of the modes I and IV are very short, only the modes II, III, V, VI and VII are considered in order to simplify the analysis of the proposed converter in *CCM* operation. Besides, the secondary leakage is ignored. During modes II and III, the following equations based on Figs.11 (b)-(c) can be written:

$$V_{L_M}^{\text{II-III}} = KV_{in} \tag{1}$$

$$V_{L_{K_1}}^{\text{II-III}} = (1-K)V_{in} \tag{2}$$

During the mode V to the mode VII, based on Figs.11 (e)-(g) the following equations can be obtained:

$$V_{L_M}^{\text{VII}} = V_{L_M}^{\text{VI}} = V_{L_M}^{\text{V}} \tag{3}$$

$$V_{L_{K_1}}^{\text{VII}} = V_{L_{K_1}}^{\text{VI}} = V_{L_{K_1}}^{\text{V}} \tag{4}$$

$$V_{C_1} = V_{in} - V_{L_{K_1}}^{\text{VI}} - (N+1)V_{L_M}^{\text{VI}} + V_{C_3} \tag{5}$$

$$V_o = V_{in} - V_{L_{K_1}}^{\text{VI}} - (N+1)V_{L_M}^{\text{VI}} + V_{C_3} + V_{C_2} \tag{6}$$

Using the volt–second balance principle on L_M and L_K to yield

$$\int_{t_1}^{t_3} V_{L_M}^{\text{II-III}} dt + \int_{t_4}^{t_7} V_{L_M}^{\text{VI}} dt = 0 \tag{7}$$

$$\int_{t_1}^{t_3} V_{L_{K_1}}^{\text{II-III}} dt + \int_{t_4}^{t_7} V_{L_{K_1}}^{\text{VI}} dt = 0 \tag{8}$$

Substituting (1)–(6) into (7) and (8), the voltage gain can be written:

$$M_{CCM} = (3 + 2NK - D)/(1 - D) \tag{9}$$

where D is duty cycle.

Based on the equation (9), it can be seen that the voltage gain is unrelated to the inductance of the primary inductor under CCM.

B. VOLTAGE AND CURRENT STRESSES ON POWER DEVICES

To simplify the voltage stress analysis on the components, the leakage inductor of secondary side is neglected. The capacitors C_1, C_2, C_3 and C_4 can be expressed as:

$$V_{C_1} = V_{in}(2 - D + NK)/(1 - D) \quad (10)$$
$$V_{C_2} = V_{C_o} = V_{in}(1 + NK)/(1 - D) \quad (11)$$
$$V_{C_3} = (1 + NK)V_{in} \quad (12)$$
$$V_{C_4} = DNKV_{in}/(1 - D) \quad (13)$$

where N means the turns ratio of the coupled inductor.

The voltage stress across the switch S and the diodes D_1, D_2, D_3, D_4, D_o are derived by

$$V_{DS} = V_o/(3 + 2NK - D) \quad (14)$$
$$V_{D_1} = V_{D_2} = V_{D_3} = V_{D_4} = V_{D_o} = (1 + NK)V_o/(3 + 2NK - D) \quad (15)$$

The on-state average current of the output diode D_o and the average discharge current of the capacitor C_2 can be expressed as

$$I_{C_2} = I_{D_o} = I_o/(1 - D) \quad (16)$$

where I_o is the output current.

During the time interval $[t_4, t_7]$, while using KCL, at junction points of the clamped diode D_4, the capacitor C_o, and the capacitor C_1, the currents of clamped diode D_4 and capacitor C_4 can be written as

$$I_{C_4} = I_{D_4} = I_o \quad (17)$$

In the classical PLCC, the average discharge current of the clamped capacitor and the on-state average current of the clamped diode are equal to $I_o/(1-D)$ in [14]–[18]. Compared with the classical PLCC, the currents of the clamped diode D_4 and the capacitor C_4 are reduced because of the effect of connection in series with the capacitors C_o and C_1.

The on-state average current of diode D_2 is calculated as

$$I_{D_2} = I_o \quad (18)$$

During the time interval $[t_4, t_7]$, while using KCL, at junction points of the secondary-side L_2 of the coupled inductor, the diode D_2, and the capacitor C_4, the current of the secondary-side L_2 of the coupled inductor can be obtained

$$I_{L_{2off}} = (2 - D)I_o/(1 - D) \quad (19)$$

During the time interval $[t_4, t_7]$, the following equation can be expressed as

$$I_{L_{1off}} = (2 - D)I_o/(1 - D) \quad (20)$$

When the switch is turned on, the on-state average current of the diode D_3 is calculated as

$$I_{D_3} = (1 - D)I_o/D \quad (21)$$

During the time interval $[t_1, t_3]$, the following equation can be expressed as

$$I_{L_{2on}} = (2 - D)I_o/D \quad (22)$$

Based on the magnetic flux conversation principle, the following equation can be expressed as

$$I_{L_{1on}} + NI_{L_{2on}} = I_{L_{1off}} + NI_{L_{2off}} \quad (23)$$

Therefore, during the time interval $[t_1, t_3]$, the average current of the primary-side L_1 of the coupled inductor is calculated as

$$I_{L_{1on}} = (2 - D)(N + D)I_o/(D - D^2) \quad (24)$$

So, the RMS values of the switch S can be obtained

$$I_{S-RMS} = \frac{(2 - D)(N + 1)\sqrt{D}P_oI_o}{(1 - D)DV_o}\sqrt{\frac{K_S^2}{12} + 1} \quad (25)$$

where P_o, V_o, K_S mean the output power, the output voltage, and the current ripple of the switch, respectively.

C. COMPARATIVE ANALYSIS OF PERFORMANCE

For the sake of demonstrating the performance, the proposed converter is compared with what were published in [17], [31], [10] and [39] as shown in Table 4. Based on this table, the voltage gain against the duty ratio of them is shown in Fig.12 (a). Then, the relationship between voltage stresses of the devices with variable duty cycle, including output capacitor, active switch and output diode of these converters is drawn under $N = 2$, as shown in Figs.12 (b)-(d). Compared with the converter mentioned in [17], the number of diode and capacitor in the presented converter are less,

TABLE 4. Performance comparison among different converters.

Topology	Converter in[17]	Converter in[31]	Converter in[10]	Converter in[39]	Proposed converter
No. of active switches	1	1	2	1	1
No. of diodes	6	4	5	8	5
No. of capacitors	6	4	5	8	5
Voltage gain	$\frac{A_7}{1-D}$	$\frac{A_8}{1-D}$	$\frac{3+D}{(1-D)^2}$	$\frac{A_{10}}{1-D}$	$\frac{A_9}{1-D}$
Voltage stress of active switches	$\frac{V_o}{A_7}$	$\frac{V_o}{A_8}$	$\frac{1-D}{3+D}$	$\frac{V_o}{A_{10}}$	$\frac{V_o}{A_9}$
Voltage stress of output diode	$\frac{NV_o}{A_7}$	$\frac{(N+1)V_o}{A_8}$	$V_o/2$	$\frac{A_{10}-4}{A_{10}}V_o$	$\frac{(N+1)V_o}{A_9}$
Voltage stress of output capacitor	V_o	V_o	V_o	V_o	$\frac{(N+1)V_o}{A_9}$
Continuous input current	No	No	Yes	Yes	Yes

where A_7=1+2N+ND, A_8=2+N+ND, A_9=3+2N-D, A_{10}=4+2N-ND-D.

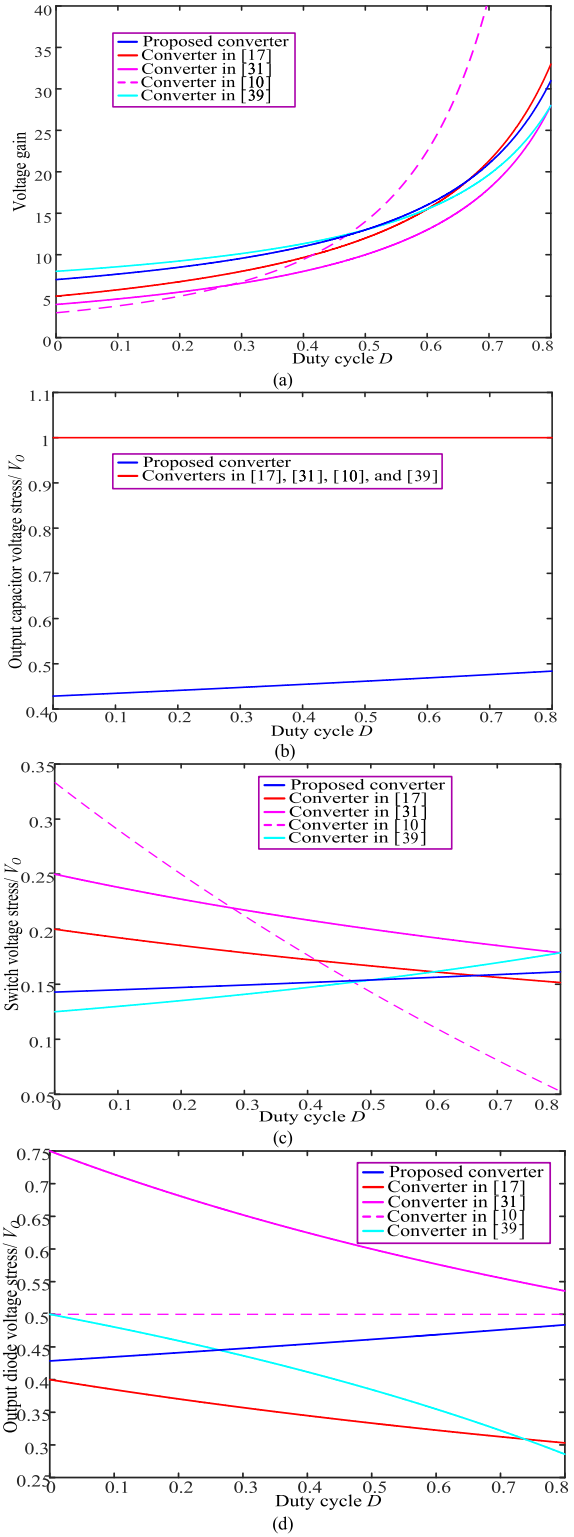

FIGURE 12. Comparative analysis among the converters under the same input voltage (V_{in} = 40V), the same output voltage (V_o = 400V), the same turns ratio (N = 2), and the same power (P_o = 400W).

therefore the cost is lower. However, the voltage stress of output diode of proposed converter is more than that of the converter mentioned in [17]. Fortunately, the voltage stress of output capacitor is far below that of the converter in [17] so that its volume is efficiently reduced. Besides, when duty cycle is less than about 0.65, the proposed converter has advantage on voltage gain and its voltage stress of active switch is lower and therefore its semiconductor devices with low on-state resistances can be adopted. Based on Fig.12, all of the performance of proposed converter is superior to that of the converter in [31], except the number of diode and capacitor. Compared with the three-level converter in [10], the number of the switch of the proposed converter is less and the number of the other devices is the same. When duty cycle is less than about 0.47, the voltage conversion in the proposed converter is higher and the voltage stress on the switch is lower. Furthermore, its voltage stress on output diode is far less than that of the three-level converter. Compared with the converter in [39], even if the number of the devices in the proposed converter are less, its voltage gain is higher under $D < 0.6$. But the voltage stress on switch is higher under $D < 0.48$ and the voltage stress on output diode is higher under $D > 0.27$. Note that the voltage stress of output capacitor of the proposed converter is far lower than that of the converters published in [17], [31], and [10], even lower than that of the three-level converter. Thus, large volume and high voltage electrolytic capacitor can be replaced by small volume and low voltage polypropylene capacitor so that the power density and efficiency of the proposed are improved.

D. CAPACITOR DESIGN

The aim of the design of capacitor C_o and capacitor C_1 is to restrict output voltage ripple ΔV, so that they are controlled in a reasonable range. When the main switch is on, C_o and C_1 provide their energy for load. Meanwhile, C_2 is charged by C_1. Therefore, the following equations can be given

$$\Delta Q_o = I_o D T_s = C_o \Delta V_{C_o} \tag{26}$$

$$\Delta Q_1 = I_o (D+1) T_s = C_1 \Delta V_{C_1} \tag{27}$$

$$\Delta V_{C_o} + \Delta V_{C_1} = \Delta V \tag{28}$$

And substituting (26) and (27) into (28), the capacitances of C_o and C_1 are designed according to the equation below

$$\sqrt{R} f_s \Delta V / [\sqrt{P_o}(1+D)] \geq D/[(1+D)C_o] + 1/C_1 \tag{29}$$

where T_s and f_s mean switching period and switching frequency, respectively.

In order to suppress the voltage spike of the main switch, avoid the excessive resonant ringing and make the clamped diode is turned off naturally, the design requirement of clamped capacitor is to select the closest capacitance value so that one half of the resonant period exceeds the maximum turn-on time of the switch. For capacitor C_1 which absorbs the energy stored in the leakage inductor in the 2-source PLCC, the following equation can be obtained

$$C_1 \geq (1-D)^2 / \pi^2 f_s^2 L_k \tag{30}$$

What should be noted in the design process of capacitor is that when polypropylene capacitor is employed, the power

of the proposed converter is limited by capacitance of the capacitors C_o and C_1.

E. SMALL-SIGNAL MODE OF THE PROPOSED CONVERTER

In order to simplify the analysis of small signal model of the proposed converter in *CCM*, during one switching period, only modes III ($[0, dT_S]$), VI ($[dT_S, \alpha T_S]$) and VII ($[\alpha T_S, T_S]$) are considered in the analytic process. According to the reference in [21], the state vector is defined as

$$x = [i_{L_M} i_{L_K} i_{L_2} \mu_{C_1} \mu_{C_4} \mu_O]' \tag{31}$$
$$k\dot{x} = Ax + Bu \tag{32}$$

And the input is defined as

$$u = [\mu_{in}] \tag{33}$$

The average model of the proposed converter can be obtained by averaging the state equations during ON and OFF periods. The converter is assumed to operate in *CCM*. Based on the mode III, during switch-on time $[0, dT_S]$ the following state matrices are given as below:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -2/L_2 & 0 & 1/L_2 \\ 0 & 0 & \frac{-1}{2C_1} & 0 & 0 & -1/RC_1 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{2C_1} & 0 & 0 & \frac{-1}{RC_1} - \frac{1}{RC_O} \end{bmatrix}$$

$$\text{and } B_1 = \begin{bmatrix} K/L_M \\ (1-K)/L_K \\ (1+N)/L_2 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{34}$$

Based on the mode VI, during switch-off time $[dT_S, \alpha T_S]$ the following state matrix equations are written by (35), as shown at the bottom of the next page.

Based on the mode VII, during switch-off time $[\alpha T_S, T_S]$, the following state matrix equations are obtained

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{NL_M} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_K} & \frac{N+1}{NL_K} & 0 \\ 0 & 0 & 0 & 0 & -1/L_2 & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 & 0 & \frac{-1}{RC_1} \\ \frac{1}{NC_4} & \frac{N+1}{-NC_4} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_1} + \frac{1}{C_O} & 0 & 0 & 0 & \frac{-1}{RC_1} - \frac{1}{RC_O} \end{bmatrix}$$

and

$$B_3 = \begin{bmatrix} 0 \\ \frac{N+2}{NL_K} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{36}$$

According to the reference in [21], the following state space average matrix equations are obtained

$$A = A_1 d + A_2(\alpha - d) + A_3(1 - \alpha) \tag{37}$$
$$B = B_1 d + B_2(\alpha - d) + B_3(1 - \alpha) \tag{38}$$

where α is equal to $d + d_c$, and d and d_c mean the ducy cycle and the duty cycle of the discharge in the capacitor C_4, respectively.

Finally, the equation (39), can be gained, as shown at the bottom of the next page.

By introducing perturbation, the state variables and the duty cycle of the matrix are replaced by the sum of dc and ac (perturbation) terms as follows

$$\begin{aligned} d = D + \hat{d};\ i_{L_K} &= [I_{L_K} + \hat{i}_{L_K}]; \\ i_{L_M} &= [I_{L_M} + \hat{i}_{L_M}]; \\ i_{L_2} &= [I_{L_2} + \hat{i}_{L_2}]; \\ \mu_{C_1} &= [V_{C_1} + \hat{\mu}_{C_1}]; \\ \mu_{C_4} &= [V_{C_4} + \hat{\mu}_{C_4}]; \\ \mu_O &= [V_O + \hat{\mu}_O] \end{aligned} \tag{40}$$

where I_{L_M}, I_{L_K}, I_{L_2}, V_{C_1}, V_{C_4} and V_o are the steady-state values of the state variables respectively.

Substituting (39) into (32), linearizing the final results and neglecting the higher order perturbation terms, and then removing the steady-state quantities, the small signal ac model of the converter is provided as follows

$$\begin{cases} \frac{d\hat{i}_{L_M}}{dt} = \frac{D-1}{NL_M}\hat{V}_{C_4} + \frac{KD}{L_M}\hat{V}_{in} \\ \frac{d\hat{i}_{L_K}}{dt} = \frac{D-1}{L_K}\hat{V}_{C_1} - \frac{2\alpha + N + 2 - ND - D}{NL_K}\hat{V}_{C_4} \\ + \frac{N + 2 - D(N+1+K)}{NL_K}\hat{V}_{in} \\ \frac{d\hat{i}_{L_2}}{dt} = \frac{-2D}{L_2}\hat{V}_{C_1} + \frac{D-1}{L_2}\hat{V}_{C_4} \\ + \frac{D}{L_2}\hat{V}_O + \frac{N+1}{L_2}D\hat{V}_{in} \\ \frac{d\hat{V}_{C_1}}{dt} = \frac{1-D}{C_1}i_{L_K}{}^{\wedge} - \frac{D}{2C_1}D\hat{i}_{L_2} - \frac{1}{RC_1}V_O{}^{\wedge} \\ \frac{d\hat{V}_{C_4}}{dt} = \frac{1-D}{NC_4}\hat{i}_{L_M} - \frac{(N+1)(1-D)}{NC_4}(1-D)\hat{i}_{L_K} \\ \frac{d\hat{V}_O}{dt} = \frac{\alpha - D}{NC_O}\hat{i}_{L_M} + (\frac{1-D}{C_1} + \frac{N + D - N\alpha - \alpha}{NC_O})\hat{i}_{L_K} \\ + \frac{D}{2C_1}\hat{i}_{L_2} - \frac{\hat{V}_O}{RC_1} - \frac{\hat{V}_O}{RC_O} \end{cases} \tag{41}$$

By adopting the Laplace transform of (41), the corresponding control-to-output transfer function can be obtained in the equation (42), as shown at the bottom of the next page.
where

$$p_1 = A_{62}A_{24} + A_{63}A_{34},\ \ p_2 = A_{42}A_{25} - A_{34}A_{35},$$
$$p_{10} = A_{43}A_{36},\ \ p_4 = A_{42}A_{24} - A_{43}A_{34},$$

$$p_3 = A_{61}A_{15} + A_{62}A_{25} + A_{63}A_{35},$$
$$p_5 = p_8A_{43}B_3, p_6 = A_{51}B_1 - A_{52}B_2,$$
$$p_8 = A_{52}A_{24}, p_7 = A_{51}A_{15} + A_{52}A_{25},$$
$$p_9 = A_{63}A_{34}, p_{11} = A_{52}A_{24}p_{10}.$$

The control block diagram of the presented converter is shown in Fig. 13. It can be seen that the controller is extremely simple and easy to implement. And it can be realized by using either digital or analog circuits.

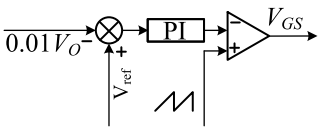

FIGURE 13. Control block diagram of the proposed converter.

F. LOSS ANALYSIS

The efficiency and voltage gain of the proposed converter are affected by the parasitic resistances of semiconductor devices and the coupled inductor. All semiconductor devices are assumed to be non-ideal, except for all capacitors. To simplify the analysis and calculation, many losses are neglected in this section, including the leakage inductor loss, the diode reverse recovery loss, magnetic core loss, switching loss and the ESR loss of capacitors. Fig.14 (a) shows the equivalent circuit of the proposed converter in which R_L denotes the copper resistances of the primary side L_1 of the coupled inductor; R_{DS} represents the conduction resistances of switch; V_D means the forward voltages drop of the diodes, and R_D is the on-state resistances of the diodes.

All current through components are approximated by the dc components by using small-ripple approximation. Then,

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{NL_M} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_K} & \frac{N-1}{NL_K} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 & \frac{-1}{RC_1} \\ \frac{1}{NC_4} & \frac{N+1}{-NC_4} & 0 & 0 & 0 & 0 \\ \frac{1}{NC_O} & \frac{1}{C_1} - \frac{1}{NC_O} & 0 & 0 & 0 & \frac{-1}{RC_1} - \frac{1}{RC_O} \end{bmatrix}$$

$$\text{and } B_2 = \begin{bmatrix} 0 \\ \frac{N+2}{NL_K} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{35}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{d-1}{NL_M} = A_{15} & 0 \\ 0 & 0 & 0 & \frac{d-1}{L_K} = A_{24} & \frac{2\alpha+N+2-Nd-d}{NL_K} = A_{25} & 0 \\ 0 & 0 & 0 & \frac{-2d}{L_2} = A_{34} & \frac{d-1}{L_2} = A_{35} & \frac{d}{L_2} = A_{36} \\ 0 & \frac{1-d}{C_1} = A_{42} & \frac{-d}{2C_1} = A_{43} & 0 & 0 & \frac{-1}{RC_1} = A_{46} \\ \frac{1-d}{NC_4} = A_{51} & \frac{(N+1)(1-d)}{-NC_4} = A_{52} & 0 & 0 & 0 & 0 \\ \frac{\alpha-d}{NC_o} = A_{61} & \frac{1-d}{C_1} + \frac{N+d-N\alpha-\alpha}{NC_O} = A_{62} & \frac{d}{2C_1} = A_{63} & 0 & 0 & \frac{-1}{RC_1} - \frac{1}{RC_O} = A_{64} \end{bmatrix}$$

and

$$B = \begin{bmatrix} \frac{Kd}{L_M} = B_1 \\ \frac{d-Kd+(N+2)(1-d)}{NL_K} = B_2 \\ (N+1)d/L_2 = B_3 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{39}$$

$$G_{vd}(s) = \frac{(p_1p_2 + sp_3)[p_5 + p_6(s^2 - p_4)]}{[(s^2 - p_9)(s^2 - p_4) + p_1p_{10} - \frac{p_1p_2+sp_3}{s^2}p_{11}][(s^2 - p_7) + \frac{p_2p_8}{s^2-p_4}]} \tag{42}$$

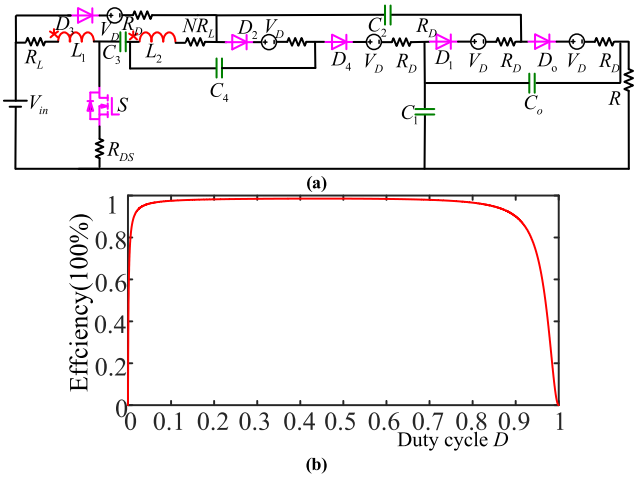

FIGURE 14. Efficiency analysis.

by using voltage-second balance and capacitor-charge balance, the voltage gain and the efficiency including conduction loss are obtained

$$M_{CCM} = \frac{\frac{3+2N-D}{1-D} - \frac{5V_D}{V_{in}}}{1 + AR_L + BR_D + CR_{DS}} \tag{43}$$

where

$$A = \frac{2(2-D)(D+N^2+ND+N)}{RD\,(1-D)^2}, B = \frac{2-D^2}{RD\,(1-D)},$$
$$C = \frac{(4N+1+2ND)(2-D)(N+1)}{RD\,(1-D)^2}.$$
$$\eta = \frac{1 - \frac{5V_D(1-D)}{(3+2N-D)V_{in}}}{1 + AR_L + BR_D + CR_{DS}} \tag{44}$$

In order to show how duty cycle and parasitic parameters influence the efficiency, the following parameters of converter are assumed: $R_L = 0.01\ \Omega$, $N = 2$, $R_{DS} = 0.0048\ \Omega$, $R_D = 0.025\ \Omega$, $R = 400\Omega$, $V_D = 0.526$V, $V_{in} = 40$ V. As the duty cycle increases from zero to 0.1, the efficiency rapidly increases as shown in Fig.14 (b). The efficiency rapidly decreases as the duty cycle increases from 0.9 to 1.

V. EXPERIMENTAL VERIFICATION

To verify the performances of the proposed converter, a prototype circuit is implemented in the laboratory, and the specifications and the rated conditions are shown in Table 5. The measured waveforms under *CCM* operation are shown in Fig.15. The current and voltage of the primary side of the coupled inductor and the voltage stress across the switch are shown in Fig.15 (a). The voltage spike caused by the leakage inductor is perfectly suppressed by the 2-source PLCC. Fig.15 (b) shows the current and voltage of the secondary side of the coupled inductor. The currents and voltages of diodes D_3 and D_4 are shown in Figs.15 (c) and (d) respectively. Fig.15 (e) shows voltages of the capacitor C_1 and C_o, which are about 220V and 180V respectively. It is can be seen that

TABLE 5. System parameters of the proposed converter.

System parameters	Specifications
Input voltage V_{in}	40V
Output voltage V_o	400V
Rated Power P_o	400W
Switching frequency: f_s	100kHz
MOSFET Switch S	FDP075N15A
Diodes D_1, D_2, D_3, D_4, D_o	MURS340
Capacitors C_1, C_o	CBB 30μF
Capacitors C_2, C_3, C_4	CBB 10μF
Coupling inductors	ER49, $N = 33:17$ $L_M = 87.8\mu$H, $L_{K_1} = 0.71\mu$H, $L_2 = 334.5\mu$H

the voltage of the output capacitor C_o is effectively decreases and less than 0.5 times of the output voltage. So, the output capacitor of the proposed converter can adopt polypropylene capacitor in place of electrolytic capacitor to reduce the cost and volume of the converter. Then, the current and voltage of output diode are shown in Fig.15 (f). The voltages of the input source and the output as well as the current flowing through the switch are shown in Fig.15 (g).

The experimental dynamic response results of the output voltage and output current under the step load variation from 200 to 400 W are shown in Fig. 16. It can be seen that the output voltage of the proposed converter is insensitive to the load variation and the voltage tracks its reference very quickly with a proper closed loop control. Fig. 17 shows the prototype. Based on the two literatures, the test efficiencies of these converters are shown in Fig.18 under $V_{in} = 40$V, $V_o = 400$V and $P_o = 400$W. According to the efficiency test, its maximum efficiency is about 96.4% at $P_o = 140$W as shown in Fig.18. Under the rated load, the efficiency of the proposed converter is to reach 93.3%.

The following equation is considered in the analysis of the power efficiency:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{45}$$

To evaluate the power losses and the power efficiency of the proposed converter, the power losses are calculated as

$$P_{Loss} = \sum (P^S_{Loss} + P^D_{Loss} + P^L_{Loss} + P^C_{Loss}) \tag{46}$$

The switching losses of the switch can be expressed as:

$$P_{swM} = (U_{DS} I_{Son} \frac{tfu + tri}{2} + U_{DS} I_{Doff} \frac{tru + tfi}{2}) f_s \tag{47}$$

where *tfu*, *tri*, I_{Son}, and I_{Doff} are voltage fall time, current rise time, drain-source current at turn-on and drain-source current at the turn-off from the datasheet, respectively. And f_s is switching frequency.

The conduction loss of the switch can be expressed as:

$$P_{CM} = I^2_{DSrms} R_{DSon} \tag{48}$$

where I_{DSrms} and R_{DSon} are the RMS current and the ON-state resistance of the active switch, respectively.

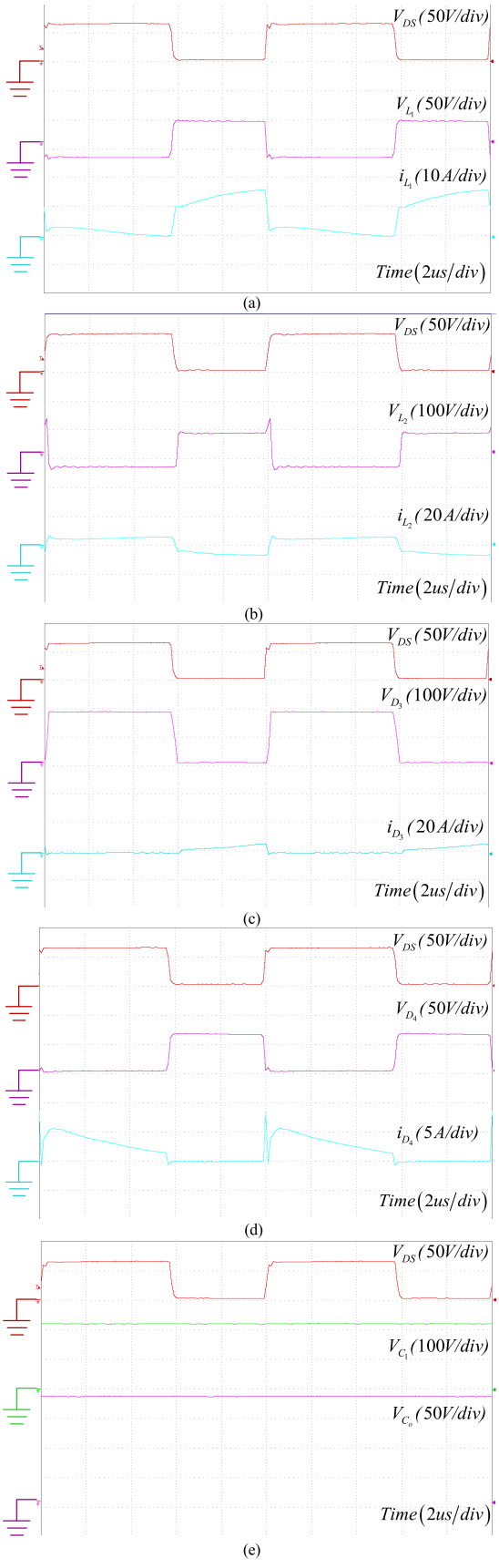

FIGURE 15. Experiment results under full-load Po = 400 W.

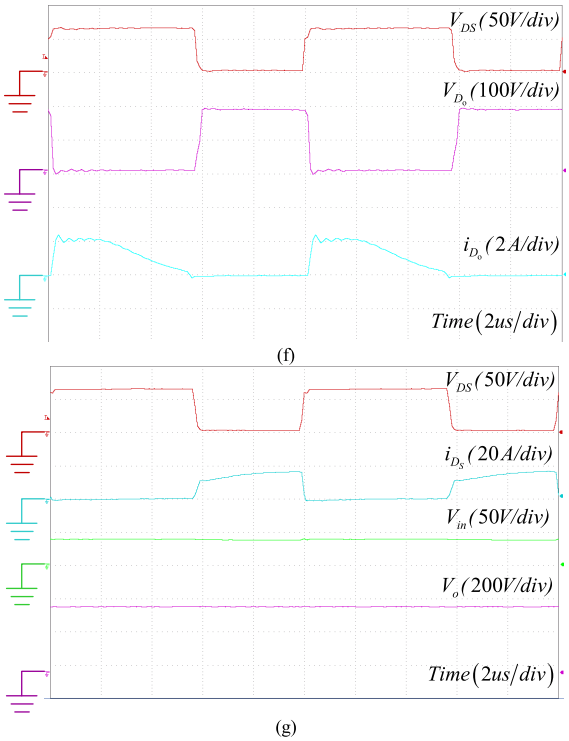

FIGURE 15. *(Continued.)* Experiment results under full-load Po = 400 W.

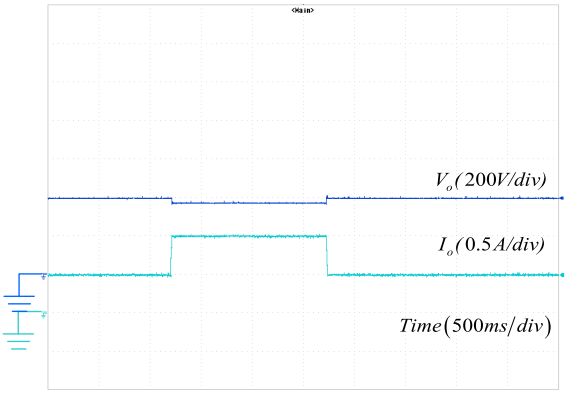

FIGURE 16. Dynamic response of output voltage and output current under step load variation from 200 to 400 W.

Therefore, the total losses of the switch can be calculated as follows:

$$P_{Loss}^{S} = P_{swM} + P_{CM} \tag{49}$$

The power losses of the diodes are calculated as follows:

$$P_{Loss}^{D}(T_j) = V_{T0}(T_j)I_F(av) + R_D(T_j)I_D^2(rms) \tag{50}$$

where T_j and $V_{T0}(T_j)$ are respectively junction temperature and threshold voltage under T_j from the datasheet, and $I_F(av)$ and $I_D(rms)$ are the average current and the RMS current of the diodes, respectively.

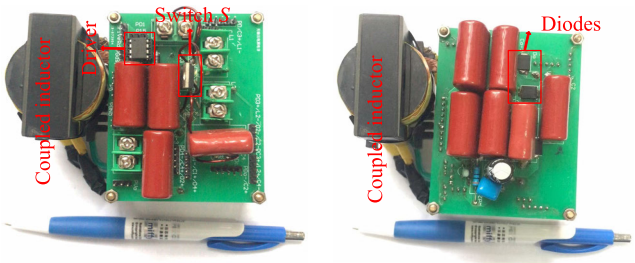

FIGURE 17. Prototype photograph of the proposed converter: (a) positive side, (b) negative side.

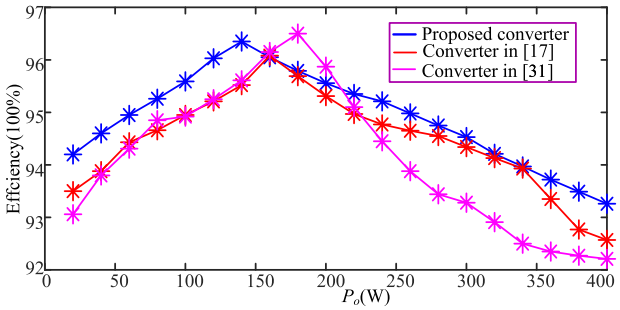

FIGURE 18. Test efficiency of 400 W prototypes.

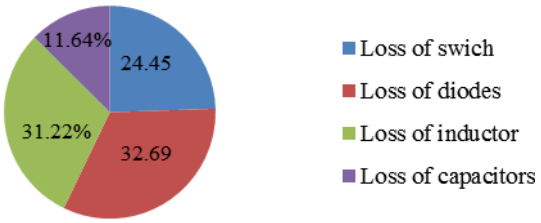

FIGURE 19. Power loss distribution at full load.

TABLE 6. Losses of power components.

Component losses	Proposed converter	Converter in [17]	Converter in [31]
Switching loss of MOSFET	5.84(W)	5.42(W)	6.51(W)
Conduction loss of MOSFET	0.72(W)	0.71(W)	0.88(W)
Conduction loss of diode D_1	2.1(W)	1.52(W)	2.28(W)
Conduction loss of diode D_2	1.36(W)	1.86(W)	2.33(W)
Conduction loss of diode D_3	2.11(W)	1.53(W)	2.64(W)
Conduction loss of diode D_4	1.62(W)	1.53(W)	/
Conduction loss of diode D_5	/	1.86(W)	/
Conduction loss of diode D_o	1.57(W)	1.34 (W)	1.86(W)
Core loss	4.84(W)	5.02(W)	4.33(W)
Copper loss	3.26(W)	3.35 (W)	3.14 (W)
Total Losses of capacitors	3.68(W)	7.03(W)	5.74(W)
Total Losses	27. 1(W)	31.17(W)	29.71(W)

Therefore, the total losses of the diodes can be calculated as follows:

$$P_{Loss}^{D} = P_{Loss}^{D_1} + P_{Loss}^{D_2} + P_{Loss}^{D_3} + P_{Loss}^{D_4} + P_{Loss}^{D_o} \quad (51)$$

TABLE 7. Volume of power components.

Converters	Switch (mm^3)	Diode (mm^3)	Capacitor (mm^3)	Coupled Inductor (mm^3)
Converter in [17]	832.58	2733.44	62329.2	80269.54
Proposed converter	1108.333	380.01	7805.332	45848.32

The power losses of the coupled inductor contain the conduction loss (P_w) and magnetic loss (P_c). The conduction loss of the coupled inductor can be calculated as follows:

$$P_w = I^2 R_{dc} \quad (52)$$

where R_{dc} is the copper resistance of the coupled inductor.

The magnetic loss of the coupled inductor can be calculated as:

$$P_c = \frac{R_{ac}}{uL} = aB_{\max} f_{sw} + cf_{sw} + ef_{sw}^2 \quad (53)$$

where R_{ac}, a, c, and e are respectively resistance due to core loss, hysteresis loss coefficient, residual loss coefficient, and eddy-current loss coefficient.

Therefore, the total losses of the coupled inductor can be calculated as follows:

$$P_{Loss}^{L} = P_w + P_c \quad (54)$$

The power losses of the capacitors due to their equivalent series resistances (ESR_c) can be calculated as follows:

$$P_{Loss}^{C} = \sum I_{RMSC}^2 ESR_C \quad (55)$$

Table 6 shows the power loss distribution of the proposed converter and the converters in [17] and [31]. Based on Table 6, Fig.19 shows the proportion of the losses in the proposed converter.

Table 7 shows the volume distribution of the different devices both the proposed converter and the converter in [17]. The power density of the converters is equal to 2.737×10^{-3} W/mm^3 and 7.254×10^{-3} W/mm^3 respectively under rated P_o = 400W. Compared with the converter in [17], employing two CBB capacitors in series as output capacitor to replace single electrolytic capacitor can efficiently improve power density. Adopting surface-mounted diode also efficiently improves power density.

VI. CONCLUSION

In this paper, modular combination of high-up converter is proposed. Then, Nc-SUC is proposed to improve the voltage gain of these converters and a novel clamp way called M-source PLCC is presented to recycle the energy stored in leakage inductor. Three family converters as examples, including a family of Boost converters with 0-Source PLCC, a family of Boost converters with 1-Source PLCC and a family of Boost converters with 2-Source PLCC, are proposed and can be imitated by various converters. The superiority of M-source PLCCs is demonstrated by those converters. Then, one clamped capacitor of M-source PLCC is connected in series with output capacitor, so that the output capacitor

voltage is efficiently downgraded. Finally, a novel converter with 2-SUC as a representative of the deduced converters is proposed and analyzed in detail, and verify its performances and the effect of the M-source PLCC in the laboratory.

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