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Conducted EMI Investigation of a SiC-Based Multiplexing Converter for EV/PHEV

JIANZHEN QU, QIANFAN ZHANG, (Member, IEEE), YANG WANG, AND SHUMEI CUI
School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China

Corresponding author: Qianfan Zhang (zhang_qianfan@hit.edu.cn)

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ABSTRACT This paper investigates the conducted electromagnetic interference (EMI) characteristics of an on-board multiplexing converter that utilizes paralleled silicon carbide (SiC) devices to achieve high efficiency and high-power density for the application in electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs). The multiplexing converter can operate as a three-phase interleaved DC/DC converter with a peak output power of 60 kW or an integrated two-stage non-isolated on-board charger (OBC) with an output power of 6.6 kW. The novelty of this paper is that it reveals that in the DC/DC mode the series resonance between the input negative lead parasitic inductance and the high frequency transmission line effects of the input power inductor will increase the conducted EMI levels, which can be mitigated by optimizing the winding methods of the power inductor or by adding a small capacitor, and reveals that in the non-isolated OBC mode the shielded cable on the battery-side will increase the grid-side EMI in the low frequency ranges, which can be suppressed by integrated installation of EMI filters without affecting the system power density. Firstly, parasitic parameters of the components of the multiplexing converter, such as the power inductors, the SiC MOSFETs and the shielded cables, are extracted and validated with impedance measurements, and the corresponding equivalent circuit models are established. Then, the conducted EMI simulation models of the multiplexing converter in different working modes are established. The influence of different interference sources and different parasitic parameters on the system EMI characteristics are analyzed, and the effective EMI suppression measures are given without affecting the system power density. Finally, the conducted EMI characteristics of the multiplexing converter and the effectiveness of the proposed EMI suppression measures are tested and verified through experiments.

INDEX TERMS Common mode (CM), electromagnetic interference (EMI), EMI modeling, EMI reduction, EMI simulation, parasitic parameters, silicon carbide (SiC) MOSFET.

I. INTRODUCTION

In the future, the fully electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs) will become the mainstream vehicles for the global automobile companies to meet the future stringent fuel consumption and emission regulations [1]. The on-board charger (OBC) can easily charge the battery to reduce the range anxiety of the end user, but it also increases the volume and weight of on-board converter system [1], [2]. The multiplexing converter that integrates OBC and electric drive systems of the EV/PHEV is a way to meet the weight, space, and cost constraints [1], [3], [4]. By application of silicon carbide (SiC) devices, the system power density can be further improved through the reduction in size of cooling systems or passive components [2], [5], [6]. With low loss, fast switching speed, and high temperature withstanding capabilities, SiC devices are considered to be the key driving force for high performance and high power density converters in automotive, aerospace and industrial applications [2], [3], [6]–[9].

However, many of the performance advantages of SiC devices are attributed to their increased switching speeds (di/dt, dv/dt) and the resulting high switching frequency capability, which raises the issues of significantly increased electromagnetic interference (EMI) in power converters [8]–[14]. As a result, costly and bulky EMI suppression measures are needed to suppress the emitted noise below the stringent EMI standard, which has become the main barrier to the increase in

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power density [15]. EMI issues must be addressed properly, otherwise, the performance benefits of SiC devices will be compromised [10].

A number of techniques can be employed to suppress the conducted EMI emissions, which may be divided broadly into two categories: those which suppress the generation of EMI at its source, and those which reduce the effectiveness of the EMI propagation paths [13], [16]. The former mainly includes the following measures: 1) Independent control of *di/dt* and *dv/dt* through the closed-loop gate driver to reduce the amplitude of the high-frequency interference signals [17]–[19]. However, with the further increase in switching speed, the application of closed-loop gate drivers in SiC devices is becoming more and more limited. 2) Suppresses the high-frequency ringing of switching voltage waveforms by adding the passive absorption circuit, such as the coreless PCB transformer [20] and the ferrite bead [9], [12], [21]. However, the size of the coreless PCB transformer is relatively large and cannot be applied to the TO-247 packaged SiC MOSFET and the ferrite bead solution is only suitable for small current (less than 10 A) applications. 3) Suppresses the turn-on current overshoots and oscillations through the soft switching technology, which reduces the differential mode (DM) EMI in the high frequency ranges [22]. However, the soft-switching technology will increase the low-frequency DM EMI and have no significant effect on the common mode (CM) EMI. The latter mainly includes the following measures: 1) Optimize the package of SiC power devices by the hybrid packaging technology to reduce the parasitic CM capacitance, which can improve the impedance characteristics of the CM EMI coupling path and can significantly reduce the system EMI levels [22]. However, designing new packages for SiC devices is expensive and time-consuming, and its long-term operational reliability needs to be verified. 2) By changing the topological structure with additional passive components (inductors or capacitors), a balanced Wheatstone bridge circuit topology can be identified in the CM equivalent circuit of the converter system, resulting in the near-ideal cancellation of CM currents and the significantly reduced conducted EMI emissions [23]–[27]. However, the balanced condition is loads-dependent and can only be achieved by adjusting the added passive components [24]. 3) Change the impedance characteristics of the EMI coupling path by adding passive EMI filters, which can eliminate the system resonance point, and attenuate the conducted EMI emissions [28]–[32]. However, the passive EMI filters can be bulky and may add significant weight to the overall system and its high frequency performance is limited by magnetic materials and other parasitic parameters [33]. More compact EMI filter design is desired in transportation applications because of the limited space [34]. In practice, a combination of these methods is utilized. In general, EMI suppression measures tend to increase the size and cost of a product, and it is desirable to seek improved tradeoffs between the conflicting demands of achieving both EMC and high performance.

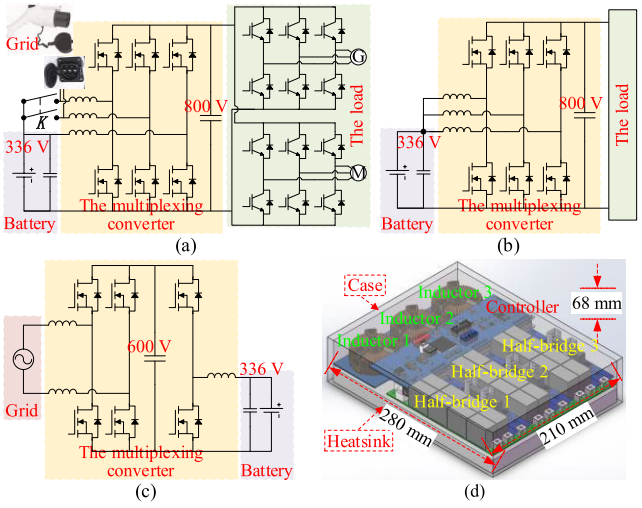

FIGURE 1. The multiplexing converter for a PHEV: (a) the electric drive system in a PHEV, (b) the DC/DC working mode, (c) the OBC working mode, and (d) the virtual prototype of the multiplexing converter.

This paper investigates the conducted EMI characteristics of an all-SiC high-power density and high-efficiency multiplexing converter, which is part of the electric drive system of PHEV as shown in Fig. 1(a). The multiplexing converter can operate as a three-phase interleaved DC/DC converter with a peak output power of 60 kW as shown in Fig. 1(b) to step the low battery voltage (336 V) up to the high dc voltage (800 V) to optimize the system efficiency in the driving mode. Interleaving has been proposed to reduce the charging current ripples and the inductor sizes [1]. The multiplexing converter can also operate as a two-stage OBC with an output power of 6.6 kW as shown in Fig. 1(c) to charge the battery from the grid, where the first stage is a full-bridge AC-DC converter and the second stage is a buck converter [35]. This power level classifies the OBC as a level II charger which can be used for residential charging applications and have a higher likelihood of widespread adoption due to the prevalence of suitable power outlets [2]. The two-stage AC-DC/DC-DC power conversion architecture provides the inherent low frequency current ripple rejection capability [36]. The final virtual prototype of the multiplexing converter is shown in Fig. 1(d), which consists mainly of three power inductors, the controller, three half-bridges based on the paralleled SiC MOSFETs, and the associated gate drivers. The dimensions of the multiplexing converter including the heatsink and the outer case are 280 mm $\times$ 210 mm $\times$ 68 mm and the total volume is about 4.0 L. The peak power density will be 15 kW/L at the peak output power of 60 kW in the DC/DC working mode.

The main contribution of this paper is that the conducted EMI simulation models of the multiplexing converter in different working modes are established, the influence of different interference sources and different parasitic parameters on the system EMI characteristics are analyzed, and the effective EMI suppression measures are given without affecting the system power density. In section II, parasitic models of the

multiplexing converter are established and validated with impedance measurements. In section III, the conducted EMI characteristics of the multiplexing converter in the DC/DC working mode are analyzed by simulation and experiments. The effective EMI suppression measures are given without affecting the system power density. In section IV, the conducted EMI characteristics of the multiplexing converter in the non-isolated OBC working mode are analyzed in the same way. The integrated EMI filters are designed to suppress the EMI levels without affecting the system power density. The conclusions are given in Section V.

II. PARASITIC PARAMETERS EXTRACTION

Parasitic parameters generally exist in all components of the multiplexing converter, such as the power inductors, the filter capacitors, the shielded cables, the SiC devices, and the printed circuit board (PCB) layouts. As the switching speed of power devices is increased gradually, the influence of parasitic parameters on the system EMI increases significantly [9], [37], [38]. These parasitic parameters will not only affect the spectrum characteristics of the EMI noise source, but also affect the impedance characteristics of the EMI coupling path. Characterization of parasitic parameters provides important information for identifying the major causes of EMI [39]. Fig. 2 shows the equivalent circuit of the multiplexing converter including parasitic parameters in the DC/DC working mode. These parasitic parameters will be extracted and measured in this section.

A. PARASITIC CM CAPACITORS OF THE PARALLELED SIC MOSFET HALF-BRIDGE UNIT

The design details of the paralleled SiC MOSFET half-bridge unit that used in the multiplexing converter, as shown in Fig. 3(a), was already given in [40], where eight discrete SiC MOSFETs are used with the distributed arrangement of dc capacitors. In this section, the parasitic CM capacitances of the paralleled unit are analyzed and compared with the measurements.

The insulating material between the SiC MOSFET and the heat sink is the ceramic (AL_2O_3) sheet with a thickness of 0.6 mm as shown in Fig. 3 (b). The parasitic CM capacitance (C_{cm}) of one TO-247 packaged SiC MOSFET in the paralleled half-bridge unit can be calculated as 31.61 pF by (1), where the ε_r (9.0) represents the relative permittivity of the AL_2O_3, the ε_0 (8.854×10^{-12} F/m) represents the permittivity of the air, the A_1 (238 mm^2) represents the area of the base plate of the TO-247 package, and the d_1 (0.6 mm) represents the thickness of the ceramic (AL_2O_3) plate. Therefore, the parasitic CM capacitances (C_{cm11}, C_{cm12}, C_{cm21}, C_{cm22}, C_{cm31}, C_{cm32}) as shown in Fig. 2 can be calculated as 126.44 pF by (2). The C_{cm} measured by an impedance analyzer E4990A is 31.97 pF, which agrees with the calculated value (31.61 pF) by (1).

$$C_{cm} = \varepsilon_r \varepsilon_0 \frac{A_1}{d_1} \tag{1}$$

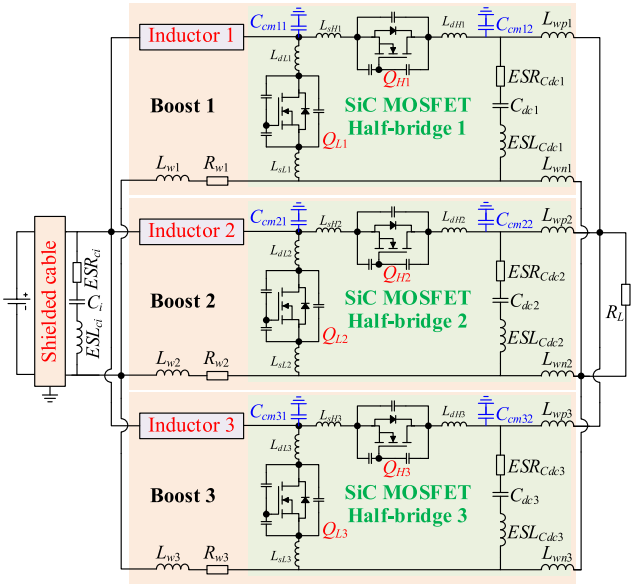

FIGURE 2. The equivalent circuit of the multiplexing converter including parasitic parameters in the DC/DC working mode.

$$C_{cm11} = C_{cm12} = C_{cm21} = C_{cm22} = C_{cm31} = C_{cm32} = 4C_{cm} \tag{2}$$

B. PARASITIC PARAMETERS OF THE DC LINK CAPACITORS

The dc capacitor is composed of eight small capacitors connected in parallel as shown in Fig. 3(a), which can improve the transient current sharing performance of the paralleled SiC MOSFETs and decrease the total power loop inductance.

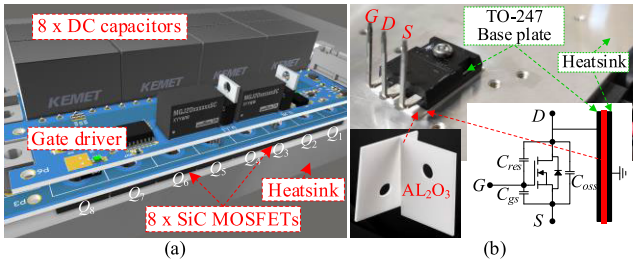

FIGURE 3. The installation of the paralleled SiC MOSFET half-bridge unit: (a) the paralleled unit installed on the heatsink, and (b) the Al_2O_3 ceramic plate for insulation.

The measured impedance curves of a single small capacitor and the total dc capacitor (including the PCB) are shown in Fig. 4, which can be synthesized easily by a resistor (*ESR*), an inductor (*ESL*), and a capacitor (*C*) in series with values: $C_1 = 5.22\ \mu$F, $ESR_1 = 11.95\ m\Omega$, $ESL_1 = 20.27$ nH, $C_{dc} = 42.03\ \mu$F, $ESR_{Cdc} = 4.41\ m\Omega$, and $ESL_{Cdc} = 9.40$ nH. The fitted curves match the measured curves very well as shown in Fig. 4. The input capacitor is measured and fitted in the same way, where the $C_i = 231\ \mu$F, the $ESR_{ci} = 5.08\ m\Omega$ and the $ESL_{ci} = 16.07$ nH.

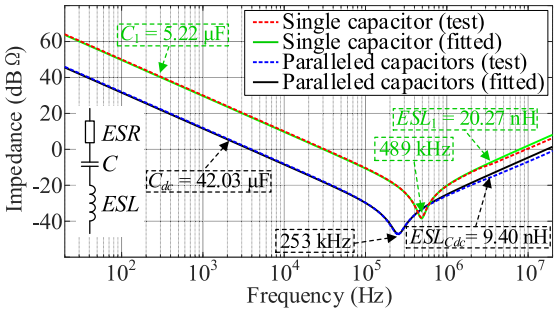

FIGURE 4. The measured and fitted impedance characteristics of the paralleled dc capacitors.

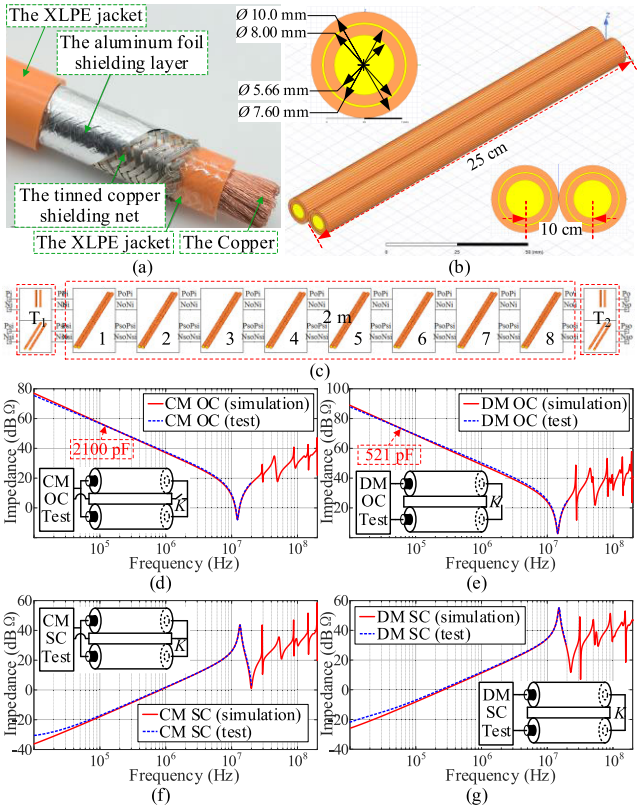

FIGURE 5. The impedance measurement and simulation of the shielded cable for EV/PHEV: (a) the shielded cable, (b) the sub-model in the Q3D, (c) the simulation model of the shielded cable in the Simplorer, (d) the simulated and measured CM OC impedance, (e) the simulated and measured DM OC impedance, (f) the simulated and measured CM SC impedance, and (g) the simulated and measured DM SC impedance.

C. PARASITIC PARAMETERS OF THE SHIELDED CABLE

The high-voltage shielded cable for EV/PHEV, as shown in Fig. 5(a), is used to connect the battery and the multiplexing converter. According to the conducted EMI test arrangement specified in the GB/T 18655-2018, the battery must be connected to the multiplexing converter through a shielded cable with a length of 1.5 m ∼ 2.0 m, and the conducted EMI test frequency range is 150 kHz ∼ 108 MHz.

Taking into account the high-frequency transmission line effects and the limitations of the Q3D mainly for quasi-static simulation applications, the simulation model of the shielded cable consists of multiple sub-models connected in series. The sub-model is shown in Fig. 5(b) with a length of 25 cm, which is one-eleventh of the wavelength at the highest test frequency of 108 MHz, which satisfies the premise of Q3D quasi-static simulation. Eight sub-models are dynamically linked in the Simplorer to simulate the impedance characteristics of the entire shielded cable, as shown in Fig. 5(c), which also dynamically links the connection terminal models for impedance test configuration (T_1 and T_2).

The impedance characteristics of the shielded cable (20 Hz ∼ 20 MHz) are extracted by an impedance analyzer E4990A. The extracted and simulated common mode open circuit (CM OC) impedance curves are shown in Fig. 5(d), where the equivalent capacitance of a pair of cables to the shield is 2100 pF in the low frequency ranges (less than 10 MHz), so the equivalent parasitic capacitance of a single cable to the shield is 1050 pF. The extracted and simulated differential mode open circuit (DM OC) impedance curves are shown in Fig. 5(e), where the equivalent capacitance between cables in the low frequency ranges is 521 pF, which is equal to the series connection of two capacitors (1050 pF). The extracted and simulated common mode short circuit (CM SC) impedance curves are shown in Fig. 5(f), and the extracted and simulated differential mode short circuit (DM SC) impedance curves are shown in Fig. 5(g). The simulated impedance curves agree well with the measured curves in the frequency ranges of 20 Hz ∼ 20 MHz, where the test frequency range is mainly limited by the test capability of the impedance analyzer in the laboratory.

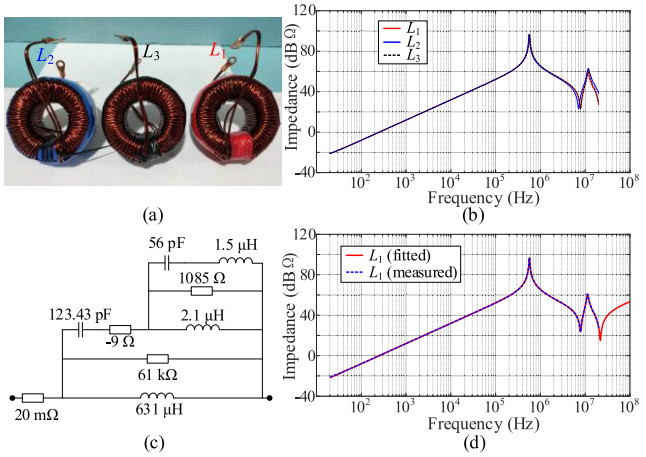

FIGURE 6. The impedance characteristics and fitted circuit model of the power inductors: (a) the input power inductors, (b) the measured impedance characteristics, (c) the fitted circuit simulation model, and (d) comparison of the measured and the fitted results.

D. PARASITIC PARAMETERS OF THE INDUCTOR

The input power inductors (L_1 ∼ L_3) used in the multiplexing converter are shown in Fig. 6(a), where two paralleled AWG13 enameled wires are wound with 56 turns on the high-flux magnetic powder core 58737 from the Magnetics.

The small signal impedance characteristics of $L_1 \sim L_3$ measured by an impedance analyzer are shown in Fig. 6(b). In the low frequency ranges (less than 300 kHz) the small signal inductance is about 631 μH. The first resonant frequency is about 570 kHz, and the equivalent parallel capacitance (*EPC*) is about 123 pF. Since the winding length of the power inductor is about 6 m, in the frequency ranges greater than 8 MHz, the impedance characteristic of the power inductor appears as the high-frequency transmission line effects of the windings.

Due to the large number of winding turns (56 turns) of the power inductor, and the winding structure and the high-frequency characteristics of the magnetic core cannot be modeled accurately, the impedance characteristics of the power inductor are fitted by an equivalent circuit in this paper. The fitted circuit simulation model of the L_1 is shown in Fig. 6(c). where the fitted parameter values are calculated from the low frequency to the high frequency according to the impedance characteristic resonance point frequency and resonance point amplitude obtained from the test [41]. The fitted impedance curve agrees well with the measured curve as shown in Fig. 6(d).

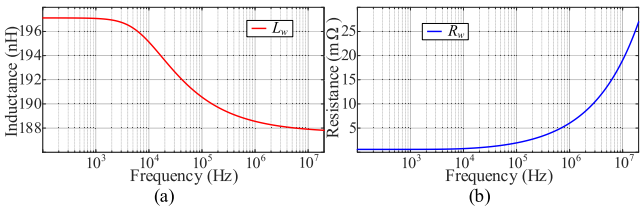

FIGURE 7. The parasitic parameters of the 6 mm^2 connecting wire with a length of 23 cm: (a) the simulated parasitic inductance, and (b) the simulated parasitic resistance.

E. PARASITIC PARAMETERS OF THE CONNECTING WIRE

The input capacitor (C_i), as shown in Fig. 2, is externally installed and connected with the multiplexing converter by a wire with a length of 23 cm and a cross section of 6 mm^2. The parasitic parameters of the connecting wire are extracted in the Q3D. The simulated parasitic inductance (L_w) is shown in Fig. 7(a). Due to the high-frequency skin effects, the L_w decreases slightly with the increase of frequency. The simulated parasitic resistance (R_w) is shown in the Fig. 7(b). Due to the high-frequency skin effects, the R_w increases significantly with the increase of frequency. In the conducted EMI test frequency ranges, the L_w plays a dominant role than the R_w, and the connecting wire can be approximated only by the parasitic inductance of 188 nH as shown in (3).

$$L_{w1} = L_{w2} = L_{w3} = 188 \quad \text{nH} \tag{3}$$

The dc capacitors (C_{dc1}, C_{dc2}, C_{dc3}) of the three DC/DC converters as shown in Fig. 2 are connected to the load by a wire with a length of 70 cm and a cross section of 6 mm^2. The connecting wire are modeled in the Q3D and can be approximated only by the parasitic inductance of 54 nH as shown in (4).

$$L_{wp1} = L_{wp2} = L_{wp3} = L_{wn1} = L_{wn2} = L_{wn3} = 54 \text{ nH} \tag{4}$$

F. PARASITIC PARAMETERS OF THE PCB LAYOUT

The PCB layout is exported to the Q3D as shown in Fig. 8(a) to extract the parasitic parameters, which has been discussed detailly in [40]. The layer stack-up of the power layout is shown in Fig. 8(b), where the layers of the positive dc-bus (DC+) and the negative dc-bus (DC-) are placed on the two adjacent layers of the PCB layout to increase the mutual couplings and reduce the parasitic loop inductances [42]. The parasitic parameters of the power layout can be neglected.

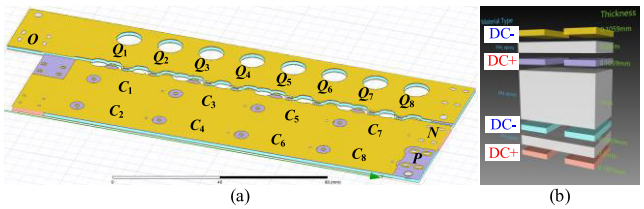

FIGURE 8. The parasitic parameters of the power layout: (a) the parasitic model in the Q3D, and (b) the layer stack-up of the power layout.

III. THE EMI ANALYSIS OF THE MULTIPLEXING CONVERTER IN THE DC/DC WORKING MODE

The conducted EMI characteristics of the single-channel DC/DC converter and the three-phase interleaved DC/DC converter are analyzed separately in this section.

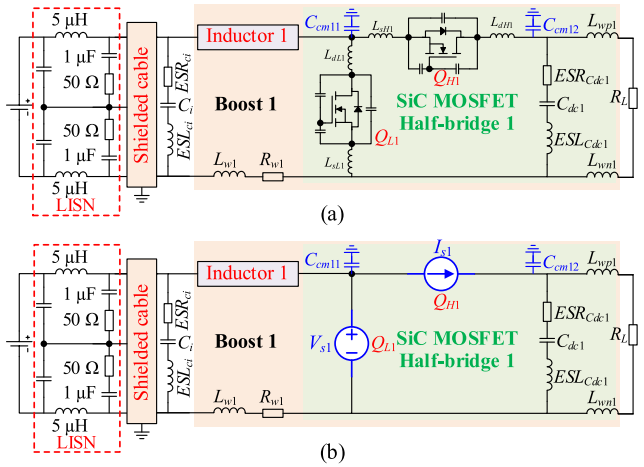

FIGURE 9. The conducted EMI analysis model of the single-phase DC/DC converter: (a) the equivalent circuit including parasitic parameters, and (b) the equivalent conducted EMI simulation model.

A. THE CONDUCTED EMI ANALYSIS OF THE SINGLE-PHASE DC/DC CONVERTER

The equivalent circuit of a single-phase DC/DC converter including parasitic parameters is shown in Fig. 9(a). According to the substitution theorem, if the two MOSFETs (Q_{H1} and Q_{L1}) along with their terminal parasitic parameters are

substituted by voltage and current sources that having the same voltage and current waveforms as the waveforms on the device terminals, the circuit behavior remains unchanged. Hence, the Q_{L1} and the Q_{H1} can be replaced by a voltage source V_{s1} and a current source I_{s1} respectively as shown in Fig. 9(b). The Q_{L1} and the Q_{H1} can also be replaced by the I_{s1} and the V_{s1} respectively, which will not affect the analyzed results.

The two equivalent noise sources (V_{s1} and I_{s1}) are considered to be not coupled and the effects of each noise source on the system conducted EMI characteristics can be analyzed separately according to the substitution theorem [7, 21, 24]. The frequency domain expressions of the CM noise $V_{CM1}(s)$ and the DM noise $V_{DM1}(s)$ of the single-phase DC/DC converter are shown in (5) and (6) respectively, where the $V_{s1}(s)$ and $I_{s1}(s)$ are the frequency domain expressions of the equivalent noise sources V_{s1} and I_{s1} respectively, the $F_{CM1\_v1}(s)$ and $F_{CM1\_i1}(s)$ are the transfer functions of the $V_{s1}(s)$ and $I_{s1}(s)$ to $V_{CM1}(s)$ respectively, and the $F_{DM1\_v1}(s)$ and $F_{DM1\_i1}(s)$ are the transfer functions of the $V_{s1}(s)$ and $I_{s1}(s)$ to $V_{DM1}(s)$ respectively.

$$V_{CM1}(s) = F_{CM1\_v1}(s) \cdot V_{s1}(s) + F_{CM1\_i1}(s) \cdot I_{s1}(s) \quad (5)$$

$$V_{DM1}(s) = F_{DM1\_v1}(s) \cdot V_{s1}(s) + F_{DM1\_i1}(s) \cdot I_{s1}(s) \quad (6)$$

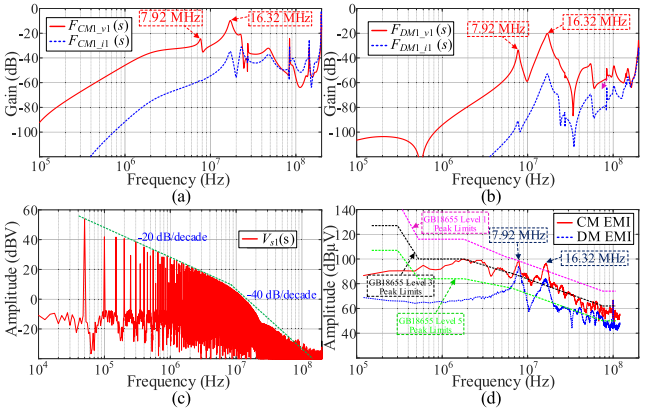

FIGURE 10. The conducted EMI characteristics of the single-phase DC/DC converter: (a) the simulated CM EMI characteristics, (b) the simulated DM EMI characteristics, (c) the spectrum of the measured noise voltage source, and (d) the CM and DM EMI test results.

The circuit simulation model equivalent to Fig. 9(b) is established in the Simplorer to analyze the $V_{CM1}(s)$ and the $V_{DM1}(s)$. The simulation results of the $F_{CM1\_v1}(s)$ and $F_{CM1\_i1}(s)$ are shown in Fig. 10(a), and the simulation results of the $F_{DM1\_v1}(s)$ and $F_{DM1\_i_1}(s)$ are shown in Fig. 10(b). The V_{s1} is the dominant noise source compared with the I_{s1}. At the same time, considering that the I_{s1} is difficult to be measured, the influence of the V_{s1} on the system EMI is analyzed below.

The frequency domain spectrum characteristics of the measured V_{s1} are shown in Fig. 10(c), and the measured CM and DM conducted EMI characteristics are shown in Fig. 10(d). The conducted EMI test platform will be shown later. The measured EMI spectra peaks come from the resonant peaks of the $F_{CM1\_v1}(s)$ and the $F_{DM1\_v1}(s)$, and the peak amplitudes exceed the GB/T 18655 level 1 peak limits.

The influences of different parasitic parameters as shown in Fig. 9(b) on the $F_{CM1\_v1}(s)$ and the $F_{DM1\_v1}(s)$ are simulated in the Simplorer. It is found that the spectra peaks of the $F_{CM1\_v1}(s)$ and the $F_{DM1\_v1}(s)$ are mainly caused by the L_{w1}. The influences of the L_{w1} on the $F_{CM1\_v1}(s)$ and the $F_{DM1\_v1}(s)$ are theoretically analyzed in the following.

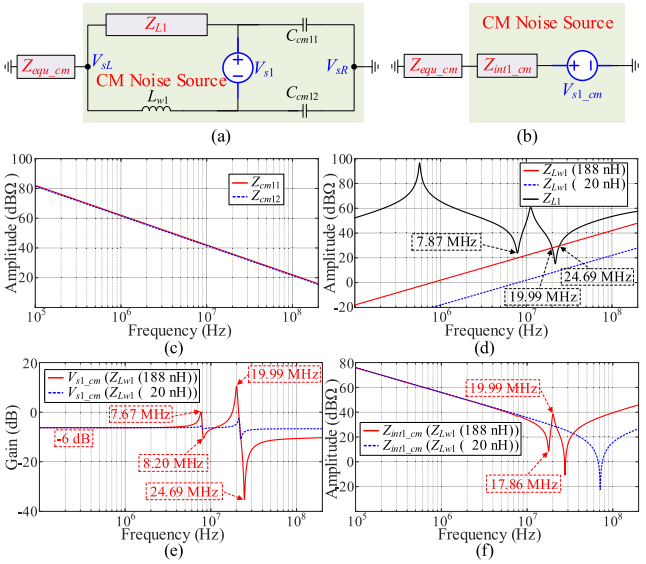

FIGURE 11. The CM EMI characteristics of the single-phase DC/DC converter: (a) the CM equivalent circuit model, (b) the simplified CM equivalent circuit model, (c) the impedance curves of the Z_{cm11} and the Z_{cm12}, (d) the impedance curves of the Z_{L1} and the Z_{Lw1}, (e) the characteristic of the V_{s1_cm}, and (f) the characteristics of the Z_{int1_cm}.

1) THE CM EMI CHARACTERISTICS

The EMI model as shown in Fig. 9(b) is simplified into the CM equivalent circuit model as shown in Fig. 11(a), where the CM impedance of the shielded cable and the LISN is represented by the Z_{equ_cm}, the impedance of the inductor 1 is represented by the Z_{L1}, the R_{w1} can be neglected compared with the L_{w1}, the input capacitor (C_i) and the dc capacitor (C_{dc1}) can be considered to be short-circuited, and the I_{s1} can be considered to be open-circuited.

A Wheatstone bridge circuit topology is formed by the L_1, the L_{w1}, the C_{cm11}, and the C_{cm12} as shown in Fig. 11(a). The equivalent voltage source V_{s1_cm} together with the equivalent internal resistance Z_{int1_cm} as shown in Fig. 11(b) can be used to express the port characteristics of the Wheatstone bridge. The frequency domain characteristics of the V_{s1_cm} and the Z_{int1_cm} are given below by numerical simulations.

In order to better explain their spectral characteristics, the impedance characteristics of the four arms of the Wheatstone bridge are given firstly. The impedance characteristics of the C_{cm11} (Z_{cm11}) and the C_{cm12} (Z_{cm12}) are shown in Fig. 11(c). The ratio of Z_{cm11} and Z_{cm12} does not change with frequency, so the midpoint potential of the right bridge arm of the Wheatstone bridge remains unchanged as $V_{sR} = 0.5V_{s1}$.

The impedance characteristics of the Z_{L1} and the Z_{Lw1} (188 nH and 20 nH) are shown in Fig. 11(d). Due to the *EPC* and the high-frequency transmission line effects, the Z_{L1} exhibits inductive or capacitive impedance characteristics in different frequency ranges, which will significantly affect the midpoint potential (V_{sL}) of the left arm of the Wheatstone bridge. For example, the impedances of the Z_{L1} and the Z_{Lw1} (188 nH) have the same amplitude but opposite phase directions at 19.99 MHz, and are in series resonance, which will significantly increase the V_{sL} and the V_{s1_cm} (V_{sL}-V_{sR}) as shown in Fig. 11(e). The impedances of the Z_{L1} and the Z_{Lw1} (188 nH) have the same amplitude and the same phase directions at 24.69 MHz, where the V_{sL} equals the V_{sR} and therefore the Wheatstone bridge is almost in a balanced state, which will significantly decrease the V_{s1_cm} as shown in Fig. 11(e).

The frequency domain characteristics of V_{s1_cm} is shown in Fig. 11(e). In the low frequency ranges (less than 6 MHz), the amplitude of Z_{L1} is much larger than Z_{Lw1}, as shown in Fig. 11(d), where the $V_{sL} \approx 0$ and the $V_{s1\_cm} \approx V_{sR} = 0.5V_{s1}$ (−6 dB). In the frequency ranges from 6 MHz to 20 MHz, if the Z_{L1} exhibits capacitive impedance, the amplitude of V_{s1_cm} will increase, and the peak value appears at the series resonance frequency (19.99 MHz). If the Z_{L1} exhibits inductive impedance, the amplitude of V_{s1_cm} will decrease.

The frequency domain characteristics of Z_{int1_cm} are shown in Fig. 11(f). The Z_{int1_cm} will be increased near the series resonance frequency (19.99) to reduce the system CM EMI, but Z_{int1_cm} will be reduced in the frequency ranges from 8 MHz to 17.86 MHz, which will increase the CM EMI in this frequency band.

The spectra peaks of the V_{s1_cm} can be suppressed by reducing the impedance of the Z_{Lw1} or increasing the impedance of the Z_{L1}. For example, there are no intersections between the Z_{L1} and the Z_{Lw1} (20 nH), therefore the spectra peaks of the V_{s1_cm} are significantly suppressed as shown in Fig. 11(c) and the Z_{int1_cm} is increased in the frequency ranges from 8 MHz to 17.86 MHz, which will reduce the CM EMI in this frequency band. In addition, the EPC of the power inductor (L_1) can be reduced by changing the winding structure, which will increase the high-frequency amplitudes of the Z_{L1} and therefore suppress the spectra peaks of the V_{s1_cm}.

2) THE DM EMI CHARACTERISTICS

The EMI model as shown in Fig. 9(b) is simplified into the DM equivalent circuit model as shown in Fig. 12(a), where the DM impedance of the shielded cable and the LISN is represented by the Z_{equ_dm}, the impedance of the inductor 1 is represented by the Z_{L1}, the R_{w1} can be neglected compared with the L_{w1}, the dc capacitor (C_{dc1}) can be considered to be short-circuited, and the I_{s1} can be considered to be open-circuited.

The equivalent voltage source V_{s1_dm} together with the equivalent internal resistance Z_{int1_dm} as shown in Fig. 12(b) can be used to express the DM noise source. The frequency

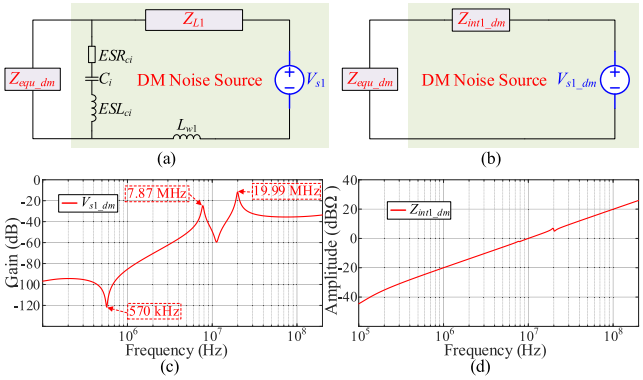

FIGURE 12. The DM EMI characteristics of the single-phase DC/DC converter: (a) the DM equivalent circuit model, (b) the simplified DM equivalent circuit model, (c) the characteristic of the V_{s1_dm}, and (d) the characteristic of the Z_{int1_dm}.

domain characteristics of the V_{s1_dm} and the Z_{int1_dm} is given below by numerical simulations.

The frequency domain characteristics of V_{s1_dm} are shown in Fig. 12(c), which mainly depends on the Z_{L1} in the frequency ranges greater than 570 kHz. The higher the Z_{L1}, the smaller the V_{s1_dm}. The high-frequency amplitudes of the Z_{L1} can be increased by optimizing the winding structures of the power inductors, which will be shown later.

The frequency domain characteristics of Z_{int1_dm} are shown in Fig. 12(d). which mainly depends on the input capacitance (Z_{ci}). Although the Z_{int1_dm} increases with frequency at a rate of 20 dBΩ/decade, the absolute value of the Z_{int1_dm} in the entire conducted interference frequency ranges can be neglected compared with the Z_{equ_dm}, which is greater than 40 dBΩ.

B. THE EMI SUPPRESSION OF THE SINGLE-PHASE DC/DC CONVERTER

The conducted EMI test platform is discussed firstly in this section. Then, the two EMI suppression measures by reducing the L_{w1} and reducing the EPC of the L_1 are given and verified by experiments.

1) THE CONDUCTED EMI TEST PLATFORM

The conducted EMI experimental test platform of the multiplexing converter in the DC/DC working mode is shown in Fig. 13(a), which mainly includes the DC LISN, the CM and DM noise separator, the mixed domain oscilloscope, the grounded copper plate, and the prototype of the multiplexing converter. The arrangement of the test platform is based on the GB/T 18655-2018, where the on-board battery is connected to a 5 μH/50 Ω DC LISN, and then connected to the multiplexing converter through a pair of shielded cable.

The conducted EMI test results of the DC LISN+ (the 336 V input phase) is shown in Fig. 13(b), where the input voltage (V_{in}), the inductor current (I_L), the output voltage (V_{dc}) and the midpoint voltage (V_{s1}) are measured

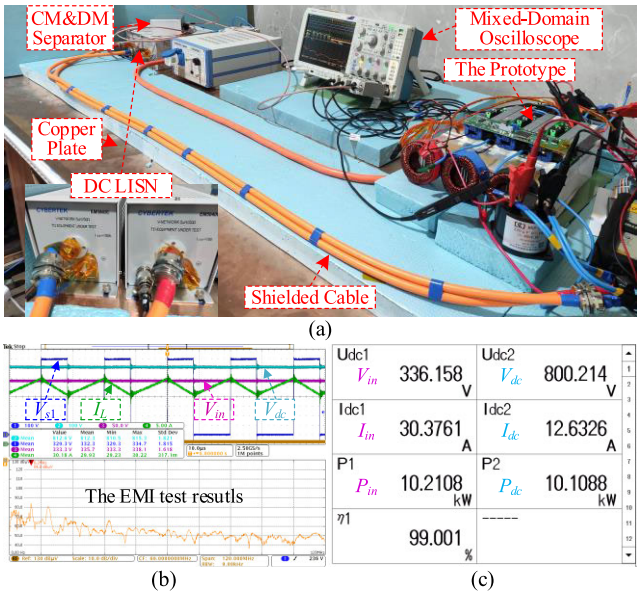

FIGURE 13. The conducted EMI test platform of the multiplexing converter in the DC/DC working mode: (a) the test platform, (b) the experimental test results, and (c) the rated working states.

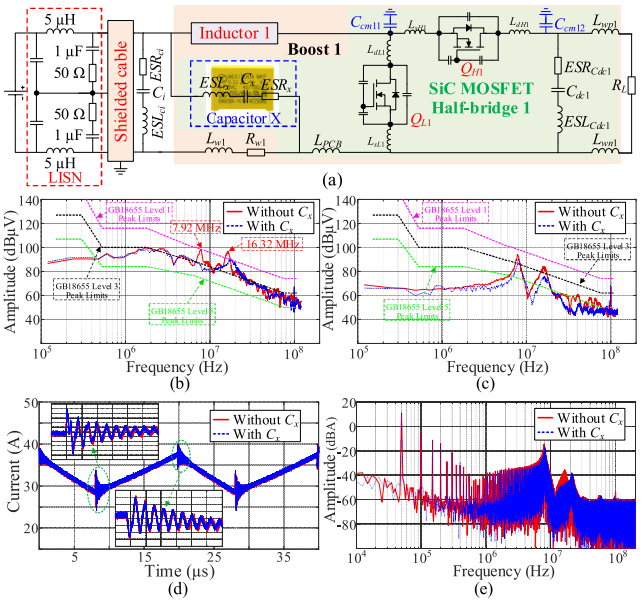

FIGURE 14. The EMI suppression by adding small X capacitor: (a) the equivalent circuit with the added small capacitor, (b) the comparison of CM EMI test results, (c) the comparison of DM EMI test results, (d) the comparison of the measured inductor currents, and (e) the comparison of the spectrum of the measured inductor currents.

simultaneously. The test results will be post-processed in MATLAB for better comparison. The rated working states of the single-phase DC/DC converter measured by the power analyzer WT5000 are shown in Fig. 13(c), where the $V_{in} =$ 336 V, the $I_L = 30.76$ A, the $V_{dc} = 800$ V, and the switching frequency $f = 50$ kHz.

The conducted EMI test results are already shown in Fig. 10(d), where the CM EMI occupies the main component in the entire EMI test frequency ranges. The resonance point frequency of the EMI test results matches well with the resonance frequency obtained by simulation, and the amplitudes at the resonance point frequencies exceed the GB/T 18655-2018 level 1 peak limits.

2) THE EMI SUPPRESSION BY ADDING SMALL X CAPACITOR

As shown in Fig. 14(a), a small packaged capacitor (C_x), such as a 0.47 μF X capacitor, is installed directly on the paralleled SiC MOSFET half-bridge unit. Due to the layout parasitic parameters of the PCB, there is a parasitic inductance (L_{PCB}) in the negative input power line between the C_x and the Q_{L1}, which is about 20 nH and much smaller than the L_{w1} (188 nH). The L_{w1} in the CM and DM equivalent circuit model as shown in Fig. 11(a) and Fig. 12(a) can now be replaced by the L_{PCB}.

The comparison of the CM EMI test results with and without the C_x is shown in Fig. 14(b), which eliminates the resonance point at the 7.92 MHz and decreases the amplitude of the resonance point at the 16.32 MHz by 6.02 dB.

The comparison of the DM EMI test results with and without the C_x is shown in Fig. 14(c), which decreases slightly the DM EMI since the DM EMI mainly depends on the impedance characteristics of the power inductor.

The comparison of the measured inductor currents with and without the C_x is shown in Fig. 14(d), and the comparison of the spectrum characteristics is shown in Fig. 14(e). The added C_x has almost no effect on the inductor current waveform.

3) THE EMI SUPPRESSION BY THE OPTIMIZATION OF THE WINDING METHOD OF THE POWER INDUCTOR

The schematic diagram and prototype of the power inductor with the traditional winding method are shown in Fig. 15(a), where two paralleled AWG13 enameled wires are wound with 56 turns on the high-flux magnetic powder core 58737 from the Magnetics. Because the single layer of the core 58737 can be wound up to 70 turns of the AWG13 Enameled wire, so 2 strands of 56 turns (112 turns in total) AWG13 enameled wire needs to be wound in two layers, where there is overlap between the input and output ports of the inductor.

The schematic diagram and prototype of the power inductor with the optimized winding method are shown in Fig. 15(b), where there is no overlap between the input and output ports of the inductor and can be considered as the single layer winding inductor. Single layer winding method provides smaller EPC and therefore provide better high frequency performance [34]. The small signal impedance characteristics of the power inductors using two winding strategies are shown in Fig. 15(c), and the compar-

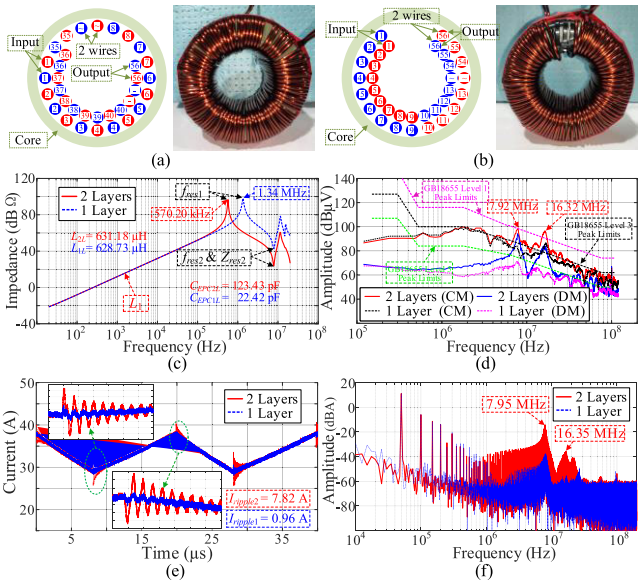

FIGURE 15. The EMI suppression by the optimization of the winding strategy of the power inductor: (a) the traditional inductor winding strategy, (b) the optimized inductor winding strategy, (c) the comparison of measured impedance characteristics, (d) the comparison of EMI test results, (e) the comparison of the measured inductor currents, and (f) the comparison of the spectrum of measured inductor currents.

TABLE 1. The parameters of the power inductors with different winding methods.

	L_1 (μH)	f_{res1} (MHz)	EPC (pF)	f_{res2} (MHz)	Z_{res2} (dBΩ)
2 Layers	631.18	0.57	123.43	7.87	23.75
1 Layer	628.73	1.34	22.42	7.94	42.89

ison of the different parameters is shown in in TABLE 1. The different winding strategies have almost no effect on the low-frequency inductance (L_1), while the EPC of the 1-layer winding method is reduced to one-sixth of the 2-layers winding method and the high-frequency impedance (Z_{res2}) is increased by 19.14 dB.

The comparison of the conducted EMI test results using two different winding power inductors is shown in Fig. 15 (d). The resonance point at the 7.92 MHz of the CM EMI is eliminated, and the amplitude of the resonance point at the 16.32 MHz is reduced by 10.42 dB. Since the DM EMI depends on the high-frequency impedance of the inductor, changing the power inductor winding method significantly suppresses the high-frequency DM EMI level.

The comparison of the measured inductor currents with two winding methods is shown in Fig. 15(e). The transient current oscillation amplitudes are significantly suppressed from 7.82 A to 0.96 A. The comparison of the spectrum characteristics of the inductor currents is shown in Fig. 15(f), where the 1-layer winding method significantly suppresses the amplitude in the frequency ranges from 1 MHz to 30 MHz.

C. THE EMI ANALYSIS OF THE THREE-PHASE INTERLEAVED DC/DC CONVERTER

The conducted EMI characteristics of the three-phase interleaved DC/DC converter composed of three identical single-channel DC/DC converters are analyzed and tested in this sub-section.

1) THE CONDUCTED EMI ANALYSIS

The equivalent circuit of the three-phase interleaved DC/DC converter including parasitic parameters is already shown in Fig. 2. According to the substitution theorem, if the MOSFETs ($Q_{L1} \sim Q_{L3}$ and $Q_{H1} \sim Q_{H3}$) along with their terminal parasitic parameters are substituted by the equivalent voltage sources ($V_{s1} \sim V_{s3}$) and current sources ($I_{s1} \sim I_{s3}$) that having the same voltage and current waveforms as the waveforms on the device terminals, as shown in Fig. 16(a), the circuit behavior remains unchanged.

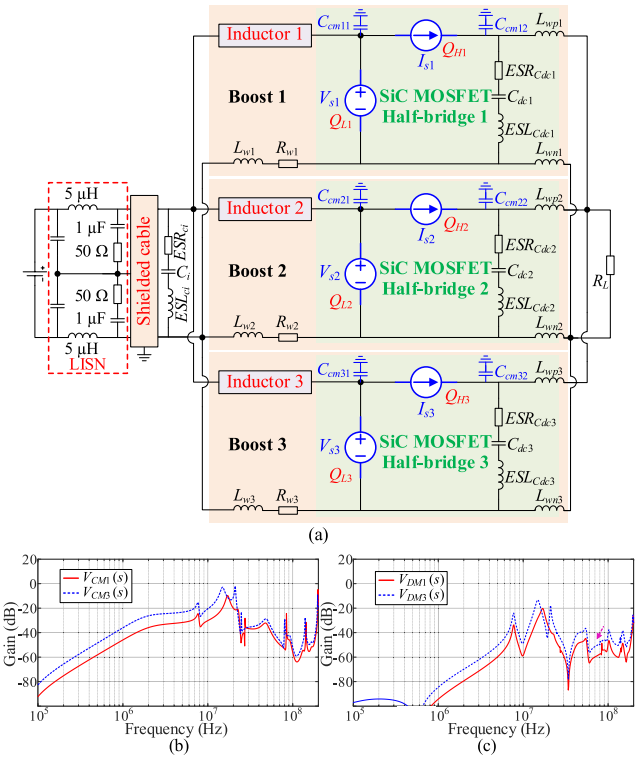

FIGURE 16. The conducted EMI characteristic of the three-phase interleaved DC/DC converter: (a) the equivalent conducted EMI analysis model, (b) the simulated CM EMI characteristics, and (c) the simulated DM EMI characteristic.

The different noise sources ($V_{s1} \sim V_{s3}$ and $I_{s1} \sim I_{s3}$) are considered to be not coupled and the effects of each noise source on the system conducted EMI characteristics can be analyzed separately according to the substitution theorem. The frequency domain expressions of the CM noise V_{CM3}(s) and the DM noise V_{DM3}(s) of the three-phase DC/DC converter are shown in (7) and (8) respectively, where the V_{s1}(s) $\sim$ V_{s3}(s) and the I_{s1}(s) $\sim$ I_{s3}(s) are the frequency domain expressions of the equivalent noise sources $V_{s1} \sim V_{s3}$ and $I_{s1} \sim I_{s3}$ respectively, the F_{CM_v1}(s) $\sim$ F_{CM_v3}(s) and the

$F_{CM\_i1}(s) \sim F_{CM\_i3}(s)$ are the transfer functions of the $V_{s1} \sim V_{s3}$ and the $I_{s1} \sim I_{s3}$ to the $V_{CM3}(s)$ respectively, and the $F_{DM\_v1}(s) \sim F_{DM\_v3}(s)$ and the $F_{DM\_i1}(s) \sim F_{DM\_i3}(s)$ are the transfer functions of the $V_{s1} \sim V_{s3}$ and the $I_{s1} \sim I_{s3}$ to the $V_{DM3}(s)$ respectively.

$$\begin{aligned} V_{CM3}(s) = {} & F_{CM\_v1}(s) \cdot V_{s1}(s) + F_{CM\_i1}(s) \cdot V_{i1}(s) \\ & + F_{CM\_v2}(s) \cdot V_{s2}(s) + F_{CM\_i2}(s) \cdot V_{i2}(s) \\ & + F_{CM\_v3}(s) \cdot V_{s3}(s) + F_{CM\_i3}(s) \cdot V_{i3}(s) \quad (7) \\ V_{DM3}(s) = {} & F_{DM\_v1}(s) \cdot V_{s1}(s) + F_{DM\_i1}(s) \cdot V_{i1}(s) \\ & + F_{DM\_v3}(s) \cdot V_{s3}(s) + F_{DM\_i2}(s) \cdot V_{i2}(s) \\ & + F_{DM\_v2}(s) \cdot V_{s2}(s) + F_{DM\_i3}(s) \cdot V_{i3}(s) \quad (8) \end{aligned}$$

The circuit simulation model equivalent to Fig. 16(a) is established in the Simplorer to analyze the $V_{CM3}(s)$ and the $V_{DM3}(s)$.

The simulation result of the $V_{CM3}(s)$ is shown in Fig. 16(b), which also shows the $V_{CM1}(s)$ for the single-phase DC/DC converter. Since the system CM loop impedance depends mainly on the CM capacitance in the 20 MHz frequency ranges, the $V_{CM3}(s)$ is higher than the $V_{CM1}(s)$ by 9.5 dB. The simulation result of the $V_{DM3}(s)$ is shown in Fig. 16(c), which also shows the $V_{DM1}(s)$ for the single-phase DC/DC converter. The $V_{DM3}(s)$ is higher than the $V_{DM1}(s)$ by 9.5 dB in the entire conducted EMI test frequency ranges.

2) THE CONDUCTED EMI TEST

The conducted EMI experimental test platform of the multiplexing converter in the three-phase interleaved DC/DC working mode is the same as shown in Fig. 13(a).

Firstly, the rated working states are measured by the power analyzer WT5000 as shown in Fig. 17(a), where the $V_{in} = 336$ V, the $V_{dc} = 800$ V, the total input power $P_{intot} = 31.87$ kW, and the switching frequency $f = 50$ kHz. The measured three-phase interleaved inductor currents of the traditional 2-layer winding power inductors are shown in Fig. 17(b), where the phase of the inductor current lags each other by 120° in sequence and the average inductor current is basically the same by using the voltage and current double closed-loop control method.

Secondly, the conducted EMI characteristics of the three-phase interleaved DC/DC converter under the rated working states (30 kW) are measured and compared with the single-phase DC/DC converter (10 kW) as shown in Fig. 17(c) and (d). The CM EMI of the three-phase DC/DC converter is higher than the single-phase converter by 9.5 dB in the low frequency ranges as shown in Fig. 17(c), which agrees with the simulated results as shown in Fig. 16(b) in the frequency ranges from 150 kHz to 20 MHz.

Finally, the conducted EMI characteristics of the three-phase interleaved DC/DC converter are measured with the added small X capacitors and the optimized 1-layer winding inductors. The conducted EMI test results of LISN+ (336 V input phase) and LISN- (0 V input phase) are shown in Fig. 17(e), which are basically the same levels in the

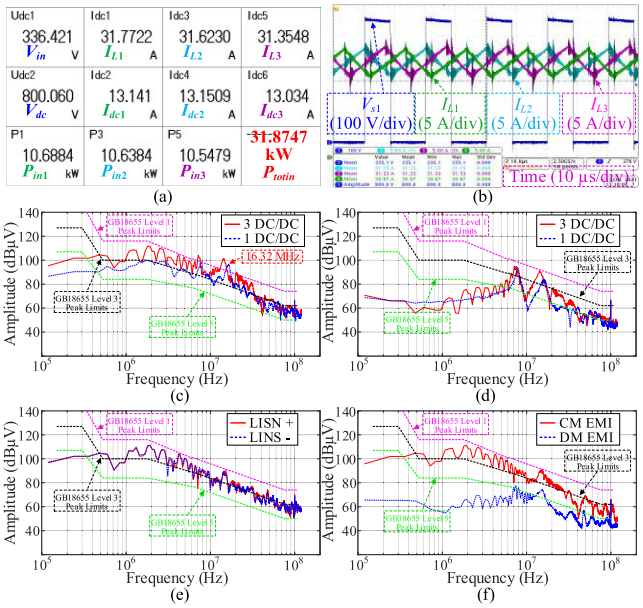

FIGURE 17. The conducted EMI test of the multiplexing converter in the three-phase interleaved DC/DC working mode: (a) the rated working states, (b) the experimental test waveforms, (c) the comparison of CM EMI test results, (d) the comparison of DM EMI test results, (e) the LISN+ and LISN- EMI test results, and (f) the CM and DM EMI test results.

conducted EMI test frequency ranges (150 kHz ~ 108 MHz). The comparison of CM and DM conducted EMI test results are shown in Fig. 17(f), where the CM EMI occupies the main component in the entire conducted EMI test frequency ranges.

Although the conducted EMI test results of the multiplexing converter in the three-phase interleaved DC/DC working mode meet the GB/T 18655-2018 level 1 peak limits, the margin is less than 6 dB in the frequency ranges from 1.5 MHz to 6 MHz, and the margin is less than 1 dB is at the 4.32 MHz and the 15.12 MHz.

In the future, as the current capacity of the SiC devices increases, the number of power devices in the SiC paralleled half-bridge unit can be reduced, which can reduce the system CM capacitance and therefore the conducted EMI levels.

IV. THE EMI ANALYSIS OF THE MULTIPLEXING CONVERTER IN THE OBC WORKING MODE

A high-frequency isolation transformer is usually used in the traditional OBC to achieve the electrical isolation between the primary AC power grid and the secondary on-board high-voltage battery, which can reduce the influence of secondary parasitic parameters on the conducted EMI of the AC grid. In order to improve the power density of the system, there are no isolations between the on-board battery and the AC grid in the OBC working mode of the multiplexing converter, so it is necessary to analyze the conducted EMI characteristics of the non-isolated OBC.

A. THE AC GRID SIDE EMI ANALYSIS OF THE OBC

The equivalent circuit of the OBC including parasitic parameters is shown in Fig. 18(a). In this paper, the front-stage

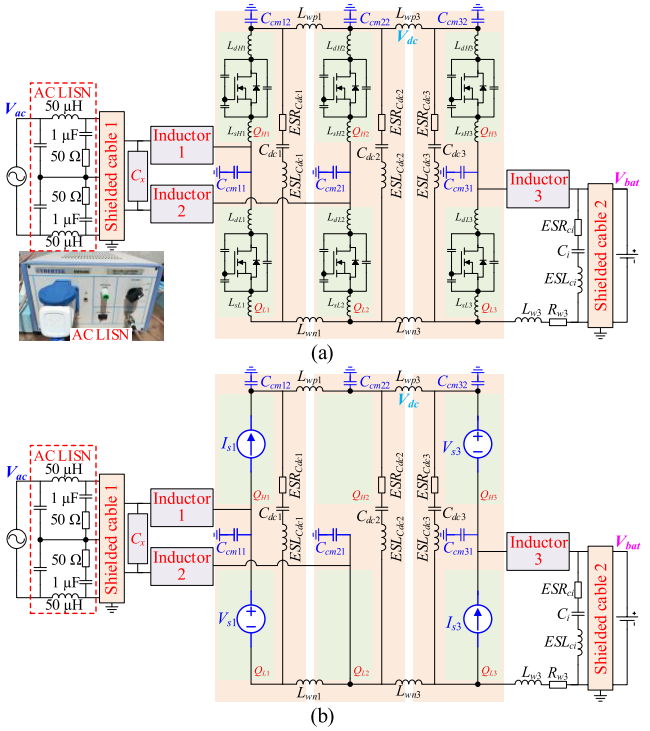

FIGURE 18. The conducted EMI analysis model of the AC grid side of the OBC: (a) the equivalent circuit including parasitic parameters, and (b) the equivalent conducted EMI simulation model.

AC/DC converter of the OBC uses the bridgeless power factor correction (BLPFC) control method. According to the substitution theorem, the equivalent conducted EMI simulation model of the OBC in the positive half cycle of the grid voltage is shown in Fig. 18(b), where the Q_{L1} and the Q_{H1} can be substituted by the equivalent voltage source V_{s1} and the current source I_{s1} respectively, the Q_{H2} remains in the open-circuit state, Q_{L2} remains in the short-circuit state, and the Q_{L3} and the Q_{H3} can be substituted by the equivalent current source I_{s3} and the voltage source V_{s3} respectively.

The different noise sources are considered to be not coupled and the effects of each noise source on the system conducted EMI characteristics can be analyzed separately according to the substitution theorem. The frequency domain expressions of the CM noise $V_{CMac}(s)$ and the DM noise $V_{DMac}(s)$ of the AC grid side of the OBC are shown in (9) and (10) respectively, where the $V_{s1}(s)$, $V_{s3}(s)$, $I_{s1}(s)$, and $I_{s3}(s)$ are the frequency domain expressions of the equivalent noise sources V_{s1}, V_{s3}, I_{s1}, and I_{s3} respectively, the $F_{CMac\_v1}(s)$, $F_{CMac\_v3}(s)$, $F_{CMac\_i1}(s)$, and $F_{CMac\_i3}(s)$ are the transfer functions of the V_{s1}, V_{s3}, I_{s1}, and I_{s3} to the $V_{CMac}(s)$ respectively, and the $F_{DMac\_v1}(s)$, $F_{DMac\_v3}(s)$, $F_{DMac\_i1}(s)$, and $F_{DMac\_i3}(s)$ are the transfer functions of the V_{s1}, V_{s3}, I_{s1}, and I_{s3} to the $V_{DMac}(s)$ respectively.

$$V_{CMac}(s) = F_{CMac\_v1}(s) \cdot V_{s1}(s) + F_{CMac\_i1}(s) \cdot I_{s1}(s) + F_{CMac\_v3}(s) \cdot V_{s3}(s) + F_{CMac\_i3}(s) \cdot I_{s3}(s) \quad (9)$$

$$V_{DMac}(s) = F_{DMac\_v1}(s) \cdot V_{s1}(s) + F_{DMac\_i1}(s) \cdot I_{s1}(s) + F_{DMac\_v3}(s) \cdot V_{s3}(s) + F_{DMac\_i3}(s) \cdot I_{s3}(s) \quad (10)$$

The circuit simulation model equivalent to Fig. 18(b) is established in the Simplorer to analyze the transfer functions of the $V_{s1}(s)$, $V_{s3}(s)$, $I_{s1}(s)$, and $I_{s3}(s)$ to the $V_{CMac}(s)$ and the $V_{DMac}(s)$ respectively.

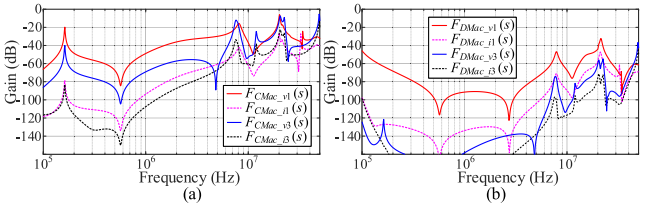

FIGURE 19. The simulated conducted EMI characteristics of the AC grid side of the OBC: (a) the simulated CM EMI characteristics, and (b) the simulated DM EMI characteristics.

The simulation results of the $F_{CMac\_v1}(s)$, $F_{CMac\_v3}(s)$, $F_{CMac\_i1}(s)$, and $F_{CMac\_i3}(s)$ are shown in Fig. 19(a), where the impacts of the $V_{s1}(s)$ and $V_{s3}(s)$ on the system CM EMI are much higher than the $I_{s1}(s)$ and $I_{s3}(s)$, and the $V_{s1}(s)$ is the main noise source in the frequency ranges below 7 MHz. The simulation results of the $F_{DMac\_v1}(s)$, $F_{DMac\_v3}(s)$, $F_{DMac\_i1}(s)$, and $F_{DMac\_i3}(s)$ are shown in Fig. 19(b), where the $V_{s1}(s)$ is the dominant noise source in the entire conducted EMI test frequency ranges (150 kHz $\sim$ 30 MHz).

Since there is a X capacitor (0.47 μF) installed on the input side of the OBC as shown in Fig. 18(a), the CM EMI occupies the main component by comparing Fig. 19(a) and (b). Therefore, only the influences of the V_{s1} and the V_{s3} on the system conducted EMI characteristics are analyzed below. The V_{s1} is the main noise source of the front-stage AC/DC converter, and the V_{s3} is the main noise source of the post-stage buck converter.

1) THE CONDUCTED EMI ANALYSIS OF THE FRONT-STAGE AC/DC CONVERTER

This subsection analyzes the influence of the main noise source V_{s1} on the CM and DM EMI characteristics of the grid side of the OBC, where the I_{s1} and I_{s3} can be considered to be open-circuited, the V_{s3} can be considered to be shorted-circuited, as shown in Fig. 20.

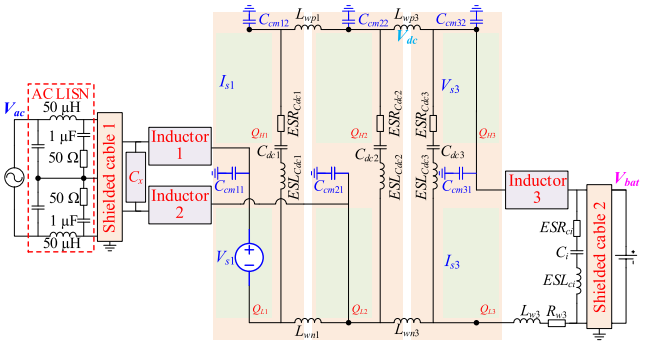

FIGURE 20. The conducted EMI analysis model of the noise source V_{s1} of front-stage AC/DC converter of the OBC.

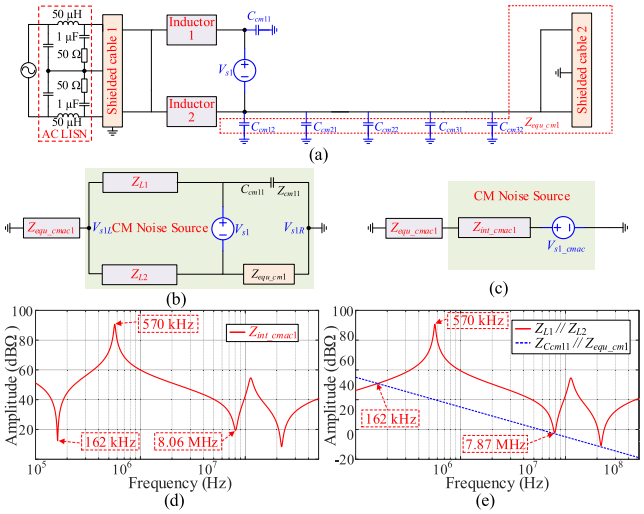

FIGURE 21. The CM EMI characteristics of the noise source V_{s1} of front-stage AC/DC converter of the OBC: (a) the simplified CM EMI analysis model, (b) the CM EMI equivalent circuit model, (c) the simplified CM EMI equivalent circuit model, (d) the characteristics of the Z_{int_cmac1}, and (e) the impedances of the Z_{L1} // Z_{L2} and the Z_{Ccm11} // Z_{equ_cm1}.

Firstly, the influences of different parasitic parameters as shown in Fig. 20 on the $F_{CMac\_v1}(s)$ are simulated in the Simplorer, which shows that the capacitors (C_x, C_i, C_{dc1}, C_{dc2}, C_{dc3}) and the parasitic inductances (L_{wp1}, L_{wn1}, L_{wp2}, L_{wn2}, L_{w3}) can be considered to be short-circuited in the conducted EMI test frequency ranges (150 kHz ∼ 30 MHz). The simplified CM EMI analysis model is shown in Fig. 21(a), which can be represented by Fig. 21(b), where the CM impedances of the shielded cable 1 and the LISN are represented by the Z_{equ_cmac1}, the impedances of the inductor 1 and 2 are represented by the Z_{L1} and the Z_{L2} respectively, the CM impedances of the shielded cable 2 and the parasitic CM capacitance excluding the C_{cm11} are represented by the Z_{equ_cm1}.

A Wheatstone bridge circuit topology is formed by the Z_{L1}, the Z_{L2}, the Z_{cm11}, and the Z_{equ_cm1} as shown in Fig. 21(b). The equivalent voltage source V_{s1_cmac} together with the equivalent internal resistance Z_{int_cmac1} as shown in Fig. 21(c) can be used to express the port characteristics of the Wheatstone bridge. The frequency domain characteristics of the V_{s1_cmac} and the Z_{int_cmac1} are analyzed below.

Since the Z_{L1} and the Z_{L2} are basically the same, the midpoint potential of the left bridge arm of the Wheatstone bridge remains unchanged as $V_{s1L} = 0.5V_{s1}$. Without considering the CM impedance of the shielded cable 2, the midpoint potential of the right bridge arm of the Wheatstone bridge remains unchanged as $V_{s1R} = 0.17V_{s1}$. Therefore, the frequency domain characteristics of the V_{s1_cmac} (V_{s1L}- V_{s1R}) can be considered unchanged.

The simulated frequency domain characteristics of the Z_{int_cmac1} are shown in Fig. 21(d). The paralleled impedance characteristics of the left arm of the Wheatstone bridge (Z_{L1} // Z_{L2}) and the paralleled impedance characteristics of the right arm (Z_{Ccm11} // Z_{equ_cm1}) are shown in Fig. 21(e). Comparing the Fig. 21(d) and (e), it can be seen that the impedance characteristic of Z_{int_cmac1} in the low frequency ranges (less than 162 kHz) depends on the CM capacitance (Z_{Ccm11} // Z_{equ_cm1}). Therefore, compared with the isolated OBC, the parasitic CM capacitance of the battery side of the non-isolated OBC will increase the system CM EMI in the low frequency ranges and the insertion loss requirement of the grid-side EMI filter. The impedance characteristics of Z_{int_cmac1} in the remaining frequency ranges depend on the input power inductors (Z_{L1}//Z_{L2}), which can be increased to reduce the system high frequency CM EMI by optimizing the inductor winding methods.

Secondly, the EMI simulation model as shown in Fig. 20 is simplified into the DM equivalent circuit model as shown in Fig. 22(a), where the DM impedance of the shielded cable 1 and the LISN is represented by the Z_{equ_dmac1}. The equivalent voltage source V_{s1_dmac} together with the equivalent internal resistance Z_{int1_dmac} as shown in Fig. 22(b) can be used to express the DM noise source. The frequency domain characteristics of the V_{s1_dmac} and the Z_{int1_dmac} are given below by numerical simulation.

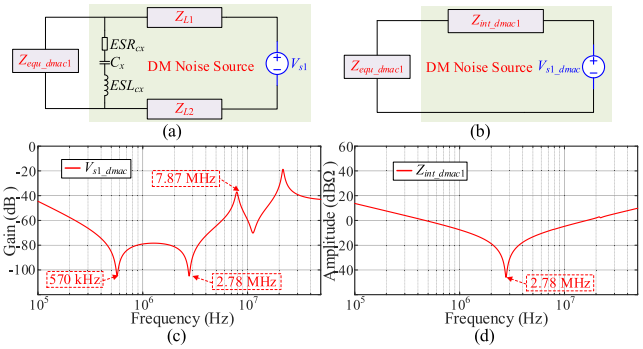

FIGURE 22. The DM EMI characteristics of the noise source V_{s1} of front-stage AC/DC converter of the OBC: (a) the DM equivalent circuit model, (b) the simplified DM equivalent circuit model, (c) the characteristic of the V_{s1_dmac}, and (e) the characteristics of the Z_{int_dmac1}.

The frequency domain characteristics of V_{s1_dmac} are shown in Fig. 22(c). In the low frequency ranges (less than 570 kHz) and high frequency ranges (greater than 2.78 MHz), it depends on the impedance of the series connected input inductor (Z_{L1} and Z_{L2}). The high-frequency amplitudes of the Z_{L1} and the Z_{L2} can be increased by optimizing the winding structures of the power inductors. In the frequency ranges from 570 kHz to 2.78 MHz, it depends on the C_x.

The frequency domain characteristics of the Z_{int_dmac1} are shown in Fig. 22(d), which mainly depends on the impedance characteristics of the C_x. The Z_{int_dmac1} can be neglected in the entire conducted EMI test frequency ranges compared with the Z_{equ_dmac1}, which is greater than 40 dBΩ.

2) THE CONDUCTED EMI ANALYSIS OF THE POST-STAGE BUCK CONVERTER

This subsection analyzes the influence of the main noise source V_{s3} on the CM EMI characteristics of the grid side of

the OBC, where the I_{s1} and I_{s3} can be considered to be open-circuited, the V_{s1} can be considered to be shorted-circuited, as shown in Fig. 23.

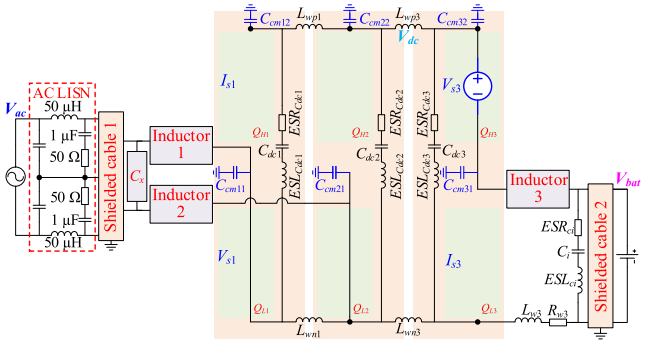

FIGURE 23. The conducted EMI analysis model of the noise source V_{s3} of post-stage buck converter of the OBC.

The influences of different parasitic parameters as shown in Fig. 23 on the F_{CMac_v3}(s) are simulated in the Simplorer, which shows that the capacitors (C_x, C_i, C_{dc1}, C_{dc2}, C_{dc3}) and the parasitic inductances (L_{wp1}, L_{wn1}, L_{wp2}, L_{wn2}) can be considered to be short-circuited in the entire conducted EMI test frequency ranges (150 kHz $\sim$ 30 MHz). The simplified CM EMI analysis model is shown in Fig. 24(a), which can be represented by Fig. 24(b), where the CM impedances of the shielded cable 1 and the LISN are represented by the Z_{equ_cmac3}, the impedances of the paralleled inductor 1 and 2 are represented by the $Z_{L1}//Z_{L2}$, the impedance of the inductor 3 is represented by the Z_{L3}, the CM impedance of the shielded cable 2 is represented by the Z_{ocable}, and the parasitic CM capacitance excluding the C_{cm31} are represented by the Z_{equ_cm3}.

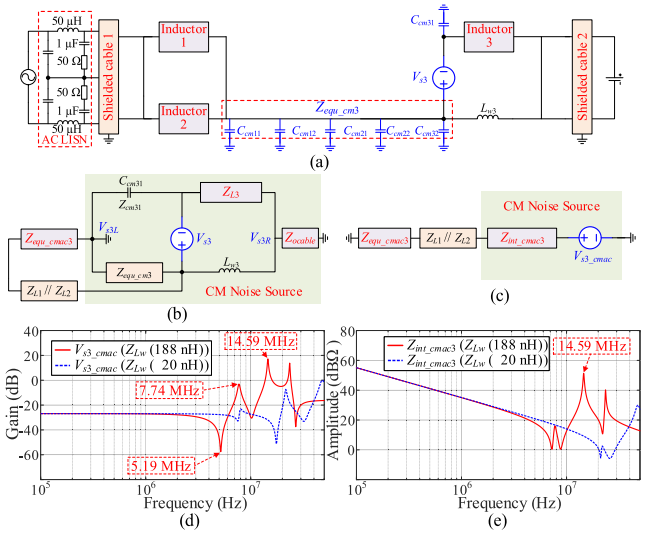

FIGURE 24. The CM EMI characteristics of the noise source V_{s3} of post-stage buck converter of the OBC: (a) the simplified CM EMI analysis model, (b) the CM EMI equivalent circuit model, (c) the simplified CM EMI equivalent circuit model, (d) the characteristics of the V_{s3_cmac}, and (e) the characteristics of the Z_{int_cmac3}.

As shown in the Fig. 24(b), The Z_{equ_cmac3} is connected in series with the $Z_{L1}//Z_{L2}$ and then connected in parallel with the Z_{equ_cm3}. Therefore, the Z_{equ_cm3} can help reduce the CM EMI. The CM EMI can be suppressed by increasing the impedance of the $Z_{L1}//Z_{L2}$, where the high-frequency impedance of the $Z_{L1}//Z_{L2}$ can be increased by optimizing the winding structures of the power inductors.

A Wheatstone bridge circuit topology is formed by the Z_{Lw3}, the Z_{L3}, the Z_{cm31}, and the Z_{equ_cm3} as shown in Fig. 24(b), where the port characteristics of the Z_{equ_cm3} affect the CM EMI. The equivalent voltage source V_{s3_cmac} together with the equivalent internal resistance Z_{int_cmac3} as shown in Fig. 24(c) can be used to express the port characteristics of the Z_{equ_cm3}. The frequency domain characteristics of the V_{s3_cmac} and the Z_{int_cmac3} are given below through numerical simulations as shown in Fig. 24(d) and (e). As analyzed before, the series resonance caused by the L_{w3} and the high-frequency transmission line effects of the L_3 will increase the CM EMI in a specific frequency ranges, which can be suppressed by optimizing the high-frequency impedance characteristics of the inductors and by adding small packaged capacitors.

Considering the V_{s1}(s) of the front-stage AC/DC converter is the dominant DM noise source in the entire conducted frequency ranges (150 kHz $\sim$ 30 MHz) as shown in Fig. 19(b), the influence of the V_{s3} on the DM EMI characteristics of the grid side of the OBC is not analyzed.

B. THE AC GRID SIDE EMI TESTS OF THE OBC

The conducted EMI experimental test platform of the multiplexing converter in the OBC working mode is almost the same as shown in Fig. 13(a), where there is an isolation transformer (10 kVA) installed between the AC grid and the AC LISN (50 μH/50 Ω) to prevent the large CM capacitance of the LISN from causing the circuit breaker protection.

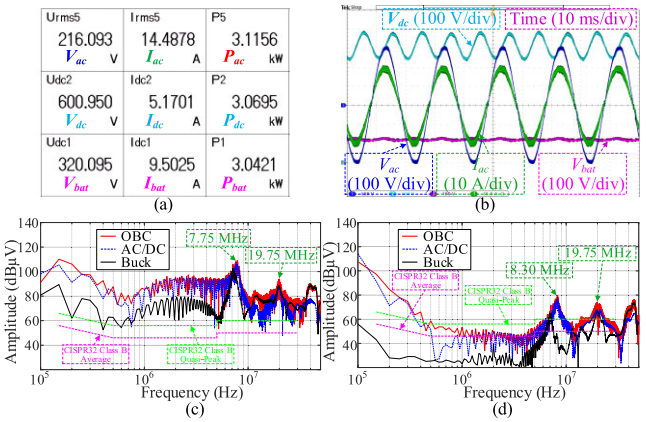

FIGURE 25. The conducted EMI tests of the multiplexing converter in the OBC working mode: (a) the rated working states, (b) the experimental test waveforms, (c) the comparison of CM EMI test results, (d) the comparison of DM EMI test results.

Firstly, the rated working states are measured by the power analyzer WT5000 as shown in Fig. 25(a), where the grid

voltage $V_{ac} = 216$ V, the grid current $I_{ac} = 14.49$ V (limited by the current capacity of the AC LISN), the input power $P_{in} = 3.12$ kW, the DC voltage $V_{dc} = 601$ V, the output voltage $V_{bat} = 320$ V, and the $f = 50$ kHz. The experimental test waveforms are shown in Fig. 25(b).

Secondly, the conducted EMI characteristics of the front-stage AC/DC converter, the post-stage buck converter, and the overall OBC are tested separately to analyze the influences of the different interference sources on the conducted EMI characteristics of the AC grid side of the OBC. When testing the conducted EMI characteristics of the front-stage AC/DC converter, the SiC MOSFET Q_{H3} is kept in the on state and the Q_{L3} is kept in the off state. When testing the conducted EMI characteristics of the post-stage buck converter, the front-stage AC/DC converter is kept in an uncontrolled rectifier state. The CM EMI test results are shown in Fig. 25(a). The front-stage AC/DC converter is the main CM noise source of the OBC in the low frequency ranges (less than 6.5 MHz) and in the frequency ranges from 7.5 MHz to 10 MHz. The DM EMI test results are shown in Fig. 25(b). The front-stage AC/DC converter is the main DM noise source of the OBC in the entire conducted EMI test frequency ranges (150 kHz $\sim$ 30 MHz).

Then, the shielded cable 2 as shown in Fig. 18(a) is removed, and now the OBC is considered to be an isolated OBC in some degree. The conducted EMI characteristics of the isolated OBC are tested as shown in Fig. 26. The output shielded cable will increase the CM EMI in the low frequency ranges (less than 350 kHz) and mid frequency ranges (6 MHz $\sim$ 8 MHz), as shown in Fig. 26(a), and do not affect the DM EMI as shown in Fig. 26(b).

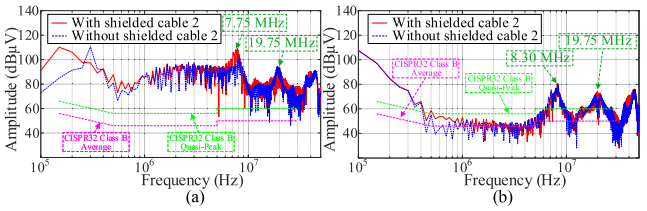

FIGURE 26. The influence of the output shielded cable 2 on the EMI characteristics of the grid side of the OBC: (a) the comparison of CM EMI test results, and (b) the comparison of DM EMI test results.

Next, the EMI characteristics of OBC using the power inductors with optimized winding method are tested and compared as shown in Fig. 27, which significantly reduces the conducted EMI in the frequency ranges from 1 MHz to 30 MHz.

Finally, the EMI characteristics of OBC with the added small packaged X capacitors (C_x) are tested and compared as shown in Fig. 28. The EMI levels of the post-stage buck at the resonance point of the 7.15 MHz can be suppressed significantly as shown in Fig. 28(a) and (b). However, since the conducted EMI characteristics of the OBC depend mainly

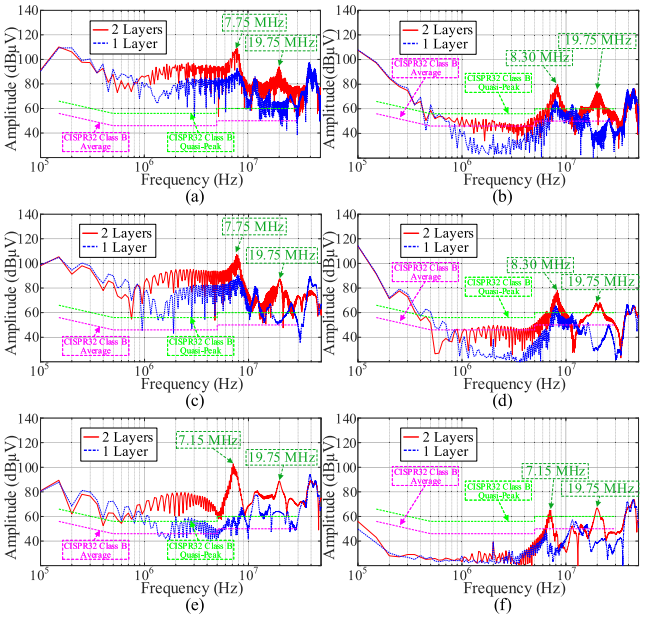

FIGURE 27. The conducted EMI test results of the OBC with different winding power inductors: (a) the comparison of CM EMI test results of the OBC, (b) the comparison of DM EMI test results of the OBC, (c) the comparison of CM EMI test results of the front-stage AC/DC, (d) the comparison of DM EMI test results of the front-stage AC/DC, (e) the comparison of CM EMI test results of the post-stage buck, and (f) the comparison of DM EMI test results of the post-stage buck.

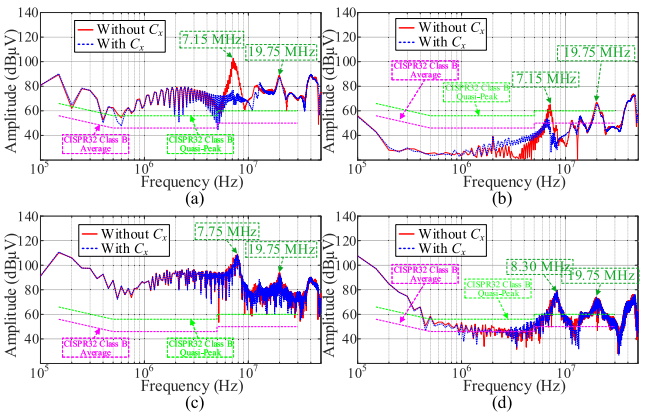

FIGURE 28. The conducted EMI test results of the OBC with added C_x: (a) the comparison of CM EMI test results of the post-stage buck, (b) the comparison of DM EMI test results of the post-stage buck, (c) the comparison of CM EMI test results of the OBC, and (d) the comparison of DM EMI test results of the OBC.

on the front-stage AC/DC converter, it has almost no effect on the conducted EMI characteristics of the OBC, as shown in the Fig. 28(c) and (d).

C. THE DESIGN OF THE INTEGRATED EMI FILTERS

By optimizing the winding method of the input power inductors, the conducted EMI levels of the grid side of the OBC are reduced in the frequency ranges from 1 MHz to 30 MHz, which can reduce the high frequency insertion

loss requirements of the EMI filter. However, the window utilization factor of the power inductors is low (20.52%) and the EMI test results of the OBC still exceed the limits of the CISPR 32-2019 as shown in Fig. 27(a) and (b). In order to meet the EMI standard limits, the grid-side EMI filter will be designed in this section to further reduce the conducted EMI levels of the OBC.

In order to reduce the influence of EMI filter on the power density of the system, the EMI filter will be designed and installed in the remaining space of the input filter inductor. A window with a diameter of 37 mm can be used inside the power inductors as shown in Fig. 6(a). The nanocrystalline ring core of L2025-W523 from VAC is selected to construct the CM inductor of the EMI filter.

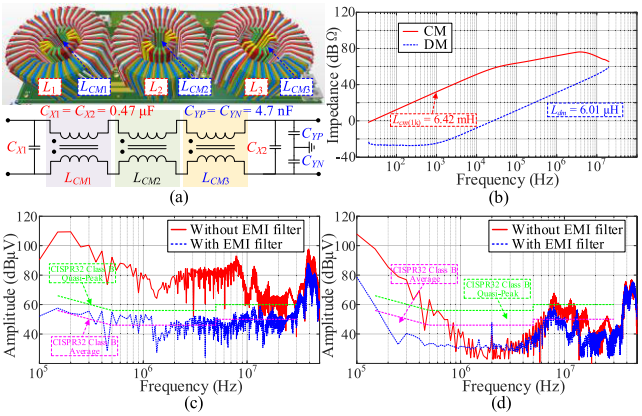

FIGURE 29. The conducted EMI test results of the OBC with added EMI filters: (a) The virtual prototype and equivalent circuit of the EMI filter, (b) the CM and DM impedance characteristics of the CM inductor, (c) the comparison of CM EMI test results of the OBC, and (d) the comparison of DM EMI test results of the OBC.

The final virtual prototype of the CM inductor (L_{CM1}, L_{CM1}, L_{CM3}) installed in the power inductors (L_1, L_1, L_3) is shown in Fig. 29(a). The CM and DM impedance characteristics of the CM inductor are shown in Fig. 29(b), where the CM inductance at 1 kHz is 6.42 mH and the leakage DM inductance is 6.04 μH.

The CM and DM EMI levels of the grid side of the OBC are significantly suppressed and meet the quasi-peak limits of CISPR 32-2019 by adding the EMI filter, as shown in Fig. 29(c) and (d), where the CM EMI is the dominant component in the frequency ranges greater than 200 kHz.

V. CONCLUSION

This paper analyzes the conducted EMI characteristics of a SiC-based multiplexing converter in the DC/DC working mode and in the non-isolated OBC working mode. Through conducted EMI simulation analysis and experimental tests, the main conclusions are as follows.

1) In the DC/DC working mode: The series resonance between the input negative lead parasitic inductance and the high frequency transmission line effects of the input power inductor will increase the conducted EMI levels in a specific frequency band. The input negative lead parasitic inductance can be reduced by adding a small packaged X capacitor, which can eliminate the CM EMI resonant spikes in a specific frequency band. The *EPC* of the input power inductor can be reduced by optimizing the winding method, which improves its high-frequency impedance characteristics, reduces the high-frequency oscillation amplitudes of the inductor currents, and significantly reduces the system EMI levels. By optimizing the winding method of the input power inductor to improve its high-frequency impedance characteristics and by adding a small packaged X capacitor to reduce the parasitic inductance of the input negative lead, the conducted EMI test results of the multiplexing converter in the DC/DC working mode meet the GB/T 18655-2018 level 1 peak limits.

2) In the non-isolated OBC working mode: Compared with the isolated OBC, the output shielded cable will increase the CM EMI levels in the low frequency ranges (less than 350 kHz) and in the mid frequency ranges (6 MHz ∼ 8 MHz). The conducted EMI characteristics of the OBC depend mainly on the front-stage AC/DC converter, which can be suppressed in the frequency ranges from 1 MHz to 30 MHz by optimizing the winding method of the input power inductors. The conducted EMI test results of the multiplexing converter in the OBC working mode meet the quasi-peak limits of CISPR 32-2019 by adding grid side EMI filters, which are installed together with the input power inductors without affecting the system power density. The structure of the integrated EMI filter will be further optimized in the future.

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JIANZHEN QU received the B.S. and M.S. degrees in electrical engineering and control engineering from the Qingdao University of Science and Technology, Qingdao, China, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the Department of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, China.

His research interests include electromagnetic interference modeling and suppression techniques.

QIANFAN ZHANG (Member, IEEE) was born in Heilongjiang, China. He received the M.S. and Ph.D. degrees from the Harbin Institute of Technology, Harbin, China, in 1999 and 2004, respectively, both in electrical engineering.

In 1999, he joined the Faculty of the Department of Electrical Engineering, Harbin Institute of Technology, where he has been a Professor, since 2010. His research interests include electric machine and drives, power electronics applied on electric vehicles, hybrid electric vehicles, integrated charging systems, and wireless power transfer systems.

YANG WANG was born in Shanxi, China. He received the B.S. degree in electrical engineering and automation from Southwest Jiaotong University, Chengdu, China, in 2020. He is currently pursuing the Ph.D. degree with the Harbin Institute of Technology, Harbin, China.

His research interest includes power electronics applied on electric vehicles.

SHUMEI CUI was born in Heilongjiang, China. She received the Ph.D. degree in electrical engineering from the Harbin Institute of Technology (HIT), Harbin, China, in 1998.

She has been a Professor with the Department of Electrical Engineering, HIT. Her research interests include the design and control of micro and special electric machines, electric drive system of electric vehicles, control and simulation of hybrid electric vehicles, and intelligent test and fault diagnostics of electric machines.

Dr. Cui serves as the Vice Director Member of the Micro and Special Electric Machine Committee and the Chinese Institute of Electronics, and a member of the Electric Vehicle Committee and the National Automotive Standardization Technical Committee.