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11-Level Operation With Voltage-Balance Control of WE-Type Inverter Using Conventional and DE-SHE Techniques

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ABSTRACT This article presents an 11-level operation of the WE (Wee)-Type inverter. The topology employs a single DC-source, has a reduced number of components, and exhibits a boosting capability. A voltage balancing algorithm is proposed where the inverter's redundant states are employed to maintain the auxiliary DC-link voltage. It is shown that with the control algorithm, the link voltage is preserved at half the primary DC-link voltage, and the 11-level operation is possible for any load. The presented 11-level WE-type structure is also compared with recent 11-level structures and has a lowest cost factor. Two modulation strategies verify the 11-level operation of the inverter: first, a modified nearest level control (MNLC) with the usage of both zero states is developed; and, second, selective harmonic elimination (SHE) is employed, where the angles are generated using a differential evolution (DE) technique. The maximum efficiency of the inverter is 97.55 %. The performance of the inverter is validated in MATLAB/Simulink and on the hardware-in-the-loop platform.

INDEX TERMS WE-type inverter, 11-level operation, boosted output voltage, modified nearest level control, differential evolution, selective harmonic elimination.

I. INTRODUCTION

Multilevel inverters (MLI) are gaining much popularity in the research community and industry for applications such as renewable energy source integration [1], and medium and high voltage drives [2] as they produce near-sinusoidal waveforms and exhibit reduced dv/dt and di/dt stresses on the switches. Conventional multilevel structures such as Flying Capacitor (FC), Neutral Point Clamped (NPC), and cascaded H-bridge (CHB) have been widely employed in industry [3], [4]. With the increase in the number of levels, the FC structure requires a large number of capacitors, the NPC structure employs a large number of clamping diodes, and the CHB structure requires as many DC sources as the number of H-bridges employed [5].

Generally, single-phase MLIs are classified as either symmetrical (SMLI) or asymmetrical (AMLI) depending on the magnitudes of the sources employed. If the sources are of the same DC value, then the structure is symmetrical; else, it is asymmetrical. The conventional NPC and FC topologies employ symmetrical sources and require a large number of switches and capacitors, and is therefore sometimes referred to as *silicone grave* in the industry when 5 or 7 level structures are discussed [6], [7]. For instance a 7-level NPC will require 12 switches, 10 diodes and 6 capacitors; 7-level FC will require 12 switches and 6 capacitors; and, CHB will require

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12 switches and 3 DC sources. On the other hand, the packed U-cell AMLI requires 6 switches and 2 capacitors only [8] Thus AMLIs have significnatly fewer switches and passive components which results in better efficiency and has led to increased research interest recently [9].

Switched-Capacitor based Multilevel Inverter structures (SCMLI) are topologies where the capacitor voltages along with the DC-sources are employed for addition or subtraction of voltages to achieve a particular voltage level along with simultaneous charging. These may be SMLI or AMLI structures based on the magnitude of the voltage sources. SCMLIs, in contrast to the conventional MLI topologies, require a minimal number of switches [9]. Further, these topologies exhibit boosting capability and require small filtering components (or not at all) [10], [11]. In recent years, the literature has presented a myriad of SCMLIs. A 7-level SCMLI structure with ten insulated gate bipolar transistors (IGBTs), four diodes, two capacitors, and a single source is proposed in [12]. Roy presents a new SCMLI based on a cross-switched MLI structure in [13]. A 9-level SCMLI structure is presented in [14]. An 11-level inverter and its cascaded operation have been recently proposed in [15].

Another category of MLI structures utilizes the advantages of FC and CHB. The first introduction to this topology was the Packed U-Cell (PUC) structure. Primarily, this structure with six switches, one DC source, and one capacitor can produce a 7-level output [8]. Vahedi *et al.* [10] presents a modified PUC (MPUC), where a ratio of 2:1 produces 7-level output. Kaif et.al. in [16] and Nidhi et.al. in [17] have extended the work by cascading the MPUC and producing a 49 and 25 level output, respectively. A modified version of PUC is presented by dividing the capacitor auxiliary DC-link into two voltage zones and creating a Packed E-cell (PEC) structure [18]. Very recently, Kim *et al.* [19] introduced a 13-level inverter that employs 14 switches, three capacitors, and a DC source.

An 11-level modular multilevel inverter utilizing a half-bridge as a basic unit for flexible AC transmission systems (FACTS) systems is considered in [20]. Saggu *et al.* [21] considers an 11-level CHB structure for harmonic mitigation in induction furnace application. An asymmetrical hybrid CHB structure is considered in [22] and [23] for three-phase applications. Other 11-level structures are discussed and compared in section III of this paper.

Recently, a 9-level inverter was presented in [11]. This work presents the 11-level operation of the same structure by balancing the voltage across the auxiliary DC link at $V_{dc}/2$. The presented inverter and its voltage balancing technique have been published in the Indian Patent Office with application number: 202011024951 A. Structurally, this inverter is similar to the topology presented in [11] and employs a single DC-source, two capacitors, and 11 IGBTs. Two of these IGBTs form a bipolar and bidirectional switch (AC-switch). The difference lies in its circuit analysis. The presented topology finds its parents in the works presented in [8] and [18]. Further, the topology of [11] is capable of generating a 9-level output. Additionally, the presented structure's cost factor is better than the 9-level counterpart due to a reduction in the number of gate driver circuits. A detailed comparison is shown in the following sections.

The modulation of the inverters is generally classified as either high-switching frequency modulation or low switching frequency modulation. Sine-PWM [24] and its variants like the ones presented in [18] and [11], space vector PWM [6] and hybrid modulation techniques [25] are some of the high-switching frequency techniques. Nearest level control (NLC) [15], [26], selective harmonic elimination [27] and selective harmonic mitigation (SHM) [28] are low-switching frequency techniques applied to single-phase inverters in literature. For SHE and SHM, the optimum angles are produced either by mathematical analysis [29] or by metaheuristic techniques like genetic algorithm (GA) [30], differential evolution (DE) [31], particle swarm optimization (PSO) [27], modified PSO, [22] and grey wolf optimization [23]. The aim is to solve the transcendental equations under a constrained environment. In this work, NLC and DE-based SHE are taken into account. NLC operation leads to reduction of lower order harmonics in the output voltage as the levels are determined by interaction with the sinusoidal reference voltage. This technique is beneficial for close-loop operations [15] and, the SHE exhibits the elimination of selected lower order harmonics as there is a direct control over the harmonic spectrum [29]. A modified NLC (MNLC) is discussed in this work where both the zero states are utilized to generate the output voltage.

This work presents an 11-level operation of a WE-type inverter in which the voltages across the capacitors is balanced by using the redundant states. It is modulated by employing two methods. The first one is a MNLC in which both zero states are employed, and the second one is the SHE whose angles are derived by employing DE. The maximum efficiency of the inverter is found to be 97.55%.

The paper is organized as follows. The next section deals with the structural analysis, switching states, and modeling of the WE-type inverter. Section III deals with comparing the presented inverter with recent 11-level inverters and [11]. Sections IV and V deal with the MNLC and DE-based SHE algorithms for the modulation of the inverter, respectively. The capacitor voltage balancing scheme using the redundant states is also presented in these sections. In section VI, power loss is performed analytically and in the PLECS environment. Finally, the paper concludes with results taken in the hardware-in-the-loop platform.

II. ANALYSIS OF WE-TYPE INVERTER FOR 11-LEVEL OPERATION

A. WE-TYPE INVERTER CIRCUIT STRUCTURE

Fig. 1 illustrates the circuit of the presented 11-level WE-type inverter topology along with its evolution from the circuits that were proposed in [8], and [18]. The arrangement consists of a DC source that comprises the main DC-link, two DC

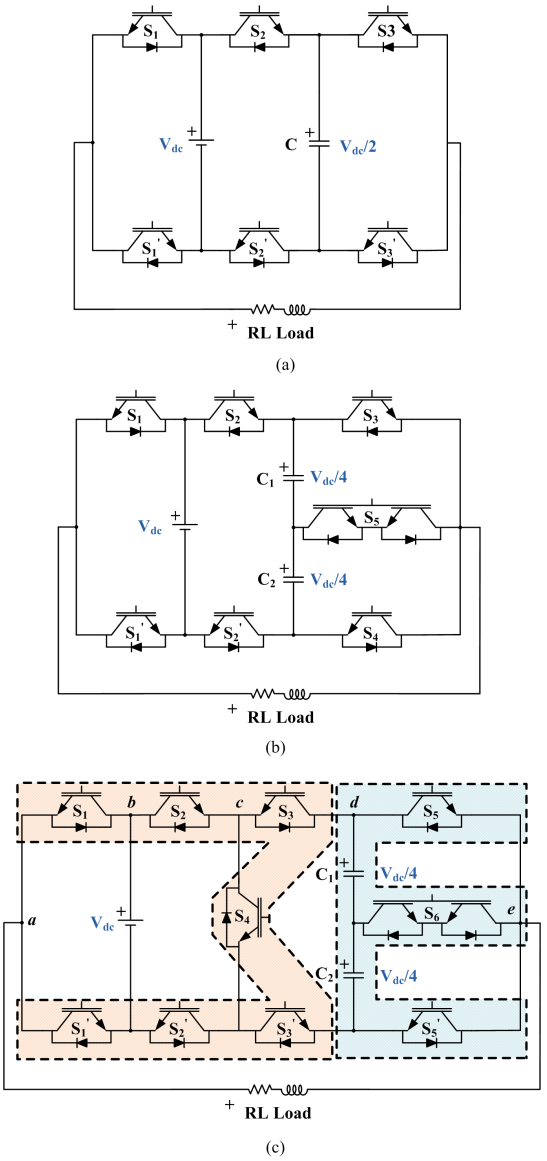

FIGURE 1. Evolution of the presented WE-type 11 level Inverter: (a) 5-level PUC topology [8], (b) 9-level PEC topology [18], and (c) Presented topology.

sources that will form the auxiliary DC-link, nine Insulated Gate Bipolar Junction Transistors (IGBTs) one antiparallel connected IGBTs forming an AC-switch. The auxiliary DC-link may be DC-sources such as batteries or PV panels, or capacitors. The switches S_1, S_2, S_3, S'_1, S'_2, S'_3 and S_4 forms W and S_5, S'_5 and the AC-switch S_6 forms alphabet E, and hence the name WE-type inverter.

With a single DC-source in its main DC-link, this topology is capable of producing a boosted output voltage. The switches S_1 and S'_1, S_2 and S'_2, S_3 and S'_3, and, S_5, S'_5 and S_6 perform in a complimentary fashion. As persistent with the asymmetrical topologies, the switches of this topology are also subjected to different voltage stresses and operational frequencies. The switches S_1, S'_1, S_2 and S'_2 are subjected to maximum voltage, which is V_{dc}, S_3, S'_3, S_4, S_5 and S'_5 are

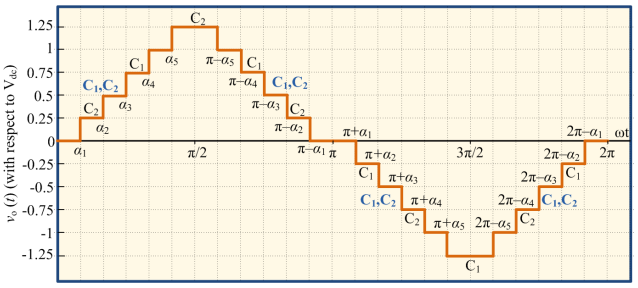

FIGURE 2. The possible eleven levels of the inverter with capacitors involved in each state.

subjected to a medium voltage of $V_{dc}/2$, and, the AC-switch S_6 is subjected to a minimum voltage of $V_{dc}/4$. The switches S_1, S'_1, S_3 and S'_3 operate on fundamental frequency, S_4 on twice the fundamental frequency, S_2 and S'_2 on eight times the fundamental frequency, and S_5, S'_5 and S_6 on twenty four times the fundamental frequency. This discussion suggests that the upper switches of the converter must block higher voltage and operate at low frequency, while the lower switches will block a lower voltage and operate at high frequency compared to the upper switches. A single voltage sensor is sufficient to balance the auxiliary DC-link voltage. Here, however, voltages across both capacitors are measured to demonstrate the converter's operation and analysis.

B. WE-TYPE INVERTER SWITCHING STATES AND MODELING

Figure 2 exhibits the possible states of the 11-level operation with the capacitors involved. All the states of the converter are presented in pictorial view in Fig. 3. Sixteen states are possible with different configurations of the switches. Out of which, one of the zero states can be a redundant state or can be utilized in the algorithm to reduce the stress of the components. Each sub-figure highlights the conduction path. The current flow from left to right in the load is the positive current. The states also explain the charging and discharging conditions of the capacitors with current directions in Table 1.

Let S_{f1}, S'_{f1}, S_{f2}, S'_{f2}, S_{f3}, S'_{f3}, S_{f4}, S_{f5}, S'_{f5} and S_{f6} represent the switching functions of S_1, S'_1, S_2, S'_2, S_3, S'_3, S_4, S_5, S'_5, S_6. The output voltage of the converter that represents all the states is derived here. Each switching function will have a value defined as:

$$S_{fj} = \begin{cases} 0 & \text{if } S_j \text{ is off} \\ 1 & \text{if } S_j \text{ is 1} \end{cases} \tag{1}$$

The output voltage expression in the preliminary form as:

$$V_o = V_{ae} = V_{ab} + V_{bc} + V_{cd} + V_{de} \tag{2}$$

where, V_{ab}, V_{bc}, V_{cd} and V_{de} are the voltages across the nodes a, b, c, d and e in Fig. 1(c). These terms can be defined according to the Karnaugh-map analysis shown in Fig. 4 as follows: For V_{ab}, Fig. 4(a) is utilized which results in:

$$V_{ab} = -V_{dc}\left(1 - S_{f1}\right) \tag{3}$$

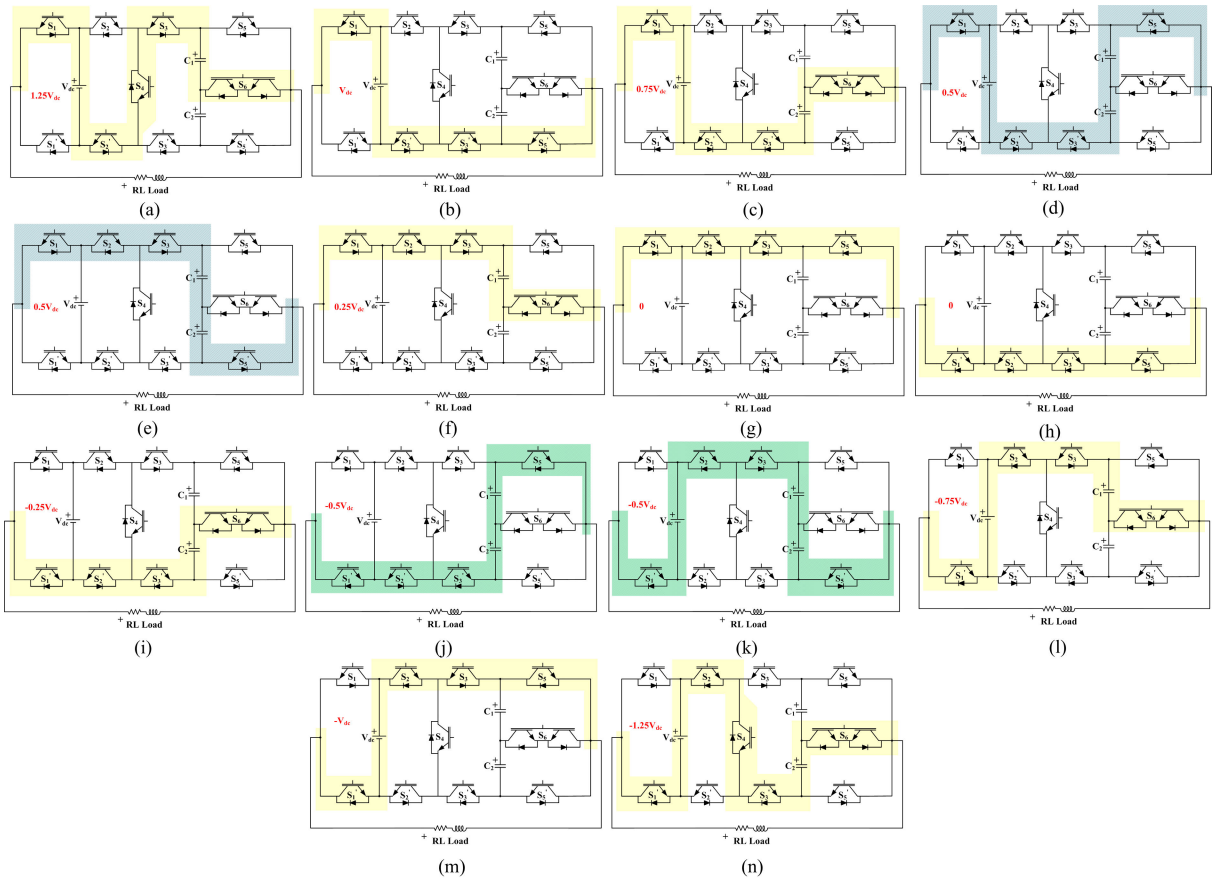

FIGURE 3. Operation states of 11-level WE-type Inverter.

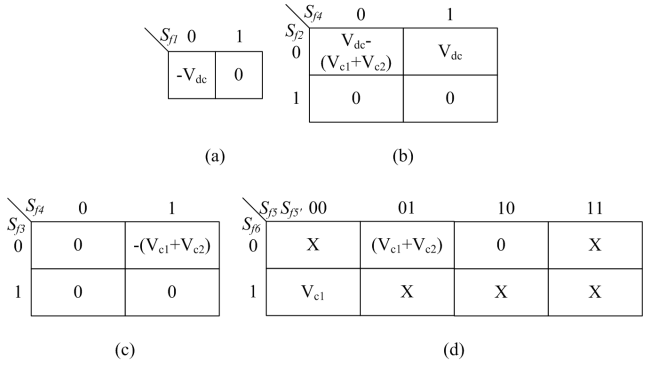

FIGURE 4. Karnaugh map based modeling of the WE-type inverter.

Similarly, Fig. 4(b)-(d) can be utilized to formulate:

$$V_{bc} = \left(1 - S_{f2}\right)\left(1 - S_{f4}\right)\left[V_{dc} - (V_{C1} + V_{C2})\right] + \left(1 - S_{f2}\right) S_{f4} V_{dc} \quad (4)$$

$$V_{cd} = -\left(1 - S_{f3}\right) S_{f4}\left(V_{C1} + V_{C2}\right) \quad (5)$$

$$V_{de} = \left(1 - S_{f5}\right)\left(1 - S'_{f5}\right) S_{f6} V_{C1} + \left(1 - S_{f5}\right)\left(1 - S_{f6}\right) S'f5\left(V_{C1} + V_{C2}\right) \quad (6)$$

Substituting the expressions defined in (3)-(6) in (2) results in:

$$V_o = V_{dc}\left[S_{f1} - S_{f2}\right] + (V_{C1} + V_{C2})\left[S_{f2} - S_{f2}S_{f4} + S_{f3}S_{f4} + S'_{f5} - S_{f5}S'_{f5} - S'_{f5}S_{f6} + S_{f5}S'_{f5}S_{f6} - 1\right] + V_{C1}\left[S_{f6} - S_{f5}S_{f6} - S'_{f5}S_{f6} + S_{f5}S'_{f5}S_{f6}\right] \quad (7)$$

Equation (7) and the following auxiliary DC-link expression will lead to all the possible states presented in the diagrams of Fig. (3) and in Table (1):

$$V_{C1} + V_{C2} = \frac{V_{dc}}{2} \quad (8)$$

C. CAPACITOR VOLTAGE BALANCING ALGORITHM

The auxiliary DC-link capacitors must be charged to a voltage of $V_{dc}/4$ for a successful 11-level operation of the inverter. For this redundant states, the output voltage level of $V_{dc}/2$ and $-V_{dc}/2$ are employed (see Table 1). Levels $V_{dc}/2$, $-V_{dc}/2$ can be produced with positive or negative currents, thus allowing a charging or discharging environment for the auxiliary DC-link capacitors.

Figure 5 shows that the number of instances required for charging and discharging of the capacitors C_1 and C_2 of the auxiliary DC-link. As it is apparent from the figure,

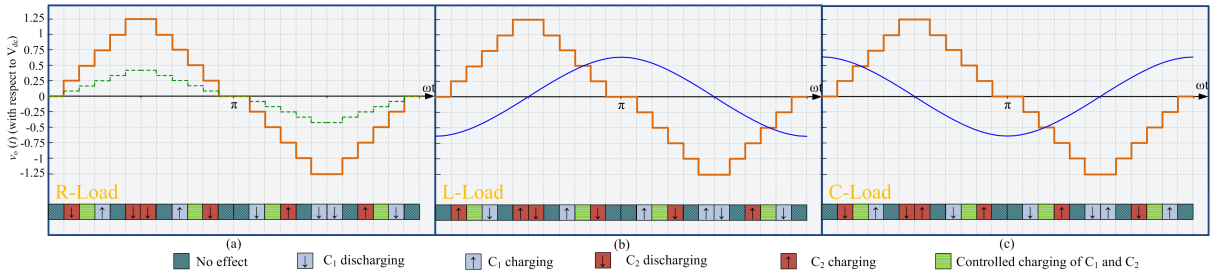

FIGURE 5. State of capacitors with (a) R-load, (b) L-load and (c) C-load.

TABLE 1. Switching states of the presented WE-type Inverter.

State	S_1	S_2	S_3	S_4	S_5	S_5'	S_6	I_o	C_1	C_2	V_o
1.	1	0	1	1	0	0	1	+	-	↓	$5V_{dc}/4$
2.	1	0	0	0	0	1	0	+	-	-	V_{dc}
3.	1	0	0	0	0	0	1	+	↑	-	$3V_{dc}/4$
4.	1	0	0	0	1	0	0	+	↑	↑	$V_{dc}/2$
5.	1	1	1	0	0	1	0	+	↓	↓	$V_{dc}/2$
6.	1	1	1	0	0	0	1	+	-	↓	$V_{dc}/4$
7.	1	1	1	0	1	0	0	+	-	-	0 (I)
8.	0	0	0	0	0	1	0	+	-	-	0 (II)
9.	0	0	0	0	0	0	1	+	↑	-	$-V_{dc}/4$
10.	0	0	0	0	1	0	0	+	↑	↑	$-V_{dc}/2$
11.	0	1	1	0	0	1	0	+	↓	↓	$-V_{dc}/2$
12.	0	1	1	0	0	0	1	+	-	↓	$-3V_{dc}/4$
13.	0	1	1	0	1	0	0	+	-	-	$-V_{dc}$
14.	0	1	0	1	0	0	1	+	↑	-	$-5V_{dc}/4$
1'.	1	0	1	1	0	0	1	−	-	↑	$5V_{dc}/4$
2'.	1	0	0	0	0	1	0	−	-	-	V_{dc}
3'.	1	0	0	0	0	0	1	−	↓	-	$3V_{dc}/4$
4'.	1	0	0	0	1	0	0	−	↓	↓	$V_{dc}/2$
5'.	1	1	1	0	0	1	0	−	↑	↑	$V_{dc}/2$
6'.	1	1	1	0	0	0	1	−	-	↑	$V_{dc}/4$
7'.	1	1	1	0	1	0	0	−	-	-	0 (I)
8'.	0	0	0	0	0	1	0	−	-	-	0 (II)
9'.	0	0	0	0	0	0	1	−	↓	-	$-V_{dc}/4$
10'.	0	0	0	0	1	0	0	−	↓	↓	$-V_{dc}/2$
11'.	0	1	1	0	0	1	0	−	↑	↑	$-V_{dc}/2$
12'.	0	1	1	0	0	0	1	−	-	↑	$-3V_{dc}/4$
13'.	0	1	1	0	1	0	0	−	-	-	$-V_{dc}$
14'.	0	1	0	1	0	0	1	−	↓	-	$-5V_{dc}/4$

↓=discharging, ↑= charging, and -=neither charging nor discharging.

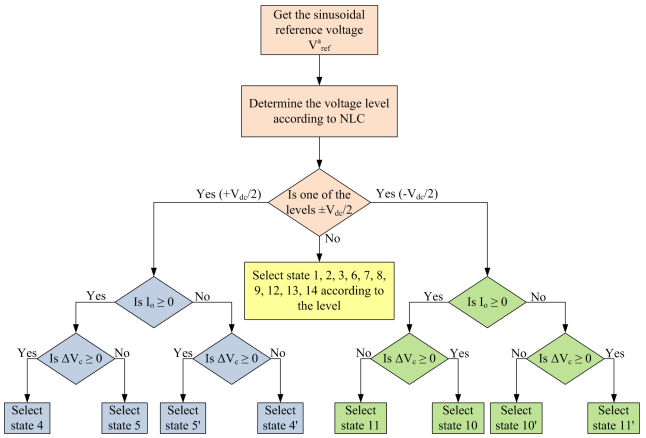

FIGURE 6. Flowchart exhibiting the algorithm employed for charging and discharging of capacitors of auxiliary DC-link.

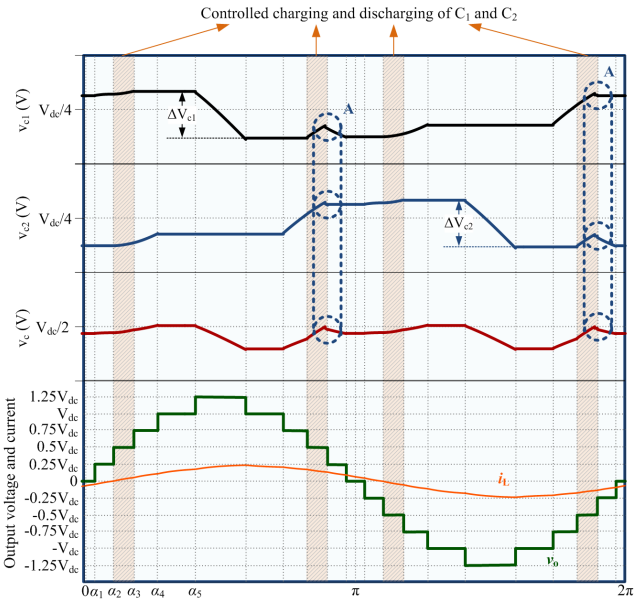

FIGURE 7. Capacitor C_1 and C_2 ripples with MNLC operation of the inverter.

the instances where the individual capacitors are charged or discharged, along with the redundant states (available at $V_{dc}/2$ and $-V_{dc}/2$) will lead to a balanced voltage of $V_{dc}/2$ at the auxiliary DC-link, with a voltage of $V_{dc}/4$ across each capacitor. Thus, instead of utilizing two sensors, only one sensor will be required to balance the auxiliary DC-link voltage. Thus to facilitate the controlled charging of discharging of the capacitors, the algorithm shown in Fig. 6 is employed. The capacitors ripple are shown in Fig. 7. At instances shown by **A**, it can be seen that as the voltage of the auxiliary DC-link reaches $V_{dc}/2$, the redundant state activates according to Fig. 6 and the capacitors start discharging.

Further, the ripple in the capacitor voltages and the peak load current can be utilized to determine the capacitor values. It is required that the ripple of the capacitors must not dip beyond 5% of the desired voltage across it; which is $V_{dc}/4$ in this case. The change in energy with a dip of ΔV_{c1} and ΔV_{c2} can be given as:

$$\Delta E_c i = \frac{1}{2} C_i \Delta V_{ci} \tag{9}$$

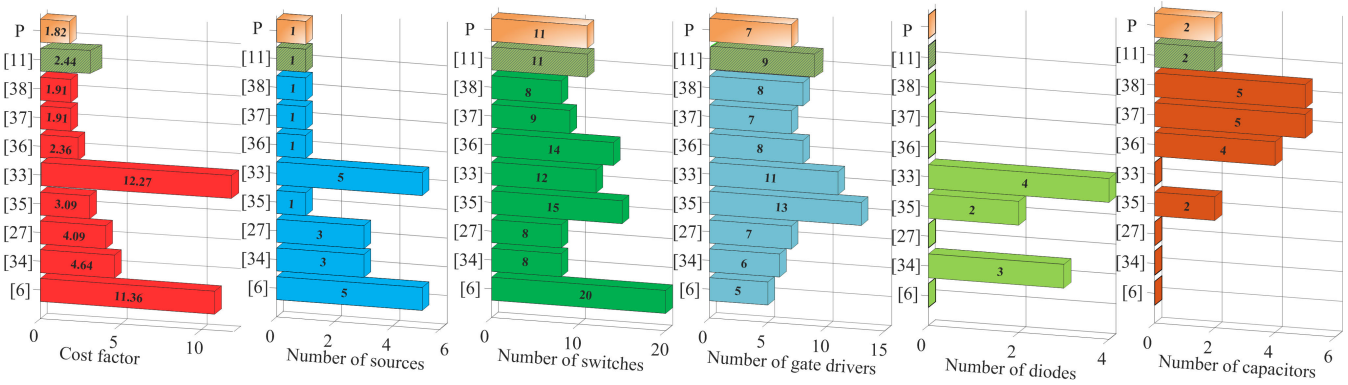

FIGURE 8. Comparison of WE-Type inverter with recent 11-level topologies and a 9-level topology of [11].

TABLE 2. Comparison of the WE-type 11-level inverter with recent topologies.

MLI	N_{level}	N_S	N_T	N_D	N_{dr}	N_C	N_L	BC	CF
[33]	11	5	12	4	11	0	0	ND	12.27
CHB [6]	11	5	20	0	5	0	0	1	11.36
[34]	11	3	8	3	6	0	0	ND	4.64
[27]	11	3	8	0	7	0	0	ND	4.09
[35]	11	1	15	2	13	2	2	5	3.09
[36]	11	1	14	0	8	4	0	5	2.36
[37]	11	1	9	0	7	5	0	1	1.91
[38]	11	1	8	0	8	5	0	1	1.91
[11]	9	1	11	0	9	2	0	2	2.44
WE-11	**11**	**1**	**11**	**0**	**7**	**2**	**0**	**1.25**	**1.82**

CF= Cost Factor, N_{level}= number of levels, N_S= number of sources, N_T= number of switches, N_D=number of diodes, N_C= number of capacitors, BC= boosting capability, ND= Can not be defined

With a consideration of 5% window, the expression can be developed as:

$$C_i = \frac{80E_c}{V_{dc}} \tag{10}$$

The energy stored in the capacitor is determined by the load [32]. In this work, the value of the capacitors is taken as 4700 μF.

III. COMPARISON WITH RECENT INVERTERS

This section is dedicated to performing a fair comparison with recently introduced 11-level inverters, which is presented in terms of number of sources employed, number of switches, number of gate driver circuits employed, number of diodes, number of passive elements, and cost factor, which is a function of the previous parameters. The comparison is presented in tabular form in Table 2 and pictorial form in Fig. 8. In order to perform the analysis, cost factor (CF) has been taken as a primary parameter, and is defined as:

$$CF = \frac{(N_T + N_{dr} + N_d + N_C + N_L) \times N_s}{N_{levels}} \tag{11}$$

As [33] employs 5 sources, it exhibits the highest cost factor of 12.27. Moreover, some switches require a high PIV rating. Next, CHB requires 20 switches in 5 H-bridge modules driven by 5 driver circuits and 5 sources of the same magnitude [6]. The larger number of switches leads to a higher cost factor. However, modularity is the key feature of this structure, which makes it an attractive topology. Reference [34] presents an 11-level structure that requires 8 switches, 3 diodes, and 3 sources of different magnitudes. Boosting capability is difficult to describe in the topologies where two or more sources of different magnitudes are employed. Reference [27] presents a 3 source 11-level structure that employs 8 switches and requires 7 gate driver circuits. In [35], 1 source, 15 switches, 2 diodes, 2 capacitors and 2 inductors are employed, leading to a cost factor of 3.09. Reference [36] introduces a single-source MLI that employs 14 switches driven by 8 driver circuits and 4 capacitors. A single-source structure with 9 switches driven by 7 driver circuits is presented in [37]; but the circuit requires 5 capacitors for successful 11-level operation. A circuit with no boosting utilizing one source, 5 capacitors, and 8 switches driven by 8 driver circuits is discussed in [38]. In contrast to these topologies, the presented 11-level WE-type inverter employs a single source, 11 switches and 2 capacitors, thereby resulting in the lowest cost factor of 1.82. A similar structure that produced 9-level output was proposed in [11], but as it requires a 2 more driver circuits, its cost factor is higher than the presented 11-level operation. However, [11] has dual boosting capability and the capacitors can be auto-balanced. In the present structure, a voltage sensor is required to balance the auxiliary DC-link voltage. Another advantage of the presented topology over the [11] is a lesser dv/dt on the switches. This is because the step in [11] is $V_{dc}/2$, while in the presented topology it is $V_{dc}/4$. The comparison is summarized in Table 2 and Fig. 8.

The standing voltages of the presented inverter are shown for every state in Fig. 9. It can be seen that the highest voltages are blocked by the upper voltages during the whole cycle. The total standing voltage (TSV) of the inverter as shown in the figure is 24 V_dc. This leads to a TSV per level (TSV/11) as 2.18 (also known as per unit TSV). Comparing with other topologies, a symmetrical CHB exhibits a TSV of 20, while [27] exhibits a TSV of 22. Reference [36] on the other hand exhibits a TSV of 32. The TSV of the presented topology when employed for 9 levels is 45 times V_{dc}.

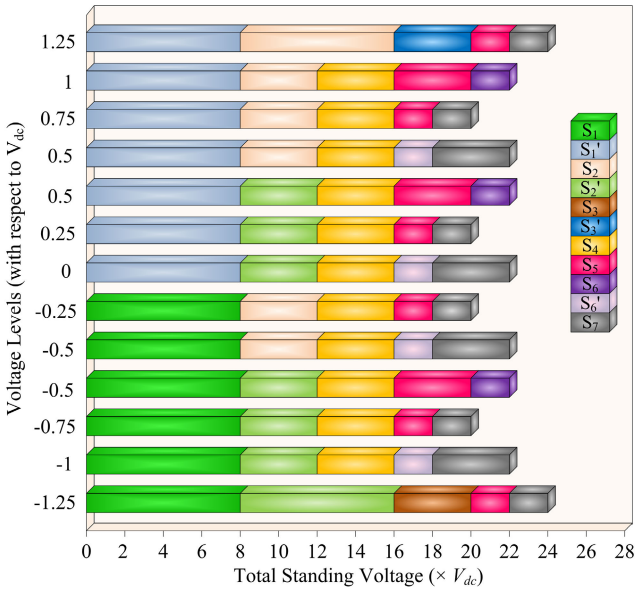

FIGURE 9. Total standing voltage of WE type 11 level inverter.

IV. MODIFIED NEAREST LEVEL CONTROL (MNLC) OF WE-TYPE 11-LEVEL INVERTER

The Pulse Width Modulation (PWM) techniques are majorly divided into the high-switching frequency and low-switching PWM techniques. Sine-PWM and space-vector modulation are some of the high-switching frequency techniques. These techniques result in higher switching losses, which reduces the efficiency of the topology [6]. On the other hand, in Nearest level control (NLC), selective harmonic elimination (SHE), and selective harmonic mitigation (SHM), low-frequency (fundamental frequency) switching is performed, which results lower switching losses. In this work, two techniques NLC and SHE, are applied to validate the inverter's performance.

MNLC is presented in this work where both zero states are employed to control the output voltage. This method ensures the least lower order harmonics in the output waveform. The concept is shown graphically in Fig. 10. The actual waveform synthesis results from the generation of the angles by comparing the reference voltage V_{ref} and the midpoint between the levels. The definition of angles on which the transition takes place can in a general form expressed as:

$$\alpha_i = \sin^{-1}\left[\frac{2i-1}{N-1}\right] \tag{12}$$

where, $i < N/2$, i is an index of the angle under calculation, and N is the possible number of levels in an MLI. The maximum value of i must be less than the number of levels in a quarter cycle. In this case $N = 11$ and $i_{max} = 5$.

Fig. 10 shows the midpoint signals as L_1 to L_{10}. These signals can be defined and generalized by a single expression as:

$$L_i = 1.5\left[1 - \left(\frac{1}{N-1}\right)\right] - 0.25k \tag{13}$$

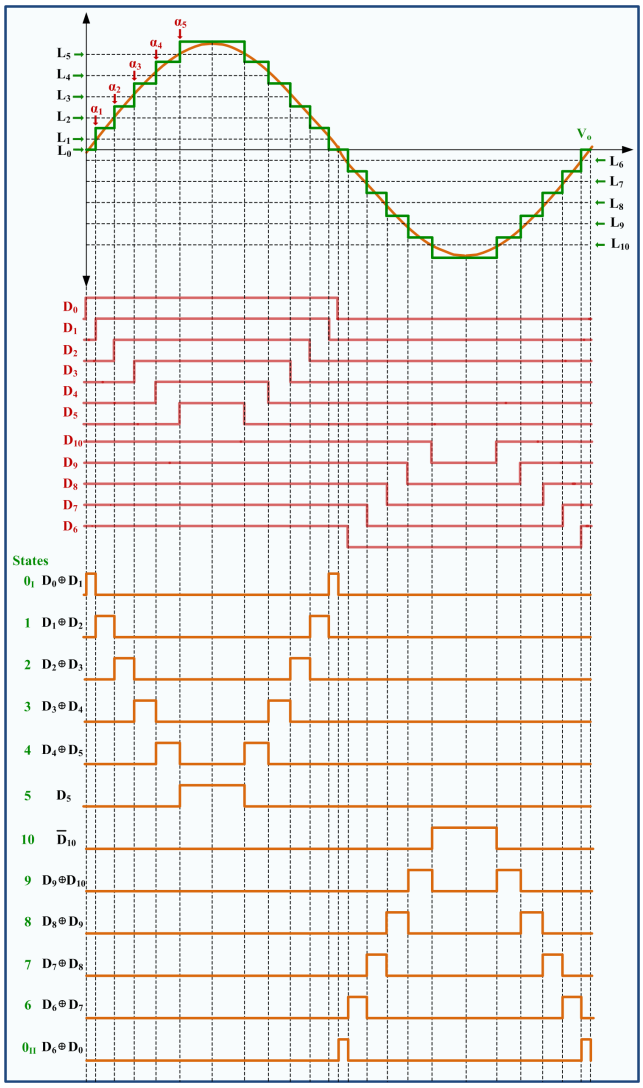

FIGURE 10. Pulse generation in MNLC.

where, $k = 1, 2, \cdots, N-1$. The constant 0 value generates a zeroth level of L_0. The comparison of values with the reference voltage leads to a generation of 11 signals named D_0 to D_{10}, as shown in Fig. 11. These signals use red color in Fig. 10. Logical operations develop the eleven states, namely from state 0 to state 10. The modification of this technique over others is the employment of both the 0 states presented in Table 1. There are two 0 states shown in Fig. 10 and Fig. 11 namely 0_I and 0_{II}. These states correspond to 0 (I) and 0 (II) in table 1. The usage of both states ensures the equal switching of both the complementary switches. Otherwise, if only one state is employed, the complimentary switches will never be used in the 0 state. The switching signals to the gate drivers of the circuits are then activated, corresponding to these states.

V. DE-SHE BASED MODULATION OF WE-TYPE 11-LEVEL INVERTER

As discussed earlier, SHE is another low-switching frequency technique. Here the angles are selected in a manner that

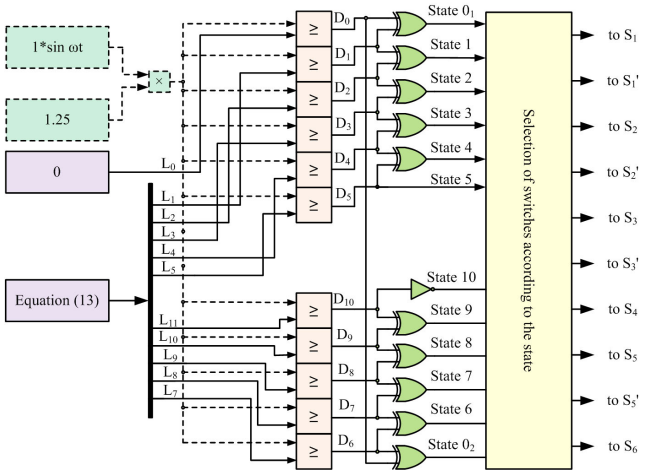

FIGURE 11. Digital system for pulse generation in MNLC.

the output voltage waveform contains no low order harmonics. Constrained controlling of few angles is possible. For example, generally (with no notch) $x-1$ harmonics can be eliminated for x level operation. The angles are determined by solving the transcendental equations. Their solution can be based on a mathematical basis [29] or by using metaheuristic techniques [16]. In this work, a metaheuristic based differential evolution is employed.

A. SELECTIVE HARMONIC ELIMINATION

The Fourier expression of the waveform shown in Fig. 2 can be written as:

$$v_o(\omega t) = A_o + \sum_{n=0}^{\infty} (A_n \cos(\omega t) + B_n \sin(\omega t)) \tag{14}$$

where, A_o, A_n and B_n are the DC component, even harmonics and the odd harmonics. The modulation strategy always ensures that quarter-wave and half-wave symmetries are maintained, and the DC component and the even harmonics are rendered zero. Therefore, the expression modifies as:

$$v_o(\omega t) = \sum_{n=0}^{\infty} (B_n \sin(\omega t)) \tag{15}$$

where, the coefficient B_n is represented as:

$$B_n = \frac{4V_{dc}}{n\pi} \sum_{j=1,3,5}^{m} \cos(n\alpha_j) \tag{16}$$

Now, as there are only five angles as the controllable parameters, only four harmonics and the fundamental can be controlled. As generally low-order harmonics are eliminated, here, third, fifth, seventh, and ninth harmonics are eliminated. The required expression is derived from (16) as follows:

$$\begin{aligned} \cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 + \cos\alpha_5 &= \frac{V_d^{max}\pi}{4V_{dc}} \\ \cos 3\alpha_1 + \cos 3\alpha_2 + \cos 3\alpha_3 + \cos 3\alpha_4 + \cos 3\alpha_5 &= 0 \\ \cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3 + \cos 5\alpha_4 + \cos 5\alpha_5 &= 0 \end{aligned}$$

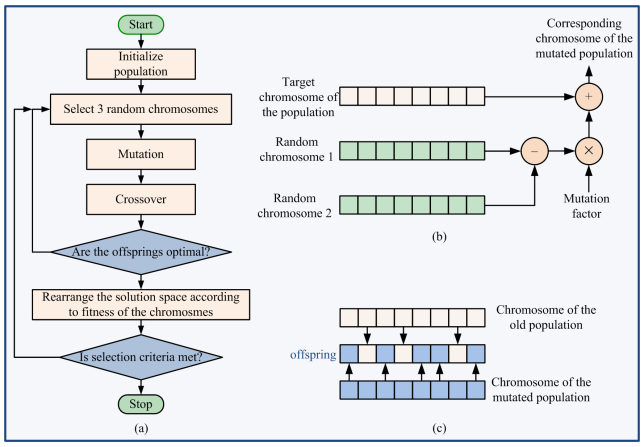

FIGURE 12. (a) Flowchart of DE, (b) mutation, and (c) crossover.

$$\begin{aligned} \cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 + \cos 7\alpha_4 + \cos 7\alpha_5 &= 0 \\ \cos 9\alpha_1 + \cos 9\alpha_2 + \cos 9\alpha_3 + \cos 9\alpha_4 + \cos 9\alpha_5 &= 0 \end{aligned} \tag{17}$$

where V_d^{max} is the magnitude of the desired fundamental voltage. Further for operation on various modulation indexes:

$$MI = \frac{\pi V_d^{max}}{2 \times \left(N_{levels}^{max} - 1\right) \times V_{dc}} \tag{18}$$

where N_{levels}^{max} is the maximum number of levels achievable by the inverter. This value is 11 in our case. The solution of these expression is performed under the constraint expressed as:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \pi/2 \tag{19}$$

B. DIFFERENTIAL EVOLUTION

Differential Evolution (DE) is an efficient and simple metaheuristic optimization technique that is utilized to solve the minimization problems that are difficult to solve with conventionally applied methods such as the Newton-Raphson method [29]. It is based on the natural process of evolution of living beings and imitates the *survival of fittest* methodology [39]. The process is briefly described in Fig. 12(a). A chromosome consists of all the variables under consideration. For example, in this work, it is required to find five optimum angles. These angles will form a chromosome of 40 bits (eight bits for each variable). A random initial population of such chromosomes is developed and rearranged according to its fitness towards the *objective function*. An objective function is developed as a minimization expression for the problem under consideration. For SHE, the function is defined by using (17) and (18) under the constrained environment of (19).

The mutation is performed next as shown for one variable of the chromosome in Fig. 12(b) where three chromosomes, including the target chromosome, is chosen. The choice of the chromosomes other than the target chromosome is purely random. The data is mutated by a factor in the range of 0 to 2. Thus a new chromosome corresponding to the target chromosome is generated and stored. A new chromosome

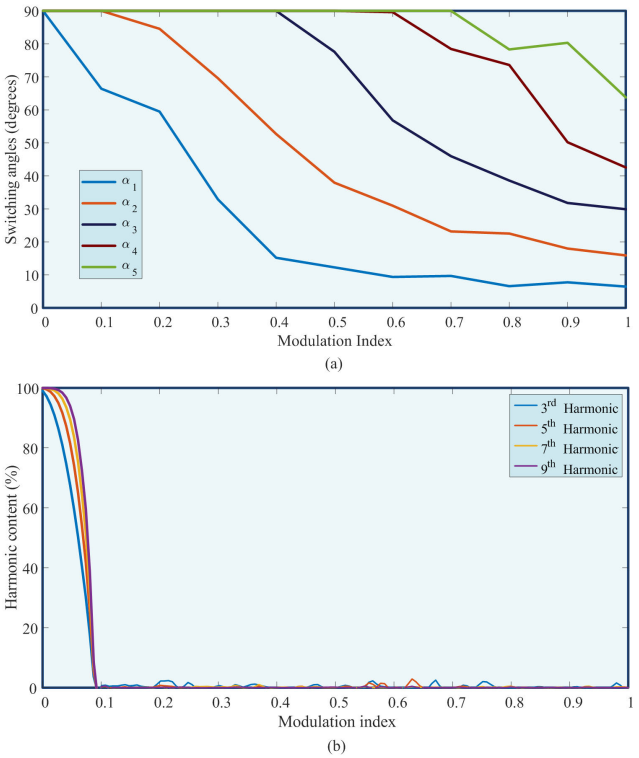

FIGURE 13. Variation in (a) switching angles, and, (b) the harmonics with change in modulation index.

is developed by randomly selecting some bits from the old chromosome and the new mutated chromosome to form a new chromosome. This step is known as *crossover*, and the chromosome is the final child or *offspring* of the target chromosomes. If the chromosome's fitness is better than the chosen chromosome, it takes its place; otherwise, it is discarded. The process repeats until a predefined number of iterations is reached.

The code for the DE algorithm based on the above discussion was developed in MATLAB. The optimal angles were obtained as the final solutions of the optimization problem for the modulation index ranging from 0 to 1. The angles with variation in MI are shown in Fig. 13(a). Fig. 13(b) demonstrates the variation of harmonic orders with the modulation index. The 11-level operation is possible till MI of 0.75. Below this value of MI the inverter will operate at 9 levels.

VI. POWER LOSS ANALYSIS

The power loss analysis generally considers the losses that occur during switching and forward conduction of the switches and diodes. In the presented circuit, only switches are employed. The theoretical analysis of the losses is presented, which is followed by power analysis in PLECS software.

A. SWITCHING LOSSES

There is power loss during the turning on and turning off of the switches. Turning on energy loss for a single switch can be considered as:

$$\begin{aligned} e_i^{on} &= \int_0^{t_{on}} v(t)i(t)dt \\ &= \int_0^{t_{on}} \left[\frac{V_{si}}{t_{on}}\right]\left[\frac{I_{on}}{t_{on}}(t_{on}-t)\right] \\ &= \frac{1}{6}V_{si}t_{on}^2 I_{on} \end{aligned} \tag{20}$$

Similarly, for turning off case:

$$\begin{aligned} e_i^{off} &= \int_0^{t_{off}} v(t)i(t)dt \\ &= \int_0^{t_{off}} \left[\frac{V_{si}}{t_{off}}\right]\left[\frac{I_{off}}{t_{off}}\left(t_{off}-t\right)\right] \\ &= \frac{1}{6}V_{si}t_{off}^2 I_{off} \end{aligned} \tag{21}$$

where, I_{on} and I_{off} are the currents after and before the turning on and turning off of a switch, respectively. V_{si} is the voltage across a switch during turn off state. The total switching loss can thus be calculated as:

$$P_{sw} = \frac{1}{T}\left[\sum_{i=1}^{N_{switch}}\left(\sum_{j=1}^{N_i^{on}} e_{ij}^{on} + \sum_{j=1}^{N_i^{off}} e_{ij}^{off}\right)\right] \tag{22}$$

B. CONDUCTION LOSSES

These losses occur while the switches and diodes are conducting. As the circuits consists of switches only, thus for any arbitrary switch:

$$P_{ci} = \left[V_s + R_s i^{\gamma}(t)\right] i(t) \tag{23}$$

where V_s is the drop across the switch in the on state, R_s is the resistance of the switch and γ is a constant mentioned in the specification sheet of the switch. The total conduction loss can be described as:

$$P_c = \frac{1}{T}\int_0^{2\pi}\sum_{i=1}^{N_{switch}} P_{ci}(t) \tag{24}$$

The total losses of the converter can now be defined as:

$$P_{loss} = P_{sw} + P_c \tag{25}$$

PLECS software is employed to determine the losses in the converter on the MNLC algorithm. IKFW50N60DH3E-IGBT model is employed for the sake of analysis. Fig. 14(a) and (b) shows the turn-on and turn-off losses with respect to V_{si} and I_{on}. Fig. 14(c) demonstrates the conduction losses with an increase in conduction current during on state (I_{on}). Fig. 14(d) shows the junction temperatures of the switches of the inverter when the temperature of the environment is kept at 40^o C. Fig.14(e) shows the efficiency curve of the inverter. The maximum efficiency in the PLECS environment is 97.55%, and with 700 W an efficiency of 96%. Fig. 14(f) considers the power losses and efficiency under different loading conditions. Table 3 is provided to present various losses across the switches at the load of 50 Ω, 100 mH.

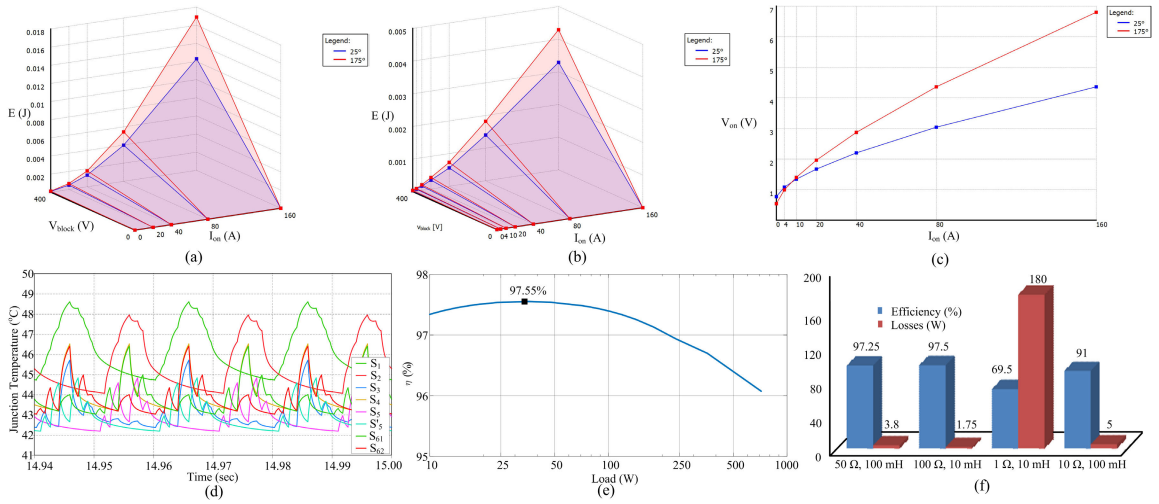

FIGURE 14. (a) Turn-on characteristics of IGBT, (b) Turn-off characteristics of IGBT, (c) Conduction losses of IGBT, (d) Junction temperatures of various switches in 40^{o} C environment, (e) Efficiency curve of the inverter, and (f) Efficiency and power losses with different loading conditions.

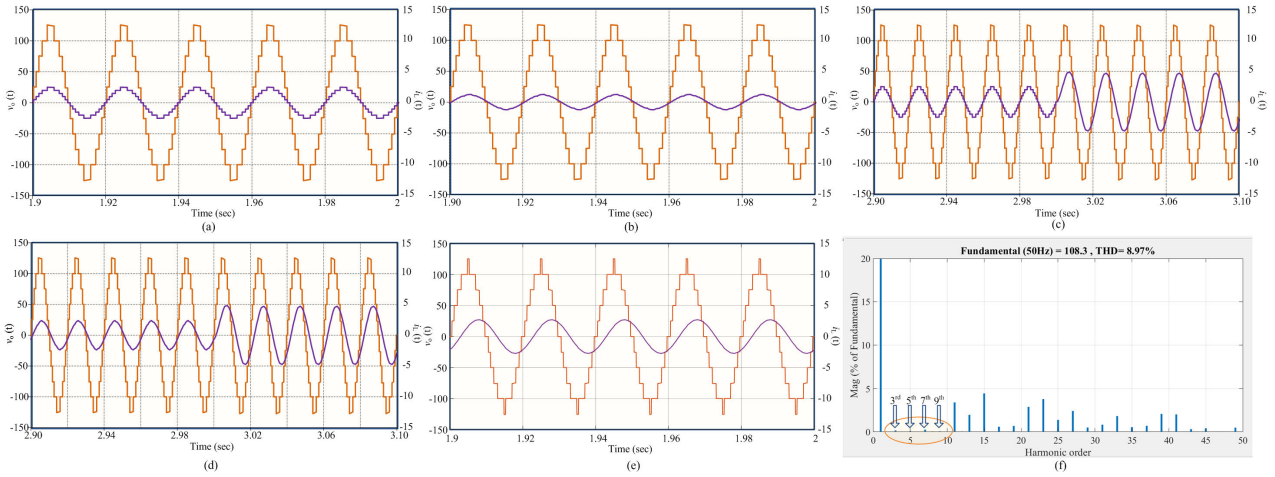

FIGURE 15. Simulation results showing the output voltage and currents using MNLC with (a) R-load of 50 Ω, (b) RL-load of 100 Ω, 50 mH, (c) Load change from 50 Ω to 20 Ω, 50 mH and (d) Load change from 50 Ω, 50 mH to 20 Ω, 50 mH; and using SHE with (e) RL load of 25 Ω, 100 mH, and (f) output voltage THD with SHE. ($V_{dc} = 100\ V$).

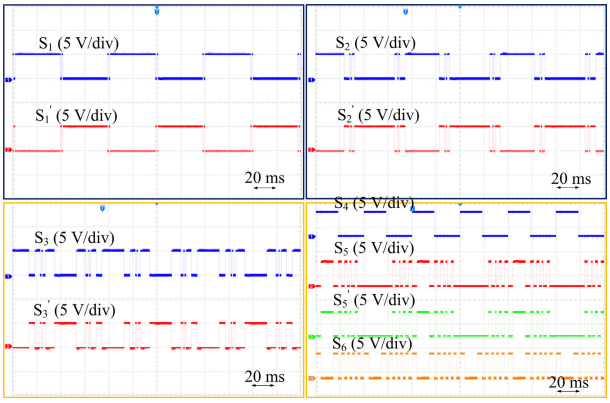

FIGURE 16. Gate signals as produced at the terminals of the HIL-402.

TABLE 3. Various losses in the switches of WE-11 inverter at the load of 50 Ω, 100 mH.

Switch	Switching Loss (W)	Conduction Loss (W)	Total (W)
S_1	0.0065	0.3827	0.3892
S_1'	0.0065	0.3832	0.3897
S_2	0.0171	0.03619	0.3790
S_2'	0.0171	0.3616	0.3738
S_3	0.0002	0.1591	0.1593
S_3'	0.0002	0.1591	0.1593
S_4	0.0006	0.197	0.1976
S_5	0.0023	0.1577	0.1600
S_5'	0.0023	0.1577	0.1600
S_{61}	0.0014	0.2124	0.2138
S_{62}	0.0014	0.2124	0.2138

VII. RESULTS AND DISCUSSION

The performance of the presented 11-level WE structure is investigated for static and dynamic loads. Modified nearest level control and selective harmonic elimination are validated. The SHE is validated for the modulation index of 0.85. Both the strategies are validated on simulation and hardware in the loop platform provided by Typhoon. For the SHE, all the angles have been determined offline, as discussed in the previous section. The inverter in simulation and HIL is operated using a 100 V and 25 V DC-source, respectively.

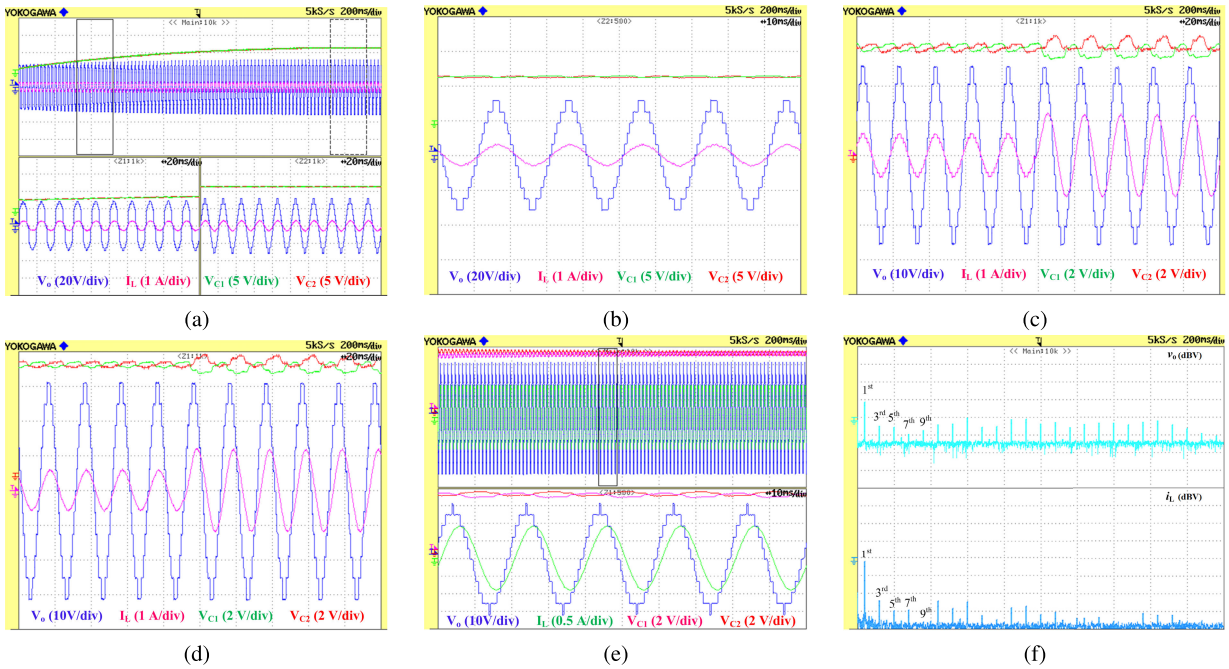

FIGURE 17. Results showing behavior of output voltage, load current, voltages across C_1 and C_2 with MNLC under (a) Initial and steady state conditions with R load (50 Ω), (b) RL- load (100 Ω, 50 mH), (c) Load change from 50 Ω to 20 Ω, 50 mH and, (d) Load change from 50 Ω, 50 mH to 20 Ω, 50 mH; and (e) with SHE with RL- load (20 Ω, 50 mH), and (f) FFT of output voltage and load current, at modulation index of 0.86.

TABLE 4. Table of simulation and HIL parameters.

S. No.	Parameters	Simulation	HIL
1.	DC Source Voltage	100 V	25 V
2.	Capacitors	4700 μF, 50 V ESR 0.05 Ω	4700 μF, 50 V
3.	Resistive Load	20, 25, 50 & 100 Ω	20, 25, 50 & 100 Ω
4.	Inductive Load	50 mH	50 mH
5.	Power frequency	50 Hz	50 Hz

TABLE 5. Angles and analysis of FFT of voltage and current at MI=0.86.

MI	α_1	α_2	α_3	α_4	α_5
0.86	8.461	18.941	35.822	54.195	86.228
Voltage FFT analysis					
Unit	1^{st}	3^{rd}	5^{th}	7^{th}	9^{th}
dBV	25.674	-18.291	-22.041	-15.898	-15.254
Peak (V)	27.178	0.172	0.112	0.227	0.244
%age	100	0.634	0.411	0.834	0.899
Current FFT analysis					
dBV	-3.896	-45.420	-54.170	-52.832	-61.094
peak (A)	0.903	0.008	0.003	0.003	0.001
%age	100	0.839	0.306	0.358	0.138

The voltage balance algorithm based on Fig. 6 is expected to maintain a voltage of 50 V in simulation and 12.5 V in HIL across the auxiliary DC-link, which in turn mandates the voltage across both the capacitors to be maintained at 25 V in simulation and 6.25 V in HIL. The performance results in a boosting of 1.25 with an output voltage peak at 31.25 V. Capacitors of 4700 μF, 50 V with an ESR of 0.05 Ω are employed in the auxiliary DC-link. The parameters are also shown in Table 4.

Simulation results are presented in Fig. 15, in which sub-figure (a) shows the results with R-load of 50 Ω, and (a) shows the results with RL-load of 100 Ω, 50 mH. Load change from R-load to RL-load and from RL-load to RL-load in sub-figures (c) and (d). Sub-figure (e) shows the results with SHE at modulation index of 0.86, and its harmonic profile is shown in sub-figure (f). The spectrum shows that the low order 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics are eliminated.

Fig. 16 shows the gating signals that are produced to turn on and off the switches on the HIL platform. Fig. 17(a) shows the inverter's performance with R-load with a resistance of 50 Ω used as a load. The waveform's initial behavior suggests that when the capacitors are discharged, a voltage equal to 25 V (V_{dc}) will appear across the load. With time, the capacitors charge and reach the desired value of the DC-link. The capacitor voltages are taken with an offset of 1 division for better visibility. Fig. 17 (b) shows the steady-state behavior of the inverter with an RL load of 100 Ω, 50 mH on a modulation index of 0.94. Fig. 17 (c) shows the inverter's dynamic behavior with a change in load from 50 Ω to 20 Ω, 50 mH. The capacitor voltage seems to have a higher ripple at the onset of the change, but the ripple reduces as the steady-state is reached. However, the ripple is more in the case of an inductive load than a purely resistive load, which suggests that the capacitor voltage ripple is dependent on the type of load employed. Similarly, a load change behavior is shown in Fig. 17 (d), where the load changes from Ω, 50 mH to 20 Ω, 50 mH.

Fig. 17 (e) shows the result of the WE-type inverter with selective harmonic elimination with an RL-load. A load of 20 Ω and 50 mH is utilized to generate the waveforms at a lagging power factor of 0.787. The operation is performed at a modulation index of 0.86 where the angles are defined from the plot (Fig 13(a)) and in Table 5. The corresponding capacitor voltages across C_1 and C_2 is also shown for 400 cycles and a zoomed view of 5 cycles. An offset

of 0.5 division for capacitor voltages is taken for better clarity. The corresponding FFT analysis is done for the output voltage and current waveforms and is shown in Fig. 17 (f). As the harmonics' values are in dBV, they are converted into the peak values of the harmonics in Table 5. The harmonic content differs from the values of simulation – firstly due to the difference in the input voltages of the simulation and HIL and secondly due to the noise in the scope. The harmonics are also compared in terms of the percentage with respect to the fundamental. The analysis of Table 5 suggests that the SHE algorithm has mitigated the concerned harmonics in the output voltage and load current waveforms, as they are below 1% of the fundamental voltage.

VIII. CONCLUSION

In this work, the 11-level operation of a WE-type inverter was presented. This topology employed a single DC-source and 11 switches to perform 1.25 times boosted operation. A detailed analysis of the circuit and its redundant states was presented. The modeling of the inverter was also presented. Comparing the WE-type 11-level inverter with recent 11-level topologies suggested the lowest cost factor among all. An algorithm to balance the auxiliary DC-link at $V_{dc}/2$ was presented, where the redundant states were utilized to balance the voltage capacitor voltages. The 11-level operation was successfully implemented in hardware-in-the-loop environment using two modulation techniques. The first was a modified nearest level control, where both the converter's zero states were utilized, and the second was selective harmonic elimination (SHE). The differential evolution technique was employed to determine the angles for switching in the SHE. The eliminated harmonic content was less than 1% of the fundamental value of voltage and current. The loss analysis of the inverter was also performed, and the inverter's efficiency was found to be 97.55%. In future work, the topology can be considered to integrate solar PV sources applied across the DC-links and integrated with grid on an experimental bench.

ACKNOWLEDGMENT

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