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A Novel High-Gain Soft-Switching DC-DC Converter With Improved P&O MPPT for Photovoltaic Applications

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ABSTRACT This paper proposes a novel high voltage gain structure of DC-DC converter with soft-switching ability for photovoltaic (PV) applications. A small size coupled inductor with one magnet core is utilized to improve the voltage conversion ratio in the proposed converter. The converter has one active MOSFET with low conducting resistance (R_{DS-ON}), which in turn reduces the conduction losses and complexity of the control section. Due to the low input current ripple, the lifetime of the input PV panel is increased, and the maximum power point (MPP) of the PV panel can be easily tracked. The MOSFET's zero-voltage and zero-current switching and diodes are the other countenance of the proposed converter, which improve its efficiency. Additionally, an improved Perturb and Observe MPP tracking (IP&O MPPT) algorithm is introduced to boost the extracted power of the input PV sources. To validate the performance of this converter, the operation modes principle, steady-state and efficiency survey, and comparison results with other same family converters are carried out. Finally, an experiential prototype is built with 20 V input, 200 V output, power rate of 200 W, and 50 kHz operating frequency to validate the mathematical analysis and effectiveness of the proposed structure. The efficiency of the proposed converter was estimated by over 95% at various power levels.

INDEX TERMS Perturb and observe algorithm, dc-dc converter, photovoltaic, MPPT, zero current switching, high efficiency.

I. INTRODUCTION

Recently researchers are focusing on solving the problems associated with Photovoltaic (PV) systems for DC distribution such as low voltage level, low reliability, and low efficiency [1], [2]. The usage of power electronic converters such as DC-DC converters is increased in some important applications, like uninterruptible power supplies (UPS) and electric vehicles (EV) [3]. DC-DC converters are considered as the best choice for control, protection, and increasing the voltage level and efficiency of renewable energy sources [4].

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The PV systems play a prominent role in the integration of hybrid renewable energy systems. However, these systems pose many challenges that should be addressed to make them more efficient and reliable [5]–[7]. One of such challenges is to locate the position of maximum power point (MPP) which changes instantaneously due to the non-linear characteristics of current-voltage (I-V) and power-voltage (P-V) that vary with varying climatic conditions (i.e., temperature and irradiance). In this regard, numerous maximum power point tracking (MPPT) algorithms were reported in the literature to accurately locate the MPP. These algorithms are different according to various aspects such as complexity, cost, type of required sensor, implementation, and effectiveness.

Among these MPPT algorithms, Perturb and Observe (P&O) algorithm is most frequently and widely used due to its easy implementation and simplicity. However, in some cases as rapid climatic variation, the conventional P&O algorithm fails in tracking the MPP. To tackle this problem, numerous improvements in the conventional P&O algorithm have been reported in the literature. In this context, the authors in [8] proposed an improved P&O (IP&O) algorithm that can reduce the MPP oscillations in steady-state operation. However, it showed a slow performance to any climatic variation. In [9], an IP&O algorithm is designed to consider the variation in voltage and power at consecutive time intervals. Therefore, if there is an increment in power caused by perturbation and not by irradiance, then the algorithm makes a decrement in power for one cycle and takes a voltage gain in the correct direction in the next cycle. Similarly, an IP&O algorithm has been presented in [10], which automatically adjust the reference step size and track the MPP in variable climatic conditions. This in turn leads to algorithm improvement of about 0.5% more efficient compared to the conventional one. In [11], the authors designed a P&O algorithm that showed an outstanding performance in steady-state operation, however, its performance is greatly affected in varying irradiance conditions. All of the above-mentioned IP&O algorithms have been tested against straightforward temperature and irradiance profiles through which the exact performance of the algorithm cannot be easily determined. Moreover, the margin of performance between conventional P&O and IP&O algorithms is insignificant.

The conventional boost DC-DC converters are the simplest choice for increasing the output voltage level and have advantages of simple design, control, and implementation [12], [13]. However, they have the drawbacks of high maximum potential stress across the diode and the power switch, and low potential conversion ratio at low duty cycles [14]. Also, for obtaining a high converter voltage gain, it should be operated at the extreme duty cycle, to enhance the potential stress and semiconductors conduction losses [15]. To improve the operation of the high voltage rate DC-DC converters for achieving a higher output voltage, many kinds of high step-up converters have been proposed, recently. These converters can be categorized into bidirectional/unidirectional, isolate/non-isolated, hard switched/soft switched (ZVS and ZCS), and current fed/voltage fed structures [16].

Moreover, there are efficacious methods for voltage incensement such as voltage multipliers (voltage multiplier rectifier and voltage multiplier cell), switched capacitors and switched inductors, multi-stage topologies like cascaded and interleaved, and magnetic couplings such as transformers and coupled inductors. Big size and cost transformers are used in isolated converters [17]. Thus, these types of DC-DC converters have high implementation cost than non-isolated structures. A coupled inductor is a vital element of the non-isolated DC-DC converters which store energy during one cycle of switching period and supply the output load during the other cycle [18]. Generally coupled inductor technique is a helpful voltage lifting method in DC-DC topologies that can be obtained through coupling the inductors with only one magnetic core. So, using a coupled inductor, two or more windings can be implemented through one core [19]. Therefore, the size of the converter can be reduced. In [20], using bi-fold Dickson VMC, a non-isolated high step-up DC-DC converter is presented for PV systems. However, the input and output ports are not common ground. The converter in [21] uses two-coupled inductor to improve the voltage gain. Nevertheless, the input current ripple is high. In [22], an interleaved non-isolated converter is proposed using a coupled inductor. This converter has low input current ripple. Nevertheless, the number of used power switches is high, which can reduce the converter's efficiency. In [23], a coupled-inductor based non-isolated converter is introduced for distributed PV application. An efficient and high voltage gain quasi-SEPIC converter is presented in [24] with a coupled inductor technique. Using one magnetic core and VMCs, a single switch with high step-up DC-DC converter with low potential stress across semiconductor components is suggested in [25]. This converter has a high number of diodes and capacitors and high input current ripple. A transformer-less high voltage conversion ratio structure is presented in [26]. This converter is not common ground and there is a diode between input and output ports. This drawback increases the EMI effects. The main disadvantages of non-isolated high step-up DC-DC converters such as operating with high duty cycle, high conduction loss of semiconductor components, low efficiency, and high potential stress across the power diodes and switches still exist in previous structures.

This paper introduces a novel structure of high voltage gain, non-isolated DC-DC converter with soft-switching capability for photovoltaic systems. The suggested topology benefits from a high efficiency, simple structure, low voltage stress across the semiconductor components, high voltage conversion ratio, low input current ripple, and a low number of components. In the proposed DC-DC converter structure, a small size and cost coupled inductor with one magnet core is used to increase the voltage conversion ratio. The suggested converter has one active MOSFET with lower conducting resistance (R_{DS-ON}) which can decrease the conduction losses and complexity of the control section. Due to the low input current ripple, the PV panel' lifetime is increased and the MPP of the PV panel can be easily tracked. The ZVS and ZCS of power MOSFET and diodes are the other features of the proposed converter which improve efficiency. In the rest of this paper, to verify the suggested converter's performance, the operation modes principle, steady-state and efficiency calculation, and comparison results with other existing models are performed. Finally, to prove the mathematical analysis and the suggested structure's effectiveness, an experiential prototype is established with 20 V input, 200 V output, 200 W power rate at 50 kHz operating frequency.

Moreover, in this paper, an IP&O algorithm is designed in which a reference voltage is a function of temperature and

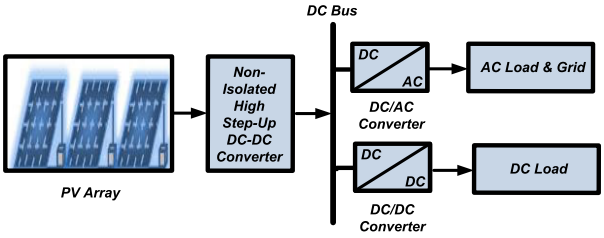

FIGURE 1. Schematic diagram of the non-isolated high step-up DC-DC converter for PV applications.

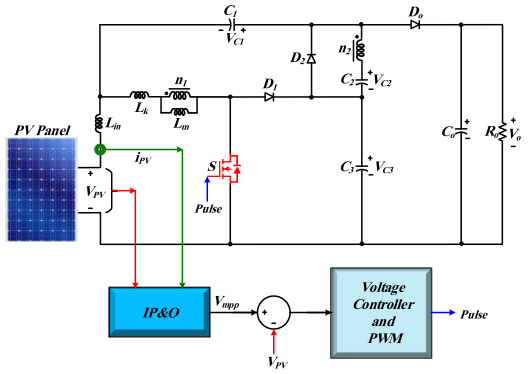

FIGURE 2. Structure of the proposed high step-up DC-DC converter for PV systems.

irradiation of the PV module which enhances the accuracy of the algorithm in a wide range of irradiance and temperature profiles.

II. THE PROPOSED MODEL AND PRINCIPLE OF OPERATION

The schematic diagram of the utilization of non-isolated high step-up DC-DC converter for PV applications is shown in Fig. 1.

As shown in this figure, the converter can track the MPP of PV panels and increase the output voltage level of the renewable sources and make them suitable to connect to a high voltage DC bus. The proposed converter's power and control circuits are illustrated in Fig. 2. Also, the main time waveforms of this structure are shown in Fig. 3.

As seen in Fig. 2, the proposed structure includes one power MOSFET (S), three diodes (D_1, D_2, and D_o), one input inductor (L_{in}), one coupled inductor (CL), and four capacitors (C_1, C_2, C_3, *and* C_o). Capacitors C_2 and C_3 along with diodes D_1 and D_2 are used to increase the voltage gain. Also, Capacitors C_3 acts as a passive clamp and reduces the voltage stress throughout the power switch S and capacitor C_1 is applied for further enhancement of the output voltage. Due to the low input current ripple, the input source can be a PV panel. A novel improved P&O algorithm is proposed, which only needs one voltage and one current sensor. The gate pulse of MOSFET S is generated by the MPPT section, which always operates in the MPP of the PV panel. The following assumptions are taken into account for facilitate the analysis:

1) The diodes (D_1, D_2, and D_o) and MOSFET S are ideal.

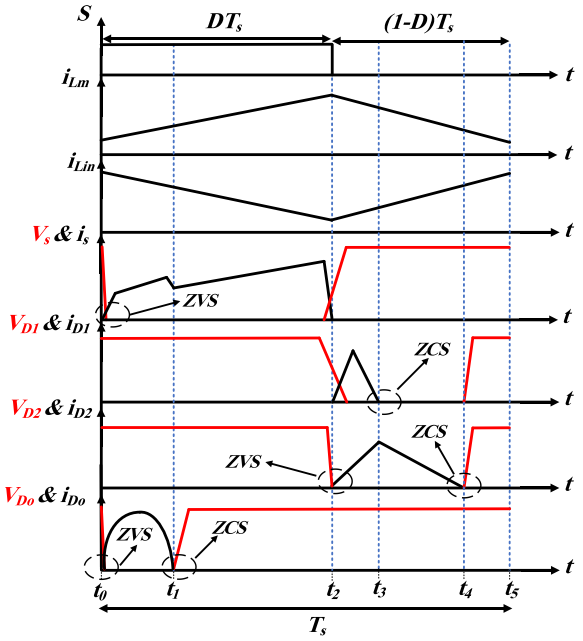

FIGURE 3. Voltage and current waveforms of the proposed converter.

2) The coupled inductor is assumed to be an ideal transformer with $N = n_2/n_1$ turns ratio, without core loss, and with one magnetizing (L_m) and one leakage (L_k) inductances.
3) The value of capacitors (C_1, C_2, C_3, *and* C_o) is large enough. Therefore, the capacitor's voltage ripple can be neglected during the switching period (T_s).

According to Fig.3, there are five modes in each T_s where modes 2 and 4 have higher time duration than the other modes. The following are the details of these modes:

Mode#1 [$t_0 < t < t_1$]: During this mode, power MOSFET S and diode D_o are turned ON in ZVS condition. Diodes D_1, D_2 are reverse biased and diode D_o is conducted. The voltage across input inductor L_{in} is negative and its current decreased linearly. However, the current of magnetizing inductance L_m is increased during mode 1. Also, Capacitors C_1 is charged, and C_2 and C_3 are discharged. As shown in Fig. 4(a), the energy of the coupled inductor's secondary side is transferred to the load through diode D_o. Equations (1) - (7) are obtained in this mode:

$$k = \frac{L_m}{L_k + L_m} \tag{1}$$

$$V_{L_m} = k\left(V_{PV} - V_{L_{in}}\right) \tag{2}$$

$$V_{n_2} = NV_{n_1} = NV_{L_m} \tag{3}$$

$$V_o = V_{C_3} + V_{C_2} + V_{n_2} \tag{4}$$

$$V_o = V_{PV} - V_{L_{in}} + V_{C_1} \tag{5}$$

$$i_{L_k} = i_{L_m} + Ni_{C_2} \tag{6}$$

$$i_{C_2} = i_{C_3} = i_{C_1} + i_{D_o} = i_{C_1} + i_{C_o} + i_o \tag{7}$$

where, k is the coupling coefficient, V_{PV} in the input voltage, V_{Lin} and V_{Lm} are the voltages across input inductance L_m,

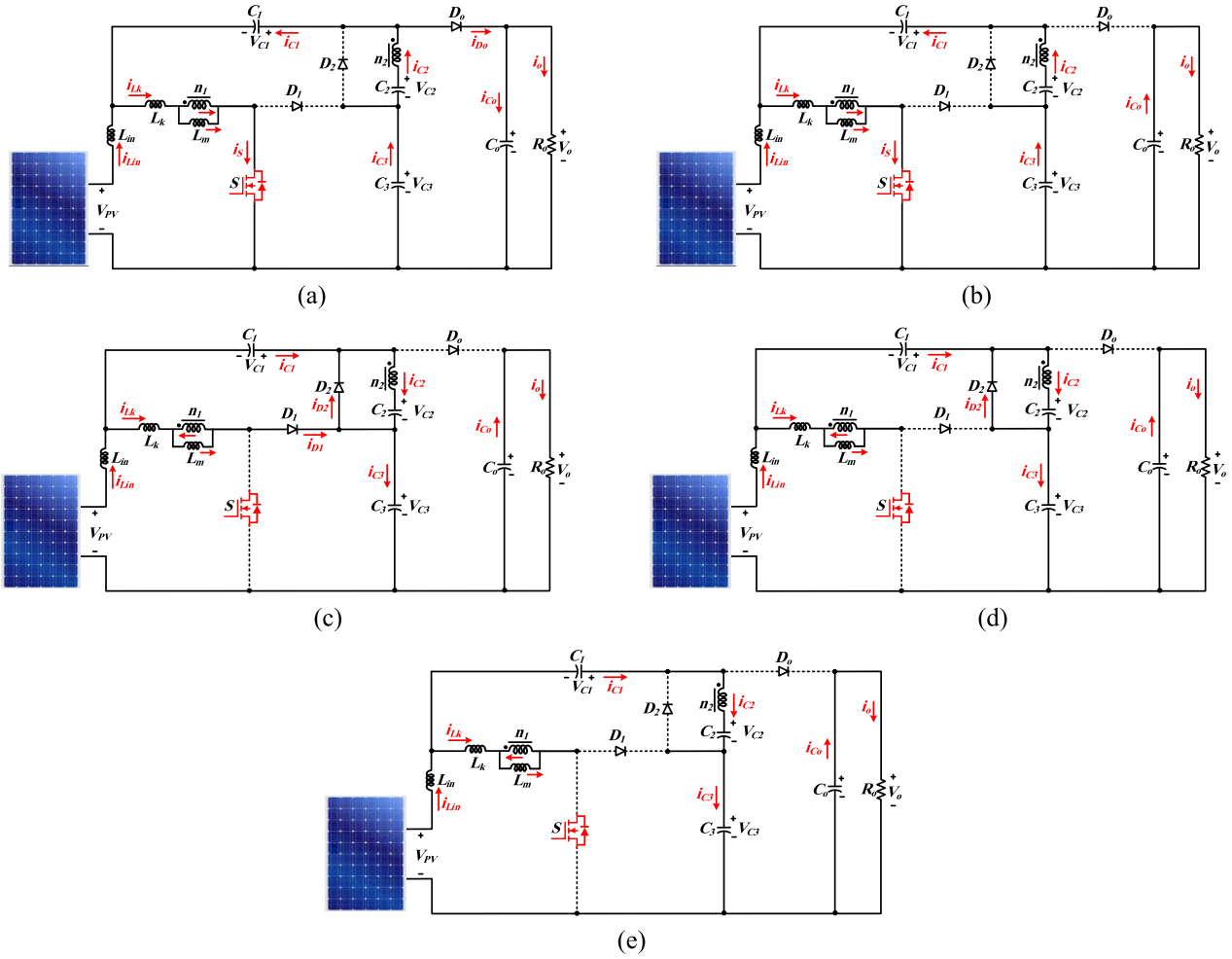

FIGURE 4. The converter equivalent circuits for different modes of operation.

and magnetizing inductance L_m, respectively. V_{n2} is the the secondary winding voltage, V_o is the output voltage. V_{C1}, V_{C2}, and V_{C3} are capacitors voltages. i_{Lk} is the leakage inductance current, i_{Lm} is the magnetizing inductance current, i_{C1}, i_{C2}, i_{C3}, and i_{Co} are the capacitors currents.

Mode#2 [$t_1 < t < t_2$]: At $t = t_1$, diode D_o is turned OFF at ZCS condition. So, its reverse recovery problem can be ignored. Power MOSFET S is still turned ON and the current of L_{in} and L_m is decreased and increased, respectively. The diodes are all turned OFF. Figure 4 (b) shows the equivalent circuit of mode 2. This figure shows that the voltage stress across diode D_1 is equal to V_{c3}. Mode 2 ends at $t = t_2$ while the diode D_2 is ON at ZVS condition. Mode 2' equations are achieved as follows:

$$-V_{PV} + V_{L_{in}} - V_{C_1} + V_{n_2} + V_{C_2} + V_{C_3} = 0 \quad (8)$$

$$i_{C_1} = i_{C_2} = i_{C_3} \quad (9)$$

Mode#3 [$t_2 < t < t_3$]: The power MOSFET S is turned OFF in this mode. The voltage across the magnetizing inductance L_m is negative and its current is decreased linearly. However, the current of L_{in} is increased during mode 3. Diode D_1 is turned ON and diode D_o is still reverse biased. Due to the forward bias of D_1, the maximum voltage of active switch S is equal to the voltage of the capacitor C_3. Also, capacitors C_2 and C_3 are charged and C_1 is discharged. The current flow of this mode is illustrated in Fig. 4 (c). Mode 3' equations are expressed as follows:

$$-V_{PV} + V_{L_{in}} + V_{n_1} + V_{C_3} = 0 \quad (10)$$

$$V_{n_2} = -V_{C_2} \quad (11)$$

$$i_{D_1} + i_{C_2} = i_{D_2} + i_{C_3} \quad (12)$$

$$i_{D_2} = i_{C_1} + i_{C_2} \quad (13)$$

where, i_{D1} and i_{D2} are the diodes' currents of D_1 and D_2, respectively.

Mode#4 [$t_3 < t < t_4$]: The power MOSFET S is maintained turned OFF in this mode. At the beginning of this mode, the diode D_1 is turned OFF at ZCS condition and its reverse recovery problem is declined by storing energy in L_k. Diode D_2 is the only semiconductor device that is in ON state during

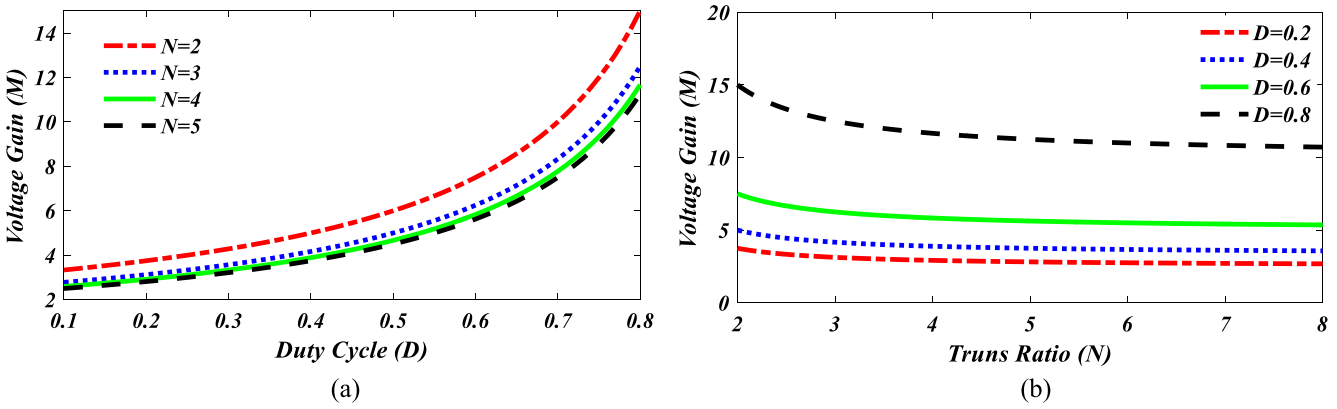

FIGURE 5. Variations of the voltage gain, (a) versus duty cycle (*D*), and (b) versus turn's ratio (*N*).

mode 4. According to Fig.4 (d), due to the forward bias diode D_2, the coupled inductor's secondary side's voltage is equal to V_{C2}. This mode ends at $t = t_4$, when diode D_2 is turned OFF at ZCS condition. Equation (14) can be written in mode 4 as follows:

$$i_{C_1} = i_{C_3} \tag{14}$$

Mode#5 [$t_4 < t < t_5$]: All the semiconductor devices are turned OFF during this mode, as shown in Fig.4 (e). The converter's load feeds by capacitor C_o, and the current of L_{in} and L_m is maintained increasing and decreasing during mode 5. Additionally, capacitors C_1 is discharged, and C_2 and C_3 are charged. The mode equation is obtained as follows:

$$V_{C_1} = V_{n_2} - V_{C_2} \tag{15}$$

According to the modes' analysis, due to the soft-switching, the power MOSFET switching loss and revere recovery problem of diodes are eliminated by the proposed converter, which can improve the entire efficiency of the PV system.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. VOLTAGE GAIN

Applying the voltage second balance principle on the input inductor L_{in} and magnetizing inductor L_m and voltage equations of the previous section, the following equations can be written for the voltage of the capacitors C_1, C_2, and C_3:

$$V_{C_1} = \frac{N - D}{(1 - D)(N - 1)} V_{PV} \tag{16}$$

$$V_{C_2} = \frac{N}{N - 1} V_{PV} \tag{17}$$

$$V_{C_3} = \frac{1}{1 - D} V_{PV} \tag{18}$$

where, N is coupled inductor turns ratio and D is the switch's duty cycle.

Finally, by using equation (4), the output voltage can be expressed based on the input PV panel's voltage, N, and D as follows:

$$V_o = \frac{2N - 1}{(1 - D)(N - 1)} V_{PV} \tag{19}$$

Figure 5 (a) and (b) show the variations of voltage gain versus D and N of the coupled inductor, respectively. Figure 5 shows that the proposed converter's voltage gain is increased with the D and N enhancement.

B. VOLTAGE STRESS

The following equation can be written for power MOSFET S and diode D_1:

$$V_S = V_{D_1} = V_{C_3} = \frac{1}{1 - D} V_{PV} = \frac{N - 1}{2N - 1} V_o \tag{20}$$

where, V_S is the voltage across power MOSFET, V_{D1} is the voltage across the diode D_1.

Also, the voltage stress across diodes D_2 and D_o can be expressed as (21):

$$V_{D_2} = V_{D_o} = V_o - V_{C_3} = \frac{N}{(1 - D)(N - 1)} V_{PV} = \frac{N}{2N - 1} V_o \tag{21}$$

where, V_{D2} is the voltage across voltage across the diode D_2 and V_{Do} is the voltage across the output diode D_o.

The voltage stress on power MOSFET S and diode D_1 are equal and diodes D_2 and D have the same value of voltage stress. Figure 6 shows the normalized voltage stresses' variations across the semiconductors versus N and a constant $D(D = 0.6)$.

C. CURRENT CALCULATION

In this section, the average and root mean square (RMS) currents are calculated. According to Fig. 2, the average currents of all diodes are equal:

$$I_{D_1}^{avg} = I_{D_2}^{avg} = I_{D_3}^{avg} = I_o \tag{22}$$

where, $I_{D_1}^{avg}$, $I_{D_2}^{avg}$, and $I_{D_o}^{avg}$ are the average currents of diodes D_1, D_2, D_o, respectively. I_o is the output current.

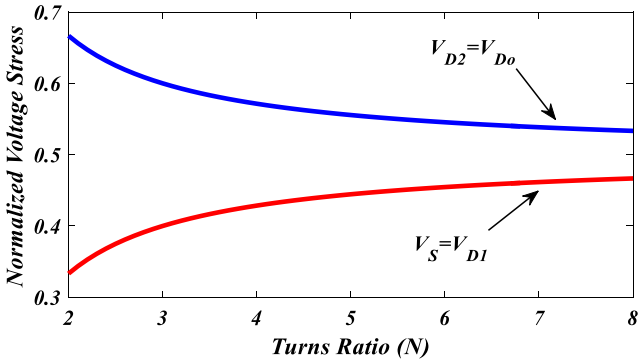

FIGURE 6. Variations of the voltage stress across semiconductors versus turns ratio (*N*).

The average currents of MOSFET are calculated as follows:

$$I_S^{avg} = \frac{(3N-1)(2N-1) - 3((N-1)(1-D))}{(2N-1)(N-1)} I_o \quad (23)$$

Also, the input and magnetizing currents are obtained as follows:

$$I_{L_{in}}^{avg} = \frac{(N-1)(1-D)}{2N-1} I_o \quad (24)$$

$$I_{L_m}^{avg} = \frac{(3N-1)(2N-1) - 3((N-1)(1-D))}{(2N-1)(N-1)} I_o \quad (25)$$

It should be noticed that the RMS currents are necessary for efficiency analysis. Equations (26)-(30), as shown at the bottom of the next page, describe the calculated diodes' RMS currents and the power MOSFET. In (26) - (29), $I_{D_1}^{rms}$, $I_{D_2}^{rms}$, and $I_{D_o}^{rms}$ represent the RMS currents of diodes D_1, D_2, D_o, respectively. Also, I_S^{rms} is the RMS current of the power MOSFET.

Also, the capacitors, input inductor, and coupled inductor's primary and secondary RMS currents are obtained as (30)-(36):

$$I_{L_{in}}^{rms} = \sqrt{\frac{(N-1)(1-D)}{2N-1}} I_o \quad (34)$$

$$I_{n_1}^{rms} = \sqrt{\frac{(3N-1)(2N-1) - 3(N-1)(1-D)}{(2N-1)(N-1)}} I_o \quad (35)$$

$$I_{n_2}^{rms} = \sqrt{\frac{1}{N(1-D)}} I_o \quad (36)$$

In (30) - (36), $I_{C_1}^{rms}$, $I_{C_2}^{rms}$, $I_{C_3}^{rms}$ and $I_{C_o}^{rms}$ are the RMS currents of capacitors C_1, C_2, C_3, and C_o, respectively. $I_{L_{in}}^{rms}$ is the RMS current of the input inductor, $I_{n_1}^{rms}$ and $I_{n_2}^{rms}$ are the RMS current of the coupled inductor primary side and secondary side, respectively.

IV. EFFICIENCY ANALYSIS

To calculate the efficiency of the DC-DC converter, the elements resistances are considered as follows:

- $R_{DS,ON}$: the MOSFET turn-on mode resistance
- $R(_{Ln1,Ln2})$: the ESR of the coupled inductors' primary and secondary winding.
- $R(_{Lin})$: the ESR of the input inductor.
- R_C: the ESR value of the capacitors.
- R_D: the diodes turn-on mode the resistance

The recommended converter's efficiency can be determined by using (37) and (38).

$$\eta_{converter} = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100\% \quad (37)$$

$$P_{Loss} = P_{MOSFET} + P_{Diodes} + P_{CL} + P_{L_{in}} + P_{Capacitors} \quad (38)$$

In equation (39), P_{MOSFET} represents the MOSFET power loss which can be written as the following:

$$P_{MOSFET} = P_{Conduction} + P_{Switching} \quad (39)$$

where, $P_{conduction}$ and $P_{switching}$ are the conduction and switching losses of the MOSFET S, respectively:

$$P_{Conduction} = R_{DS-ON} \left(I_S^{rms}\right)^2 \quad (40)$$

$$P_{Switching} = \frac{1}{2} f_s (t_{rS} + t_{fS}) I_S^{avg} V_S \quad (41)$$

where, t_{rs} and t_{fs} are the rise and fall times of the MOSFET and f_s is the switching frequency.

P_{Diodes} is the losses of the diodes:

$$P_{Diodes} = P_{Conduction,D} + P_{Forward\_Voltage} \quad (42)$$

where, $P_{conduction\_D}$ and $P_{Forward\_Volatge}$ are the conduction losses of the diode and forward voltage losses, respectively:

$$P_{Conduction\_D} = \sum_{i=1}^{Number\ of\ Diodes} R_{D_i} \left(I_{D_i}^{rms}\right)^2 \quad (43)$$

$$P_{Forward\_Voltage} = \sum_{i=1}^{Number\ of\ Diodes} V_{D_i} I_{D_i}^{avg} \quad (44)$$

The conduction losses of the coupled and input inductor can be expressed as follows:

$$P_{CL} = R_{L_{n1}} \left(I_{n_1}^{rms}\right)^2 + R_{L_{n2}} \left(I_{n_2}^{rms}\right)^2 \quad (45)$$

$$P_{L_{in}} = R_{L_{in}} \left(I_{L_{in}}^{rms}\right)^2 \quad (46)$$

The capacitors power loss P_C can be written as follows:

$$P_{Capacitors} = \sum_{i=1}^{Number\ of\ Capacitors} R_{C_i} \left(I_{C_i}^{rms}\right)^2 \quad (47)$$

V. DESIGN CONSIDERATIONS

A. INDUCTORS

The value of L_{in} and L_m can be calculated using (48):

$$L = \frac{V_L D}{\Delta i_L f_s} \quad (48)$$

where, Δi_L is the inductor current ripple.

In order to obtain the CCM condition, the input and magnetizing inductances current ripple should be assumed as follows:

$$\Delta i_L \leq \frac{I_L^{avg}}{2} \tag{49}$$

So, the value of L_{in} and L_m can be calculated based on input voltage, duty cycle, switching frequency, and output average current as follows:

$$L_m \geq \frac{2D\,(2N-1)\,(N-D)\,V_{PV}}{f_s\,[(3N-1)\,(2N-1)-3\,(N-1)\,(1-D)]} \tag{50}$$

$$L_{in} \geq \frac{2ND\,(2N-1)\,V_{PV}}{f_s\,(N-1)^2\,(1-D)} \tag{51}$$

Using equation (19), N of the coupled inductor is given as follows:

$$N = \frac{M\,(1-D)-1}{M\,(1-D)-2} = \frac{\frac{V_o}{V_i}\,(1-D)-1}{\frac{V_o}{V_i}\,(1-D)-2} \tag{52}$$

As can be seen in equation (52), V_{in}, V_o, and duty cycle (D) affect the number of coupled inductor's turns ratio (N).

B. CAPACITORS

The value of the capacitors can be calculated using (53):

$$C = \frac{i_C D}{\Delta V_C f_s} \tag{53}$$

where, ΔV_C is the capacitor voltage ripple and assumed as (54):

$$\Delta V_C \leq 2\% V_C \tag{54}$$

By using (54) ΔV_C can be neglected. Therefore, the value of the capacitors can be written versus duty cycle, switching frequency, input voltage, and the output average current as (55)- (58):

$$C_1 \geq \frac{D\,(1-D)\,(N+1)\,I_o}{2\% f_s\,(N-D)\,V_{PV}} \tag{55}$$

$$C_2 \geq \frac{DI_o}{2\% f_s N\,(1-D)\,V_{PV}} \tag{56}$$

$$C_3 \geq \frac{(1-D)\,I_o}{2\% f_s D V_{PV}} \tag{57}$$

$$C_o \geq \frac{D\,(1-D)\,(N-1)\,I_o}{2\% f_s\,(2N-1)\,V_{PV}} \tag{58}$$

$$I_{D_1}^{rms} = \sqrt{\frac{1}{1-D}}I_o \tag{26}$$

$$I_{D_2}^{rms} = \sqrt{\frac{(2N-1)\,(N-1)}{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}}I_o \tag{27}$$

$$I_{D_o}^{rms} = \sqrt{\frac{1}{1-D}}I_o \tag{28}$$

$$I_S^{rms} = \frac{(3N-1)\,(2N-1)-3\,((N-1)\,(1-D))}{(2N-1)\,(N-1)}\sqrt{\frac{(2N-1)\,(N-1)}{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}}I_o \tag{29}$$

$$I_{C_1}^{rms} = \sqrt{\frac{(N-1)\,(1-D)}{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}}\left(\frac{(2N-1)\,(N+1)}{(N-1)\,(1-D)}I_o\right) \tag{30}$$

$$I_{C_2}^{rms} = \sqrt{\frac{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}{N^2\,(2N-1)\,(N-1)\,(1-D)}+\frac{1}{(N-1)^2}}\left(\frac{(2N-1)\,(N+1)}{(N-1)\,(1-D)}I_o\right) \tag{31}$$

$$I_{C_3}^{rms} = \sqrt{\frac{(N-1)\,(1-D)}{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}}\left(\frac{(2N-1)}{(1-D)}I_o\right) \tag{32}$$

$$I_{C_o}^{rms} = \sqrt{\frac{N\,((2N-1)-2\,(N-1)\,(1-D))-(2N-1)+(N-1)\,(1-D)}{N^2\,(2N-1)\,(N-1)\,(1-D)}}I_o \tag{33}$$

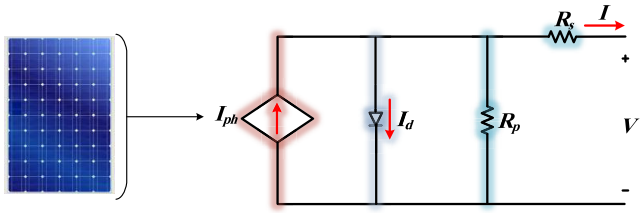

FIGURE 7. Single-diode model of a PV panel.

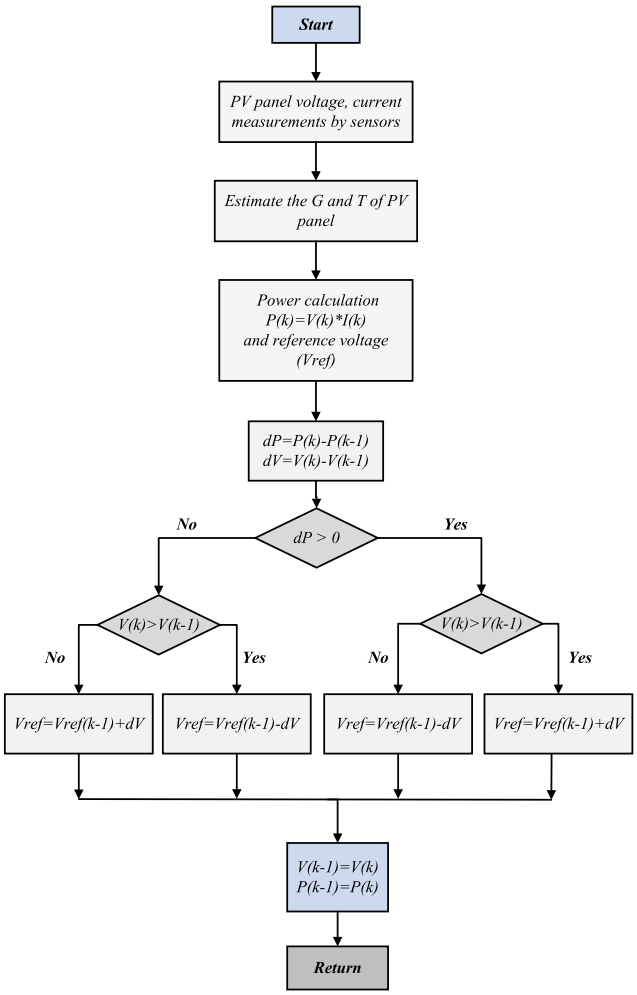

FIGURE 8. Flowchart of the proposed IP&O algorithm for MPPT.

VI. THE PROPOSED IP&O ALGORITHM FOR MPPT OF INPUT PV PANEL

A. PV PANEL MODELING

In this paper, the used PV panel model is single-diode, considering the parallel and series resistances as shown in Fig. 7.

The model parameters are determined based on the introduced method in [27], [28]. The current-voltage (I-V) relation is written as follows:

$$I = I_{ph} - I_0 \left[\exp\left(\frac{V + IR_s}{aV_t} \right) - 1 \right] - \frac{V + IR_s}{R_p} \quad (59)$$

where I_{ph} is the PV panel photocurrent generated from the solar radiation received by the PV panel surface and

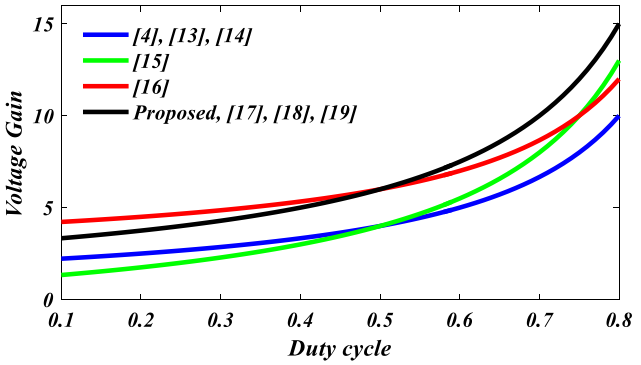

FIGURE 9. Comparison between the proposed converter and the existing structures in terms of voltage gain, ($N = 2$).

calculated by (60), I_0 is the diode reverse saturation current and given by (61), R_s and R_p are PV panel series and parallel resistances, respectively. a is the ideality factor of the diode, and T is the PV panel surface temperature. V_t is the PV panel thermal voltage calculated by (62).

$$I_{ph} = \left(I_{ph,n} + k_i \left(T - Tn\right)\right) \frac{G}{G_n} \quad (60)$$

$$I_0 = \frac{I_{ph} - \frac{V_{oc,n}}{R_p}}{\exp\left(\frac{V_{oc,n}}{aV_t}\right) - 1} \quad (61)$$

$$V_t = \frac{N_s kT}{q} \quad (62)$$

In (60) and (61), G is the irradiation level on the PV panel surface, k_i is the temperature coefficient of the short-circuit current, $I_{ph,n}$, and $V_{oc,n}$ are the PV panel photocurrent and open-circuit voltage under STC. N_s is the number of series-connected PV cells within the PV panel, q is the elementary charge, k is Boltzmann's constant [29]–[31].

B. IMPROVED P&O (IP&O)

The classic P & O algorithm uses a constant reference voltage to track the MPP of the PV panel. This reference voltage is obtained from equation (63).

$$V_{ref} = k \times V_{oc} \quad (63)$$

where, k is a constant coefficient, and its value is between 0.71 and 0.78. This method can acceptably track the MPP of the PV panel in STC conditions. For low irradiance value, this method isn't accurate (because k is constant and the accuracy of equation (63) isn't acceptable for low irradiance range). In the proposed improved P&O, to enhance the MPPT accuracy of the P&O algorithm, equation (64) is used for reference voltage calculation [32].

$$V_{ref} = \frac{V_{mpp}^{STC}}{1 + \delta \ln\left(\frac{G_n}{G}\right)} + k_v(T - T_n) \quad (64)$$

where, δ is a constant coefficient, which its value is adjusted to 0.05. V_{mpp}^{STC} is the MPP voltage of the PV panel in the STC

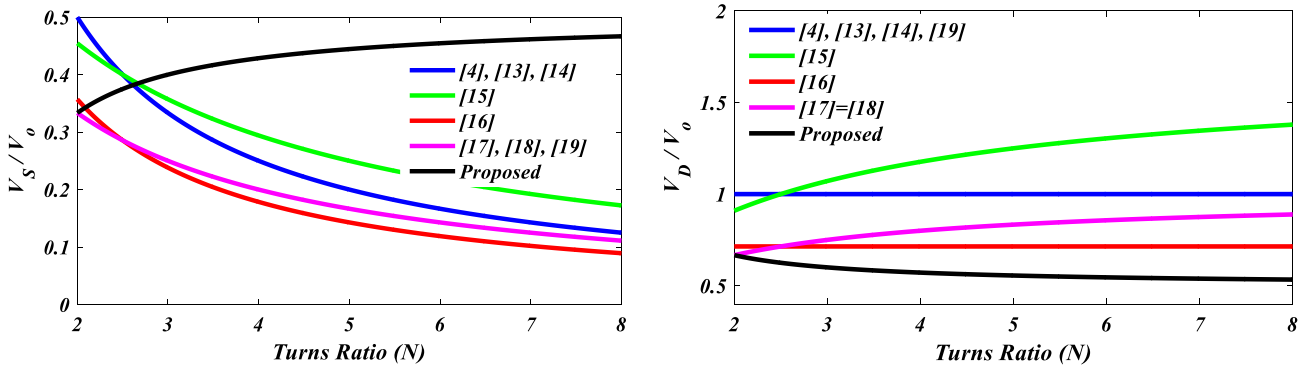

FIGURE 10. Voltage stress comparison between the proposed converter and the other introduced structures, (a) across power switches, (b) across diodes ($D = 0.6$).

conditions (can be obtained from PV panel datasheet), and k_v is the open-circuit thermal-voltage coefficient. Considering equation (64), the reference voltage of the P&O algorithm is a function of the PV panel's temperature and irradiance. Therefore, for any temperature and irradiance range, the improved algorithm's accuracy is higher than the classical P&O, even in low irradiance value (exp: under 400 W/m^2). According to the method introduced in [33], first, the photocurrent of the PV panel is estimated by (65). Then, the PV panel irradiance is calculated via (66) as follows:

$$I_{ph} = I + I_0 \left(exp\left(\frac{V + IR_s}{aV_t} \right) - 1 \right) + \frac{V + IR_s}{R_p} \quad (65)$$

$$G = \frac{I_{ph} G_n}{I_{ph,n}} \quad (66)$$

In these relations, the value of I is measured by the current sensor, and the PV panel voltage is measured using a voltage sensor. It should be noted that the values of R_p, R_s, and a change with the PV panel irradiance and temperature variation. However, their effect is minimal on the value of I_{ph}, and all of these parameters are calculated at STC conditions. After estimating of PV panel irradiance level (G), its surface temperature (T) is estimated by (67) as follows:

$$GA_m = VI + U_{pv} A_m (T - T_n) \quad (67)$$

U_{pv} is the overall heat exchange coefficient, A_m is the PV panel surface area, and Ta is the ambient temperature [34], [35]. The proposed method should be noticed the same as classical P&O uses from two sensors (current and voltage sensors. So, these methods' cost is equal, but the proposed method has better performance in terms of MPPT accuracy and speed. The flowchart of the presented IP&O algorithm is shown in Fig.8.

VII. COMPARISON STUDY

In this part, a comparison between the proposed converter with a high voltage rate and other converters is provided. In this comparison, voltage gain, voltage stress throughout the power switches, and the diodes, number of used components, soft switching, and efficiency are taken into account. This comparison is summarized in Table 1. It has to be mentioned that the value of $N = 2$ in this section. According to this table, the converters in [17]–[19], and the suggested converter have the highest voltage gain between the introduced converters in Table 1. Also, Fig.9 shows the voltage gain comparison. It should be noticed that the DC-DC converter in [17] suffers from a lack of soft switching on semiconductor components. The presented converter in [18] has an equal number of elements and similar voltage stress conditions across power switches and diodes. However, the proposed converter's efficiency at 200 W output power level is higher than this converter. The total number of components in [19] is equal to 16, which is higher than the suggested converter.

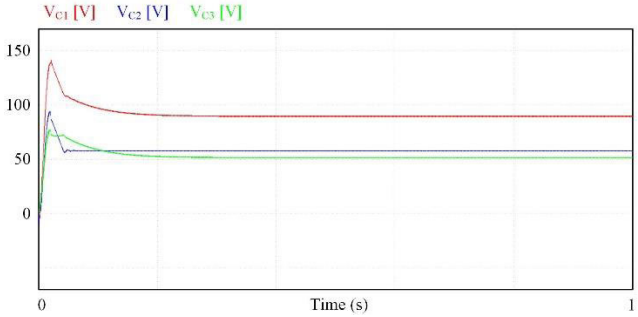

FIGURE 11. Simulation result of the capacitor voltages.

Figure 10 (a) shows the voltage stress across power switches of the mentioned converters. The proposed converter has higher voltage stress than the other topologies for $N > 3$. However, for a higher coupled inductor's turns ratio, the power loss is increased and consequently, the total efficiency is decreased. Therefore, operating of a DC-DC converter in low turns ratio number is preferred. Also, for $N = 2$, only [16] has lower voltage stress across the power switch than the presented converter. However, the suggested converter in [16] suffers from lack of soft switching, a high

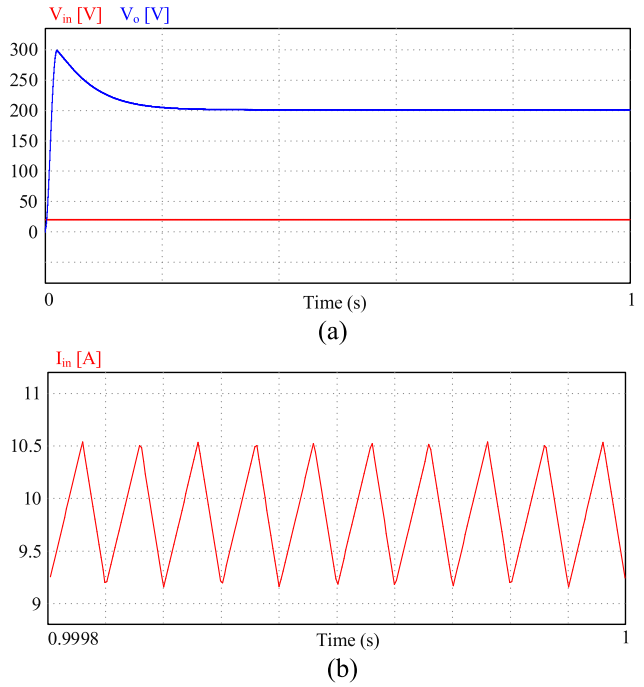

FIGURE 12. Simulation result of the capacitor voltages of the proposed converter, (a) V_o-V_{in}, (b) I_{in}.

number of components, high voltage stress across diodes, and low efficiency. Figure 10 (b), presents the maximum voltage stress across diodes. According to this figure, the proposed converter has the lowest voltage stress between the converters shown in Table 1. Due to the soft switching conditions, the proposed converter has an acceptable efficiency at full load conditions.

Table 2 presents the cost comparison of the proposed converter with other structures is shown in. It is obvious from Table 2 that the proposed converter has a cost-effective. The cores number and N value can be decreased by increasing the power rating. Meanwhile, the nominal values of the power components are decreased by increasing the power rating, so it can be said that the proposed converter is work in high power rating with high efficiency and lower cost. Therefore, by comparing the suggested topology with other previous coupled inductor-based DC-DC structures, it can be concluded that the proposed topology benefits from high voltage gain, low voltage stress of the semiconductors, soft-switching capability, and high efficiency with an acceptable number of components. Furthermore, the proposed converter can perform the MPPT of PV panels. All of these benefits make the proposed converter to be a proper candidate for PV applications.

VIII. SIMULATION RESULTS

This section provides the simulation result of the proposed converter. PSIM software is used to simulate the proposed converter. The proposed structure is simulated at $f_s = 50$ kHz, $V_{in} = 20, N = 3/2$, and D $= 0.6$ in 200 W load power

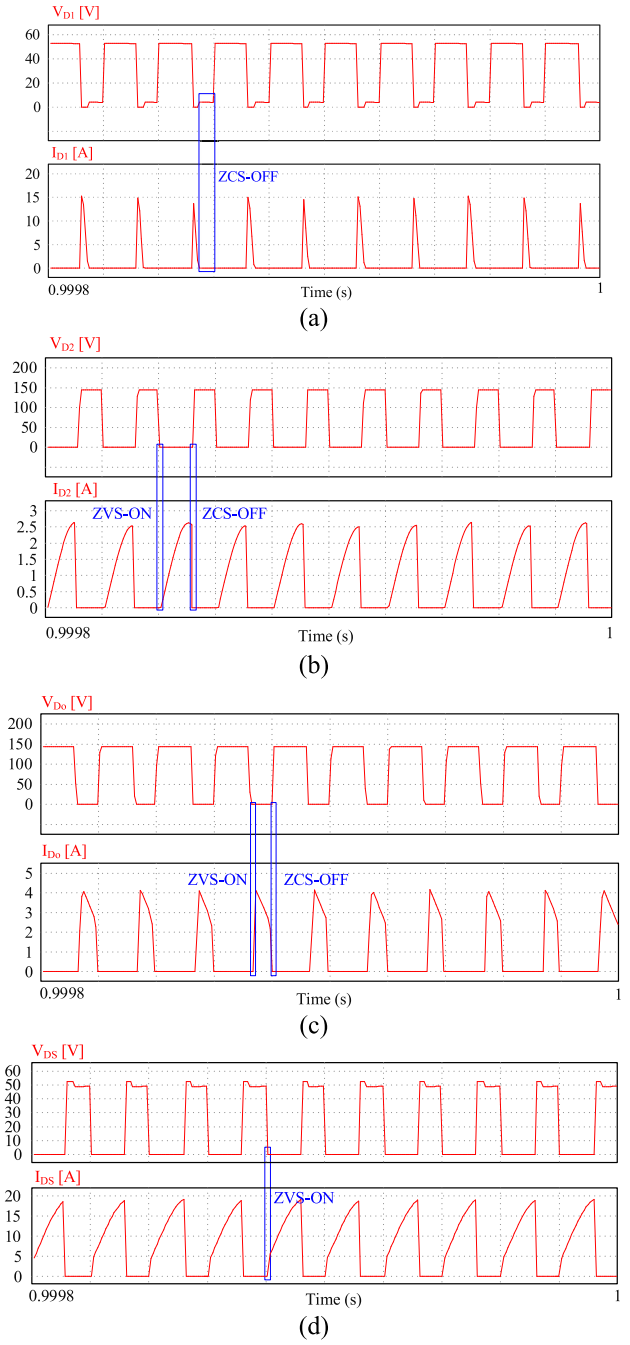

FIGURE 13. Simulation result of the capacitor voltages proposed, (a) V_{D1}-I_{D1}, (b) V_{D2}-I_{D2}, (c) V_{Do}-I_{Do} and (d) V_{sw}-I_{sw}.

level. The capacitors voltage waveforms are demonstrated in Fig. 11. The capacitors voltages are 88 V, 57 V, and 50 V, respectively. The input and output voltage waveforms are indicated in Fig. 12 (a). The input voltage is 20 V, which is increased to 201 V. The input current waveform is depicted in Fig. 12 (b). The diode D_1 voltage and current simulation results are depicted in Fig. 13 (a) that are 50 V and 15 A, respectively. This figure shows that the ZCS condition is in OFF-state of diode D_1. Figure 13 (b), presents the voltage and current waveform of diode D_2, which are 147 V and

TABLE 1. Comparison of the proposed DC-DC structure with high voltage rate and other similar structures.

Converter	Number of components					Voltage Gain	V_s/V_o	V_D/V_o	Efficiency at 200 W, %	Soft Switching
	Mag*	S*	D*	C*	Total					
[4]	2	2	2	3	9	$\frac{N}{1-D}=5$	$\frac{1}{N}=0.5$	1	95.5	Yes
[13]	2	1	2	2	7	$\frac{N}{1-D}=5$	$\frac{1}{N}=0.5$	1	95.9	Yes
[14]	2	1	2	4	9	$\frac{N}{1-D}=5$	$\frac{1}{N}=0.5$	1	94	Yes
[15]	2	1	4	3	10	$\frac{1+ND}{1-D}=5.5$	$\frac{1}{1+ND}=0.45$	$\frac{N}{1+ND}=0.9$	93.8	No
[16]	1	2	5	3	11	$\frac{N(2-D)}{1-D}=7$	$\frac{1}{2N(2-D)}=0.17$	$\frac{1}{2-D}=0.71$	94.55	No
[17]	2	1	3	3	8	$\frac{N+1}{1-D}=7.5$	$\frac{1}{N+1}=0.33$	$\frac{N}{N+1}=0.66$	-	No
[18]	2	1	3	4	10	$\frac{N+1}{1-D}=7.5$	$\frac{1}{N+1}=0.33$	$\frac{N}{N+1}=0.66$	94.6	Yes
[19]	2	4	5	5	16	$\frac{N+1}{1-d}=7.5$	$\frac{1}{N+1}=0.33$	1	95	Yes
Proposed	2	1	3	4	10	$\frac{2N-1}{(1-D)(N-1)}=7.5$	$\frac{N-1}{2N-1}=0.33$	$\frac{N}{2N-1}=0.66$	96.04	Yes

*S=switch, *D=diodes, *C=capacitors, *Mag= Magnet Core, N=2, and D=0.6.

TABLE 2. Cost comparison of the proposed DC-DC structure with other structures.

Converter	Cost of components				
	Cores	Switches	Diodes	Total cost of Capacitors	Total
[4]	2×4.83$	2×2.64$	2×1.56$	3.4$	21.46$
[13]	2×5.96$	2.72$	2×3$	3.56$	24.2$
[14]	2×5.96$	2.96$	2×0.15$	4.15$	19.33$
[15]	2×5.56$	1.01$	4×3$	2.88$	27.01$
[16]	5.83$	2×3$	3×1.69$, 2×1.13$	9.18$	28.34$
[17]	2×6.37$	3.95$	3×3.4$	6.66$	33.55$
[18]	2×5.83$	2.41$	3×1.04$	11.18$	28.37$
[19]	2×5.83$	2×2.5$	5×4.23$	12.99$	50.8$
Proposed	2×2.77	7.51$	3×3$	3.32$	25.37$

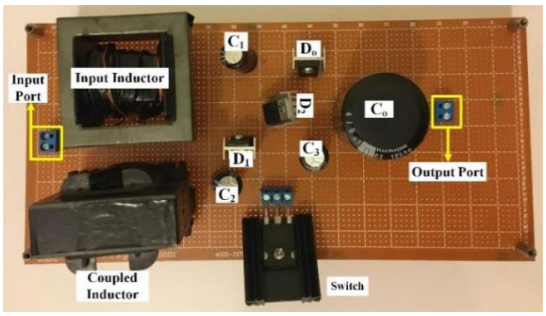

FIGURE 14. The experimental prototype of the proposed converter.

2.6 A, respectively. The voltage and current simulation results of the diode D_o, are illustrated in Fig. 13 (c) that are about 147 V and 4.1 A, respectively. From Figs. 13 (b) and 13 (c), it can be found that diodes D_2 and D_o have ZVS-ON and ZCS-OFF condition, that leads to increase the overall efficiency of the suggested converter. The simulation results of the drain-source voltage and drain-current of the power switch are showed in Fig. 13 (d), which are about 50 V and 17 A, respectively. Besides, there is ZVS condition in ON-state of the switch.

IX. EXPERIMENTAL RESULTS

A. LABORATORY RESULTS OF THE PROPOSED STRUCTURE

To show the proficiency of the proposed converter, it has been tested at f_s = 50 kH, V_{in} = 20, and D = 0.6 in 200 W load power level. The experimental prototype of Fig. 14 includes the following components:

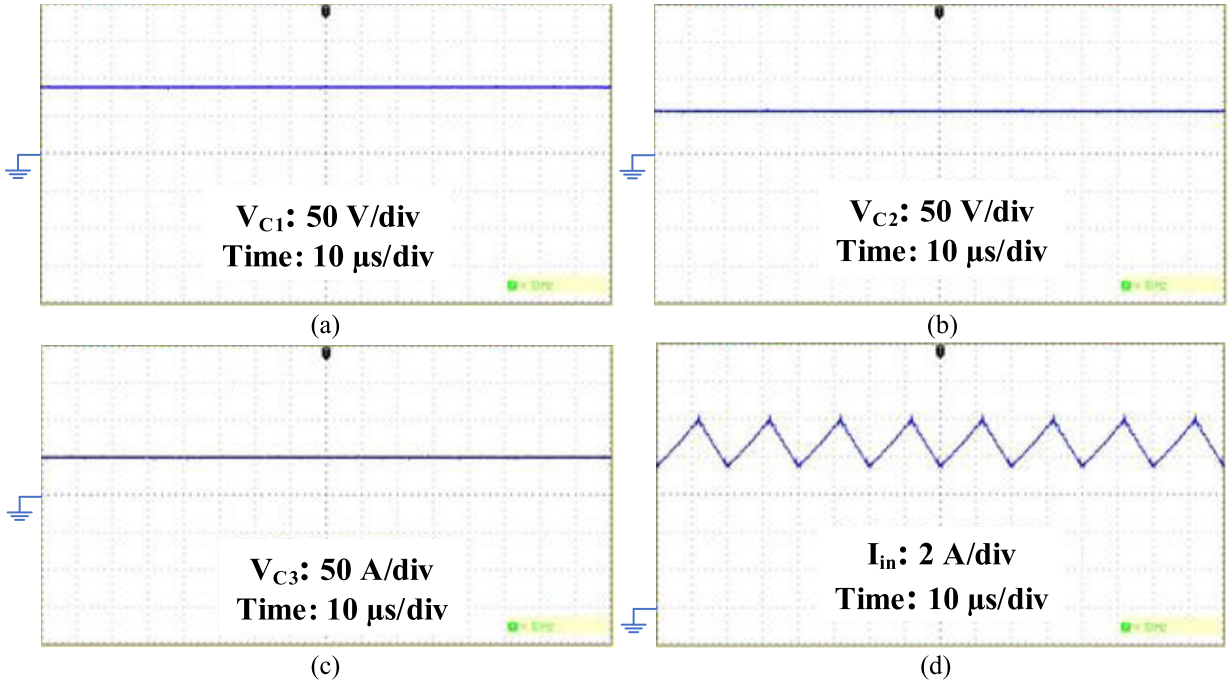

FIGURE 15. Experimental measurement of the proposed converter, (a) V_{C1}, (b) V_{C2}, (c) V_{C3}, and (d) I_{in}.

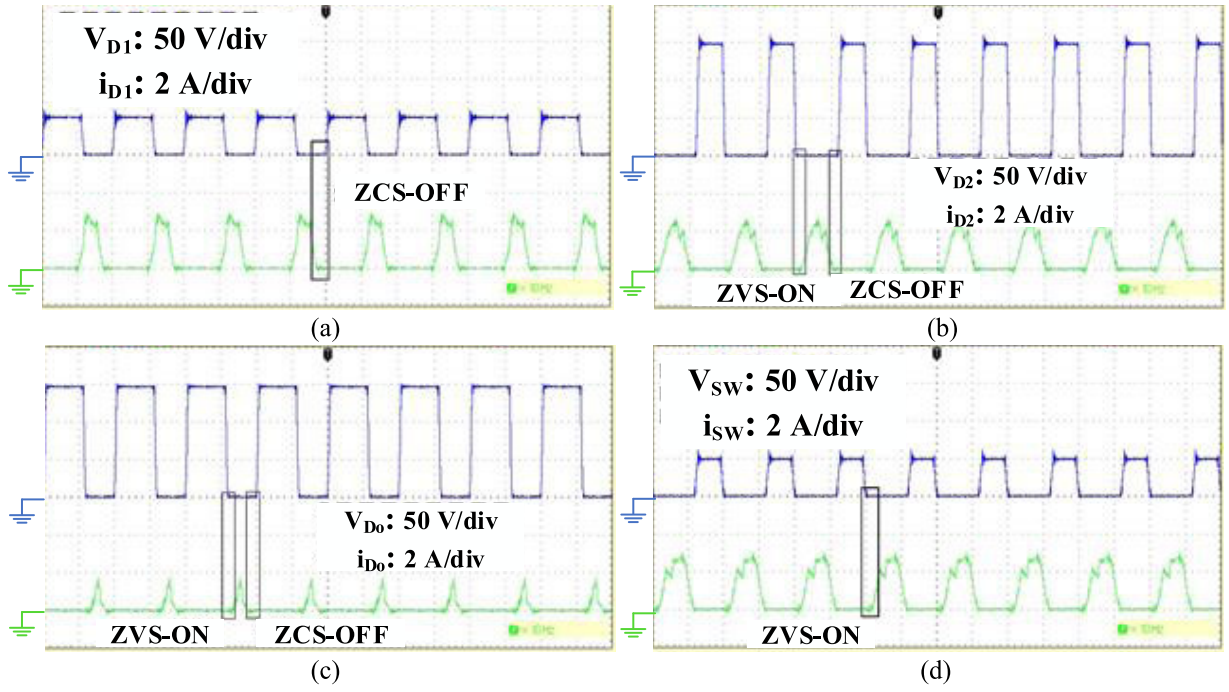

FIGURE 16. Experimental measurement of the proposed converter, (a) V_{D1}-I_{D1}, (b) V_{D2}-I_{D2}, (c) V_{Do}-I_{Do} and (d) V_{sw}-I_{sw}.

- The capacitors are the electrolyte model and their capacity is 100 μF in 200 V.
- The output capacitor which is used to reduce the output voltage ripple is the electrolyte model and its capacity is 400 μF in 400 V.
- The diodes D_1, D_2 and D_o are fast recovery diode. The MUR2060 model has been utilized, which is low cost and low voltage drop diode. The maximum reverse voltage and forward current of this diode are 200-600 V and 20 A, respectively.

FIGURE 17. Experimental measurement of the proposed converter, (a) V_{in}, and (b) V_o.

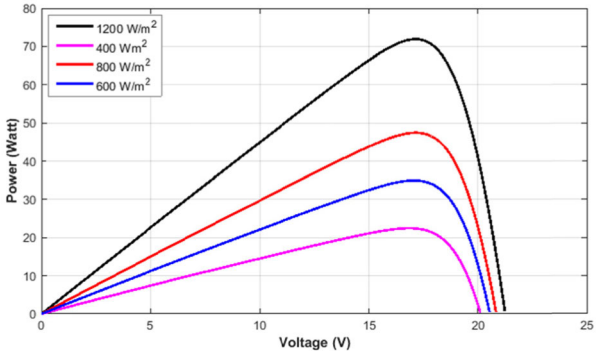

FIGURE 18. The P-V curves of case 1.

- MOSFET is used for the power switch of the suggested converter. The MOSFET model is STW55NM60 with $R_{DS-ON=}$0.047. This type has merits of low input capacitance and gate charge, and low gate resistance. The maximum drain-source voltage and drain-current of these switches are 600 V and 51 A, respectively.
- EPCOS B66344 coupled inductor with Ferrite core EE55 model. Besides, the input inductor is EPCOS B66344 model with ferrite core EE50. The turn ratio of the coupled inductor equal to $N = 3/2$.
- For measuring the experimental waveforms, the Digital Signal Oscilloscope with GDS-10748 model has been utilized. The input source is RN-3005-D model DC supply. For switching the power circuit of the suggested converter, the ATMEGA16 microcontroller has been used.

The specifications of the circuit components of the prototype are indicated in Table 3.

The main waveform of the proposed converter is indicated in Figs.15-17. Figure15 shows the capacitor voltage waveforms and input current waveform. The measured voltage of the capacitor C_1 is 88 V in indicated in Fig.15 (a). As illustrated in Fig.15 (b), the measured voltage of the capacitor C_2 is 57 V. The measured voltage of the capacitor C_3 is 50 V as indicated in Fig.15 (c). The input current waveform is illustrated in Fig.15 (d). It can be found from Fig.15 (d) that

TABLE 3. Circuit components specifications of the prototype.

Element	Specification
Switch	STW55NM60
Diodes	MUR2060
L_{in}	500 µH
L_m	Ferrite core EE50, 250 µH
C_1,C_2 and C_3	200 V/100 µF
C_o	400 V/400 µF
L_{k1} and L_{k2}	2 µH

the current ripple of the input current is low, which increases the lifetime of the converter. Figure 16 presents the voltage and current waveform of the switch and diodes. The voltage and current of diode D_1 are shown in Fig.16 (a), which are about 50 V and 15 A, respectively. The ZCS condition of the diode D_1 in OFF-state is indicated in this figure that decreases diode's reverse recovery losses. From Fig.16 (b), the maximum voltage and the maximum current of diode D_2 are 147 V and 2.6 A, respectively. The diode D_2 is started to conduct in ZVS condition and turned off in ZCS condition. There is ZVS in ON-state and ZCS in OFF-state conditions for diode D_o like diode D_2, which is indicated in Fig.16 (c). Regarding this figure, the voltage and current of diode D_o is near 147 V and 4.2 A, respectively. The voltage and current waveform of the main switch is depicted in Fig.16 (d) that are about 50 V and 17 A, respectively. As seen in this figure, the active MOSFET is switched on in ZVS condition, which decreases the switching losses of the suggested converter. All semiconductor devices such as diodes and switches have soft-switching capability that increases the proposed converter's overall efficiency. The input voltage and output voltage waveforms of the proposed structure are shown in Figs.17 (a) and 17 (b), respectively. The input voltage is 20 V, which has been increased to about 197 V with a poor voltage ripple.

B. SIMULATION RESULTS OF MPPT IMPLEMENTATION

In this section, the PV system's performance is tested and compared with the conventional P&O algorithm in two

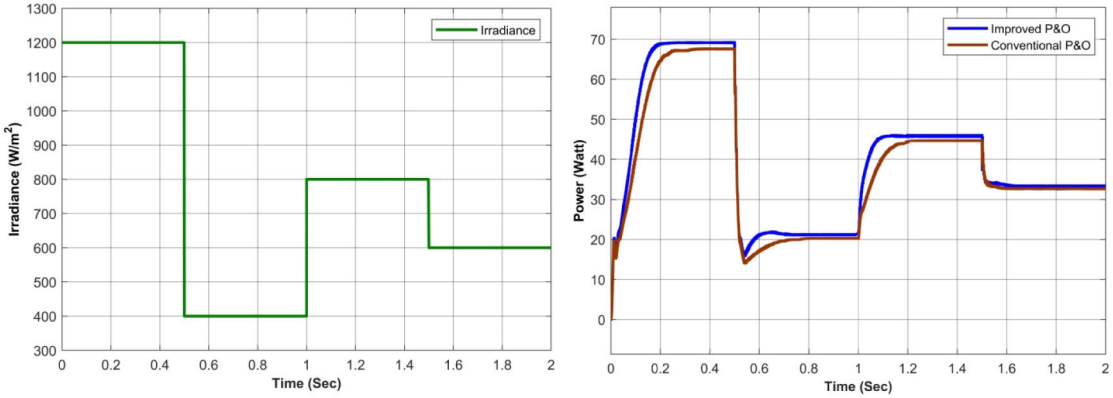

FIGURE 19. MPPT results at different irradiances and T= 25°*C* (a) PV panel varying irradiance and (b) output power.

TABLE 4. Data sheet of the PV panel MSX60.

PV Panel Parameters at STC	Values
Maximum Power (P_{max})	60 W
Open Circuit Voltage $(V_{oc,n})$	21.1 V
Maximum Power Voltage (V_{mp})	17.1 V
Short Circuit Current $(I_{sc,n})$	3.8 A
Maximum Power Current (I_{mp})	3.5 A
Number of Series Cells (N_s)	36
Temperature Coefficient of I_{sc} (k_i)	3 $\frac{mA}{°C}$
Temperature Coefficient of V_{oc} (k_v)	-0.08 $\frac{V}{°C}$
Overall heat exchange (U_{pv})	28.8 $\frac{W}{m^2K}$
PV panel area (A_m)	0.5547 m^2

different cases in which there is a sudden or rapid change in irradiance and temperature. The used PV panel model is MSX60, and its specifications are given in Table 4.

- *Case1: Variation in Solar Irradiance*

In this case, the MPPT algorithm's performance is assessed with a fixed surface temperature of 25 0C and a rapid variation in irradiance. The P-V curves of this case are shown in Fig.18. Initially, the irradiance level is set to 1200 W/m^2 at a time interval [0 0.5] *sec* and is dropped rapidly at 0.5 *sec* to 400 W/m^2. The solar irradiance kept constant till 1 *sec*, and at 1 *sec* it is increased rapidly to 800 W/m^2. Whereas the solar irradiance is again decreased rapidly at 1.5 *sec* and the value of irradiance remains constant in the time

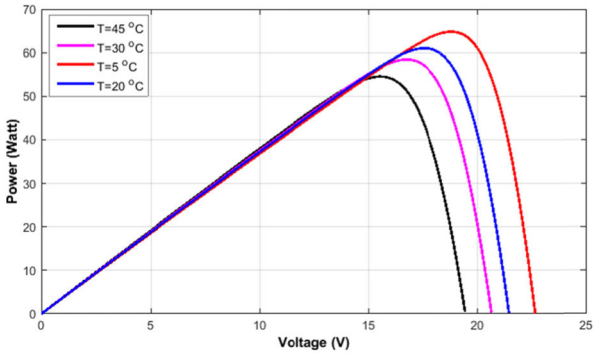

FIGURE 20. The P-V curves of case 2.

interval (1.5, 2) *sec* as presented in Fig. 19 (a). The output power of these varying irradiances is shown in Fig. 19 (b). Generally, it can be noticed that both the algorithms show an outstanding performance and quite similar behavior for rapid variation in irradiance at different time intervals. However, the classical P&O algorithm's transient response is slightly slower compared to the IP&O algorithm.

- *Case 2: Variation in Temperature*

In this case, the MPPT operation is carried out with a constant irradiance (1000 W/m^2) and varying temperatures. The P-V curves of this case are shown in Fig. 20. The value of panel surface temperature is increased or decreased every 0.5 *sec* as presented in Fig.21 (a). The power curves with varying temperatures of both the algorithm are shown in Fig.21 (b). The performance of the P&O algorithm is greatly affected in this case. In all the time intervals, P&O's performance of P&O is deficient compared to IP&O except in interval 1.5∼2 *sec* where both the algorithms show the same performance. In terms of performance, the worst scenario occurs when the temperature is at 45 ^0C, in this time interval (0∼0.5 *sec*), the system does not reach its stabilized state.

The efficiency curve for different levels of power rating is shown in Fig. 22. The efficiency is piloted by considering $N = 1.5, D = 0.6$, and $f_s = 50$ kHz. The maximum

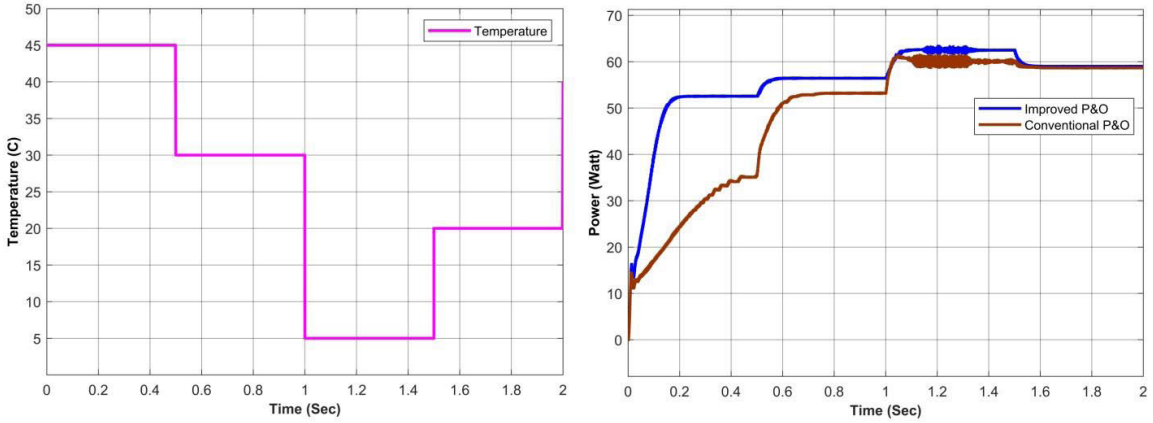

FIGURE 21. MPPT results at different temperatures and G= 1000 W/m^2 (a) PV panel varying surface temperature and (b) output power.

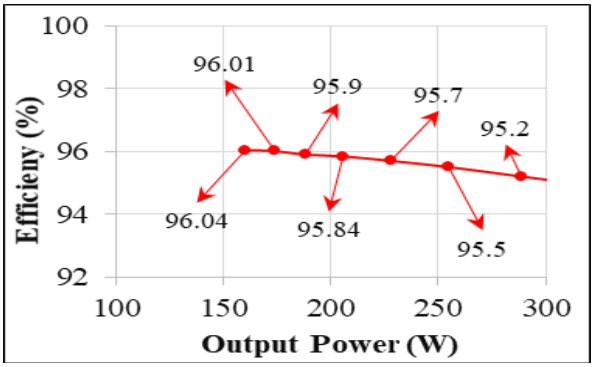

FIGURE 22. The measured efficiency of the proposed structure in various load powers.

efficiency of the mentioned topology is about 96% at input voltage 20V and output power 150W, which is depicted in Fig. 22. The full-load efficiency is approximately 95.2% at 300W. It is obvious that the tested efficiency of the recommended topology has a low tolerance when the load is changing between 150W-300W. Hence, the suggested topology's overall efficiency at all power levels is greater than 95%, which is recommended to employ in PV generations.

X. CONCLUSION

This paper proposed a novel structure of non-isolated DC-DC converter with high voltage gain and soft-switching capability for PV applications. The presented converter benefits from 1) high voltage gain, 2) low input current ripple, 3) high efficiency, 4) simple structure, 5) peak voltage throughout the semiconductor components and 6) low components count. In the presented non-isolated DC-DC converter, a small size and cost coupled inductor with one magnet core is used to increase the voltage conversion ratio. The suggested topology has only one active MOSFET with lower conducting resistance (R_{DS-ON}), which can decrease the control section's conduction losses and complexity. Due to the low input current ripple, the lifetime of the input PV panel is increased and the MPP of the PV panel can be easily tracked. Soft switching conditions include ZVS and ZCS of power MOSFET, and diodes are the other features of the proposed converter which improve efficiency. Additionally, an improved P&O MPPT algorithm is suggested to increase the extracted power from the input PV sources. In the rest of this paper, to verify the performance of the suggested converter, the operation modes principle, steady-state and efficiency calculation, and comparison results with other similar converters are provided. The outcomes of this study proved the theoretical analysis and the efficiency of higher than 95% at different power levels.

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