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Power Quality Enhancement in Sensitive Local Distribution Grid Using Interval Type-II Fuzzy Logic Controlled DSTATCOM

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ABSTRACT In the current scenario, integration of renewables, growth of non-linear industrial and commercial loads results in various power quality issues. Among commercial utilities connected to the grid, hospital-operated loads include sensitive, linear, non-linear, and unbalanced loads. These loads are diverse as well as prioritized, which also causes major power quality issues in the local distribution system. Due to its widespread divergence, it leads to harmonic injection and reactive power imbalance. Distribution Static Compensator (DSTATCOM) is proposed as a solution for harmonic mitigation, load balancing, reactive power imbalances, and neutral current compensation. The present work utilizes Interval Type-2 Fuzzy Logic Controller (IT2FLC) with Recursive Least Square (RLS) filter for generating switching pulses for IGBT switches in the DSTATCOM to improve power quality in the Local Distribution Grid. The proposed approach also shows superior performance over Type 1 fuzzy logic controller and Conventional PI controller in mitigating harmonics. For effective realization, the proposed system is simulated using MATLAB software.

INDEX TERMS Local distribution grid, DSTATCOM, interval type 2 fuzzy logic controller, power quality, and recursive least square filter.

I. INTRODUCTION

Electrical distribution systems are designed to operate under certain voltage and current values, which are sinusoidal in nature [1]. Adopting new technologies results in increased utilization of non-linear load, which poses a major problem of power quality. Non-linear loads tend to stress the system in terms of damaging equipment, current flow through neutral conductors, distortion in current and voltage waveforms, overheating and power factor reduction [2]. Generally, health care facilities require high quality of power to operate their loads at a better performance [3]. But the load concentration in these medical facilities are diverse and consists of light, heavy, non-linear, linear, balanced and unbalanced models. Also, the majority of them are controlled digitally, and they are sensitive too [4]. A typical trade-off between the control and operation is not recommended. For a load to be controlled by digital means, it requires Switched Mode Power Supplies (SMPS) which are less sensitive to good power quality. Heavy loads such as X-ray machines, Computed Tomography (CT) and Magnetic Resonance Imaging (MRI) scan machines, lighting loads at operation theatre and equipment's at Intensive Care Unit (ICU) and Critical Care Unit (CCU) facilities are major power polluters [5]. The operation of these

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types of the load is unavoidable due to their high degree of sensitivity which on disconnection leads to damage or loss of human life [6].

The majority of the loads connected by commercial utilities are heavy and inductive in nature, which can cause voltage sag and swell during load switching. Mitigation of these power quality issues can be achieved with the help of Custom Power Devices (CPD's) [7]. Improvement of power quality is attained by injecting either voltage or current or both into the system at the point of common coupling (PCC) [8]. As a result of this, the terminal voltage is controlled, which results in an improved power factor. CPD's can be of various types such as Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR), and so on [9]. DSTATCOM offers better performance and reliability by injecting necessary reactive power. When there is a sudden removal of large loads, the DSTATCOM provides better voltage support than SVC and other CPD's. Under a non-linear operating range, the DSTATCOM perfectly controls its output current independent of AC system voltage [10]. The DSTATCOM has faultless response time and it has the ability to easily interface with energy storage systems like large capacitors, batteries, Fuel Cell (FC). The DSTATCOM interfaced with FC is proposed in [11].

The control algorithms for DSTATCOM are of many types and its topologies are discussed in [12]. Most commonly used Instantaneous Reactive Power Theory (IRPT), Synchronous Reference Frame Theory (SRFT), and Instantaneous Symmetrical Component Theory (ISCT). The control procedure based on the composite observer is explained in [13]. In [14], the Euclidean Direction Search technique (EDST) is used for the control of VSC along with a zig-zag transformer for the compensation of neutral current. As an advancement of ANN, the Chebyshev functional expansion based artificial neural network (ChANN) algorithm has been proposed in [15].

For effective control of DSTATCOM, controllers other than conventional PI controllers are preferred. Controllers based on Artificial Intelligence (AI) such as Fuzzy Logic Controller (FLC) and Artificial Neural Network (ANN) based controller are presented in [16], [17] and the THD values are compared with the PI controller [18]. When compared to the AI controllers mentioned above, the proposed Interval IT2FLC can handle the uncertainty better than Type-1 Fuzzy Logic Controllers (T1FLC) [19], [20]. The IT2FLC has the membership functions as an interval with Upper (U) and Lower (L) functions. So, it is an interval bounding the uncertain data. This helps in obtaining precise output than other AI techniques [21]–[23]. Thus, IT2FLC provides precise control over the system and hence minimum THD can be achieved [24], [25]. The primary contributions of our work are three-fold:

- Design of IT2FLC with RLS filter based DSTATCOM to enhance power quality in Local Distribution Grid (LDG)
- A comprehensive simulation study on the power quality of the LDG with and without the proposed DSTATCOM configuration

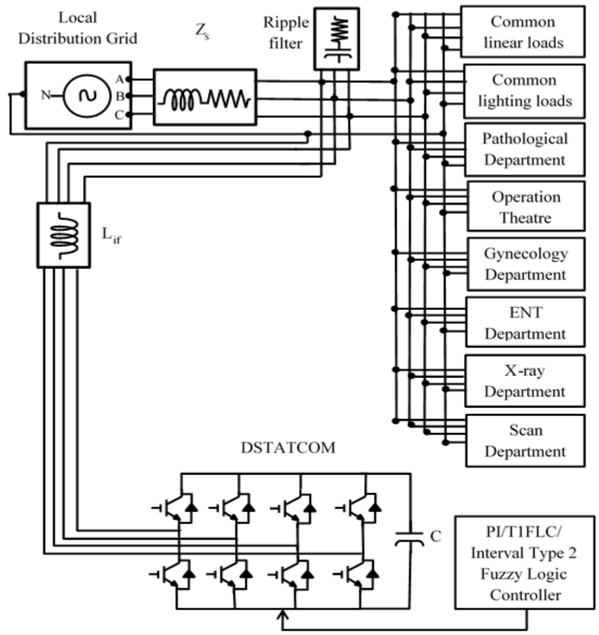

FIGURE 1. Proposed DSTATCOM configuration with interval Type-2 fuzzy logic controller.

- The harmonic spectrum is depicted in detail and the proposed RLS filter based IT2FLC controlled DSTATCOM is compared with the conventional PI, T1FLC controlled DSTATCOM

The article organization is as follows. Section II deals with the system configuration model for the study. Next, a detailed analysis of loads that are connected to the system is provided. This is followed by the design procedure for DSTATCOM that is to be utilized as a mitigating device. Section IV describes in detail the control algorithm formulation for the DSTATCOM operation. Section V gives a detailed analysis of the results obtained during the simulation. In addition, the proposed method is discussed and compared with other similar methods. Finally, the work is concluded in Section VI.

II. SYSTEM CONFIGURATION

A three-phase four-wire local distribution grid (LDG) is modeled with sensitive hospital loads, as shown in Fig. 1. The core concentration of the work falls on analyzing the loads at the medical facility along with the RLS filter and IT2FLC based DC voltage controller. The real-time data of a hospital is used for load modeling. The proposed load model consists of a combination of heavy, linear, non-linear, and unbalanced loads at varying times. The LDG of capacity 11 kV is supplied to the hospital loads of 415 V via a step-down transformer. A DSTATCOM is connected in shunt with the LDG and helps mitigate the current harmonics, neutral current, reactive power compensation, and load balancing.

IT2FLC is used as the reference current generator for DSTATCOM and the generated current eliminates the reactive component of the load. Thus, the source current component is reduced only to real terms leaving behind the reactive terms. As an effect of this, the reactive power burden of the generator is released by the DSTATCOM.

III. SYSTEM MODELING

The load modeling plays a crucial role in this proposed work. The hospital consists of linear, non-linear, balanced and unbalanced loads. There are numerous DC loads connected to the AC supply via a rectifier. The hospital loads are much sensitive to power quality issues. Various classes of medical loads [26] are considered for the proposed system. There are various departments like ICU, pathological department, operation theatre, ENT department, gynecological department, X-ray department, scan centers, and so on. The total load in the system depends on various factors like peak loads, critical loads, continuous operation, and seasonal loads.

A. DC BUS VOLTAGE

Usually, the DC voltage $\boldsymbol{V_{dc}}$ value should be higher than the AC voltage amplitude. Hence, $\boldsymbol{V_{dc}}$ is determined from the voltage of PCC at LDG. The $\boldsymbol{V_{dc}}$ is calculated from (1)[2]

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}mi} \tag{1}$$

where, m is the modulation index and it is chosen as one, V_{LL} is the line-to-line ac voltage of the DSTATCOM. The obtained value of V_{dc} is 677 V with V_{LL} as 415 V. So, the DC voltage reference $V_{dc}{}^{*}$ is selected as 700 V.

B. DC BUS CAPACITOR

The DC bus capacitor plays an important role and it is designed on the basis of variation in the DC voltage. The DC bus capacitor ($\boldsymbol{C_{dc}}$) is designed from (2) [2]

$$\frac{1}{2}\boldsymbol{C_{dc}}\left[\left(\boldsymbol{V_{dc}^{*}}\right)^{2}-\left(\boldsymbol{V_{dc}}\right)^{2}\right]=\boldsymbol{k3V_{ph}\left(aI\right)t} \tag{2}$$

where, V_{ph} is the phase voltage and $V_{ph} = 240$ V, I is the phase current, t is the recovery time of the DC bus voltage & $t = 0.04$s, a is overload factor & $a = 1.2$ and $k = 0.1$. The value of C_{dc} is calculated and is approximated to 10000 μF.

C. AC INDUCTOR

The AC inductor is designed based on the ripple current and the switching frequency. The AC inductor is designed from (3) [2]

$$L_{if} = \left(\sqrt{3}*m*V_{dc}\right)/\left(12*a*f_{sw}*i_{cr}\right) \tag{3}$$

where, f_{sw} is switching frequency and it is chosen as 10 kHz. The value of the AC inductor is calculated as 2.25 mH.

D. RIPPLE FILTER

The ripple filter is designed with a capacitor in series with a resistor. A high pass filter of the first order is modeled and is used to filter high-frequency signals of the PCC voltage.

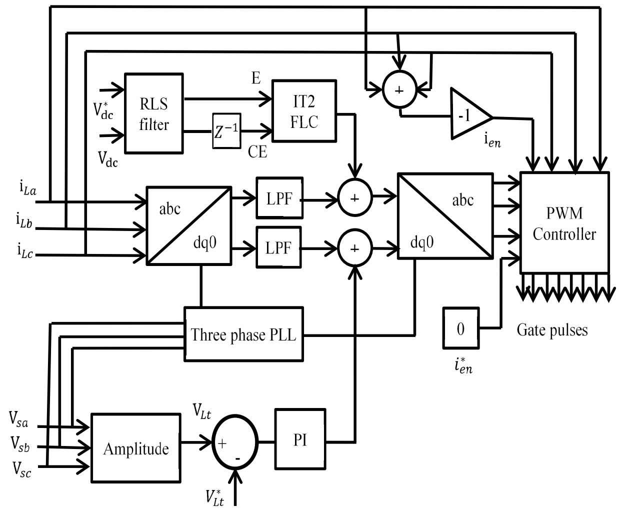

FIGURE 2. Control algorithm for the IT2FLC based DSTATCOM with RLS filter.

The values of the capacitor and resistor are calculated from equations (4) to (5) [2].

$$\mathrm{R_{rf}} * \mathrm{C_{rf}} \leq \mathrm{T_s} \tag{4}$$

If the switching time is low,

$$\mathrm{R_{rf}} * \mathrm{C_{rf}} \leq \frac{1}{4\mathrm{f_s}} \tag{5}$$

The resistance value is selected as 5Ω and the capacitance for the filter is obtained by equation (6) [2],

$$5 * \mathrm{C_{rf}} \leq 1/4 * 10000 \tag{6}$$

IV. CONTROL ALGORITHM

In this work, IT2FLC based SRF is formulated to generate a reference current signal for the proposed DSTATCOM and the corresponding structure is shown in Fig. 2. The SRF theory operation commences with the transformation of the voltages and currents into the $\alpha - \beta - 0$ axis. The $d - q$ axis represents the d-direct axis and the q-quadrature axis.

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{8}$$

The angle θ is obtained from the Phase Locked Loop (PLL) in reference to the $\alpha - \beta$ axis. Using this, a reference $\mathrm{d} - \mathrm{q}$ frame is established. The conversion of $\alpha - \beta - 0$ to $\mathrm{d} - \mathrm{q} - 0$ frame is given as,

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{pmatrix}\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{9}$$

The $d-q$ component of current is the sum of their respective DC and AC components and given as,

$$i_d = i_{dDC} + i_{dAC} \tag{10}$$
$$i_q = i_{qDC} + i_{qAC} \tag{11}$$

The generation of reference source current is given by (12)

$$i_d^* = i_{dDC} + i_{d2} \tag{12}$$

where, i_{d2} is the output of IT2FLC of the DC voltage controller.

There should be no zero-sequence component at the PCC and the reference source current should be in-phase with the voltage. By reverse transformation, the $d-q-0$ frame is transformed again to $\alpha-\beta-0$ axis.

$$\begin{bmatrix} i_{s0}^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} 0 \\ i_d^* \\ 0 \end{bmatrix} \tag{13}$$

The reverse transformation is applied to the source current and converted from $\alpha-\beta-0$ frame to $a-b-c$ frame.

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 0 & 1 & 0 \\ 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i_{s0}^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} \tag{14}$$

The IT2FLC is used as the DC voltage controller, and its performance is compared with the T1FLC and PI controllers. Using the PI controller, the AC terminal voltage (V_{Lt}) at the PCC is controlled with respect to the reference terminal voltage (V_{Lt}^*). The reactive component of current is the output of the PI controller. This helps in regulating the AC voltage of the PCC at LDG. The AC terminal voltage (V_{Lt}) at the PCC is calculated from the AC source voltages of the three phases (V_{sa}, V_{sb}, V_{sc}) as,

$$V_{Lt} = \sqrt{\frac{2}{3}}\sqrt{(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)} \tag{15}$$
$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}\left(V_{te(n)} - V_{te(n-1)}\right) + K_{iq}V_{te(n)} \tag{16}$$

where, the terminal voltage error is$V_{te(n)} = V_{Lt}^* - V_{Lt(n)}$, n is the number of samples, K_{pq}, K_{iq} are the PI controller gains.

The reference current in the quadrature axis is calculated as,

$$i_q^* = i_{qDC} + i_{qr} \tag{17}$$

This is again transformed to $\alpha-\beta-0$ axis as follows,

$$\begin{bmatrix} i_{s0}^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} 0 \\ i_d^* \\ i_q^* \end{bmatrix} \tag{18}$$

The reverse transformation is applied to the source current and converted from $\alpha-\beta-0$ frame to $a-b-c$ frame.

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 0 & 1 & 0 \\ 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i_{s0}^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} \tag{19}$$

The reference value of the reference current is zero. This helps in neutralizing the load-neutral current. The comparison is made between the extracted current and the reference currents. The amplification of the error is performed by the PI controller. This is compared with the carrier signal, which is triangular. This helps in generating the gate pulses for the 6 switches in VSC. The gate pulses for the 4$^{\text{th}}$ leg of DSTATCOM are generated on the basis of the comparison made between the extracted neutral current (i_{en}) and the reference neutral current (i_{en}^*). These are attained from equations (20) and (21).

$$i_{en}^* = 0 \tag{20}$$
$$i_{en} = -(i_{ea} + i_{eb} + i_{ec}) \tag{21}$$

A. RLS FILTER

The RLS filter helps in computing the output in its filtered form, error, and the weights for the provided actual signal and the reference signal [23]. The estimation of the least square of the coefficients of the filter is performed with the identified initial conditions. The filter keeps on being updated by the new data from the old estimated data. The main objective function $F(n)$ of this filter is to minimize the error [24].

$$F(n) = \sum_{k=1}^{n} \eta_n(n)e^2(n) \tag{22}$$

where, $\eta_n(n)$ is the weighting factor, $e(n)$ is the error and n represents the iteration number.

The error is calculated from the equation (23),

$$e(n) = V_{dc}^*(n) - V_{dc}(n) = V_{dc}^*(n) - w^T(n-1)x(n) \tag{23}$$

where, V_{dc}^* is the reference DC voltage, V_{dc} is the DC estimated voltage i.e. the actual DC voltage

$$x(n) = [x(n)\ \ x(n-1)\ \ \cdots\cdots\ \ x(n-M+1)]^T \tag{24}$$
$$w(n) = [w_1(n)\ \ w_2(n)\ \ \cdots\cdots\ \ w_M(n)]^T \tag{25}$$

where, M is the vector length.

The equations below show the weight of the RLS filter after the update.

$$k(n) = \frac{P(n-1)x(n)}{\lambda + x^T(n)P(n-1)x(n)} \tag{26}$$
$$w(n) = w(n-1) + k(n)e(n) \tag{27}$$
$$P(n) = \frac{1}{\lambda}\left[P(n-1) - k(n)x^T(n)P(n-1)\right] \tag{28}$$

where, $k(n)$ is the kalman gain vector, $P(n)$ represents the input correlation matrix inverse, λ indicates the forgetting factor. The forgetting factor value stays at 0 to 1. The filter attains fast convergence when the value of λ is nearer to 1. The λ value can be calculated from,

$$1 - \frac{1}{2L} < \lambda < 1 \tag{29}$$

where, L is the length of the filter.

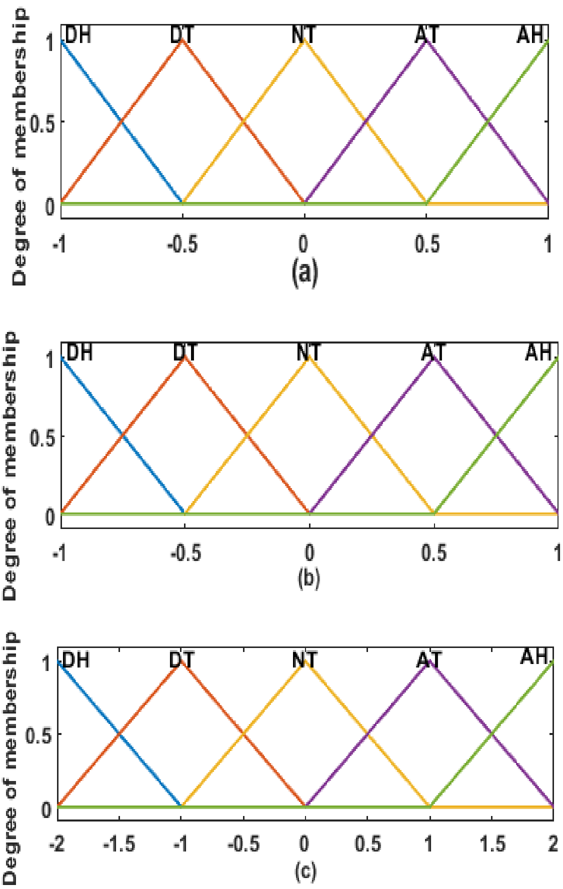

FIGURE 3. Membership functions of T1FLC as DC voltage regulator (a) Error (b) Change in error (c) output.

B. TYPE 1 FUZZY LOGIC CONTROLLER

The FLC gives better performance, less complicated and precise control when compared to conventional techniques. The input variables are error (E) and Change in Error (CE) and the output. The CE is calculated by the equations (30) and (31).

$$E\,(k) = V_{dc}^{*} - V_{dc(k)} \tag{30}$$

$$CE\,(k) = E\,(k) - E\,(k-1) \tag{31}$$

where k is the time sample. The E, CE, and the output are divided into five fuzzy sets and the Membership Functions (MFs) are shown in Fig. 3. The triangular MFs are chosen for the T1FLC DC voltage controller in this paper. When comparing to other types of MFs, triangular MFs have earlier settling time, less overshoot, less complex as well as precise output. The MFs are DH (Depreciate Huge), DT (Depreciate Tiny), NT (Neutral), AT (Appreciate Tiny), and AH (Appreciate Huge). The centroid method is used in the defuzzifier module to estimate the output of this T1FLC. The output is given to the current regulator for the extraction of reference current signals. The output is i_{d2} which uses the rule base provided in Table 1.

TABLE 1. Rule base for T1FLC.

E / CE	DH	DT	NT	AT	AH
DH	NT	NT	AH	AH	AH
DT	NT	NT	AT	AT	AT
NT	AT	NT	NT	NT	DT
PS	DT	DT	DT	NT	NT
AH	DH	DH	DH	NT	NT

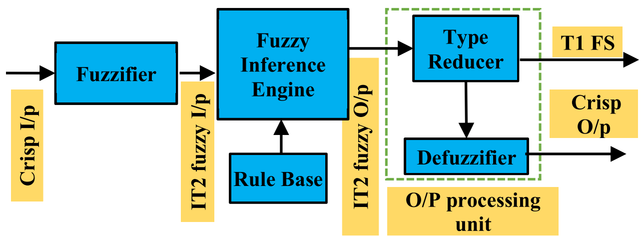

FIGURE 4. Interval Type 2 fuzzy logic controller working scheme.

C. INTERVAL TYPE 2 FUZZY LOGIC CONTROLLER

The Interval Type 2 FLC (IT2FLC) works more effectively in handling the imprecise data when compared to T1FLC. In T1FLC, the membership values are single, while the membership functions of IT2FLC are intervals instead of single values. The MFs of IT2FLC have Lower (L) and Upper (U) regions. The IT2FLC has an additional step of Type Reduction (TR). This TR helps in reducing the IT2 fuzzy sets into IT1 fuzzy sets. Also, the footprint of uncertainty present in the IT2FLC provides better performance than conventional PI and type1 fuzzy logic controller in a complex system. So, IT2FLC is employed in the proposed system to improve performance. In addition, IT2FLC provides more precision, less complex and fast convergence [15]. The basic working scheme of Interval Type 2 Fuzzy Logic Controller is given in Fig. 4. It comprises of fuzzifier, rule base, fuzzy inference system, type reduction and defuzzifier blocks. The crisp value is converted to type 2 fuzzy sets through the fuzzifier block. The rules are stored in the rule base. A type2 fuzzy set output is generated through a fuzzy inference system based on the input fuzzy sets and the stored rules. The type reduction block is used to convert the type2 fuzzy set to the type1 fuzzy set before converting to the crisp value. Finally, the crisp output is obtained from the defuzzifier block. The E and CE are divided into three fuzzy sets each. The MFs of E and CE and the surface view are shown in Fig. 5. The surface view gives the relationship of two inputs and one output in the 3D view.

There are numerous approaches in TR. Most extensively, the Karnik Mendel (KM) TR method is used. But, in this work, the Nie-Tan TR method is selected. The Nie Tan method provides more precise output, less complex and swift convergence when compared to KM and other TR methods.

The error (E) MFs are chosen as trapezoidal MFs and the change in error (CE) MFs are the combination of trapezoidal

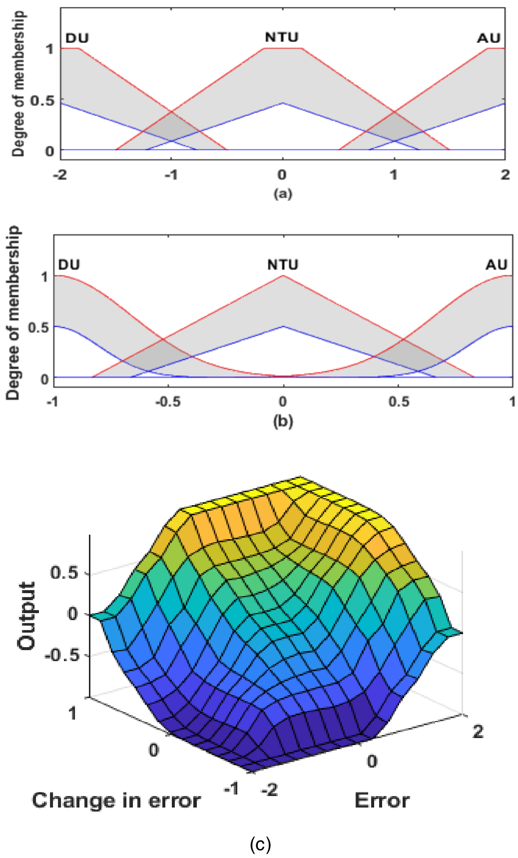

FIGURE 5. Membership functions of IT2FLC (a) Error (b) Change in error (c) Surface view.

TABLE 2. Rule base for IT2FLC.

E / CE	D	NT	A
D	D	D	NT
NT	D	NT	A
A	NT	A	A

as upper MF and Gaussian as lower MF for providing accurate results. The MFs are D (Depreciate), NT (Neutral) and A (Appreciate). The Nie-tan method is used as the TR method. The output is based on the rule base provided in Table 2.

When comparing with T1FLC, the number of rules in IT2FLC gets decreased. So, the speed of the Vdc controller increases when compared to T1FLC, and also computation time is reduced. The IT2FLC provides better interval and mapping of values which helps in executing the rules accordingly. So, it is evident that IT2FLC is faster and precise than T1FLC.

V. SIMULATED RESULTS AND ANALYSIS

This paper analyzes and quantifies the effect of power quality issues arising due to sensitive loads at the hospitals and a novel method to improve power quality, thus making the distribution grid reliable. PQ improvement is achieved by

TABLE 3. System parameters.

Parameters	Value
Supply Voltage (V)	415 V
Supply Frequency (f)	50 Hz
Interfacing inductor (L_f)	5 mH
DC Link capacitor (C_{dc})	3300 μF
Ripple Filter (R_f, C_f)	5Ω, 30μF
Load Power (W)	1414 W
Switching Frequency	10 kHz
K_p	1
K_i	1

TABLE 4. Comparison of source current THD.

LITERATURE	CONTROLLER	SOURCE CURRENT THD (%)
[10]	RGA OPTIMIZED PI	4.44
PROPOSED	PI	4.77
	T1 FLC	4.56
	T2FLC	4.43

incorporating IT2FLC based DSTATCOM combined with an RLS filter which provides better THD. The simulation parameters are listed in Table. 3

Initially, the system is operated without DSTATCOM and parameters such as source voltage, source current, load voltage and load current waveforms are obtained and shown in Fig. 6. As a next step, the system is simulated with DSTATCOM connected across the load, in addition to the source and load waveforms, DSTATCOM voltage and currents are also obtained. In order to quantify the measure of power quality, harmonic spectrum for both cases are obtained at times of peak load operation, and the results are tabulated in Table 4. Detailed discussion for both the cases is handled in sub-sections A and B.

A. PERFORMANCE ANALYSIS OF LDG WITHOUT DSTATCOM

Generally, hospitals consist of diverse and sensitive loads connected both in single and three-phase connections along with a neutral conductor. The loads are modelled with the help of the datasheet of the respective load equipment. The 108-kW linear and lighting load consisting of numerous LED lamps of different power ratings 12 W, 16 W, 32 W, 36 W, 40 W are treated as a continuous operating load. This includes the loads at emergency units such as ICU, CCU. These loads are not only sensitive but also critical. In this system, the PD and the OT loads are connected from 0.2 s to 0.4 s since its operating time is mostly from 6.00 A.M to 11.00 A.M. The GD and ENTD loads are connected from 0.4 s to 0.5 s since its operating time is mostly from 9.00 A.M to 1.00 P.M. The XD and SD loads are connected from 0.4 s to 0.6 s, indicating that it works from 9.00 A.M to 4.00 P.M. The XD and SD loads are heavy loads and treated as single- phase, non-linear loads. There is a peak load of 178 W from 0.4 s to 0.5 s. Fig.6 shows the performance of the hospital loads connected with the LDG without DSTATCOM. In Fig.6, V_s signifies the source

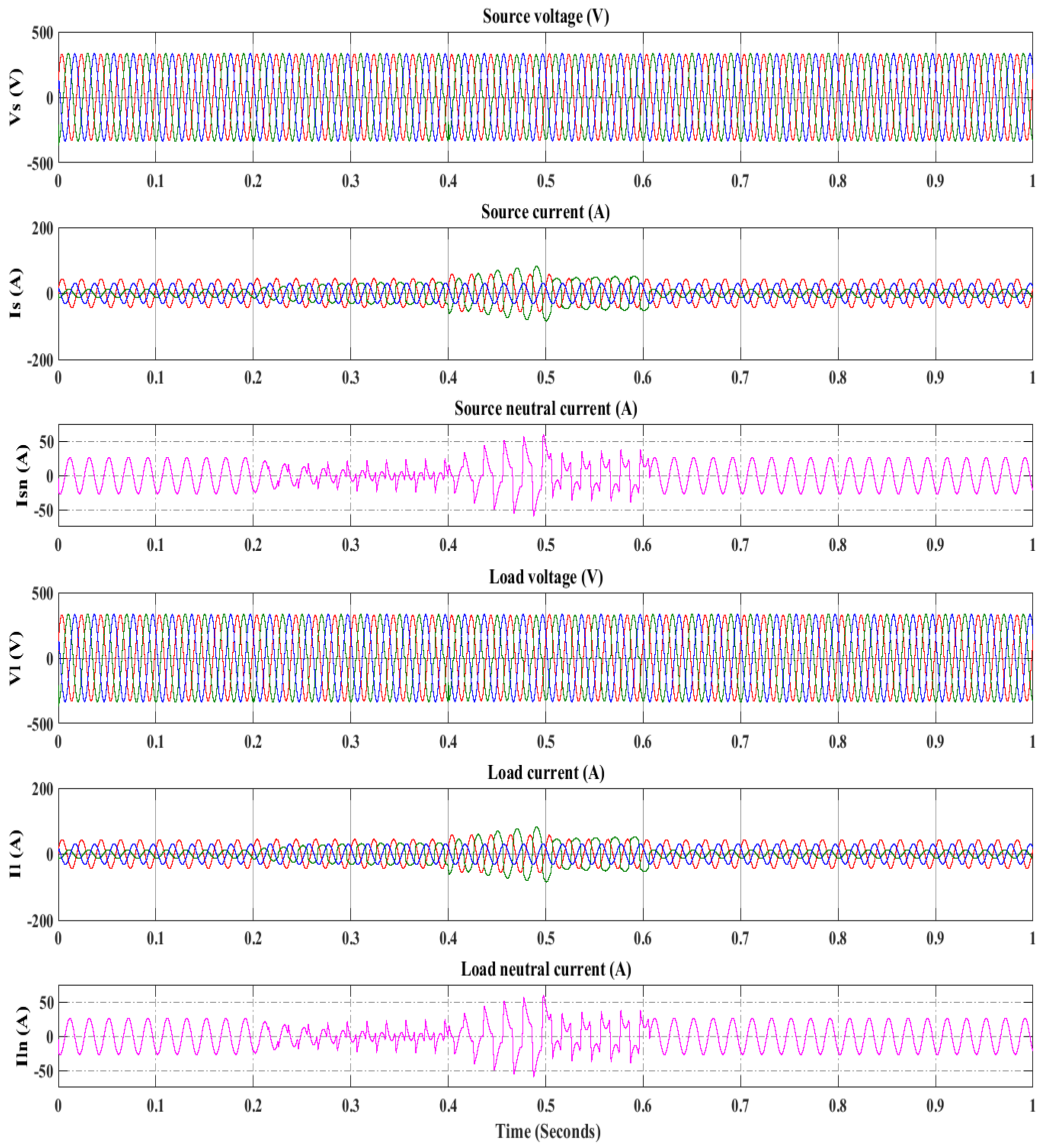

FIGURE 6. Source and Load current waveforms of the hospital loads connected to LDG without DSTATCOM.

voltage, I_s denotes the source current, I_{sn} indicates the neutral current on the source side, V_l is the load voltage, I_l is the load current and I_{ln} indicates the neutral current on the load side. From 0.4 s to 0.6 s, the heavy, unbalanced and non-linear loads are operated. This leads to severe current harmonics and hence distortion in the source current waveform. Although the entire system contains both linear, non-linear, balanced and unbalanced loads, the severity of the disturbance due to loads occurs from 0.4 s to 0.5 s. From 0.5 s to 0.6 s, the disturbance due to non-linear loads reduces slightly and at the same time, power consumption slightly decreases as the GD and ENTD loads are disconnected from 0.5 s. At 0.6 s, all the heavy unbalanced load from PD, OT, GD, ENTD, XD and SD are shut down, indicating the night time. The remaining linear continuously operated loads are still connected to the system.

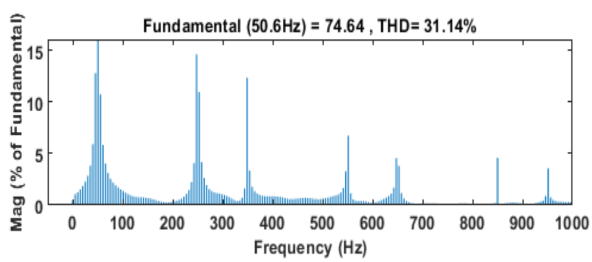

FIGURE 7. Phase B harmonic spectrum.

From Fig. 6 it can be observed that the XD and SD loads draw heavy current and create an unbalance as well as injects harmonic into the system. Due to the operation of non-linear loads, the source current is unbalanced and hence distortions occur, which results in higher THD. Also, loads at the X-ray

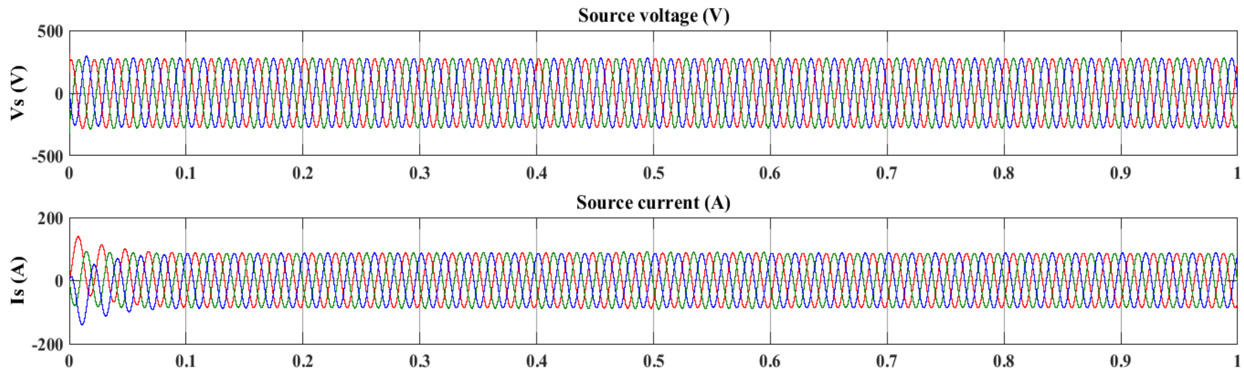

FIGURE 8. Source current waveforms of the hospital loads connected to LDG with DSTATCOM.

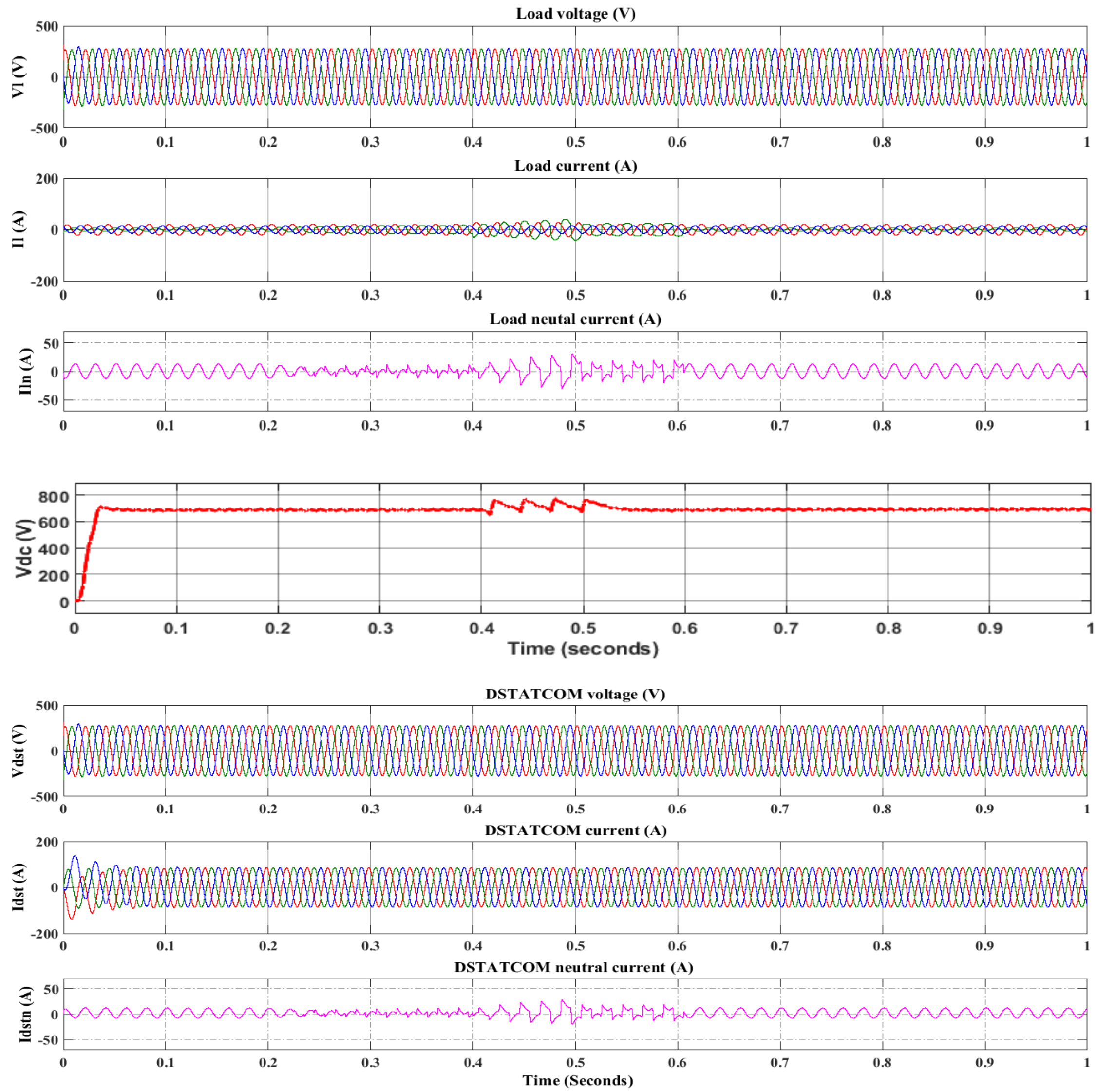

FIGURE 9. Load current waveforms of the hospital loads connected to LDG with DSTATCOM.

and scan departments are high in capacity, which consumes power in several kW. This facilitates the enormous flow of neutral current in the system. The neutral current flow starts to increase from 0.2 s and at 0.4 s, nearly 50 A of current flows in it. This indicates that the entire hospital load is connected to the system and thus, peak power consumption occurs.

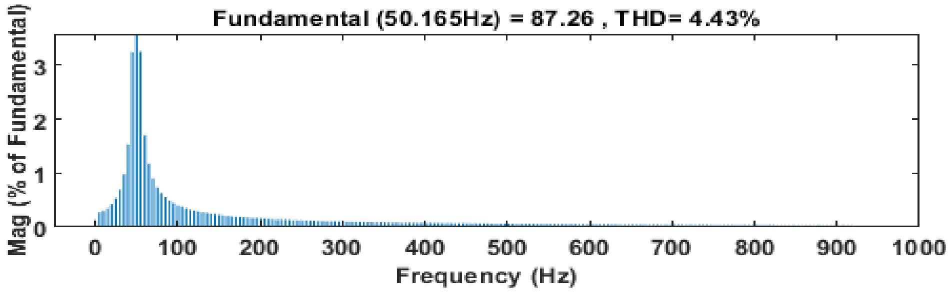

FIGURE 10. Source current harmonic spectrum with DSTATCOM.

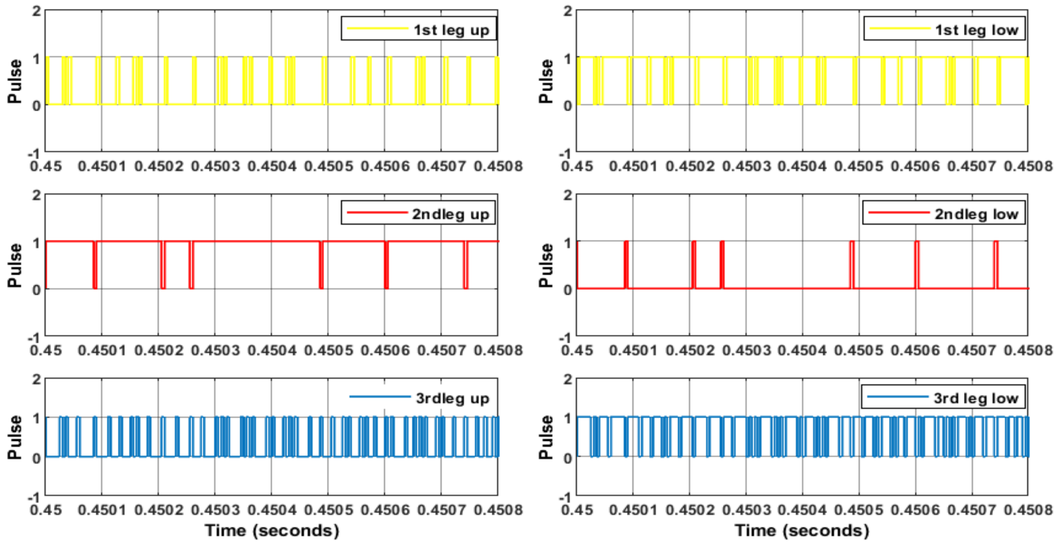

FIGURE 11. Switching pulses generated for DSTATCOM switches.

As per the IEEE- 519 standard, the THD should be less than 5%. The majority of the heavy non-linear loads are connected in phase B. Particularly, from 0.4 to 0.5 s,in which the entire load of the hospital is connected to the system, it is identified that the THD of the source current for phase A at 0.2 s is 8.94%, at 0.4 s is 13.77%, at 0.5 s is 14.46% and at 0.6 s is 9.36%. The THD of the source current of phase B at 0.2 s is 28.65%, at 0.4 s is 31.14%, at 0.5 s is 29.50% and at 0.6 s is 29.34%. As per the data, the bulk loads are connected in phase B followed by phase A. So, the current drawn is also larger in phase B from 0.4 s to 0.5 s which is followed by phase A. The perceived THD of the source current in phase C at 0.2 s is 19.13%, at 0.4 s is 13.59%, at 0.5 s is 16.85% and at 0.6 s is 7.07%. Because of the large non-linear loads, the THD is greater in phase B when compared to phase A and phase C. Critical loads of OT and PD are connected in phase A and phase C from 0.2 s to 0.4 s. So, the current drawn by these two phases are greater than phase B. The sample harmonic spectrum of Phase B for 5 cycles at 0.4 s is shown in Fig. 7.

B. PERFORMANCE ANALYSIS OF THE SYSTEM WITH DSTATCOM

There are various light and heavy loads connected individually as single-phase loads and three-phase loads. This causes severe load imbalance, harmonics due to non-linear loads and a huge amount of current in the neutral conductor. These power quality issues are mitigated using DSTATCOM. PI controller, T1FLC and IT2FLC are the controllers used in the control of DC voltage in the DSTATCOM. Fig. 8 and Fig. 9 shows the performance of the hospital loads connected with the LDG system with DSTATCOM and IT2FLC. V_{dst} indicates the DSTATCOM voltage, I_{dst} signifies the DSTATCOM current, I_{dstn} denotes the compensating neutral current from DSTATCOM. The DSTATCOM compensates the power quality issues by injecting the essential current (I_{dst}). This compensating neutral current makes the source current (Is) to be sinusoidal and balanced. V_{dc} indicates the DC voltage with IT2FLC based DSTATCOM. The IT2FLC provides precise control when compared with T1FLC and PI controllers. The IT2FLC aids in maintaining the V_{dc} almost near the reference DC voltage 700 V during varying load conditions. The RLS filter provides filtered error output and it recursively performs and squares the error to provide the best possible output. The forgetting factor helps in attaining swift convergence. Moreover, it works at high speed and performs perfectly even when the difference between the reference DC voltage and the actual DC voltage is diminutive. This feature of the RLS filter enhances the DSTATCOM performance. The RLS filter

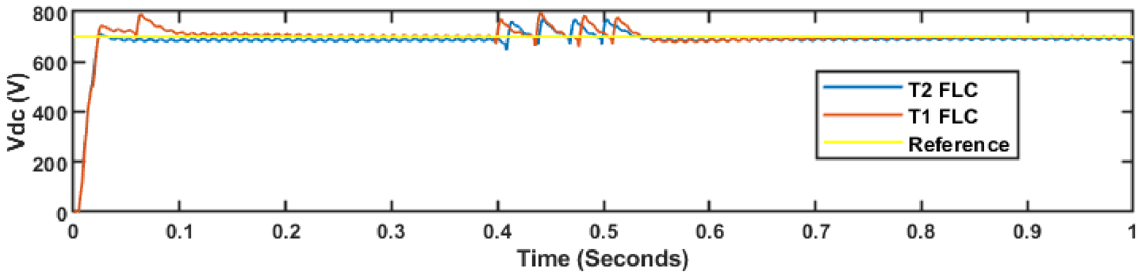

FIGURE 12. **Dynamic response of controllers based on DC link voltage.**

TABLE 5. **Comparison of performance characteristics.**

Parameter	Controller	
	T1 FLC	T2 FLC
Rise Time (ms)	14.7	14.2
Settling Time(ms)	648.1	525.6
Peak time (ms)	440.9	443.1
Overshoot (%)	13.79	11.20
Peak (V)	795.48	771.52

operates with better precision than the conventional LPF. The precise error output from the RLS filter is taken as one of the inputs to IT2FLC. The change in error is the other input for IT2FLC. Since the error output of the RLS filter is accurate, the CE is also precise. The usual performance of IT2FLC is better than the PI and T1FLC. With the aid of RLS filter, the performance of IT2FLC in controlling the DC voltage is precise and perfect. This can be realized with the V_{dc} waveform shown in Fig. 9. This V_{dc} output after compensation is more precise than the PI and T1FLC controllers. The harmonic spectrum of the Phase B source current for 5 cycles from 0.4 s with IT2FLC based DSTATCOM is shown in Fig. 10. From the harmonic spectrum, the source current THD for phase A at 0.2 s is 4.16%, at 0.4 s is 4.33%, at 0.5 s is 4.19% and at 0.6 s is 3.57%. The THD of the source current of phase B at 0.2 s is 4.35%, at 0.4 s is 4.43%, at 0.5 s is 4.25% and at 0.6 s is 3.98%. As per the data, the bulk loads are connected in phase B followed by phase A. The perceived THD of the source current in phase C at 0.2 s is 4.14%, at 0.4 s is 4.36%, at 0.5 s is 4.17% and at 0.6 s is 3.76%. The DSTATCOM effectively reduces the harmonics by injecting the required compensating current at varying load conditions. The higher THD of various phases under varying load conditions without compensation is drastically reduced to below 5% with the installation of IT2FLC based DSTATCOM comprising of RLS filter. Table 4 summarizes the source current THD values in percentage with and without DSTATCOM installation for time-varying load conditions.

From Table 4, it is evident that the IT2FLC based DSTATCOM with RLS filter shows better performance in terms of both harmonics and neutral current compensation than the PI and T1FLC based controllers. This control strategy of DSTATCOM exhibits improved performance at all types of loading conditions over a diverse time period. The neutral current mitigation is also carried out effectively with the help of this novel approach. The switching pulses generated by the proposed IT2FLC based DSTATCOM is given in Fig. 11.

The dynamic response of the controllers based on the DC link voltage is shown in Fig. 12 and the corresponding performance characteristics are listed in Table 5.

VI. CONCLUSION

The performance of IT2FLC based DSTATCOM has been validated in this work and satisfactory results corroborate its effectiveness when sensitive loads are connected to the grid. With proficient behavior of control along with its fast response, it has been proved effective in mitigating harmonics. The simulated results and tabulation highlight the efficacy of the proposed controller over conventional ones. This paper paid close attention to the effective operation of the local distribution grid with sensitive loads which are the source of disturbances from the generation viewpoint. Integration of IT2FLC based DSTATCOM in the system significantly reduces the total harmonic distortion in the system and the RLS filter helps in fine-tuning it to the acute levels. Also, substantial improvement in the total harmonic distortion is aided by reducing the harmonic value of currents at the source side and provides a much better profile of voltage and current waveforms. Neutral current flow due to unbalanced loads is mitigated with the help of the fourth leg of VSC. Summarized results show that THD levels are less when compared with PI controller and T1FLC at various time instant.

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