IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 12, 2021, accepted April 8, 2021, date of publication April 12, 2021, date of current version April 23, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3072688

Threshold-Variation-Tolerant Coupling-Gate α-IGZO Synaptic Transistor for More Reliably Controllable Hardware Neuromorphic System

DONGYEON KANG[1], JUN TAE JANG[1], SHINYOUNG PARK[1], MD. HASAN RAZA ANSARI[2], (Member, IEEE), JONG-HO BAE[1], (Member, IEEE), SUNG-JIN CHOI[1], DONG MYONG KIM[1], (Member, IEEE), CHANGWOOK KIM[2], SEONGJAE CHO[3], (Senior Member, IEEE), AND DAE HWAN KIM[1,3], (Senior Member, IEEE)

[1]School of Electrical Engineering, Kookmin University, Seoul 02707, Republic of Korea
[2]Circadian ICT Research Center, Kookmin University, Seoul 02707, Republic of Korea
[3]Department of Electronic Engineering, Gachon University, Seongnam-si 13120, Republic of Korea

Corresponding authors: Seongjae Cho (felixcho@gachon.ac.kr) and Dae Hwan Kim (drlife@kookmin.ac.kr)

This work was supported in part by the Ministry of Science and Information & Communications Technology (ICT) of Korea (MSIT) under Grant 2016R1A5A1012966, Grant 2016M3A7B4909668, and Grant 2020R1A2B5B01001979; and in part by the Ministry of Trade, Industry, and Energy of Korea (MOTIE) under Grant 10080513.

ABSTRACT Hardware-oriented neuromorphic computing is gaining great deal of interest for highly parallel data processing and superb energy efficiency, as the candidate for replacement of conventional von Neumann computing. In this work, a novel synaptic transistor constructing the neuromorphic system is proposed, fabricated, and characterized. Amorphous indium-gallium-zinc-oxide (α-IGZO) and Al_2O_3 are introduced as the channel and gate dielectric materials, respectively. Along with the high functionality and low-temperature processing viability, geometric peculiarity featuring extended gate structure improves the performances of the proposed transistor as synaptic component in the neuromorphic system. The insight into the substantial effect of optimal device structure design on energy efficiency is highlighted.

INDEX TERMS Hardware-oriented neuromorphic computing, parallel data processing, energy efficiency, synaptic transistor, amorphous indium-gallium-zinc-oxide, extended gate, device structure design.

I. INTRODUCTION

The amount of data in need for realizing the artificial intelligence (AI), internet of things (IoT), and real-time data services has been tremendously expanded and the demand on big-data processing capacity has been drastically increased in accordance. This necessity of vast data processing calls for innovation in the processing system toward highly parallel and ultra-low-energy computing capabilities [1]. The conventional computer architecture that has been lasting more than a half of century, von Neumann architecture, is capable of high-speed and high-precision arithmetic operations through logic processing. However, power consumption per chip getting higher, joule heating becoming more serious with chip complexity, and system speed bottleneck due to serial data processing have much room to resolve [2]–[5]. In order to overcome these limits and increase the parallel computing capability more importantly valued in the massive data processing, new computing architecture has been sought and neuromorphic system is on the leading edge in recent days [6]–[9]. The neuromorphic system realizes various neural networks defined by mathematical and software approaches through hardware. The application of the neuromorphic system is more specified for learning, inference, and recognition through hardware-sense realization of human nervous system represented by synapse and neuron. By switching the approach to hardware-initiated method, ultra-low energy consumption can be pursued, by which the genuine feature of how human brain energy-efficiently works is more fundamentally mimicked. By the help of brain-inspired interconnections among the synaptic components and the neurons, highly fast parallel operations are made possible with the superiority to the conventional von Neumann architecture which is mainly specified for series computing [10]–[12]. The electrical analogy of weight change in biological synapse, change in the number of

The associate editor coordinating the review of this manuscript and approving it for publication was Jiang Wu.

neurotransmitters between pre- and post-synaptic neurons communicating with spikes, is realized by modulation of electrical conductance in the synaptic device. The spiking neural network (SNN) can be implemented for either off-chip learning or on-chip learning. In the former learning method, the synaptic devices only receive the weights pre-determined in the processing unit and perform the vector multiplication, which boosts the overall system speed for operation. On the other hand, in the latter one, the weights of the synaptic devices are determined by the neuron operations, which makes the system more autonomous with higher resemblance to the biological nervous system run by spike-timing-dependent plasticity (STDP). A relatively larger portion of the researches on synaptic device design have been dedicated to off-chip learning system working in cooperation with separately prepared processing unit, getting rid of the necessity of rather complicated design part which equips a synaptic device with the STDP responsivity.

In this work, a novel synaptic device based on field-effect transistor (FET) operated by coupling gate, coupling-gate amorphous indium-gallium-zinc-oxide (α-IGZO), or shortly, CG-IGZO synaptic transistor is designed, fabricated, and characterized. Although there have been related research results on either FET-based or GZO-based synaptic devices recently [13], [14], in this work, a novel structuring with CG is regarded as a distinctive aspect in designing a synaptic transistor. By introducing the peculiar gate structuring, the synaptic weight can be more discriminatively tuned in the highly reproducible and practical ways of both fabrication and layout design. A forward step has been made upon the FET technology and functional material by delving into a more exquisite device structure design for synaptic operations with higher reliability. It is shown that the synaptic operations gain higher reliability with the help of proposed channel material and novel device structuring. Further, the STDP learning capability is validated for the on-chip neuromorphic system.

II. DEVICE FABRICATION

Memristors have been widely studied as synaptic devices for neuromorphic application owing to its great geometric resemblance with the biological synapse which can be modeled as a two-terminal unit [15], [16]. However, it has been quite challenging to achieve the full functions of biological synapse via operations of two-terminal memristors. Addition of the third terminal would provide better proximity in describing the synapse behaviors with higher degrees of completeness and flexibility [17]. On the material side, amorphous-oxide-semiconductor (AOS) thin-film transistors (TFTs) are known to have higher field mobility, small subthreshold swing, low-temperature processing viability, and optical transparency in the visible-light range. Among the AOS materials, α-IGZO has demonstrated a relatively wide energy bandgap of 3.0 eV, high uniformity in its deposition processing, excellent on/off current ratio in the applications for FETs, and high Si processing compatibility

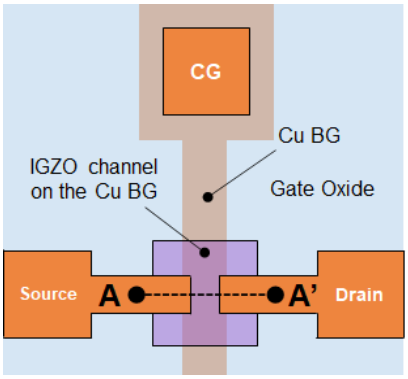


FIGURE 1. Layout schematic of the CG-IGZO synaptic transistor.

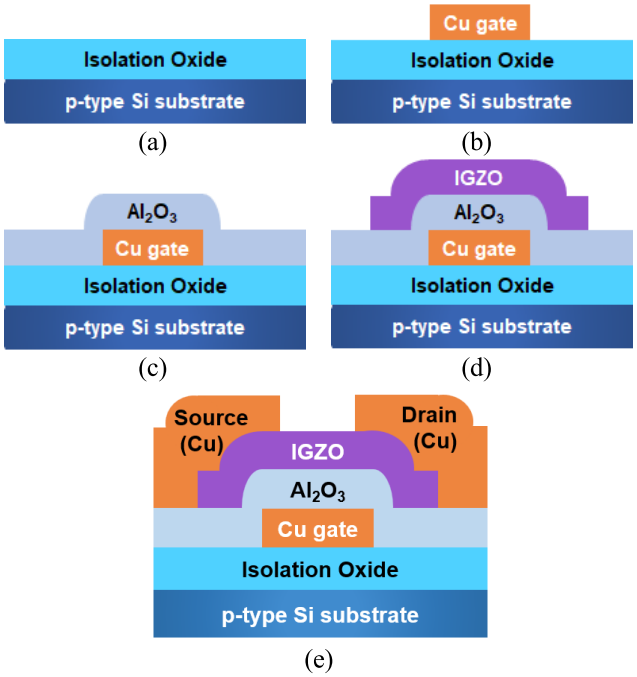


FIGURE 2. Fabrication process of the CG-IGZO synaptic transistor. (a) Wafer preparation and isolation oxide deposition. (b) Cu deposition and patterning for BG. (c) Al_2O_3 deposition by LT ALD for gate insulation. (d) IGZO deposition and patterning for constructing the channel. (e) Cu deposition and patterning for source and drain electrodes.

at the back-end-of-the-line (BEOL) [18], [19]. Moreover, high sustainability of its electrical and optical characteristics under the modular stresses has allowed the applications of α-IGZO to expand into the flexible electronics and bioelectronics [20], [21]. For these reasons, α-IGZO FET synaptic device has been designed and fabricated. Fig. 1 shows the layout schematic of the CG-IGZO synaptic transistor. The Cu CG is constructed on the bottom gate (BG) with the insertion of gate oxide between them, which will be clearly demonstrated by the process integration. Fig. 2(a) through (e) shows the process integration for fabricating the CG-IGZO synaptic transistor. Each sequence is explained by accompanying the cross-sectional views along the cutline adjoining point A and A' in Fig. 1. p-type (100) Si wafers were initially cleaned by sulfuric peroxide mixture (SPM) for preparing

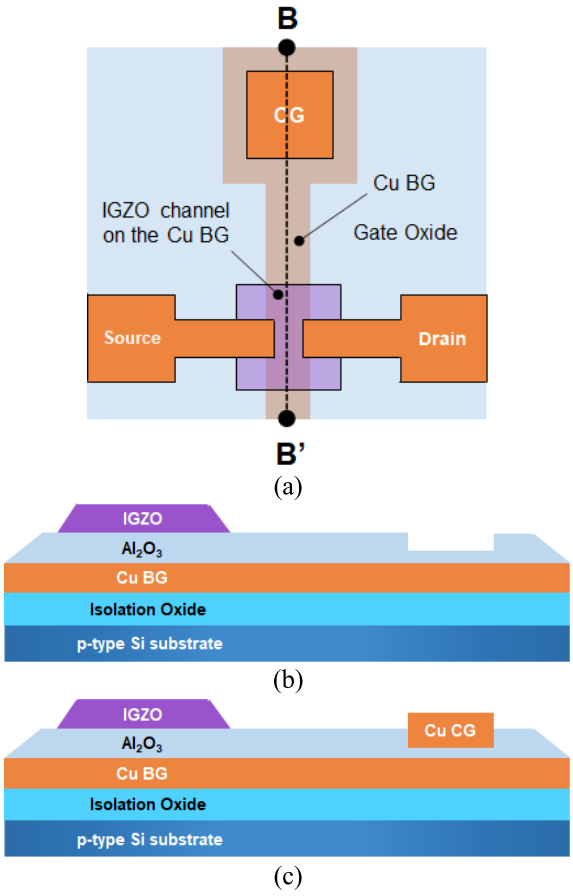


FIGURE 3. Layout schematic of the CG-IGZO synaptic transistor and the cross-sectional views along the gate line. (a) Cutline at the device center along the gate line. Cross-sectional views of the device (b) before and (c) after the Cu deposition for CG formation.

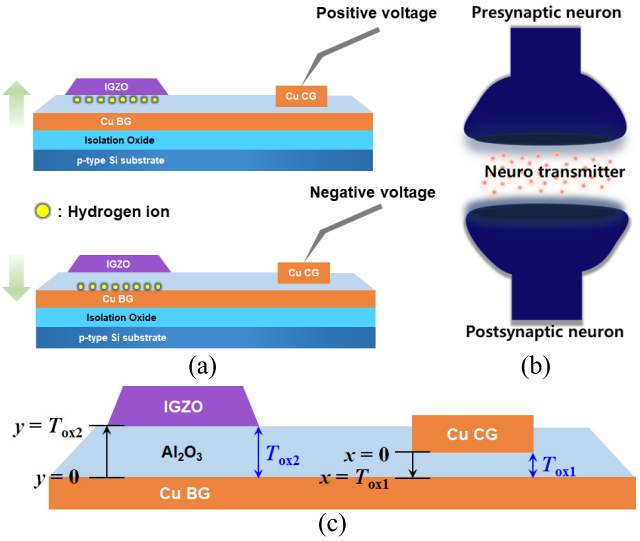


FIGURE 4. Operation physics and design variables. (a) Movements of hydrogen ions in response to CG voltage. (b) Schematic illustration of the biological synapse and neurons. (c) Oxide thicknesses in the transistor and CG regions as processing design variables.

the device fabrication. Then, SiO_2 was thermally grown with a thickness of 50 nm for electrical isolation between the substrate and the device active region as shown in Fig. 2(a). Cu was deposited by an electron-beam (e-beam) evaporator with a thickness of 20 nm for constructing the metal BG as shown in Fig. 2(b). Then, 40-nm-thick Al_2O_3 was deposited for gate insulator (GI) by a low-temperature (LT) atomic layer deposition (ALD) with $Al(CH_3)_3$ and H_2O precursors at 80 °C as shown in Fig. 2(c). Next, 35-nm-thick IGZO layer was deposited by a radio-frequency (RF) sputter at room temperature and patterned for the device channel region as shown in Fig. 2(d). The bombardment Ar/O_2 gas mixture was provided with flow rates of 3/0.1 standard cubic centimeter per minute (SCCM), the processing pressure was 5 mTorr, and the RF power was 150 W. Subsequently, Cu was deposited by an e-beam evaporator with a thickness of 30 nm and patterned to construct the source and drain metal electrodes as shown in Fig. 2(e). The critical dimensions of the source and drain junctions were determined to have overlaps with the Cu BG. Fig. 3(a) shows the layout schematic of the CG-IGZO synaptic transistor with new adjoining points B and B' for demonstrating the cross-sectional views along the gate line. After the source and drain electrodes are constructed, the gate oxide is locally etched by buffered oxide etching (BOE) in order to define the region for CG. The square CG was designed to have smaller area than the square BG area so that the electric field induced by an external voltage applied to CG is transferred to BG without loss in the capacitive manner. Fig. 3(b) schematically shows the cross-sectional view of the fabricated device, in which it is found that the BG and CG are not physically but capacitively connected through the thinner gate oxide region defined by BOE. In the end, Cu is deposited by an e-beam evaporator to construct the Cu metal electrode as schematically shown in Fig. 3(c).

III. THEORETICAL BACKGROUND

The Al_2O_3 has relatively weak AlO-H bonding matrix when the ALD process is performed at a low temperature. This bonding is weak enough to be broken by an electric field. Thus, in the proposed device, vertical gate voltage has the controllability over the hydrogen ions which are weakly bound to AlO and easy to break the bond and move as shown in Fig. 4(a) [22]. This operation provides the modulation of channel conductance which can be inferenced as synaptic weight, by which the biological analogy to the change in strength of synaptic connectivity schematically shown in Fig. 4(b) is realized in the electrical hardware sense [23]. In the existence of net positive charges in the oxide layer of a metal-oxide-semiconductor (MOS) capacitor, the flat-band voltage shift (ΔV_{FB}) is defined by Eq. (1).

$$\Delta V_{FB}(\varphi_s) = \frac{1}{\varepsilon_{ox}}\left[-\int_0^{T_{ox}} x\rho_{net}(x)dx + T_{ox}Q_{it}(\varphi_s)\right] \quad (1)$$

Here, ε_{ox} and T_{ox} are the electrical permittivity and physical thickness of gate oxide. $\rho_{net}(x)$ is the net volume charge density at location x in the unit of C/cm^3. Q_{it} is the areal interface charge density in the unit of C/cm^2. Since the total

charge density per unit area in the gate oxide (Q_{ox}) as the sum of bulk and interface charges is expressed by Eq. (2), ΔV_{FB} is simplified to Eq. (3) and (4).

$$Q_{ox}(\varphi_s) = -\frac{1}{T_{ox}}\int_0^{T_{ox}} x\rho_{net}(x)dx + Q_{it}(\varphi_s) \tag{2}$$

$$\Delta V_{FB} = -\frac{T_{ox}Q_{ox}}{\varepsilon_{ox}} \tag{3}$$

$$\Delta V_{FB}(x) = -\frac{xQ_{ox}}{\varepsilon_{ox}} \tag{4}$$

Here, $x = 0$ and $x = T_{ox}$ indicate the metal-oxide and oxide-semiconductor interfaces, respectively. Based on the MOS capacitor theory, the moving hydrogen ions as a function of gate voltage (V_{GS}) would result in continuous shift of threshold voltage (V_{th}) in the fabricated CG-IGZO synaptic transistor. Consequently, the hysteresis characteristics are predicted to be observed in the transfer curves for a round trip of forward and backward V_{GS} sweeps. In general, the hysteresis is undesirable phenomenon to void in the usual MOSFET applications. However, in this case that the collective movement of hydrogen ions is repeatedly and predictably controllable, V_{th}, in other words, the channel conductivity can be precisely determined. This feature has the high applicability in realizing the synaptic operation of potentiation and depression [24], [25]. A larger V_{th} shift allows to have wider window into which a larger number of weights can be modulated. The hysteresis, or equivalently, V_{th} shift can be analytically expressed in the following procedure.

$$V_{th} = V_{FB0} - \frac{xQ_{ox}}{\varepsilon_{ox}} + \frac{|Q_{dm}|}{C_{ox}} + 2\phi_F \tag{5}$$

V_{FB0} is the flat-band voltage when there is no oxide charge. Q_{dm} is the areal charge density in the unit of C/cm^2 in the semiconductor depletion region. ϕ_F is the potential difference converted from the difference between Fermi level and intrinsic Fermi level in the neutral region.

$$V_{th,positive} = V_{FB0} - \frac{T_{ox}Q_{ox}}{\varepsilon_{ox}} + \frac{|Q_{dm}|}{C_{ox}} + 2\phi_F \tag{6}$$

$$V_{th,negative} = V_{FB0} + \frac{|Q_{dm}|}{C_{ox}} + 2\phi_F \tag{7}$$

$V_{th,positive}$ indicates V_{th} in the steady state that the movements of mobile oxide charges by a positive gate voltage stops eventually at a certain location. $V_{th,negative}$ denotes the V_{th} in the steady state that the opposite process takes place.

$$\Delta V_{th} = V_{th,positive} - V_{th,negative} = -\frac{T_{ox}Q_{ox}}{\varepsilon_{ox}} \tag{8}$$

This MOSCAP theory can be applied for describing the operation physics of the proposed synaptic transistor, and its V_{th} and hysteresis can be mathematically expressed.

$$V_T = V_{T2} + V_{FB0} - \frac{T_{ox1}Q_{ox1}A_1x + T_{ox2}Q_{ox2}A_2y}{\varepsilon_{ox}} \tag{9}$$

$$V_{T0} = V_{T2} + V_{FB0} \tag{10}$$

$$V_{T,final} = V_{T2} + V_{FB0} - \frac{Q_{ox1}A_1T_{ox1}^2 + Q_{ox2}A_2T_{ox2}^2}{\varepsilon_{ox}} \tag{11}$$

$$V_{hysteresis} = \left|V_{T0} - V_{T,final}\right| = \frac{Q_{ox1}A_1T_{ox1}^2 + Q_{ox2}A_2T_{ox2}^2}{\varepsilon_{ox}} \tag{12}$$

Q_{ox1} is the total charge of the hydrogen ions in the oxide between CG and BG in Fig. 4(c) and Q_{ox2} is that in the oxide between BG and the IGZO channel. T_{ox1} and T_{ox2} indicate the respective oxide thicknesses. Also, A_1 and A_2 are the areas of Cu CG and the IGZO channel, respectively. Thus, Eq. (9) through (12) shows that the hysteresis characteristics are dependent on the amount of charges, thickness, area, and electrical permittivity of the CG and channel oxide layers.

In a more macroscopic view, the structure of synaptic transistor consists of two capacitors connected in series, in which the voltage applied on the CG are transferred to the channel in the capacitive manner. The relation between effective $V_{GS,in}$ on the channel and the externally imposed gate voltage $V_{GS,ex}$ can be identified by charge neutrality.

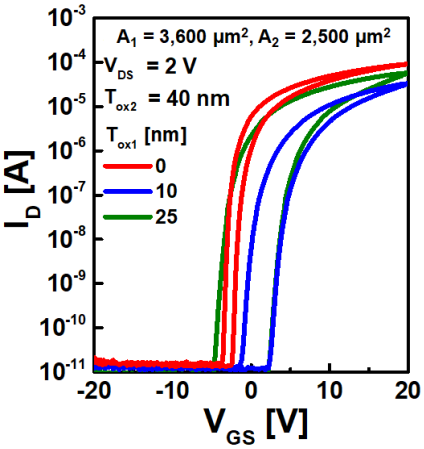
$$C_{ox1}\left(V_{GS,ex} - V_{GS,in} - V_{FB}\right) = C_{ox2}\left(V_{GS,in} - V_{T2} - \frac{yQ_{ox2}A_2T_{ox2}}{\varepsilon_{ox}}\right) \tag{13}$$

$$\begin{aligned} V_{GS,in} &= \frac{C_{ox1}}{C_{ox1}+C_{ox2}}\left(V_{GS,ex} - V_{FB}\right) + \frac{C_{ox2}}{C_{ox1}+C_{ox2}}\left(V_{T2} - \frac{yQ_{ox2}A_2T_{ox2}}{\varepsilon_{ox}}\right) \\ &= \frac{\frac{\varepsilon_{ox}A_1}{T_{ox1}}}{\frac{\varepsilon_{ox}A_1}{T_{ox1}}+\frac{\varepsilon_{ox}A_2}{T_{ox2}}}\left(V_{GS,ex} - V_{FB}\right) + \frac{\frac{\varepsilon_{ox}A_2}{T_{ox2}}}{\frac{\varepsilon_{ox}A_1}{T_{ox1}}+\frac{\varepsilon_{ox}A_2}{T_{ox2}}}\left(V_{T2} - \frac{yQ_{ox2}A_2T_{ox2}}{\varepsilon_{ox}}\right) \\ &= \frac{1}{1+\frac{T_{ox1}}{T_{ox2}}\frac{A_2}{A_1}}\left(V_{GS,ex} - V_{FB0} + \frac{xQ_{ox1}A_1T_{ox1}}{\varepsilon_{ox}}\right) + \frac{1}{1+\frac{T_{ox2}}{T_{ox1}}\frac{A_1}{A_2}}\left(V_{T2} - \frac{yQ_{ox2}A_2T_{ox2}}{\varepsilon_{ox}}\right) \end{aligned} \tag{14}$$

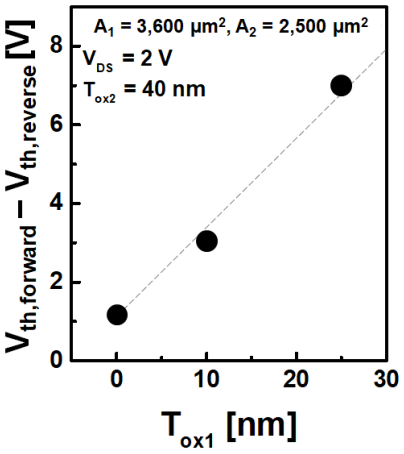
Under the condition that all the internal charges have moved to $x = T_{ox1}$ and $y = T_{ox2}$, the current-voltage (I-V) equation of the synaptic transistor can be formulated as below:

$$I_D = \mu\frac{C_{ox1}C_{ox2}}{C_{ox1}+C_{ox2}}\frac{W_2}{L_2}\frac{1}{1+\frac{T_{ox1}A_2}{T_{ox2}A_1}} \times \left(V_{GS,ex} - V_{FB0} - V_{T2} + \frac{Q_{ox1}A_1T_{ox1}^2 + Q_{ox2}A_2T_{ox2}^2}{\varepsilon_{ox}}\right)^2 \tag{15}$$

As the result, the synaptic transistor with CG has the current characteristics of which hysteresis increases with CG area A_1 and channel area A_2 and both hysteresis and current



(a)



(b)

FIGURE 5. Hysteresis characteristics from the fabricated CG-IGZO synaptic devices with different T_{ox1} values at a fixed T_{ox2} = 40 nm.

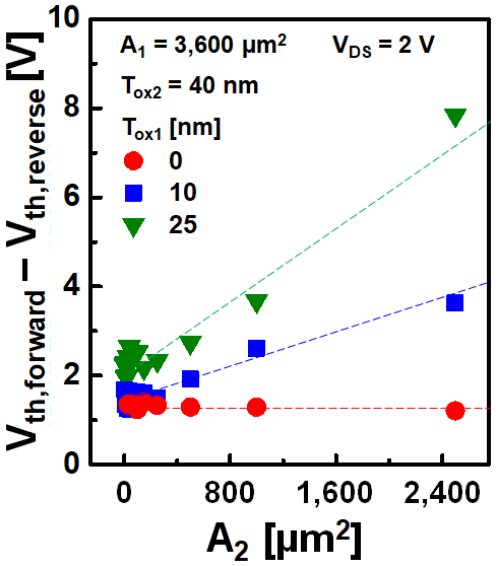


FIGURE 6. Analytical analysis of hysteresis depending of critical dimension in the fabricated CG-IZGO synaptic transistor. V_{th} shift as a function of A_2 at different T_{ox1} values of 0, 10, and 25 nm.

increase with CG oxide thickness T_1 and channel oxide T_2. The hysteresis characteristic is closely related with change in conductance, or equivalently, synaptic weight taking place while performing either potentiation or depression operations.

The current equation in Eq. (15) can be rewritten as a pure function of A_2 by replacing L_2 by $L_2 = A_2/W_2$. As the result, a rational function which has the second-order polynomials in terms of A_2 in both nominator and denominator of the function is obtained but the denominator has a root of zero. It has a geometric implication that a very high conduction current (mathematically, infinite) shows a monotonic decrease as a function of A_2 and asymptotically approaches a convergence value. The wider the hysteresis is, the larger change in synaptic weight is resulted in. The key in designing the proposed synaptic transistor is proven to lie in the optimization of oxide thicknesses between CG and BG and between BG and the conducting channel of the synaptic transistor.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The fabricated synaptic transistors have different CG oxide thicknesses of $T_{ox1} = 0$ nm (direct contact between CG and BG), 10 nm, and 20 nm, while width/length (W/L) dimensions are set to $W/L = 50/50\,\mu$m. The gate voltage V_{GS} was swept over a large enough range between -20 V and 20 V with an interval of 0.1 V so that the effective location of internal charges can be controlled over the entire geometrical range between 0 and T_{ox}. A Keithley 4200A-SCS Parameter Analyzer was used for the electrical characterization. Fig. 5(a) shows the initial I-V curves from the fabricated synaptic transistors with different T_{ox1}'s. The voltage sweep was conducted in the round-trip manner so that the hysteresis can be clearly observed. Further, the measurement under each condition was performed on eight different devices for proving the higher credibility and reproducibility of the synaptic operations. Fig. 5(b) shows the hysteresis extracted from Fig. 5(a). The threshold voltages were read by constant current method at $I_D = 10^{-9}$ A and hysteresis value was defined to be the difference between threshold voltages for forward sweep and for reverse sweep, $V_{hysteresis} = V_{th,forward} - V_{th,reverse}$. Fig. 6 depicts the hysteresis as a function of channel area A_2 at different T_{ox1}'s. As predicted from the theoretical background, it is experimentally reassured from Fig. 6 that hysteresis has the strong positive relations with A_2 and T_{ox1}. In particular, the dependence of hysteresis on T_{ox1} is revealed to be hyper linear in accordance with Eq. (12). The allowed total length of ion movement in the oxide is determined by T_{ox1} and the additionally required synaptic operation voltage is dependent on effective vertical location of the charges. Fig. 7(a) shows the voltage schemes for potentiation, read (inference), and depression operations, respectively. In order to perform the potentiation and depression operations, gate overdrive ($V_{GS} - V_{th}$) of 7 V and -3 V were applied, respectively, for 700 μs. In these operations, drain voltage (V_{DS}) is set to 0 V, in order for purely vertical movements of the charges

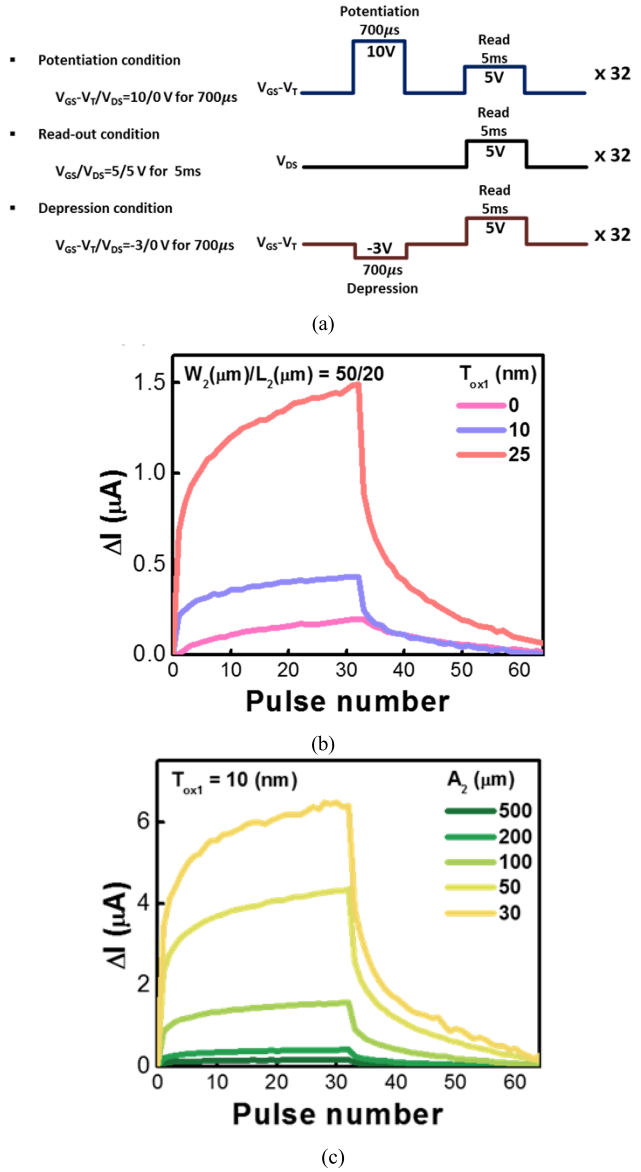


FIGURE 7. Synaptic operation characteristics. (a) Operation schemes for potentiation, read (inference), and depression. Conductance modulation characteristics depending on (b) CG oxide thickness T_{ox1} and (c) channel area A_2.

across the oxide regions. Read operation is carried out at $(V_{GS} - V_{th}, V_{DS}) = (5\text{ V}, 5\text{ V})$. The potential and depression operations were performed 32 times each in the consecutive manner to investigate the gradual change in read current. Fig. 7(b) shows the read current as the pulse operation is preceded for the synaptic devices with $W/L = 50/20\ \mu$m with different T_{ox1}'s of 0 nm, 10 nm, and 25 nm. The change in drain current (ΔI) is the difference between actual read current at a specific point and the initial current value before conducting any synaptic operation. Current changes over the consecutive potentiation pulses are depicted up to the pulse number of 32 and those over the repeated depression pulses are shown afterward up to number of 64. It is clarified by Fig. 7(b) that the amount of change in current modulation gets larger as T_{ox1} increases at a given gate overdrive. Fig. 7(c) demonstrates the weight change over the synaptic operations at different A_2's at a fixed $T_{ox1} = 10$ nm. The scaling of A_2 is made by controlling channel length L_2 for 50, 20, 10, 5, and 3 μm while the channel width W_2 is constant at 10 μm. It is confirmed by Fig. 7(c) that smaller A_2 (shorter L_2) makes the conductance change more distinguishable. Thus, it can be reasoned that the correlation between the proposed model and the experimental part can be found. It has been shown in this work that the synaptic operation can have the improved tolerance against the threshold voltage variation by widening the usable voltage range for more distinctive synaptic operation characteristics and getting the hysteresis under control, by the help of the novel structuring with extended gate. Moreover, controlling the oxide thicknesses and effective contact area has a substantial effect in changing the synaptic operation characteristics, which surely is an engineering variable from the neuromorphic system point of view.

V. CONCLUSION

In this work, an advanced synaptic transistor based on IGZO thin-film transistor has been proposed, fabricated, and characterized. The improved synaptic operations attribute to a novel structure featuring coupling gate and alumina prepared at a low temperature by atomic layer deposition. From the theoretical study, it has been found that the hysteresis characteristics can be practically altered by a set of design parameters of T_{ox1}, T_{ox2}, A_1, and A_2. Furthermore, stronger dependences of the synaptic operations have been traced on T_{ox1} and A_2, more experimentally. The proposed device structure featuring the extended gate has been proven to provide the distinct weight tunability of a synaptic transistor through its dependence on thickness of the oxide beneath the coupling gate and the channel width/length which can be rather easily in the device fabrication and layout design levels. A new application of IGZO in the synaptic transistor toward the hardware neuromorphic system has been evaluated with highly feasible and practical process integration and design.

ACKNOWLEDGMENT

Dongyeon Kang and Jun Tae Jang contributed equally to this work.

REFERENCES

[1] G. Brewka, "Artificial intelligence—A modern approach by stuart Russell and Peter Norvig, Prentice-Hall. Series in artificial intelligence, Englewood Cliffs, NJ," *Knowl. Eng. Rev.*, vol. 11, no. 1, pp. 78–79, Mar. 1996.

[2] S. Fusi, M. Annunziato, D. Badoni, A. Salamon, and D. J. Amit, "Spike-driven synaptic plasticity: Theory, simulation, VLSI implementation," *Neural Comput.*, vol. 12, no. 10, pp. 2227–2258, Oct. 2000.

[3] J. von Neumann, "First draft of a report on the EDVAC," *IEEE Ann. Hist. Comput.*, vol. 15, no. 4, pp. 27–75, Jun. 1993.

[4] J. Koo, J. Kim, S. Ryu, C. Kim, and J.-J. Kim, "Area-efficient transposable crossbar synapse memory using 6T SRAM bit cell for fast online learning of neuromorphic processors," *J. Semicond. Technol. Sci.*, vol. 20, no. 2, pp. 195–203, Apr. 2020.

[5] S. N. Truong and K.-S. Min, "New memristor-based crossbar array architecture with 50-% area reduction and 48-% power saving for matrix-vector multiplication of analog neuromorphic computing," *J. Semicond. Technol. Sci.*, vol. 14, no. 3, pp. 356–363, Jun. 2014.

[6] J.-H. Ryu, B. Kim, F. Hussain, M. Ismail, C. Mahata, T. Oh, M. Imran, K. K. Min, T.-H. Kim, B.-D. Yang, S. Cho, B.-G. Park, Y. Kim, and S. Kim, "Zinc tin oxide synaptic device for neuromorphic engineering," *IEEE Access*, vol. 8, pp. 130678–130686, Jul. 2020.

[7] C. D. Wright, P. Hosseini, and J. A. V. Diosdado, "Beyond von-Neumann computing with nanoscale phase-change memory devices," *Adv. Funct. Mater.*, vol. 23, no. 18, pp. 2248–2254, May 2013.

[8] C.-S. Poon and K. Zhou, "Neuromorphic silicon neurons and large-scale neural networks: Challenges and opportunities," *Frontiers Neurosci.*, vol. 5, pp. 108-1–108-3, Sep. 2011.

[9] C. Lee, J. Lee, M. Kim, J. Woo, S.-M. Koo, J.-M. Oh, and D. Lee, "Two-terminal structured synaptic device using ionic electrochemical reaction mechanism for neuromorphic system," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 546–549, Apr. 2019.

[10] S. B. Laughlin, R. R. de Ruyter van Steveninck, and J. C. Anderson, "The metabolic cost of neural information," *Nature Neurosci.*, vol. 1, no. 1, pp. 36–41, May 1998.

[11] N. K. Upadhyay, H. Jiang, Z. Wang, S. Asapu, Q. Xia, and J. J. Yang, "Emerging memory devices for neuromorphic computing," *Adv. Mater. Technol.*, vol. 4, no. 4, pp. 1800589-1–1800589-13, Jan. 2019.

[12] D. A. Drachman, "Do we have brain to spare?" *Neurology*, vol. 64, no. 12, pp. 2004–2005, Jun. 2005.

[13] S.-Y. Min and W.-J. Cho, "CMOS-compatible synaptic transistor gated by chitosan electrolyte-Ta_2O_5 hybrid electric double layer," *Sci. Rep.*, vol. 10, no. 1, pp. 15561-1–15561-8, Sep. 2020.

[14] Y. Liu, X. Wang, W. Chen, L. Zhao, W. Zhang, W. Cheng, Z. Zhuo, J. Wang, T.-L. Ren, and J. Xu, "IGZO/Al_2O_3 based depressed synaptic transistor," *Superlattices Microstruct.*, vol. 128, pp. 177–180, Apr. 2019.

[15] W. Chen, W. Lu, B. Long, Y. Li, D. Gilmer, G. Bersuker, S. Bhunia, and R. Jha, "Switching characteristics of W/Zr/HfO_2/TiN ReRAM devices for multi-level cell non-volatile memory applications," *Semicond. Sci. Technol.*, vol. 30, no. 7, pp. 075002-1–075002-7, Jun. 2015.

[16] K. M. Kim, J. J. Yang, J. P. Strachan, E. M. Grafals, N. Ge, N. D. Melendez, Z. Li, and R. S. Williams, "Voltage divider effect for the improvement of variability and endurance of TaO_x memristor," *Sci. Rep.*, vol. 6, no. 1, pp. 20085-1–20085-6, Feb. 2016.

[17] Y. Nishitani, Y. Kaneko, M. Ueda, T. Morie, and E. Fujii, "Three-terminal ferroelectric synapse device with concurrent learning function for artificial neural networks," *J. Appl. Phys.*, vol. 111, no. 12, pp. 124108-1–124108-6, 2012.

[18] J. T. Jang, J. Park, B. D. Ahn, D. M. Kim, S.-J. Choi, H.-S. Kim, and D. H. Kim, "Effect of direct current sputtering power on the behavior of amorphous indium-gallium-zinc-oxide thin-film transistors under negative bias illumination stress: A combination of experimental analyses and device simulation," *Appl. Phys. Lett.*, vol. 106, pp. 123505-1–123505-5, Mar. 2015.

[19] R.-J. Lyu, Y.-H. Chiu, H.-C. Lin, P.-W. Li, and T.-Y. Huang, "High-gain, low-voltage BEOL logic gate inverter built with film profile engineered IGZO transistors," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Apr. 2016, pp. 1–2.

[20] L.-L. Chi, J.-C. Chou, W.-Y. Chung, T.-P. Sun, and S.-K. Hsiung, "Study on extended gate field effect transistor with tin oxide sensing membrane," *Mater. Chem. Phys.*, vol. 63, no. 1, pp. 19–23, Feb. 2000.

[21] J.-H. Jeon and W.-J. Cho, "High-performance extended-gate ion-sensitive field-effect transistors with multi-gate structure for transparent, flexible, and wearable biosensors," *Sci. Technol. Adv. Mater.*, vol. 21, no. 1, pp. 371–378, Jan. 2020.

[22] Y.-H. Chang, M.-J. Yu, R.-P. Lin, C.-P. Hsu, and T.-H. Hou, "Abnormal positive bias stress instability of In-Ga-Zn-O thin-film transistors with low-temperature Al_2O_3 gate dielectric," *Appl. Phys. Lett.*, vol. 108, no. 3, pp. 033502-1–033502-4, Jan. 2016.

[23] P. B. Pillai and M. M. De Souza, "Nanoionics-based three-terminal synaptic device using zinc oxide," *ACS Appl. Mater. Interfaces*, vol. 9, no. 2, pp. 1609–1618, Jan. 2017.

[24] W. Zhu and J. Li, "Synaptic learning and forgetting behavior in Ag/AlN/Al memristor with O_2 annealing effect," *IEEE Access*, vol. 7, pp. 163358–163364, Nov. 2019.

[25] Y. Zhao, D. Yu, Z. Liu, S. Li, and Z. He, "Memtransistors based on non-layered In_2S_3 two-dimensional thin films with optical-modulated multi-level resistance states and gate-tunable artificial synaptic plasticity," *IEEE Access*, vol. 8, pp. 106726–106734, Jun. 2020.

DONGYEON KANG received the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2020, where he is currently pursuing the M.S. degree with the School of Electrical Engineering.

JUN TAE JANG received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, South Korea, in 2014 and 2016, respectively, where he is currently pursuing the Ph.D. degree with the School of Electrical Engineering.

SHINYOUNG PARK received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, South Korea, in 2018 and 2020, respectively. She is currently working as an affiliated Researcher with Kookmin University.

MD. HASAN RAZA ANSARI (Member, IEEE) received the M.Tech. degree in nanotechnology from the Vellore Institute of Technology, Vellore, India, in 2016, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology (IIT), Indore, India, in 2019. He is currently working as a Postdoctoral Fellow with the Department of Electronic Engineering, Gachon University, South Korea. His current research interests include advanced logic devices, emerging memory devices, and neuromorphic devices and circuits.

JONG-HO BAE (Member, IEEE) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology, South Korea, in 2011, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea, in 2018. He is currently an Assistant Professor with the School of Electrical Engineering, Kookmin University, Seoul.

SUNG-JIN CHOI received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2012. He is currently an Associate Professor with the School of Electrical Engineering, Kookmin University, Seoul, South Korea.

DONG MYONG KIM (Member, IEEE) received the B.S. *(magna cum laude)* and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, MN, USA, in 1993. Since 1993, he has been a Professor with the School of Electrical Engineering, Kookmin University, Seoul. His research interest includes modeling and characterization of semiconductor devices.

CHANGWOOK KIM received the B.S. and M.S. degrees from the Department of Chemistry, Sogang University, Seoul, South Korea, in 1993 and 1995, respectively, and the Ph.D. degree from the Department of Chemistry, Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003. Since 2016, he has been a Research Professor with the Circadian ICT Center, Kookmin University, Seoul. His research interests include circadian rhythm, color science, and computational chemistry.

SEONGJAE CHO (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2004 and 2010, respectively. He is currently an Associate Professor with the Department of Electronic Engineering, Gachon University, Seongnam, South Korea. His research interests include emerging memory devices, nanoscale CMOS devices, group-IV optical devices, and neuromorphic devices and integrated circuits.

DAE HWAN KIM (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1996, 1998, and 2002, respectively. He is currently a Professor with the School of Electrical Engineering, Kookmin University, Seoul. His current research interests include nano CMOS, oxide and organic thin-film transistors, biosensors, and neuromorphic devices.