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Improved Controller and Design Method for Grid-Connected Three-Phase Differential SEPIC Inverter

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ABSTRACT Single-ended primary-inductor converter (SEPIC) based differential inverters (SEPIC-BDI) have received wide concerns in renewable energy applications due to their modularity, galvanic isolation, decreased power stages, continuous input current, and step up/down capability. However, its design still has several challenges related to component design, the existence of complex right half plane (RHP) zeros, and increased sensitivity to component mismatches. In this context, this paper presents an improved control and enhanced design method for the three-phase SEPIC-BDI for grid-tied applications. A generalized static linearization approach (SLA) is proposed to mitigate the low-order harmonics. It practically simplifies the control complexity and decreases the required control loops and sensor circuits. The mismatch between the SEPIC converters in each phase is highly mitigated due to the independent operation of the SLA in each phase and the output dc offset currents are reduced. The proposed enhanced design methodology modifies the SEPIC open-loop transfer function by moving the complex RHP zeros to the left half-plane (LHP). Therefore, a simple proportional-integral (PI) controller effectively maintains converter stability without adding higher-order compensators in the literature. Moreover, a straightforward integrator in the control loop eliminates the negative sequence harmonic component (NSHC) and provides a low computational burden. Simulations and experimental results based on 200V, 1.6 kW, 50 kHz prototype with silicon carbide (SiC) devices are provided to validate the effectiveness of the proposed work. The results show that the proposed controller and design method achieve pure output current waveforms at various operating points of the inverter and dc voltage variations.

INDEX TERMS Differential inverter, renewable energy applications, negative sequence harmonic component, power converters, power losses, single-ended primary-inductor converter (SEPIC).

I. INTRODUCTION

With the increased deployment and investments of renewable energy sources (RESs), such as photovoltaics (PV), wind generation system, and fuel cells, power converters have become key contributors in ensuring reliable and efficient conversion of the extracted power from RESs to the loads and/or utility grid [1]–[3]. Conventional inverters utilize two/three legs to build single/three-phase voltage source inverters (VSIs). However, the integration of the recent RESs

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with the utility grid needs DC-AC conversion circuits with voltage boosting capability and low common-mode voltage (CMV) [4]. In order to fulfill these requirements, integration of line frequency transformer (LFT) between inverter and grid is the simple and straightforward solution [5]. However, the existence of LFT complicates the system in addition to increasing the system weight and cost, particularly in small-rating conditions (<5 kW), which represent major of recent installed inverter ratings [6], [7]. The existence of LFT deteriorates the RES through decreasing system efficiency, lowering power density, and increasing electromagnetic interference (EMI) problems. Many inverter topologies have been presented in the literature for replacing LFT with high boosting DC-DC converters. Though the overall efficiency of the inverter has been improved, two control loops are essential to regulate DC-link voltage and to control the injected current to the grid. Furthermore, smooth operation of DC-link voltage requires the utilization of large electrolyte capacitors, which adversely affect the inverter reliability and operating lifetime [8]–[10].

Several single-stage inverter solutions have been proposed in the literature for enhancing the power conversion efficiency and reliability [11]–[13]. In [13]–[17], single-stage boost inverter (SSBI) topologies have been proposed to achieve higher output AC voltage. The addressed SSBI can be classified into two main configurations; The first configuration uses three high frequency transformers (HFTs) for ensuring the galvanic isolation and mitigating CMV [13], [18], [19]. Three H-bridge converters are used on the primary sides of the HFTs to convert the DC input voltage into the three-phase voltage. However, additional bridge converters are provided on the secondary sides of the HFTs to control the generated three-phase voltages. Every H-bridge converter in the primary sides of HFTs processes only the power of its specified phase, which equals to one-third of the inverter power. Although this configuration guarantees low power rating for the semiconductor devices, it requires high number of power switches. This in turn makes the implementation and control process more complex and unreliable. The second configuration is based on eliminating the electrolytic DC-link capacitor that is essential in the two-stage configuration. However, the control complexity is increased, and both the DC-DC converters and VSI have to process the full power [14], [15]. From another side, several topologies have been proposed by replacing the DC-DC converters with impedance networks and diodes, such as Z-source inverters and split-source inverters [16], [17]. However, these configurations still lack for the galvanic isolation between the input and output.

In this context, differential inverter topologies have been developed to combine all the features of the previous two configurations [20]–[23]. In differential inverter topologies, each leg of VSI is replaced with a DC-DC converter, as shown in Fig. 1. The prominent feature of this simple structure is achieved through combining merits of traditional VSI and DC-DC converters in one compact single-stage. Similar to VSIs, the differential inverter can be controlled using a single

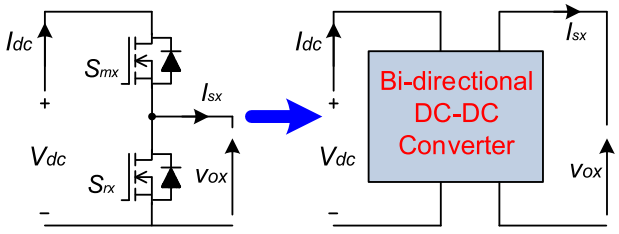


FIGURE 1. Single leg representation of the VSI and differential inverter.

parameter (like modulation index in VSIs), which does not need complex control parameters. Furthermore, the utilized DC-DC converters have many features such as using small passive elements. This in turn ensures the reliable operation of the differential inverter with reduced weight and volume. It can also provide voltage higher than or lower than input voltage magnitude with bidirectional power processing capability. Additionally, the utilization of HFT-based DC-DC converters provides the galvanic isolation and hence the elimination of leakage currents.

Therefore, the main features and advantages of differential inverters can be summarized as follows:

- Each DC-DC converter in the three/single differential inverters processes one-third/half of the inverter power. Therefore, lower components ratings are needed.
- Independent control of the DC-DC converters in differential inverters simplifies the modular construction by adding paralleled DC-DC converters.
- Failure of one DC-DC converter in the differential structure does not mean the whole failure of the system. This attractive feature improves the inverter reliability and system availability.
- Modular for various multi-phase inverter systems.

Several topologies and control techniques have been proposed in the literature for differential inverters [20]–[23]. In [20], a single-phase 500W differential inverter based on a two-boost converters has been presented for a standalone application. The control function is based on using sliding-mode control and PWM continuous modulation scheme (CMS). In [21], a 1kW buck-boost single-phase differential inverter has been introduced, where voltage-mode control using a static linearization approach (SLA) is implemented. In which, the SLA is implemented by function known as $F(\phi)$. In [22], a three-phase differential inverter using two SEPIC converters has been presented to utilize the full voltage range of the four-switch inverter. The presented inverter is controlled by integral sliding mode control technique, while the voltage gain is limited by the input DC voltage. It is worth mentioning that sliding-mode control theory was extensively used with differential inverters as in [20], [22], [24] due to their superior features. Moreover, recent sliding-mode control techniques, such as adaptive second-order and high-order controllers can effectively enhance differential buck inverters [25]–[29]. Moreover, these techniques can reduce the mismatched

TABLE 1. Comparison of the proposed contribution with exiting literature.

Ref		Ref [20]	Ref [21]	Ref [22]	Ref [30]	Ref [37]	Ref [38]	Ref [39]	Ref [40]	Ref [41]	Proposed
Topology		Boost	Buck-boost	SEPIC	Boost	Cuk	Buck-boost	Cuk	Cuk	SEPIC	SEPIC
No. Phases		Single	Single	Three	Three	Three	Three	Three	Single	Three	Three
Load		Resistive	Resistive	Resistive	Resistive	Resistive	Grid-tied	Resistive	Resistive	Grid-tied	Grid-tied
Rating (kW)		0.5	1	0.4	1.4	2.5	2.5	0.5	0.5	1.6	0.2-1.6
Converter Design		Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & ratings	Ripple & control
Design Consideration		Passive-only	Passive-only	Passive-only	Passive-only	Passive-only	Passive-only	Passive-only	Passive-only	Passive-only	Passive, active, control
THD %		1.24	–	No –	6	6	1.02	6	5.5	4.087	3.26
HFT		No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Measured η %		–	Peak 89.0	–	–	–	Theory 95.00	Peak 91	Peak 92	Peak 89.744	Peak 90.12
Control	Type	nonlinear	linear	nonlinear	nonlinear	linear	linear	linear	linear	linear	linear
	Imp	Sliding	voltage	Sliding	Sliding	PI&PR	PR	PR	PR	Type-II	PI
	No. Loops	–	1	–	–	2	3	1	5	2	2
PWM	Scheme	CMS	CMS	CMS	CMS	CMS	CMS	DMS	DMS	CMS	MCMS
	SLA	–	F(Ø)	–	–	V-ratio	V-ratio	V-ratio	V-ratio	V-ratio	V-ratio
	sensing	NR	NR	NR	NR	NR	NR	V_{dc}	V_{dc}	No	No
	NSHC	–	No	–	–	Yes	Yes	No	–	Yes	Yes

uncertainties, which existed in traditional sliding-mode controllers [27], [29].

Three-phase differential inverters utilizing three boost converters have been presented in several articles [25], [30]–[36]. In [36], the differential boost inverter is combined with a battery-supported circuit for fuel cell applications. Moreover, five buck-boost converters have been implemented in three-phase differential inverters [37], [38]. The buck-boost converters can provide better performance with continuous input-current, which is essential for photovoltaic (PV) applications. In addition, a simple control technique based on proportional resonance (PR) compensator has been applied for non-isolated and isolated topologies. Also, a three/single differential inverter based on three/two Cuk converters has been proposed in [39] and [40], respectively. In both circuits, a PWM discontinuous modulation scheme (DMS) is used to reduce the circulating power. The static linearization block is based on the voltage ratio of Cuk converters and sensing signal of input voltage.

In [41], [42], a three-phase inverter has been proposed based on three isolated SEPIC converters for grid-tied applications. The SEPIC converter provides a continuous input current and galvanic isolation using two switches and few passive elements. In [41], the negative sequence harmonic component (NSHC), which is being generated at the output terminals of the differential inverters, is mitigated. The mathematical analysis for NSHC has been presented, and its effects on the DC input voltage have been validated using simulation and experimental results. Furthermore, a modular SEPIC-based differential inverter (SEPIC-BDI) has been proposed in [42]. Three SEPIC modules are utilized in each phase to increase the inverter power. The modular structure is developed based on the input-parallel output-parallel connection of the SEPIC modules.

Table. 1 provides a detailed comparison for the addressed differential inverters in the literature compared to the proposed one. It can be seen that most of the addressed differential topologies lack for detailed converter design. The design process of these topologies only considers the required ripple components (large-signal modeling) and the power rating of the utilizing components to check the voltage and current stress. However, they did not consider the effect of selected passive elements on the performance of control techniques. Moreover, the addressed topologies lack information about the robust relationship between the pulse width modulations of differential inverters and their static linearization approaches. An application of simple, generic, and easy-implemented static linearization approach results in improving highly the operation of differential inverters by reducing the number of control loops, control complexity, and employed sensing circuits. Finally, all previous topologies did not include the implementation steps of their static linearization approach. Therefore, this paper focuses on the controller, modulation technique, converter design considerations with static linearization approach, and harmonics compensation capability issues to fill this critical gap.

Motivated by the above-mentioned issues and challenges in SEPIC-BDI, this paper presents an improved control and enhanced design method for grid-tied three-phase single-stage isolated SEPIC-BDI. The main contributions of this paper can be summarized as follows:

- A generalized static linearization approach (SLA) is proposed in this paper. Although this approach is briefly discussed in [41], [42] for analysing the inverter operation, this paper provides the detailed generalized implementation steps. The simplicity and generality to be applied to other DC-DC converter types have been investigated.
- Independent application of SLA and the necessity for eliminating the feedforward sensing is presented. This feature can dramatically reduce the mismatch between SEPIC converters in addition to reducing the required control loops. Moreover, superiority of the proposed SLA method over conventional PWM methods of VSIs is also validated.
- An improved design strategy for designing the components of SEPIC inverter is proposed in this paper. This strategy can effectively move the complex RHP zeros to LHP side. It decreases the non-minimum phase of the utilized SEPIC converters from 630^o to 450^o.
- The small non-minimum phase response facilities the use of PI compensator instead of high-order compensator (PID [42], and type-II [41]). It can effectively reduce the computational burden of the controller. Moreover, the new designed parameters of the utilized SEPIC converter enhances the inverter efficiency.

The rest of the paper is organized as follows: The principal operation of the SEPIC-BDI, CMS modulation, and operation of utilized SEPIC converters are covered in Section II. The existed practical issues of SEPIC-BDI with conventional CMS is presented in Section III. Additionally, the proposed static linearization approach SLA is also illustrated. The proposed enhanced design method of SEPIC elements is covered in section IV. In section V, the developed control technique is described. Results, discussions and inverter losses are provided in section VI. Finally, the conclusion is provided in Section VII.

II. SEPIC-BASED DIFFERENTIAL INVERTER: WORKING PRINCIPAL AND CONVENTIONAL MODULATION SCHEME

The basic building structure of differential inverters is shown in Fig. 1. For three phase differential inverter, three legs are needed for proper operation, where ($x \in \{u, v, w\}$). Each inverter leg has at least one DC-DC converter, which is designed based on the required rated power. All the converter legs share the same input source voltage V_{dc}. The output voltages are differentially connected on the AC side terminal (grid e_{sx}). Fig. 2 shows the schematic diagram of the differential inverter using three SEPIC converters, which has been presented in [41], and it will be focused in this paper.

Among the different DC-DC converters, SEPIC converter has several advantages, such as the non-inverting step-up/down capability, and the input/output isolation using small HFT. It has been utilized in several applications, such as point of load (POL) converters, battery-powered systems, and power factor correction (PFC) converters [43]–[45]. SEPIC converter has only two switches (main switch S_{mx} and synchronous switch S_{rx}). The two switches in each phase leg operate in complementary manner as in the upper/lower switches of conventional VSI. In addition, the SEPIC inverter has one input inductor L_x, two film capacitors (coupling capacitor C_x and output capacitor C_{ox}). It is worth mentioning that SEPIC converters exhibit several additional advantages, such as continuous input current, which is being necessary to extract the maximum power from PV sources, increased voltage gain and reduced voltage stresses on the power switches [38].

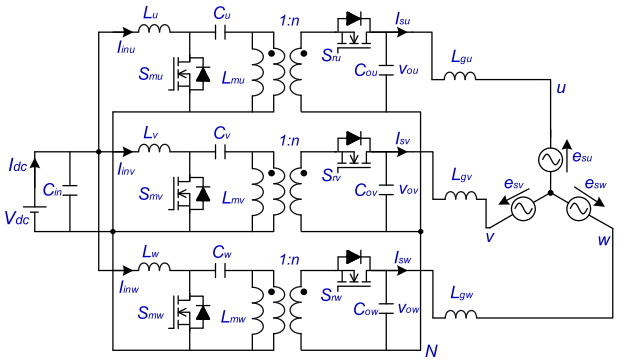


FIGURE 2. Circuit schematic of the isolated SEPIC-BDI.

A. CONVENTIONAL CONTINUOUS MODULATION SCHEME (CMS) OF DIFFERENTIAL INVERTERS

Modulation of the conventional three-phase VSI is derived using bipolar pulse width modulation (PWM). It is developed by comparing the modulation index ($m \leq 1$) with a sinusoidal signal at the grid-frequency F_g, which can be expressed as:

$$\begin{bmatrix} d_u \\ d_v \\ d_w \end{bmatrix} = m \times \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (1)$$

where $\omega = 2\pi F_g$ is the radian frequency of the grid. d_x is the duty ratio of each inverter leg. Moreover, another modulation technique based on a 120^o phase-shifted modulation signals is applied to generate three-phase voltage where, the output signal is compared with a sawtooth signal (switching-frequency F_s) to produce the gate signals of the complementary switches in each phase leg. Continuous modulation scheme (CMS) has been widely used in differential inverters as shown in Fig. 3 [20], [25].

According to CMS, each DC-DC converter generates a sinusoidal AC output voltage imposed on a DC biased voltage due to the unipolar characteristics of all DC-DC converters. The AC component of each converter equals to the phase voltage of its connected phase of the grid. Therefore, the output voltages amplitudes of all converter can be expressed as

follows:

$$\begin{bmatrix} v_{ou}(t) \\ v_{ov}(t) \\ v_{ow}(t) \end{bmatrix} = \begin{bmatrix} E_{dcu} + E_m \sin(\omega t) \\ E_{dcv} + E_m \sin(\omega t - \frac{2\pi}{3}) \\ E_{dcw} + E_m \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (2)$$

where, $v_{ox}(t)$ represents the instantaneous output voltage of each phase, E_{dc} denotes to the DC component of the output voltage, and E_m is the peak AC component of the output voltage. For symmetrical operation, it can be assumed that:

$$E_{dcu} = E_{dcv} = E_{dcw} = E_{dc} \quad (3)$$

Afterwards, the DC biased voltages are canceled and decoupled from the grid voltage by the differential connection of converters due to the symmetrical operation. The line-to-line voltages of the differential inverter can be expressed as follows:

$$\begin{bmatrix} E_{suv}(t) \\ E_{svw}(t) \\ E_{swu}(t) \end{bmatrix} = \begin{bmatrix} V_{ou}(t) - V_{ov}(t) \\ V_{ov}(t) - V_{ow}(t) \\ V_{ow}(t) - V_{ou}(t) \end{bmatrix} = \sqrt{3}E_m \begin{bmatrix} \sin(\omega t + \frac{\pi}{6}) \\ \sin(\omega t - \frac{3\pi}{6}) \\ \sin(\omega t + \frac{5\pi}{6}) \end{bmatrix} \quad (4)$$

It worth noticing that both the DC and AC components of the output voltage are generated by the same converter and should be larger than the voltage of input source to achieve step-up voltage ratio. In this context, the voltage gain of the utilized DC-DC converter is divided equally between the DC and AC components. Therefore, the static gain of differential inverter is expressed as follows:

$$M = 0.5\frac{v_{ox_m}}{V_{dc}} \quad (5)$$

where, v_{ox_m} represents the maximum amplitude of the output voltage of the utilized DC-DC converter. Furthermore, unlike the modulation index of the VSI shown in (1), the value of M depends on the boosting capability of the DC-DC converter.

B. MODES OF OPERATIONS FOR THE UTILIZED DC–DC CONVERTERS IN DIFFERENTIAL INVERTERS

By assuming pure active power with unity power factor for SEPIC-BDI, the output current of phase leg u in the SEPIC differential inverter can be expressed as follows:

$$i_{sx} = I_m \sin(\omega t) \quad (6)$$

where I_m represents the peak value of the output phase current. Whereas, the voltage ratio of SEPIC inverter can be expressed as follows:

$$\frac{v_{ox}(t)}{V_{dc}} = \frac{vi_{inx}(t)}{i_{sx}(t)} = \frac{nd_x}{1 - d_x} \quad (7)$$

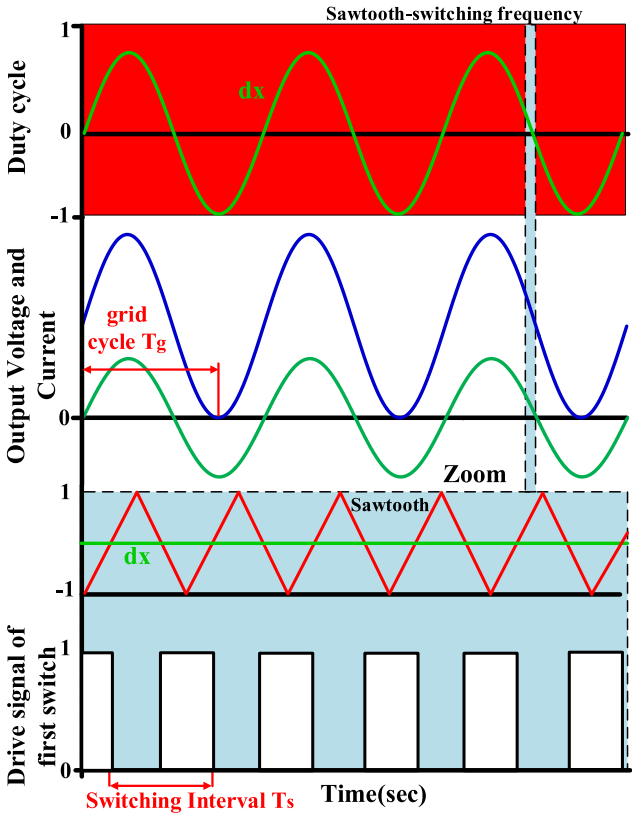


FIGURE 3. Traditional CMS PWM of differential inverters.

Using (6) and Using (7), the input current of the SEPIC converter can be obtained as follows:

$$i_{inx}(t) = I_m \sin(\omega t) \times \frac{nd_x}{1 - d_x} \quad (8)$$

By using CMS, (8) can be rewritten as follows:

$$i_{inx}(t) = I_m \sin(\omega t) \times \frac{n \sin(\omega t)}{1 - \sin(\omega t)} \quad (9)$$

By combining (5) and (9), the input current of SEPIC is obtained as follows:

$$i_{inx}(t) = 0.5MI_m + MI_m \sin(\omega t) \times -0.5MI_m \cos(2\omega t) \quad (10)$$

According to (10), the input current of each SEPIC converter depends on the output phase current and the static gain of the differential inverter. Fig. 4 shows the duty cycle using CMS, the input and the output currents of the SEPIC obtained at (6) and (10). In the positive cycle of grid current, SEPIC converter processes the input power similar to the leg of conventional VSI. However, during the negative cycle, the unipolar operation of SEPIC converter (positive output voltage) with the negative cycle of grid current introduces a pulsating power at twice the line frequency, as shown in Fig. 4. This pulsating power introduces a negative sequence harmonic component (NSHC) in the output current of each converter. It is worth to notice that this issue is also existed in the other existing differential inverters based on buck, boost or buck-boost converters. Referring to Fig. 4, the grid

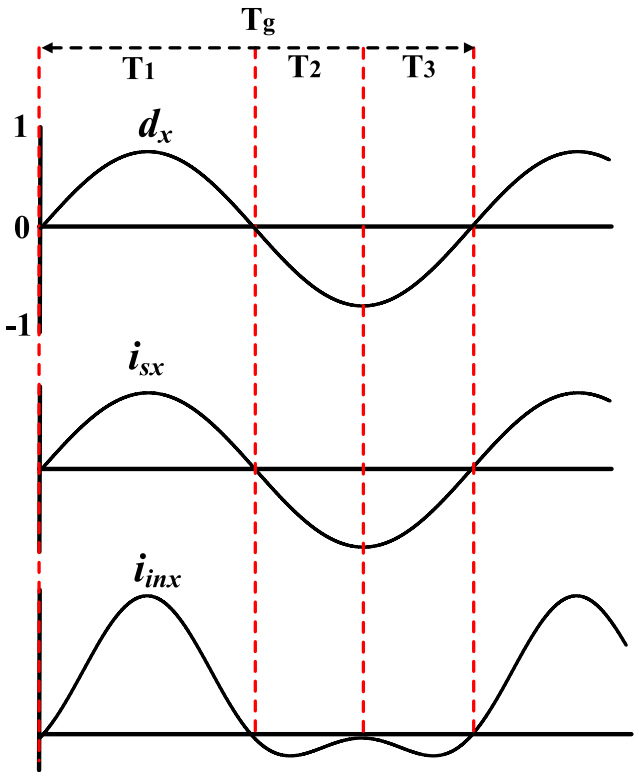


FIGURE 4. Mathematical representation of duty cycle, output and input currents using CMS.

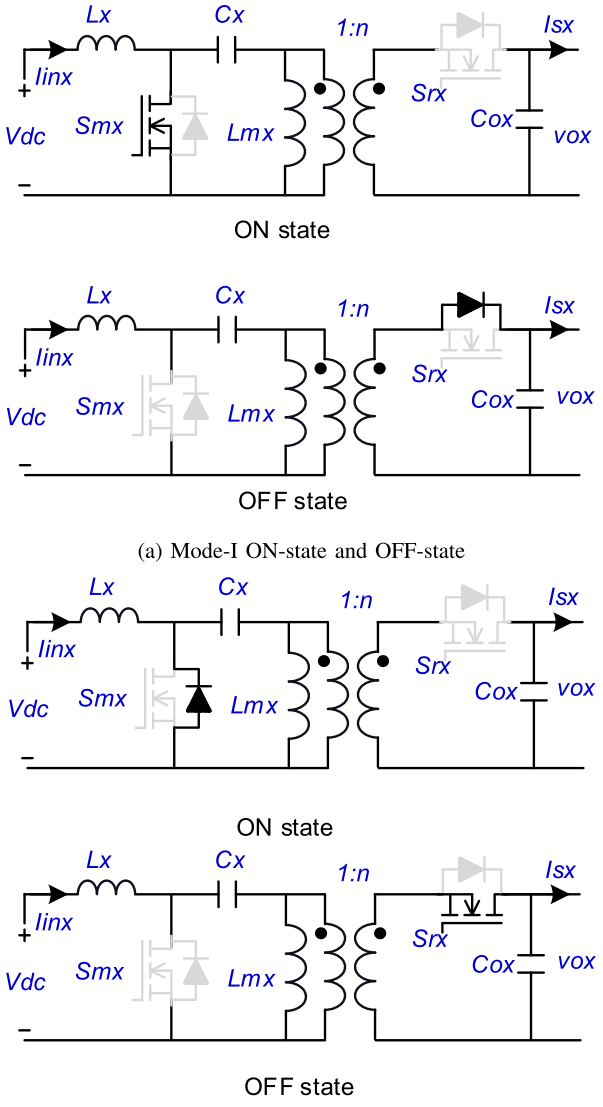


FIGURE 5. Switching states of the proposed SEPIC converters.

cycle T_g is divided into three different periods for all SEPIC converters: For period T_1, the duty cycle d_x is higher than 0.5. Hence, the input current i_{inx} and the output grid current i_{sx} are positive. In this situation, Mode-I for positive power flow is obtained, wherein the converter power flows from the input source to the grid. In the second period T_2, the duty cycle d_x is low and the currents i_{inx} and i_{sx} are negative, which means that the power flows from the other two SEPICs and circulates among them and the same analysis can be applied for period T_3. The difference between T_2 and T_3 is the origin of the current. In T_2, the current flows from the second SEPIC, whereas in T_3, the current flows from the third SEPIC. To achieve appropriate power conversion, Mode-II is introduced for $T2$ and T_3 for negative power flow.

Fig. 5 shows the various operating modes of the SEPIC-BDI. In Mode-I, the power flow is processed by the complimentary switching operation of the main switch S_{mx} and the body diode of the synchronous switch S_{rx}. In this interval, S_{mx} is turned ON and the input inductor captures the energy form the DC source. The HFT inductance is charged from the coupling capacitor and the output capacitor is responsible for supplying the grid-current. S_{mx} is turned OFF in the next switching interval as indicated in Fig. 5a. The input inductor charges the coupling capacitors and provides the current to the grid. The complementary operation of synchronous switch and body diode of main switch processes the negative power flow. Both operating modes are symmetrical, which is being a distinct advantage for bidirectional power flow without extra control circuits.

III. PRACTICAL ISSUES OF CONVENTIONAL CMS, AND THE PROPOSED SLA METHOD

Fig. 6 shows the equivalent model of the three-phase grid-connected differential inverter. The proper connection is validated by integrating grid inductance L_{gx} between each SEPIC converter and the connecting phase of the grid as shown in Fig. 2. Whereas, R_{gx} represents the DC resistance of the grid inductor.

According to Fig. 6, the output voltages and currents of SEPIC converters are related as follows:

$$i_{sx}(t) = \frac{v_{ox}(t) - e_{sx}(t)}{L_{gx} + R_{gx}} \tag{11}$$

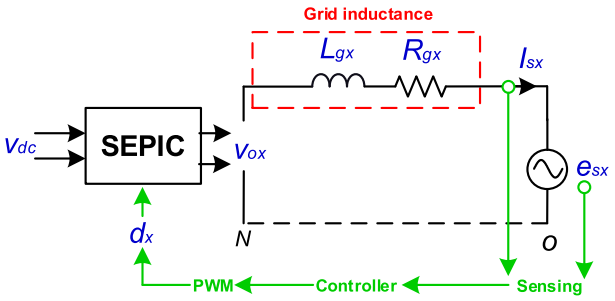


FIGURE 6. Equivalent model of three-phase differential inverters and the basic idea of their control technique implementation.

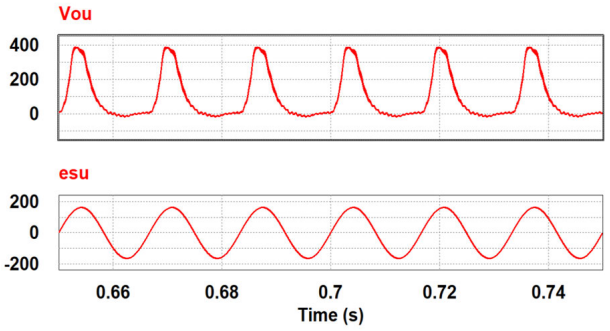


FIGURE 7. Simulation results of the output voltage and grid voltage of one SEPIC at SEPIC-BDI using CMS.

As clarified above, the output voltage amplitude of the SEPIC converter is divided between the AC and DC components. Then, (11) can be rewritten as follows:

$$i_{sx}(t) = \frac{0.5v_{ox}(t)}{L_{gx} + R_{gx}} \tag{12}$$

From (12), it can be seen that the grid current control of the differential inverter cannot be achieved by comparing the reference signal of grid current with the sensed one. However, it needs a pure output voltage waveform of each SEPIC converter that is greatly matched with the gird voltage waveform. Therefore, any distortion on the output voltage amplitude is reflected to the grid current even with using robust control techniques. The main reasons of this distortion can be summarized as follows:

- The nonlinear dynamic response between the output voltage and the sinusoidal duty cycle that is generated by CMS.
- The small non-minimum phase response, which is being produced due to the existence of complex right half plane (RHP) zeros of the SEPIC converters as proven in [41], [42].
- The mismatch between the three paralleled SEPIC converters especially when (3) is not achieved.

In this work, the aforementioned issues and NSHC are addressed by proposing generic static linearization approach and improved design methodology for SEPIC converter. Fig. 7 shows the simulation results for the output voltage waveform of SEPIC-BDI using CMS modulation. There is a significant mismatch between the waveforms of output voltages and the grid voltage waveforms. The reason for this mismatch is the dynamic behavior of the SEPIC passive elements (inductors and capacitors), which is generated by the sinusoidal duty cycle d_x waveform. According to the simulation results, low-order harmonics at the 2^{nd}, 3^{rd}, 4^{th} and 5^{th} order exist in the output voltage. This mismatch is reflected on the grid current and hence the total harmonics distortion (THD) is increased in accordance. This practical issue needs an internal controller for the output voltage modulation with several control loops, which increase the control complexity and affect the inverter stability.

A linearization strategy has been proposed in [21] by adding $F(\phi)$ for buck-boost based differential inverter. However, this strategy cannot be considered as a straightforward solution. A more proper solution can be done by comparing the characteristics of buck and buck-boost converters and conventional CMS modulation. The voltage gain of the buck converter is given as:

$$\frac{v_{ox}}{V_{dc}} = d_x \tag{13}$$

From (13), the gain of a buck-based differential inverter is similar to the modulation index of VSI as illustrated in (1). Therefore, by merging the corrected voltage ratio of the SEPIC converter, the mismatch issues can be eliminated. It can be expressed as follows:

$$\begin{aligned} d_x &= m = \frac{v_{ox}}{V_{dc}} \quad \text{for buck converter} \\ d_x &= \frac{v_{ox}}{v_{ox} + nV_{dc}} \quad \text{for isolated SEPIC converter} \end{aligned} \tag{14}$$

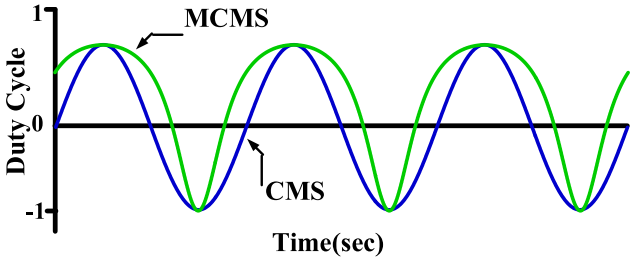


FIGURE 8. Comparison between conventional CMS and the proposed MCMS schemes for SEPIC-BDI.

It can be seen from (14) that the proposed modified CMS modulation (MCMS) is capable of achieving the static linearization approach by merely integrating the SEPIC converter's duty cycle calculation in CMS modulation. Therefore, no additional control loops are required for the previously addressed low-order harmonics in Fig. 7. Fig. 8 shows the difference between the conventional CMS and the proposed MCMS PWM modulation. Furthermore, Fig. 9 shows the simulation results for the output voltage waveform of

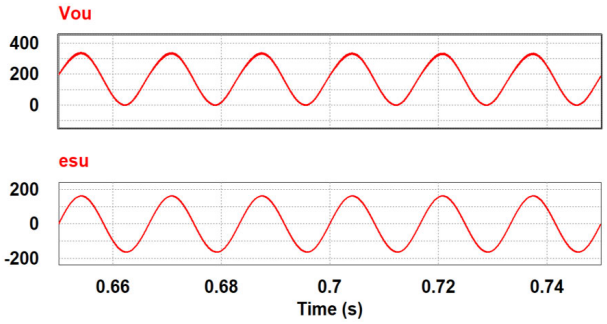


FIGURE 9. Simulation results of the output voltage and grid voltage of one phase leg of SEPIC-BDI using proposed MCMS.

SEPIC-BDI using MCMS modulation. It is worth mentioning that all low-order harmonics are mitigated and the matches between the output voltage of SEPIC and the grid voltage are high. This concept has been developed also in [37], [38], however, the implementation steps of the static linearization function are not explained. Moreover, the developed methods in [39], [40] use static linearization block based on the voltage ratio of Cuk converters, however, this proposal needs a feedforward signal of the input source. In this work, the proposed MCMS implementation provides a different application as it does not need any feedforward signals, which reflects its simplicity and applicability.

IV. PROPOSED ENHANCED DESIGN METHODOLOGY OF SEPIC ELEMENTS

A 1.6 kW case study has been established using SEPIC-BDI converter integrated with three-phase grid of 200 V line-line voltage (rms) with a DC input voltage source of 100 V. The grid and switching frequencies are selected to be $F_g = 60$ Hz and $F_s = 50$ kHz. Since every SEPIC leg processes one-third of the inverter power, the power and rms output current of single SEPIC leg can be expressed as follows:

$$P_{SEPIC} = \frac{P_{DBI}}{3} = \frac{1600}{3} = 533.33 \text{ W} \tag{15}$$

$$i_{sx} = \frac{P_{SEPIC}}{E_m} = \frac{533.33}{200/\sqrt{3}} = 4.6187 \text{ A} \tag{16}$$

The proposed MCMS requires variable duty cycle so the maximum possible range of the duty cycle of SEPIC converter is selected to be $0.1 \leq d_x \leq 0.8$.

A. LARGE-SIGNAL MODEL

The large-signal model aims to obtaining SEPIC elements based on the desired voltage ripple and current ripple of inductors and capacitors. The average current of the input-inductor and the magnetizing inductance of the SEPIC converter are obtained as follows:

$$\begin{aligned} i_{inx} &= i_{Lx} = \frac{n i_{sx} d_x}{1 - d_x} \\ i_{Lmx} &= n i_{sx} \end{aligned} \tag{17}$$

Similarly, the average voltage of the coupling capacitor and the output capacitor are obtained as follows:

$$\begin{aligned} V_{Cx} &= V_{dc} \\ V_{Cox} &= V_{ox_m} = 2E_m \end{aligned} \tag{18}$$

Large inductors and capacitors can achieve small ripple components, as indicated in (19) and (20), however it increases the inverter size and hence it has severe limitations.

$$\begin{aligned} L_x &\geq \frac{d_x V_{dc}}{2\Delta i_{Lx} F_s} \\ L_{mx} &\geq \frac{d_x V_{dc}}{2\Delta i_{Lmx} F_s} \end{aligned} \tag{19}$$

$$\begin{aligned} C_x &\geq \frac{n i_{sx} d_x}{2\Delta V_{Cx} F_s} \\ C_{ox} &\geq \frac{n i_{sx} d_x}{2\Delta V_{Cox} F_s} \end{aligned} \tag{20}$$

In this paper, the authors prioritize the converter size by choosing small passive elements with small parasitic components. Nevertheless, the variable duty cycle of SEPIC-BDI introduces variable voltage and current ripples as well. The duty cycle range limits the ripple window of voltage and current. The critical limits exist at the highest duty cycle of the inverter. At $d_x = 0.8$, the percentage of peak to average value of current ripples in input-inductor L_x and magnetizing inductance of HFT L_{mx} are assumed to be 20% and 30%, respectively. This assumption is acceptable for a small inverter with fair efficiency because the higher ripple increases the conduction losses and deteriorates inverter efficiency [46]. The percentage of the peak to average value of voltage ripple in coupling capacitor C_x and output capacitor C_{ox} is assumed to be 5% to provide grid current with acceptable THD. Therefore, L_x=153 μH and L_{mx}= 408μH are obtained using (19) and (20). Also, C_x and C_{ox} are attained in the same manner and they equal to 10 μF, 3.2 μH, respectively.

B. SMALL-SIGNAL MODEL

The SEPIC topology represents a buck-boost converter with four passive elements and they determine the dynamic response of the SEPIC-BDI. The open-loop control-to-output transfer function can be represented as follows:

$$G_{vd}(s) = \frac{v_{ox}(s)}{d_x(s)} = G_0 \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{21}$$

where, G_0 represents the dc-gain of SEPIC, a_o-a_3 represent the zeros constants, and b_o-b_3 are the poles constants. Fig. 10 shows the root locus of (21) at $d_x = 0.1 - 0.8$. The transfer function has two complex poles and one complex zero at the left-half plane in addition to a single RHP zero. It demonstrates a non-minimum phase response and limits the inverter bandwidth to less than the worst-case frequency (1.7 kHz). Due to the differential operation, the poles and zeros move simultaneously at the grid-frequency cycle. This strolling adds a new challenge for the inverter control because the complex zeros move towards the right half-plane, especially at high duty cycles. For example, at d_x=0.8, the complex RHP

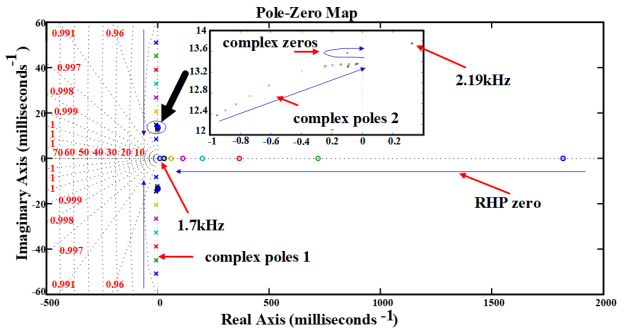


FIGURE 10. Pole-Zero map of open-loop transfer function at d_x = 0.1 - 0.8.

zeros is located at 2.19 kHz. In this case, the total phase delay equals to 630^o and the mismatch between output voltage and grid voltage increases. Consequently, the control requires high-order compensator or non-linear controllers to decrease non-minimum phase response and to get a stable performance as demonstrated in [22], [41].

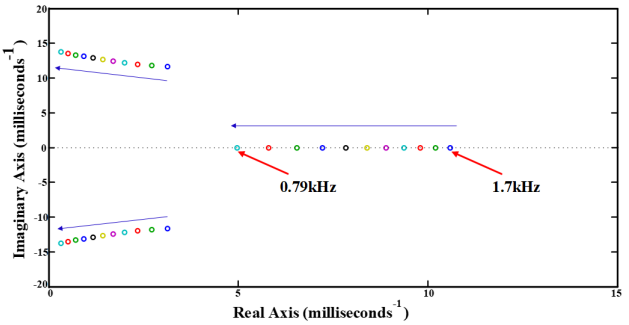


FIGURE 11. Pole-Zero map of d_x = 0.8 at different inductor DC resistance R_{dcr}=0-1Ω with 0.1 Ω step.

C. PROPOSED ENHANCED DESIGN METHODOLOGY

Although high-order compensator and nonlinear controllers can provide an improved performance for SEPIC converter in several applications, they require high computational burdens and/or analog controllers. They can also increase the cost and complexity of the SEPIC-DBI. On the other hand, increasing the parasitic resistance of the utilized SEPIC moves the complex RHP zeros from the right half-plane toward the left half-plane, as shown in Fig. 11. It shows also the root locus of the utilized SEPIC converter at different DC resistances of the input-inductor L_x. The DC resistance is changed from 0 Ω to 1 Ω with a 100 mΩ step. Although the RHP complex zeros move toward the left-half plane, 1 Ω parasitic resistance is still insufficient to cross the left half-plane. Besides, the high DC parasitic resistance limits the bandwidth by decreasing the single RHP zero frequency from 1.7 kHz to 0.79 kHz. This method reduces the voltage gain of the SEPIC and the static gain of the SEPIC-BDI. Also, it deteriorates the inverter efficiency in addition to limiting the controller bandwidth.

Alternatively, the proposed enhanced strategy is carried out by changing L_{mx} and L_x ratio without violating the large-signal model. Fig. 12 shows the root locus when L_x= 153μH is changed from 410 μH, and L_{mx} is changed from 450 μH - 700μH with a 50 μH step. It is worth noticing that the complex RHP zeros are moving toward the left half-plane, especially at higher values of L_{mx}. It is ultimately moved again to the left half-plane at 650 μH and 700 μH. Also, increasing L_{mx} has a small effect on the single RHP zero location, where it is just changed from 1.68 kHz to 1.61 kHz.

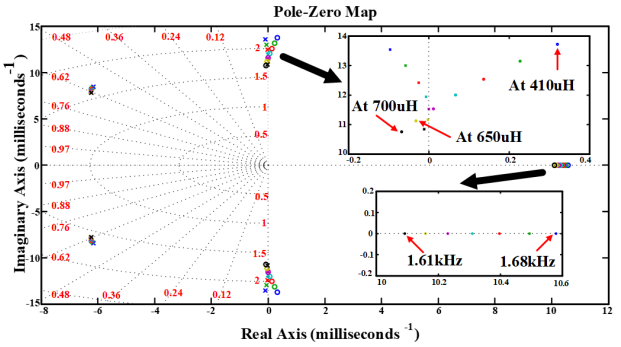


FIGURE 12. Pole-zero map at d_x=0.8 for magnetizing inductance changing from 410 μH and 450-700 μH with 50μH step.

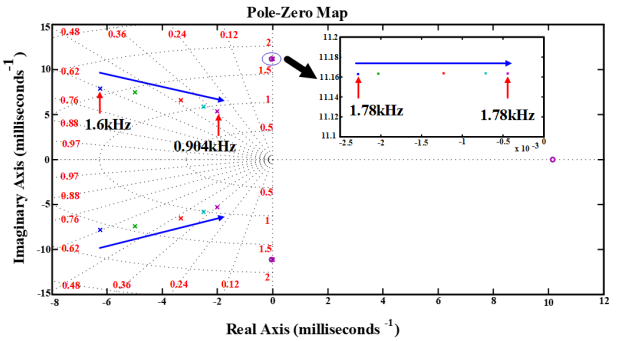


FIGURE 13. Pole-zero map at d_x=0.8 for output capacitance changing from 3.2 μF and 4-10 μF with 2 μF step with constant coupling capacitor of 10 μF.

From Fig. 12, it is better to increase the magnetizing inductance L_{mx} from 408 μH to 650 μH. It can completely mitigate the harmful effects of complex RHP zeros. The new L_{mx}=650 μH has a close bandwidth to the old one. Fig. 13 shows the effect of increasing the value of C_{ox}. The first complex poles are only changed with a resonance frequency between 1.6 kHz to 0.904 kHz, where the other poles and zeros remain constant. All the obtained values are acceptable because the poles frequency is still higher than 20-30% of RHP zero frequency. Fig. 14 shows the pole-zero map of the SEPIC converter at higher values of C_x. It can be seen that the coupling capacitor affects directly the second complex poles and the complex zeros. It does not affect the first complex poles and single RHP zero. From Fig. 14, the value

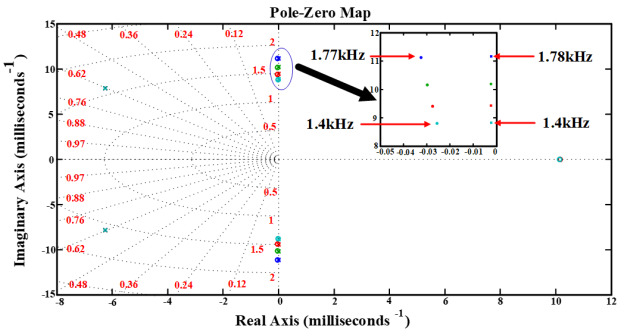


FIGURE 14. Pole-zero map at $d_x = 0.8$ for coupling capacitor changing from 10 μF to 16 μF with 2μF step ans constant output capacitor of 3.2 μF.

TABLE 2. Final selected parameters of the proposed SEPIC-BDI.

Circuit parameters	Symbols	Value
Output power	P	0.2-1.6 kW
Input DC voltage	V_{dc}	100-120 V
Grid voltage, L.L	E_{suv}, E_{svw}, E_{swu}	200 V
Grid frequency	F_g	60 Hz
Switching frequency	F_s	50 kHz
Input inductance	L_x	153 μH
HFT inductance	L_{mx}	650 μH
HFT turns ratio	n	1
Coupling capacitor	C_x	14 μF
Output capacitor	C_{ox}	3.3 μF
Grid inductance	L_{gx}	4 mH

of C_x=14 μH is better as it has acceptable resonant frequency and smaller ripple for the capacitor voltage. It is interesting to interpret that the parasitic DC resistances of inductors and capacitors are assumed zero to decouple between the proposed enhanced design methodology and the traditional solution, which improves the dynamic response of the SEPIC converter by increasing the parasitic resistances [47]. Then, the actual parasitic resistances of the proposed SEPIC converter augments the stability of the SEPIC-BDI. Table. 2 shows the final selected parameters of the SEPICs using the proposed enhanced design strategy.

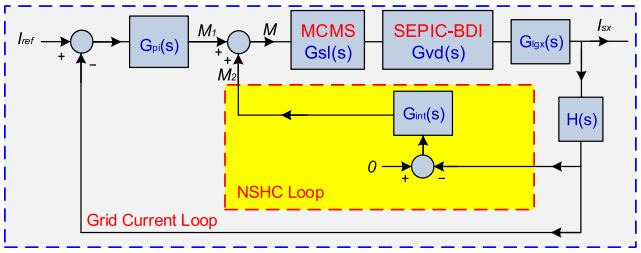


FIGURE 15. Control blocks of the proposed SEPIC-BDI.

V. PROPOSED IMPROVED CONTROL TECHNIQUE

Fig. 15 shows the block diagram of the proposed improved controller for SEPIC-BDI. It realizes the control function using two control loops and the proposed SLA method. The first loop regulates the grid-current to follow the sinusoidal reference signal, whereas the second loop compensates the NSHC. Referring to Fig. 6, the transfer function of grid inductance is given as follows:

$$G_{Lgx}(s) = \frac{i_{sx}(s)}{v_{ox}(s)} = \frac{0.5}{L_{gx}s + R_{gx}} \tag{22}$$

Accordingly, the SLA is implemented using control block $G_{Lgx}(s)$. The input is the static gain of SEPIC-BDI and the output is the duty cycle for SEPIC converters. Solving equations (2) and (14), the duty cycle of first SEPIC is obtained as follows:

$$d_u(t) = \frac{E_{dcu} + E_m \sin(\omega t)}{E_{dcu} + E_m \sin(\omega t) + nV_{dc}} = \frac{0.5}{L_{gx}s + R_{gx}} \tag{23}$$

Since both components of SEPIC are equal and they depend on the value of M, then (23) can be rewritten as follows:

$$\begin{aligned} d_u(t) &= \frac{V_{dc}nM(1 + \sin(\omega t)}{V_{dc}nM(1 + \sin(\omega t) + nV_{dc}} \\ &= \frac{M(1 + \sin(\omega t)}{M(1 + \sin(\omega t) + 1} \\ &= \frac{M_u(t)}{M_u(t) + 1} \end{aligned} \tag{24}$$

Therefore, the transfer function of the SLA method is expressed as follows:

$$\begin{aligned} D_u + d_u(s) &= \frac{M + m_u(s)}{M + m_u(s) + 1} \\ &= \frac{M}{M + m_u(s) + 1} + \frac{m_u(s)}{M + m_u(s) + 1} \end{aligned} \tag{25}$$

where, $m_u(s)$ represents the small signal of the static gain of SEPIC-BDI. Using only small signal part of (25), the small-signal of the proposed MCMS is obtained as follows:

$$G_{SL}(s) = \frac{m_u(t)}{M + 1} \tag{26}$$

It is worth mentioning that the implementation of the proposed MCMS, as shown in (25) and (26), does not require feedforward signal from the input voltage. Moreover, its implementation is more simple as in the conventional VSI, where, the single parameter M controls the output of differential inverter. The transfer function of SEPIC has a fourth-order dynamic model with one RHP zero due to the developed enhanced design strategy. Therefore, simple PI control is sufficient to validate the bandwidth beyond 20% to 30% of the RHP and to achieve grid current control as well. Therefore, the transfer function of the controller is based on the traditional PI control and it is expressed as follows:

$$G_{pi}(s) = K_p + \frac{K_i}{s} \tag{27}$$

The PI controller modulates the error between the actual grid-current and reference value, wherein the output of PI compensator is expressed by M_1. In the second loop, the output current of the proposed inverter to the utility grid is sensed and compared with zero to eliminate NSHC. Then,

an integrator $G_{int}(s)$ is designed to modulate the error and results the output M_2. Finally, both components are added to obtain the final static gain of each SEPIC as follows:

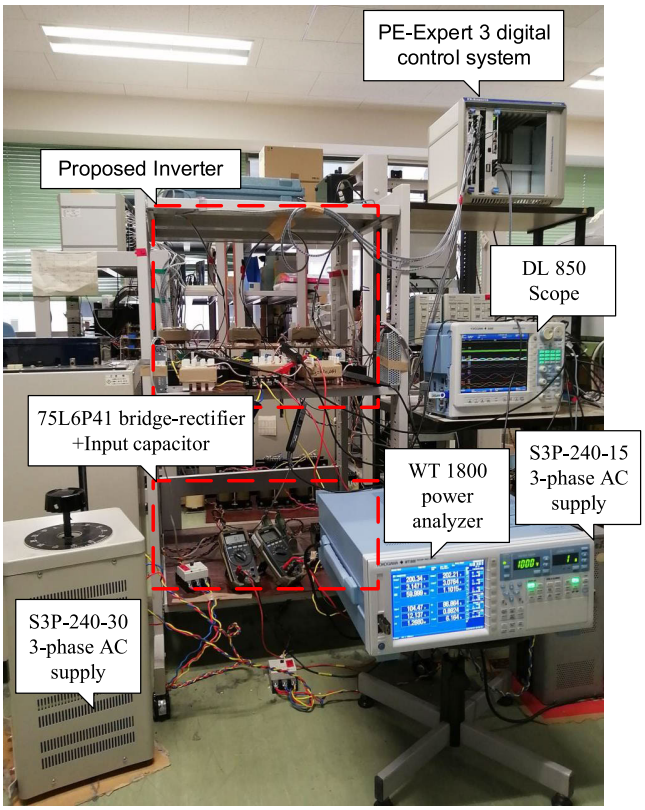
$$M = M_1 + M_2 \tag{28}$$

VI. EXPERIMENTAL RESULTS AND DISCUSSION

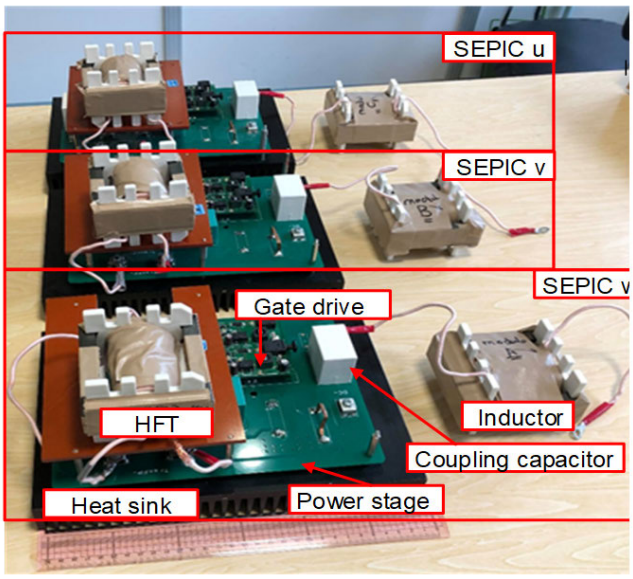
Fig. 16 describes the experimental test setup of the SEPIC-BDI. The system components and measurements are based on the inverter shown in Fig. 2. The setup uses a 3-phase AC supply (S3P-240-30) with 0-240 V and 10.4 kVA rating. This AC supply is connected to a six-diode bridge-rectifier (75L6P41) followed by 6000 μF to provide pure variable DC voltage to emulate the time-variant characteristics of renewable energy sources. Another variable 3-phase AC supply (S3P-240-15) with voltage range between 0-240 V and 5.2 kVA rating is used to represent the grid side. The voltage, current and power analysis are recorded experimentally using Yokogawa DL850 Scope and Yokogawa WT 1800 power analyzer. The LA55-P and LV25-P are employed for sensing the grid line-to-line voltages and the three-phase currents, respectively. The experimental setup is also shown in Fig. 16. The SEPIC inverter is implemented using three separate power stages to provide a modular inverter. The gate drive of each SEPIC is designed on the same power stage for independent control. Isolated DC-DC converter (ISE0524A) from XP power is integrated into the designated gate drive to form gate isolation. It is a cost-effective solution in driving low-side (main switch) and high-side (synchronous switches) using the same driver chip. A high-performance SiC power MOSFET (C2M0040120D) is used for both switches.

The input inductor and HFT are implemented using an inexpensive ferrite core (EER-94) and Litz wire with a bobbin 0.198 and conductor resistance ((3.14 $m\Omega/m$)). It provides efficient elements with low-cost and hence better performance can be obtained. The coupling capacitor is a film capacitor (C4AEOBW5140A3JJ) with 900 V and 14 μF to enhance the reliability of the proposed inverter. The output capacitor is also a film capacitor (C4AEQBU4330A11J) with 900 V and 3.3 μF. The snubber circuit is designed based on previous capacitor, 4.7 kΩ resistance and diode. The input capacitance is selected to be 120 μF and implemented by four paralleled film capacitors (C4AEHBW5300A3JJ). The details of the experimental parameters are illustrated in Table. 3 and Table. 4. The control technique is realized using PE-Expert 3 digital control system. It is embedded with TI high-speed floating-point DSP TMS320C6713. The MWPE3 Xilinx FPGA board (XC3S500E) is linked with the DSP board for generating the gating pulses of power switches with a 50 kHz carrier frequency. Table. 5 illustrates the control parameters of the employed experimental setup.

Fig. 17 illustrates the experimental results at V_{dc}= 100 V and 120 V, respectively. The input current is continuous with a minimal switching ripple. As the SEPIC-BDI is operated by a variable duty cycle, the input and output currents of the utilized SEPIC converters vary periodically with the grid



(a) Setup



(b) Prototype

FIGURE 16. Experimental setup and prototype of the SEPIC-BDI.

frequency. The injected grid current is synchronized with grid voltage and introduces pure active power with a unity power factor. Fig. 18 shows the duty cycles of the three inverter legs and the static gain of differential inverter at V_{dc}=100 V and P=1.6 kW. The signal of d_x is compared with a (-1:1) sawtooth signal having 50 kHz switching frequency to generate the switches pulses. The symmetrical duty cycles

TABLE 3. Experimental parameters of magnetic elements of SEPIC-BDI.

Component	Parameters	Value
Input inductor	Inductance L_x	158.8, 155.7, 160μH
	Core type	EER-94
	Core material	MB4, ferrite
	No. of windings	35
	DC resistance R_{dcr}	180mΩ
HFT	Magnetizing L_{mx}	663.2, 659.2,673.4μH
	leakage Inductance	5.11, 5.37, 5.4μH
	Core type	EER-94
	Core material	MB4, ferrite
	No. of windings (pry, sec)	15, 15
	R_{on} (pry, Sec)	40mΩ, 45mΩ

TABLE 4. Experimental parameters of switches and passive elements of proposed SEPIC-BDI.

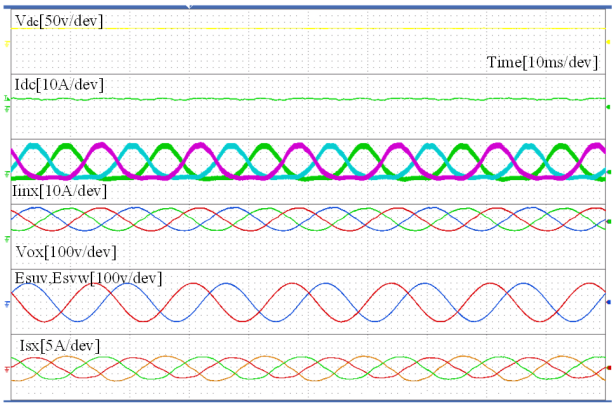
Component	Parameters	Value
Switches	Part number	C2M0040120D
	On resistance	40mΩ
	Forward voltage	1.8 V
	Rise and fall time	52ns, 3ns
Capacitors	Part number, C_x	C4AEHBW5300A3JJ
	ESR (C_x)	3.6mΩ
	Part number, C_ox	C4AEQBU4330A11J
	ESR (C_ox)	11.2mΩ
Snubber circuit	Snubber Capacitor	C4AEQBU4330A11J
	ESR (snubber capacitor)	11.2mΩ
	diode	SCS220AG
	Resistance	AP821
Grid inductor	Inductance L_{gx}	4mH
	Resistance of L_{gx}	200mΩ

TABLE 5. Control parameters of experimental setup.

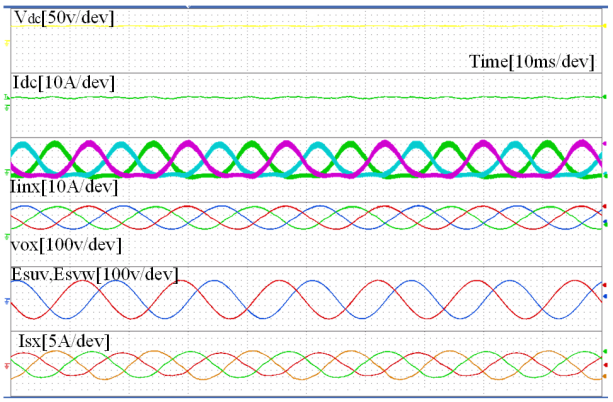
Controller	Parameters	Value
Controller 1 (PI)	K_p	0.002
	K_i	1×10^{-6}
Controller 2 ($\int$)	Gain	1
	Frequency	1×10^{-4}

and constant static gain indicate the high performance of proposed MCMS method.

Fig. 19 shows the FFT analysis of the obtained experimental grid-current at different input DC voltages and 1.6 kW output power. The proposed improved controller enhances the waveforms by reducing the NSHC to diminutive values. The maximum percentage of NSHC is less than 0.7% and it is decreased at higher DC voltage values. Fig. 19d shows the THD of the grid-current at different power. At full power, the THD is 4.25%, 4.11%, and 3.26% at DC voltages of 100 V, 110 V, and 120 V, respectively. The THD is lower than 5% at various DC voltages and load conditions with only two exceptions at 100 V DC with loads 200 W and 300 W. Table. 6 illustrates the DC offset of the grid current, which are resulted from SEPIC converters mismatch. It can be seen that this percentage is small as it is measured at V_{dc}= 100 V to be 0.422%. Moreover, this value is reduced to be less than 0.1% at V_{dc}= 120 V. Furthermore, the third-order harmonics of the input current for the first SEPIC is also measured. Its maximum value is 3.938% at V_{dc}= 110 V.



(a) V_{dc}=100 V



(b) V_{dc}=120 V

FIGURE 17. Experimental results of the proposed SEPIC-BDI at different input voltages.

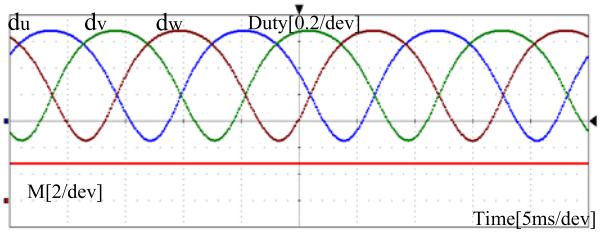


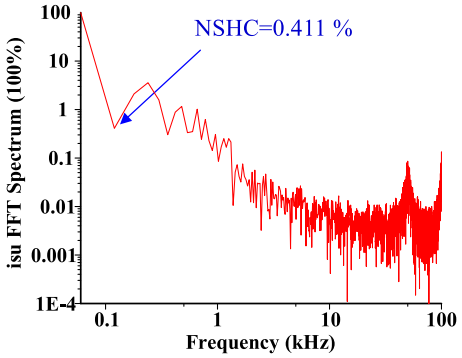
FIGURE 18. Duty cycle and static gain *M* of proposed SEPIC-BDI at V_{dc}=100 V.

TABLE 6. DC offset and third-order harmonics of SEPIC-BDI.

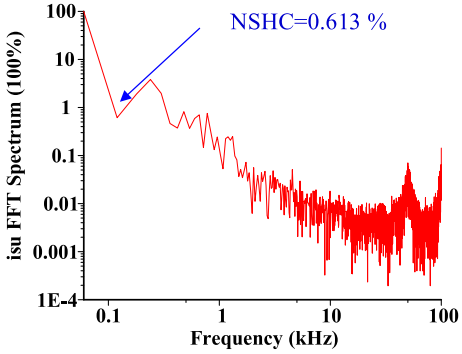
DC voltage	DC component of i_{su}	3rd harmonic component of i_{inu}
V_{dc}=100 V	0.422	3.584
V_{dc}=110 V	0.147	3.938
V_{dc}=120 V	0.0189	3.17

This small percentage is achieved due to the successful operation of proposed SLA and proposed MCMS method.

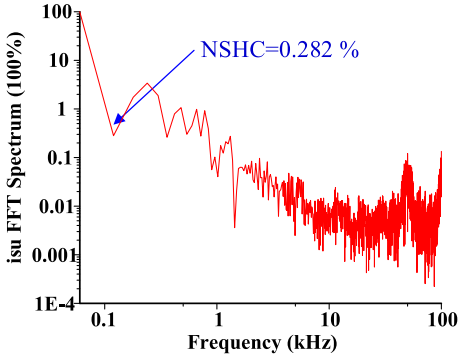
The voltage and current of the primary and synchronous switch are measured experimentally to check the voltage and current stress as illustrated in Fig. 20a. It can be seen that



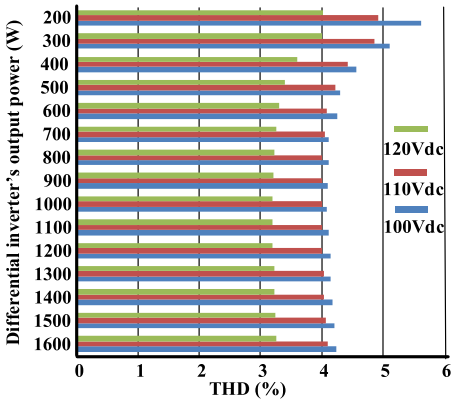
(a) V_{dc}=100 V



(b) V_{dc}=110 V



(c) V_{dc}=120 V



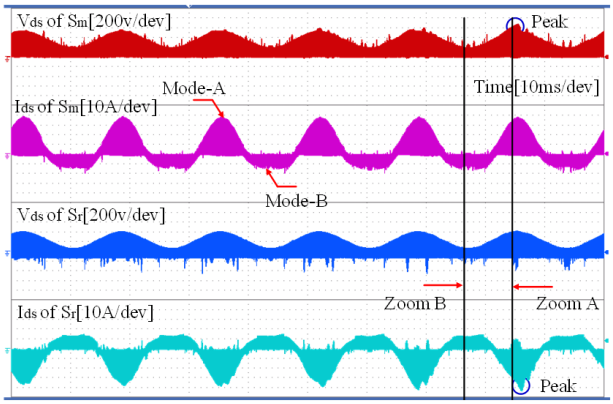
(d) THD

FIGURE 19. FFT grid-current and THD at different conditions.

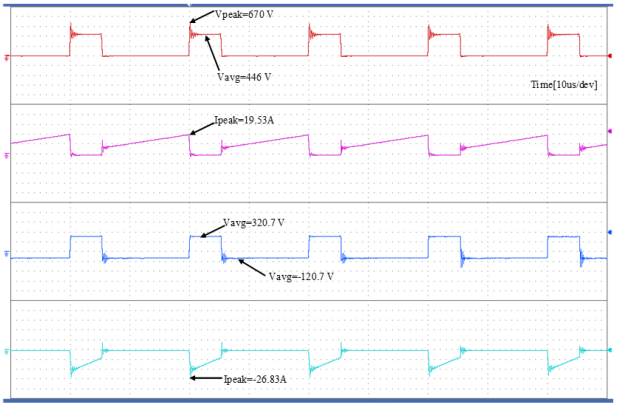
both switches operate according to the proposed controller and the various operating modes (mode-I and mode-II) are obtained in accordance. The inverter is capable of managing the forward and circulating power efficiently. The maximum peak voltage of power switches equals to 688 V (blue circle), including the drain-source voltage, voltage ripple component and the damped voltage spikes of leakage inductance at HFT. The maximum current is obtained at the body diode of the synchronous switch and it equals to 40.4 A. Both voltage and current peaks are limited successfully under the predetermined limits because of the snubber circuit, which damps it out under the safe operation zones of the utilized switches. Fig. 20b shows the switches operation at Mode-I by zooming-in the results from Fig. 20. The instant duty cycle at this voltage is 0.75. It is validated that the main switch and body diode process the forward power. Fig. 20c shows the switches operation at mode-II by zooming the results from Fig. 20. The instant duty cycle at this voltage is 0.32. The reverse power is diverted by the synchronous switch and body diode of the main switch. Finally, Fig. 20b,Fig. 20c show the effective operation of both switches at the switching frequency.

Fig. 21a shows the voltage and current of input inductor and HFT at grid-frequency and switching-frequency. Both magnetic elements operate simultaneously and achieve mode operations (mode-I and mode-II). They manage forward and reverse power by charging and discharging states. The maximum peak voltage and the maximum current of the input inductor are 670 V and 28.3 A, respectively. The maximum peak voltage and the maximum current of HFT are 570 V and 31 A. It can be seen that these worst-case of voltages and current conditions that include the average values, ripple components, and switching voltage and current spikes are under the saturation limits set during the design process of magnetic elements. Fig. 21b shows the voltage and current waveforms at Mode-I by zooming-in Fig. 21. The instant duty cycle at this voltage is 0.75. It can be seen that the input voltage of the inductor equals to the input DC voltage and the primary voltage of HFT at charging and discharging states, respectively. Fig. 21c shows the voltage and current waveforms at mode-II by zooming-in Fig. 21. The instant duty cycle at this voltage is 0.365. The inductor current in both charging and discharging states is negative, which indicates the reverse power processing. Fig. 21b, and Fig. 21c show the tight operation of input inductor and HFT at the switching frequency. The obtained results prove the accuracy of the proposed design criteria of the SEPIC-BDI.

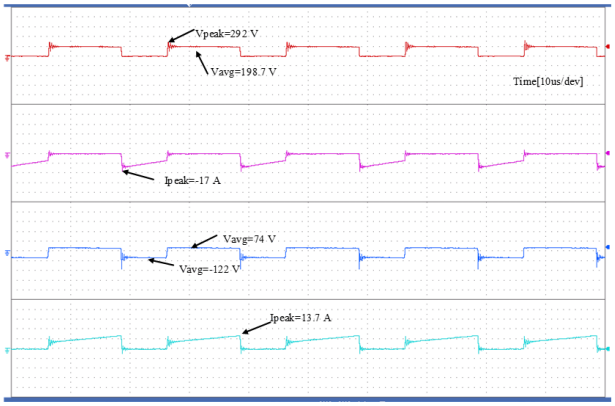
Fig. 22 shows the measured efficiency profile of the SEPIC-BDI at different DC input voltages (100 V,110 V and 120 V) for output power variations between 0.2 kW and 1.6 kW. The measured efficiency range considers the possible voltage and current variations of different renewable energy applications. It can be noted that the efficiency increases linearly at higher DC input voltages, especially at output power ranges higher than 0.6 kW. The maximum efficiency of the proposed differential inverter is 90.12% at 700 W, which is higher than the efficiency (87.99%) at full rated power (1.6 kW).



(a) Full waveforms

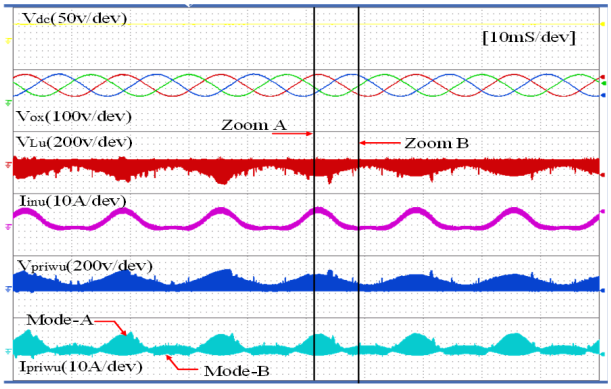


(b) Zoom A

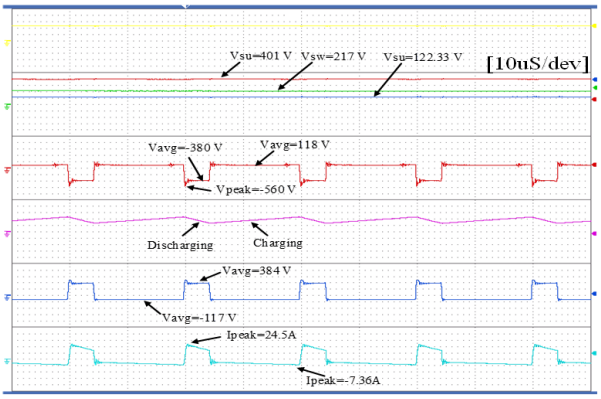


(c) Zoom B

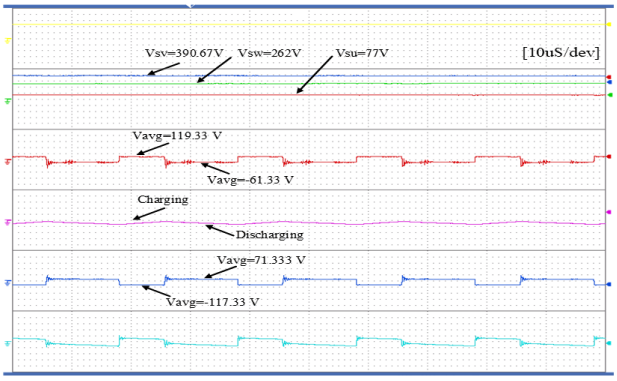
FIGURE 20. Switches voltage and current Stress of SEPIC-BDI.



(a) Full waveforms



(b) Zoom A



(c) Zoom B

FIGURE 21. Voltages and currents of magnetic elements at SEPIC-BDI.

Fig. 23 shows the power-loss distribution of the enhanced SEPIC-BDI at different DC input voltages for full output power (1.6 kW). This loss-division is calculated by modeling the parameters of utilized components such as MOSFET devices, magnetic elements (input inductor and HFT), capacitors, and other components under the developed method. These parameters are obtained from the relevant datasheets, as shown in Table. 3 and Table. 4. The dominant power losses for V_{dc}=100 V are associated with HFT with 29.19%. The power losses of the input inductor and switches are 27.9% and 26.95%, respectively. The rest of the power losses is generated from grid-inductance, snubber circuits, control circuit, and wiring, giving a total of about 15.88% share. It is worth mentioning that the power losses of the main switches represent 17.05% share, which are being larger than those of synchronous switch 9.9% due to its operation during Mode-I. The voltage and current peaks in this mode are higher than of mode-II. The power losses of capacitors are lower than 1% due to the small ESR resistance of utilized film

TABLE 7. Comparison between SEPIC-BDI and other three-phase boost inverter topologies.

Reference	Topology	Power (KW)	C	L	S	D	Control	HFT	CMV	THD	Efficiency
Ref [48]	Two-stage (boost+VSI)	6.5	1	1	6	1	PWM	No	No	5%	NA
Ref [49]	Two-stage (LLC+VSI)	0.4	2	0	10	0	PWM+ZVS	Yes	Yes	5%	95.5%
Ref [50]	HFT-based H-bridge	NA	0	0	24	0	CSVPWM	Yes	Yes	NA	NA
Ref [16]	Z-source	0.45	2	2	6	1	FCS-MPC	No	NA	NA	NA
Ref [17]	Split-source	2.0	1	1	6	3	MSVPWM	No	No	NA	NA
Ref [51]	Switched Capacitor	NA	2	0	8	2	SVPWM	No	Yes	0.7%	NA
Proposed	Differential	1.6	6	3	6	0	MCMS	Yes	Yes	4.25%	90.12%

C = Capacitors, L = inductors, S = Switches, D = Diodes, and NA = Not Available

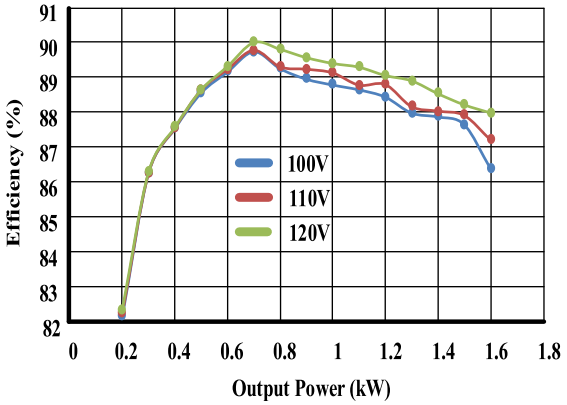
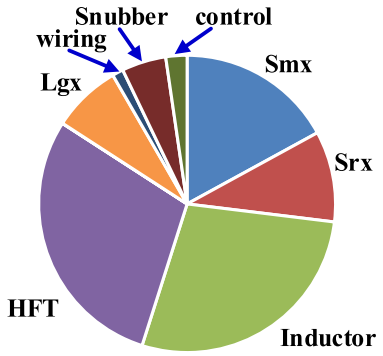
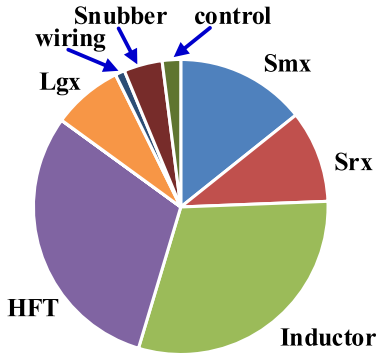


FIGURE 22. Experimental measured efficiency of the proposed SEPIC-BDI.



(a) V_{dc}=100 V



(b) V_{dc}=110 V

FIGURE 23. Power-loss distribution of SEPIC-BDI at full power and different input DC voltage conditions.

capacitors. For higher DC input voltage, the power loss of HFT increases to about 29.9% and 30.43%, and the inductor losses increase to 29%, and 30.24%, whereas the power losses in the main switches are reduced to about 25.54% and 24.83%, at V_{dc}=110 V and V_{dc}=120 V, respectively.

Table. 7 provides a short comparison of the proposed SEPIC-BDI with other three-phase boost inverter topologies. The considered topologies in the comparison include two stage converters based on boost topology [48] and LLC topology [49], HFT-based H-bridge topology [50], Z-source inverter [16], split source inverter [17], and switched capacitor topology [51]. The proposed topology has only six switches as in the traditional VSI topologies. Moreover, the performance of capacitors and inductors of utilized SEPIC converters in this topology are enhanced in this paper. For instance, the inductors are lower, and the utilized capacitors are film capacitor types. Moreover, this topology provides isolation and CMV elimination using the same set of components and small HFT. It is worth mentioning that conventional boost inverters need many switches to develop isolation, as illustrated in references [49] and [50]. Finally, the proposed enhanced control is simple and did not need power control kits for implementation.

VII. CONCLUSION

An enhanced design methodology and improved controller for three-phase SEPIC-BDI inverter have been proposed for grid-connected renewable energy applications. Additionally, this paper presented a generalized method based on the static linearization approach (SLA) for mitigating the low-order harmonic components, which are usually inherent by differential inverters. The superiority and effectiveness of the proposed controller and SEPIC-BDI inverter system are validated using simulation and experimental results at voltage range (100-120 V) and power range (0.2-1.6 kW). By using the proposed SLA method with the SEPIC-BDI system, the mismatch effects between the different SEPIC converters are alleviated and the DC offset components in the output currents are eliminated. Moreover, by selecting the converter parameters based on the proposed enhanced design methodology, more stable operation can be obtained by moving the complex RHP zeros to the LHP. Therefore, a simple PI controller is needed to maintain converter stability compared to the required nonlinear controllers and high order compensator types in the existing methods in the literature.

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