IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 30, 2021, accepted April 4, 2021, date of publication April 9, 2021, date of current version July 12, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3072161

Research on Multi-Port DC-DC Converter Based on Modular Multilevel Converter and Cascaded H Bridges for MVDC Applications

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ABSTRACT Aiming at the low-voltage DC distribution network system and combining the characteristics of F2F structure and ISOP-DAB structure DC transformer, this paper proposes a DC transformer structure based on modular multilevel converter (MMC) and cascaded H-bridge. First of all, this paper analyzes several different cases. Case 1 proposes a type of equal carrier-phase-shift pulse-width modulation (CPS-PWM) of MMC, which can produce an equal five-level voltage waveform. In the meanwhile, another unequal CPS-PWM control is proposed to produce an unequal five-level voltage waveform. According to the descriptions of case 2, the quasi-square-wave-modulation method with a wide gain range can greatly reduce the insulation design difficulty of the intermediate AC side high-frequency transformer and the voltage stress on the AC side. Case 3 demonstrates the extended-phase-shift (EPS) control of three-port DC-DC converter. Combining the voltage sorting algorithm of voltage sequencing and cyclic switching, a strategy of voltage equalization for grouped capacitors is proposed. Considering the various application scenarios of actual working conditions, the soft switching characteristics and multi-port power characteristics of the DC transformer are analyzed. In order to verify the feasibility of the DC transformer structure and its control strategy, a simulation model was built in Matlab/Simulink and the results were verified. The results are in accordance with the theoretical analysis.

INDEX TERMS Cascaded H-bridge, group voltage equalization algorithm, modular multilevel converter, Quasi-square wave modulation.

I. INTRODUCTION

With the development of the economy, the problem of resource shortage and the pressure of environmental degradation have initially become prominent. so the large-scale development of green and sustainable energy is imperative. The application of new renewable energy sources such as water, wind, light, and geothermal are the only way for countries in the world to achieve environmental protection and sustainable economic development. In my country's ''Twelfth Five-Year Plan'', wind power and photovoltaic power generation will account for 3% and 0.4% and 5% and 0.6% respectively by 2015 and 2020 [1]–[3]. For sustainable distributed energy, the DC power distribution system can better access and absorb it.

At present, DC power conversion technology has become a hot research topic in the industry. Internationally, scientific research institutions such as Tokyo Institute of Technology in Japan, Aachen University of Technology in Germany, ABB Company, etc. Domestic universities, enterprises and scientific research institutions such as Tsinghua University, Huazhong University of Science and Technology, and the Institute of Electrical Engineering of the Chinese Academy of Sciences have all implemented DC transformer topology and control methods. Extensive discussions and researches containing topology selection are also implemented [4], [12].

Among the DC transformer topologies currently suitable for high-voltage and high-power applications, the DC transformer topology based on the input series output parallel

The associate editor coordinating the review of this manuscript and approving it for publication was Kan Liu.

(ISOP) structure is the most studied and most mature topology [5], [6].The entire DC transformer is composed of independent DC/DC converters. On the one hand, each converter is connected in series on the input side to bear the higher-level voltage of the medium voltage DC input side. On the other hand, through the parallel connection on the output side, It can split huge power and current equally on the low-voltage side. The most commonly used topology of DC/DC converters is the dual-active-bridge (DAB) converter, which has the functions of DC-DC voltage conversion and bidirectional energy transmission. The two sides of the converter are electrically isolated by the high-frequency transformer (HFT). The main problems of the DC transformer with this structure are the difficulty of high-frequency transformer insulation design, the voltage mismatch with DC bus voltage fluctuations and the low reliability caused by the concentrated capacitance on the series side.

For MMC side, the most common used control method is carrier phase-shift pulse-width modulation (CPS-PWM) method, which poses phase displacement among different carriers. Through the comparisons between reference wave and carriers, the trigger signals of corresponding SMs are produced.

For the connection between medium and high voltage DC buses, some researchers have proposed a DC transformer with a face-to-face structure (F2F) based on Modular Multilevel Converter (MMC) [11], [12]. Modular multilevel converters have the characteristics of easy expansion, simple redundant design, and high maintainability. They have been widely used in high-voltage direct current transmission systems. In high-voltage and high-power DC conversion occasions, MMC also has greater advantages. However, in the case of medium-voltage and low-voltage power distribution levels, the structural characteristics of MMC will lead to a great increase in cost and losses [14]–[18], [19], [20]–[22].

Combining the advantages and disadvantages of MMC and ISOP-DAB structure, this article adopts a structure based on MMC and cascaded H bridge for medium and low voltage DC distribution network, as shown in Fig.1. The medium voltage side of this structure bears the voltage of the medium voltage level through the MMC. It improves the reliability of the equipment. The low-voltage side is connected in series on the AC side through multiple cascaded H-bridges to adapt to the low-voltage bus voltage and larger current. On this basis, this article adopts a quasi-square-wave-modulation strategy with a wide gain range, which can effectively improve the power transmission characteristics of the DC transformer. At the same time, a module voltage equalization strategy combining voltage sequencing and switch table cycle is proposed to improve its voltage equalization effect [19]–[21].

Compared with conventional DAB output port, there are many advantages of output parallel (OP) structure.

When energy is transferred between different buses, a large power capacity is required. The capacity of a single converter and the voltage stress of the power switch are limited, which cannot meet the power demand of the system. At this time, it is an important solution in the project to realize the expansion of multiple medium and small power grade converters through a modular combination (OP structure). The modular combination scheme can effectively increase the power capacity, reduce the stress of the power tube, and enhance the redundancy of the system. If the interleaved phase-shifting control method is adopted between the modulation signals of each module, the system current ripple and the design parameters of the filter components can be further reduced.

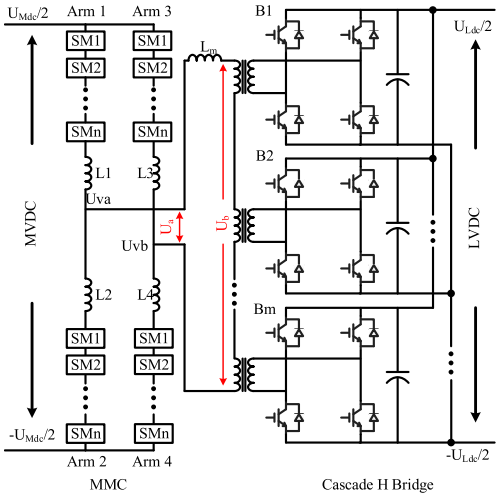

FIGURE 1. DC transformer topology based on MMC and H-bridge hybrid structure.

On the one hand, compared with the conventional DAB DC-DC converter, OP structure can be applied into high-output-current scenario with the same output voltage level. Taking the storage system for instance, within the range of charging current, the charging rate of OP converter is higher than that of DAB. On the other hand, with many cascaded H bridges, under the same output voltage level, the ability of power transmission of OP structure is much higher than that of DAB.

For transformer, with the same output-current level, the current stress flowing through each transformer of OP structure is much lower than that of single DAB, which is beneficial to the effective employment of transformer's window. Under high-current-stress condition, the litz wire and copper foil are employed into the manufacture of transformer, resulting in the complicated manufacture and low utilization of transformer.

II. WORKING PRINCIPLE ON THE MMC PORT OF DIFFERENT MULTI-PORT DC-DC CONVERTERS IN DIFFERENT CASES

In this section, several cases are discussed in detail, which introduce different combinations among phase-shift ratios, topology and CPS-PWM method. Case 1 presents the

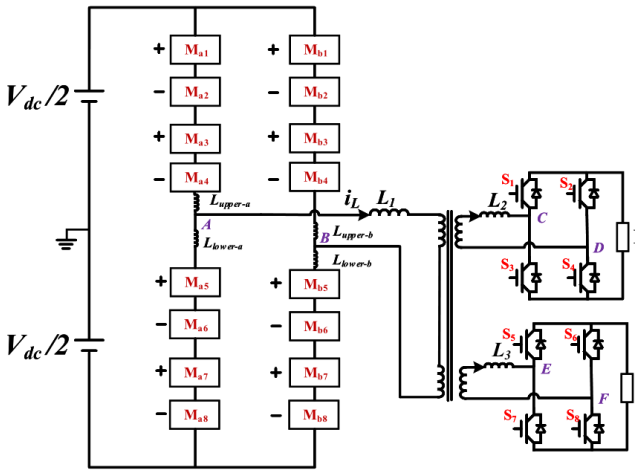

FIGURE 2. Proposed topology mentioned in case 1.

DC-DC converter composed of input port based on MMC and two output ports based on cascaded H bridges, which is depicted clearly in Fig.2. The basic control scheme of primary side contains equal CPS-PWM control and Unequal. There is a brief demonstration in Fig.5 and Fig.6 about case 2, elaborating a novel topology made up of input side based on MMC and four output ports based on cascaded H bridges. Case 3 introduces three-port DC-DC converter based on cascaded H bridges, which operates under extended-phase-shift (EPS) control. The current stress and backflow power on the primary side are decreased dramatically compared with single-phase-shift (SPS) control.

Case 1: Based on aforementioned illustrations, a DC-DC converter consisting of input side based on MMC and two output ports based on cascaded H bridges. MMC consists of two different phases, which are denoted as A and B respectively. Each phase contains two different arms and there are 4 SMs on a single arm. The DC side is divided into two parts and the value of each part is $V_{dc}/2$, where the midpoint of DC side is zero. The primary side based on MMC employs CPS-PWM method to produce stair waveform for power transmission. The phase displacement between the primary side and output port 1 is same as that between the primary side and output port 2, meaning that there is no energy exchange between output ports. The detailed messages are demonstrated in Fig.2.

By employing CPS-PWM control, the AC equivalent output waveform on the primary side is nine-level stair waveform and the AC equivalent output waveform on the secondary side is square waveform. The magnitude and direction of power transmission can be controlled by adjusting the phase displacement between the primary AC voltage V_{AB} and secondary AC voltage of either V_{CD} or V_{EF}. The equivalent circuit is demonstrated apparently in Fig.3.

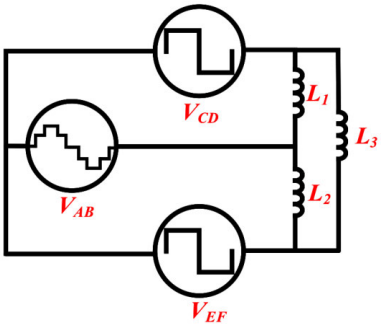

FIGURE 3. Equivalent circuit of proposed topology in case 1.

The output voltages of A and B are anti-phase. Likewise, the reference waveforms of either upper arm or lower arm in both phase A and B are also anti-phase.

The reference waveform of both upper arm and lower arm in phase A and B are expressed as follows.

$$V_{ref-upper-A} = \frac{V_{dc}}{2} + \frac{V_{dc}}{2}\sin(\omega t) \tag{1}$$

$$V_{ref-lower-A} = \frac{V_{dc}}{2} - \frac{V_{dc}}{2}\sin(\omega t) \tag{2}$$

The single phase of MMC is depicted in Fig.4 apparently. The relationship among output voltage V_o, the voltage of upper arm V_{upper} and the voltage of upper arm V_{lower} is depicted as follows.

$$V_o = \frac{v_{lower} - v_{upper}}{2} \tag{3}$$

Ignoring the voltage across the buffer inductor, the AC output voltage of MMC V_o is mainly determined by upper arm voltage V_{upper} and lower arm voltage V_{lower}. Through employing the CPS-PWM control, the basic characteristics of AC output stair waveform relies on the insertion sequence of SMs.

For single phase of MMC, the reference waveform of upper arm and lower arm are anti-phase. Nevertheless, the phase displacement between upper arm and lower arm is zero. The insertion sequences between upper arm and lower arm are different as well. The configuration among reference waveform, carriers and insertion sequence are presented in Fig.4 clearly.

Taking case 1 as a typical example of CPS-PWM control, the AC equivalent output voltage is a nine-level stair waveform. The insertion of entire CPS-PWM control begins from the lower arm, where the insertion sequence is from SM_5 to SM_8. However, the insertion of the upper arm starts from SM_1 to SM_4.

Assuming that all capacitor voltages are well balanced and the capacitor voltage is denoted as V_c, the maximum output voltage and the minimum output voltage of MMC are $2V_c$ and $-2V_c$ respectively.

The output voltage of MMC on the primary side can be derived as follows. Especially, the phase-shift angle among

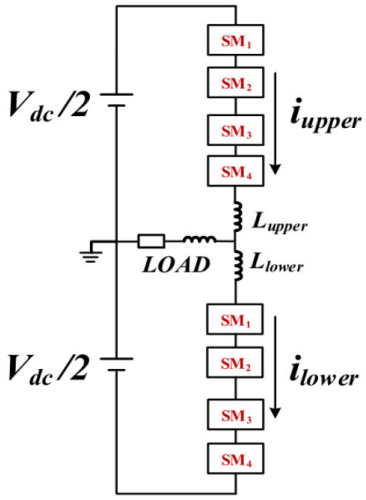

FIGURE 4. Single phase of MMC.

carriers is equal.

$$V_o = V_A - V_B \tag{4}$$

According to the illustration in Fig.4, the time slot among different output voltage level keeps the same.

What's more, in order to decrease the total harmonics distortion (THD), the time slot of highest output voltage level should be increased.

With the identical insertion sequence of SMs, the phase-shift angle between the carrier of SM_8 and SM_1 widens whereas that between other carriers reduces and maintains same.

Due to the structural characteristics of this DC-DC converter, the secondary output voltage V_{h2} can be concluded as

$$V_{h2} = V_{cd} + V_{ef} \tag{5}$$

V_{h2} is also a square waveform, where the amplitude is twice of V_{cd} whereas the phase keeps the same.

Owning to the symmetrical characteristic of primary voltage waveform, the time slot of the appearance of the stairs waveform is denoted as d in the period of $T/4$.

Taking the equal CPS-PWM control in half of switching period T_{hs} for example, the operation states in each period are illustrated as follows. The phase-shift ratio between the primary voltage V_{h1} and the secondary voltage V_{h2} is marked as D. The time slot when output voltage keeps constant is chosen as d_1. The turn ratio of magnetizing transformer is selected as 1.

The configuration of carriers, reference waveform and insertion sequence of SMs is shown in Fig.5 apparently. And the specific configuration under this unequal CPS-PWM control and the insertion sequences of sub-modules are also demonstrated in Fig.6. At the same time, the configurations of AC equivalent output voltage V_{h1} on the primary side and V_{h2} on the secondary side are depicted in

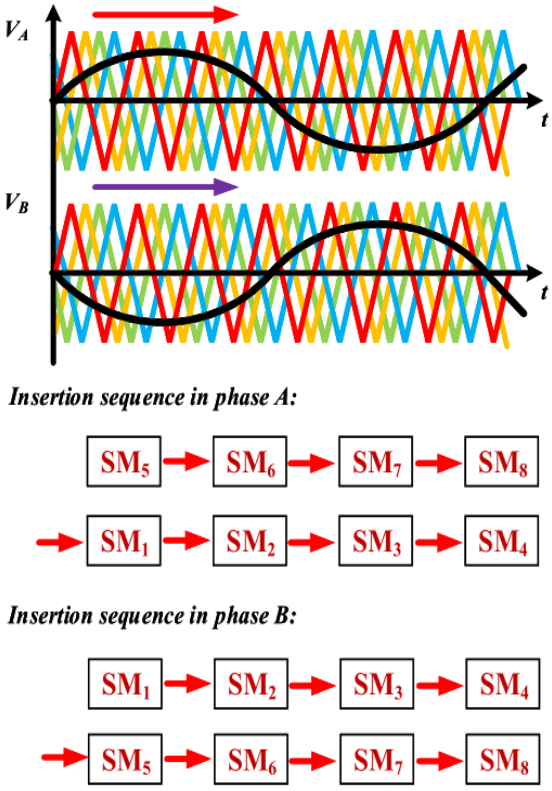

FIGURE 5. Configuration of carriers, reference waveform and insertion sequence of SMs under equal CPS-PWM control.

Fig.7 apparently.

$$V_{h1} = \begin{cases} 0, & t \in [0, t_1] \\ \dfrac{V_c}{dT_{hs}}t - \dfrac{d_1 V_c}{d}, & t \in [t_1, t_2] \\ V_c, & t \in [t_2, t_3] \\ \dfrac{V_c}{dT_{hs}}t - \dfrac{(2d_1 + d)V_c}{d}, & t \in [t_3, t_4] \\ 2V_c, & t \in [t_4, t_6] \\ -\dfrac{V_c}{dT_{hs}}t + \dfrac{(3d_1 + 2d)V_c}{d}, & t \in [t_6, t_7] \\ V_c, & t \in [t_7, t_8] \\ -\dfrac{V_c}{dT_{hs}}t + \dfrac{(4d_1 + 3d)V_c}{d}, & t \in [t_8, t_9] \\ 0, & t \in [t_9, t_{10}] \end{cases} \tag{6}$$

$$V_{h2} = \begin{cases} -V_{dc}, & t \in [t_0, t_5] \\ V_{dc}, & t > t_5 \end{cases} \tag{7}$$

Case 2: In the ISOP type DC transformer, the power unit usually selects type DAB, which can achieve voltage conversion, electrical isolation, and the ability to achieve soft switching of the device. Power flow control based on phase-shift control is easy to implement and has a larger output adjustment range.

Case 2 also illustrates the near square waveform modulation, which combines the high ability of power transmission of square waveform modulation and the low-THD-content characteristics of sine waveform modulation.

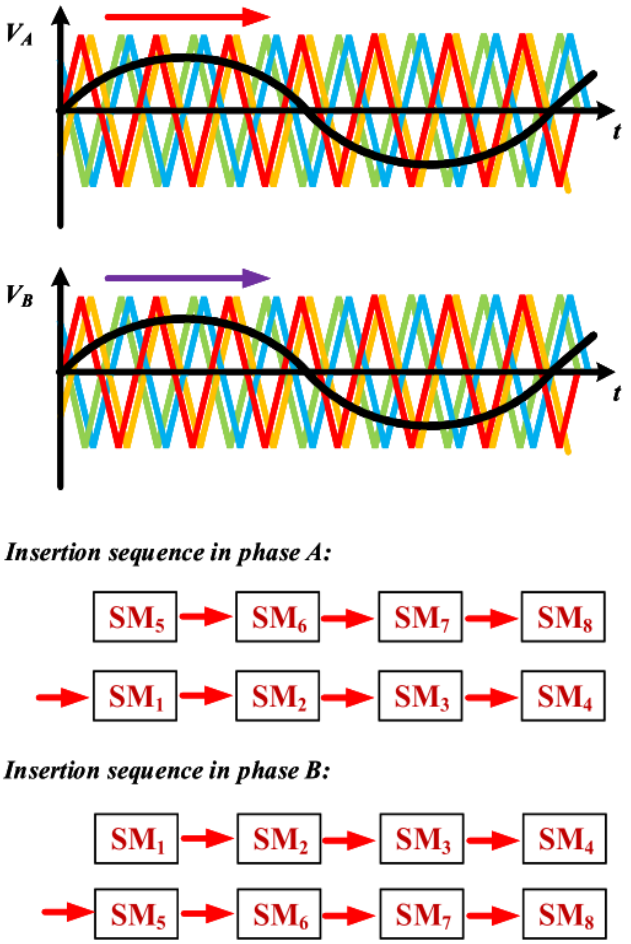

FIGURE 6. Configuration of carriers, reference waveform and insertion sequence of SMs under unequal CPS-PWM control.

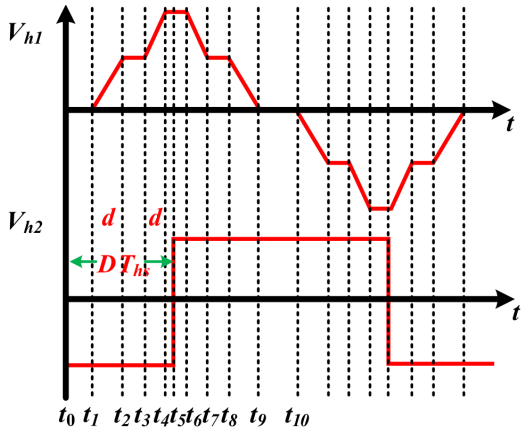

FIGURE 7. The configuration of AC equivalent output voltage on both the primary side and the secondary side.

In DC transformers based on MMC and cascaded H-bridge structures, phase-shift control is also used for power transmission. By adjusting the phase difference between the MMC side inverter voltage U_{Mac} and the cascaded H-bridge inverter voltage U_{Lac}, the power transmission between the MMC side and the cascaded H-bridge side can be controlled. The structure of Fig.1 is simplified as the equivalent circuit model

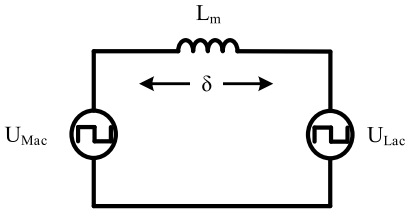

FIGURE 8. Phase-shift control power.

in Fig.8. The medium-voltage side MMC and the low-voltage side cascaded H-bridge can be regarded as two AC voltage sources.

$$P = \begin{cases} \dfrac{V_{Mac}V_{Lac}}{2f_sL_m}[D(1-D)], & 0 < D < 1 \\ \dfrac{V_{Mac}V_{Lac}}{2f_sL_m}[D(1+D)], & -1 < D < 0 \end{cases} \tag{8}$$

Among them: V_{Mac} -medium voltage side inverter voltage amplitude/V; V_{Lac}-low voltage side inverter voltage amplitude/V; f_{s} -AC waveform frequency / Hz; L_{m} -AC side power inductor and transformer leakage inductance Coupling/H; D——Phase shift angle unit value/V, that is $D = \delta/\pi$, δ is phase shift angle/rad.

From equation (8), the output power of the phase-shifting DC transformer is mainly determined by the switching frequency, inductance value, phase-shift ratio and AC voltage amplitude. When the phase-shift angle is greater than 0, that is, the phase of AC equivalent output voltage on medium-voltage side is ahead of that on low-voltage side. The power flows from the medium voltage side to the low voltage side. When the phase shift angle D is 0.5, it reaches the peak value of transmission power; when the phase-shift angle is less than 0, it means phase of AC equivalent output voltage on medium voltage side lags behind that on low voltage side. The power flows from the low voltage side to the medium voltage side. When the phase shift angle D is -0.5, the peak value of transmission power is reached, which is easy to realize the control of the power transmission flow direction and size.

For the phase-shift type DAB converter, the square wave is the only AC waveform that can be used for modulation. In the DC transformer based on MMC and cascaded H-bridge, the modulation of sine wave and triangle wave can be realized through different modulations. Comprehensive comparisons among several modulation methods, under the same voltage amplitude, square wave modulation has the strongest power transmission capability while control complexity and switching frequency are low. However, triangle wave modulation and sine wave modulation have smaller voltage stress and harmonics content. Through comprehensive consideration, quasi-square-wave modulation has combined advantages among aforementioned modulation methods.

The voltage waveform diagram of the near square wave modulation is shown in Fig.9.

Suppose the amplitude of the near square wave voltage is v_{peak}, the period is T, and the level switching duration is dT.

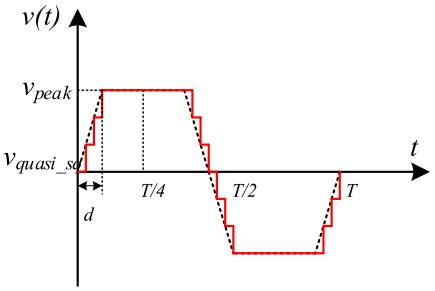

FIGURE 9. Quasi-square wave modulation waveform.

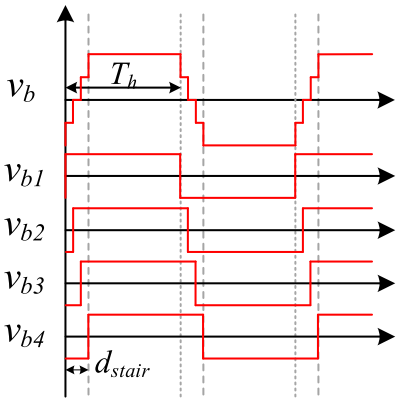

FIGURE 10. Cascaded H-Bridge quasi-square Wave.

In the process of level switching, a total of k levels are set, k is usually greater than or equal to 5, and the height of each level of voltage ladder is $2v_{peak}/(k-1)$. Due to the limitation of the switching frequency and the level switching time, the number of voltage steps k cannot be too large.

Compared with the control method of the MMC on the medium voltage side, due to the limitation of the topology of the low voltage side cascaded H bridge, each H bridge can only invert a two-level square wave voltage, and cannot achieve greater gain as flexible as the MMC Voltage transformation ratio. Therefore, in the cascaded H-bridge part, the main control strategy is to coordinate the near-square wave phase shift control on the medium voltage side.

As shown in Fig.10, taking the number of H-bridges as an example, the quasi-square-wave v_b generated by the cascaded H-bridge is synthesized by the square waves $v_{b1} \sim v_{b2}$ generated by the inverter of several H-bridges connected in series. There is a phase delay between each H bridge at a time, and the delay time is $d_{stair}T_h/3$. Among them, d_{stair} is the ratio of the near-square-wave ladder process time to the near-square-wave half-cycle duration, which is the same as the near-square-wave ladder process time generated by the medium voltage side MMC inverter.

By adopting a modulation method with a wide gain range, the ratio of AC voltage amplitude to DC voltage can be flexibly configured on the basis of making full use of all modules. Without considering the MMC redundant module, the wide gain range modulation method is shown in Fig.11.

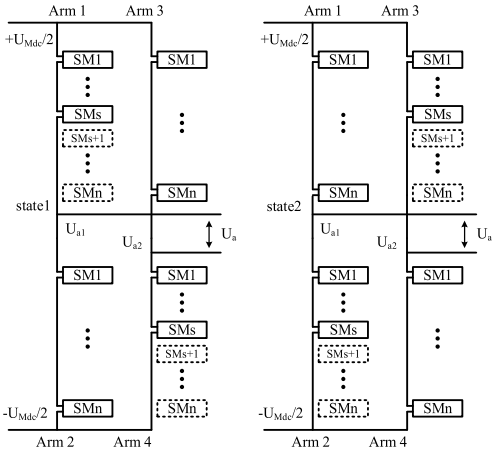

FIGURE 11. Wide gain range modulation.

In state 1, s sub-modules are inserted in the bridge arms 1, 4, n sub-modules are inserted in the bridge arms 2, 3, it is considered that the capacitor voltage of each sub-module in the bridge arm is balanced, and the midpoint potential of the bridge arms 1 and 2 can be written U_{a1} and the midpoint potential U_{a2} of bridge arms 3 and 4:

$$U_{a1} = \frac{n}{s+n}U_{Mdc} + (-\frac{1}{2})U_{Mdc} \tag{9}$$

$$U_{a2} = \frac{s}{s+n}U_{Mdc} + (-\frac{1}{2})U_{Mdc} \tag{10}$$

Equation (9) and (10) can be subtracted to obtain the expression of AC side voltage U_a:

$$U_a = \frac{s-n}{s+n}U_{Mdc} \tag{11}$$

It can be seen from formula (11) that the AC side voltage can be flexibly configured by changing the number of s and n, and the gain control from DC voltage to AC voltage amplitude can be adjusted.

By adjusting the gain, the following goals can be achieved:

(1) Reduce the AC voltage amplitude, thereby reducing the number of high-frequency transformers in the AC link and the difficulty of electrical insulation;

(2) The s+n sub-modules invested in each phase of MMC share the DC side voltage, so the number of sub-modules under the same medium voltage level can be reduced;

(3) When the DC side voltage fluctuates, the gain can be adjusted to keep the AC side voltage amplitude matched to avoid the increase of current stress, power return and loss.

The AC voltage and current waveforms with quasi-square-wave modulation are shown in Fig.12, where the inverter voltage U_a on the medium voltage side leads the inverter voltage U_b on the low voltage side.

Since the AC voltage has periodic symmetry, only half of the cycle time T_h is considered, and the step time is recorded as $D_{stair}T$. The medium voltage MMC side voltage and the low voltage side cascaded H-bridge inverter voltage can be

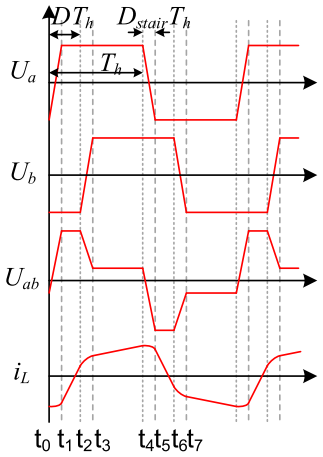

FIGURE 12. Voltage and current waveform under quasi-square-wave phase-shift control.

expressed as equations (12) and (13):

$$U_a = \begin{cases} (2jt-1)V_{Mac}, & t \in [0, t_1] \\ V_{Mac}, & t \in [t_1, t_4] \end{cases} \tag{12}$$

$$U_b = \begin{cases} -kV_{Mac}, & t \in [0, t_2] \\ [2j(t-DT_h)-1]kV_{Mac}, & t \in [t_2, t_3] \\ kV_{Mac}, & t \in [t_3, t_4] \end{cases} \tag{13}$$

Among them: t_0——0 moment; t_1——$D_{\text{stair}}T_{\text{h}}$ moment; t_2——DT_{h} moment; t_3——$(D + D_{\text{stair}})/T_{\text{h}}$ moment; t_4——T_{h} moment; j——$1/(D_{\text{stair}}T_{\text{h}})$ moment.

According to formulas (12) and (13), the current on the power inductor in the half cycle can be obtained:

$$\begin{aligned} & i_L(t) \\ &= \int_0^t \frac{U_{ab}}{L}dt = \int_0^t \frac{U_a - U_b}{L}dt \\ &= \begin{cases} i_L(0) + \dfrac{1}{L}((jt-1)V_{Mac} + kV_{Mac})t, & t \in [0, t_1] \\ i_L(t_1) + \dfrac{1}{L}(1+k)V_{Mac}(t-t_1), & t \in [t_1, t_2] \\ i_L(t_2) + \dfrac{1}{L}(V_{Mac} \\ \quad -(j(t+t_2-2D)-1)kV_{Mac})(t-t_2), & t \in [t_2, t_3] \\ i_L(t_3) + \dfrac{1}{L}(1-k)V_{Mac}(t-t_3), & t \in [t_3, t_4] \end{cases} \end{aligned} \tag{14}$$

According to the half-period symmetry of AC, $i_L(t_0) = -i_L(t_4)$, the expression of AC current at $t_0 \sim t_3$ in equation (14) can be obtained:

$$\begin{cases} i_L(0) = \dfrac{V_{Mac}T_h}{2L}[(1+k)D_{stair} - 2Dk - 1 + k] \\ i_L(t_1) = \dfrac{V_{Mac}T_h}{2L}[(1+3k)D_{stair} - 2Dk - 1 + k] \\ i_L(t_2) = \dfrac{V_{Mac}T_h}{2L}[(k-1)D_{stair} + 2D - 1 + k))] \\ i_L(t_3) = \dfrac{V_{Mac}T_h}{2L}[(1+k)D_{stair} + 2D - 1 + k)] \end{cases} \tag{15}$$

According to the voltage and current on the AC side, the AC transmission power can be calculated by the integration of the AC port voltage and current, as shown in equation (16):

$$\begin{aligned} P &= \frac{1}{T_h}\int_0^{T_h} U_{\text{a}}(t)i_L(t)\text{d}t \\ &= \frac{kV_{Mac}^2}{2f_sL}[D(1-D) - \frac{D_{stair}^2}{24}] \end{aligned} \tag{16}$$

Case 3: Under this case, a typical three-port DC-DC converter based on cascaded H bridges is analyzed in detail. The topology among the input port and the output ports is selected as full-bridge topology.

When it comes to the differences between this three-port DC-DC converter and the conventional dual-active-bridge (DAB) under EPS control, several specific advantages should be proposed.

The voltage waveform on the secondary side is a special condition, where the phase-shift ratio between V_{ab} and V_{cd} is equal to that between V_{ab} and V_{ef}. In common condition, these two phase-shift ratios are different, leading to a three-level output voltage on the secondary side. Therefore, the operation state of this three-port DC-DC converter under EPS control is similar to the operation of DAB under three-phase-shift (TPS) control. Additionally, the direction and amplitude of power flow among different ports are manipulated by the phase-shift ratios among different AC equivalent output voltage waveforms.

Obviously, compared with the EPS control of DAB, three-port DC-DC converter under EPS control contains more operation modes, which leads to the complicated analysis about control modes. Furthermore, these papers analyze basic conditions of power flow and corresponding optimizations on current stress.

There are a large quantities of operation states under TPS control. Some states can convey energies from primary side to secondary side directly. Nevertheless, some states could not transfer energy from the primary side to the secondary side, where the energy is stored into the inductor temporarily. For this state, the first step is that the energy is transferred from the primary side to the inductor. At the same time, the second step is that the energy is transferred from the inductor to the secondary side.

The common AC equivalent voltage waveforms including V_a on the primary side and V_b on the secondary side of three-port DC-DC converter under EPS control are shown in Fig.13 in detail. And the equivalent circuit of three-port DC-DC converter is depicted in Fig.14 clearly.

As a result, first of all, the conventional EPS control of DAB is a special condition of three-port DC-DC converter under EPS control, where the value of phase-shift ratios are chosen as the same value among different AC equivalent waveforms of different output ports. Secondly, when it comes to the power flow among different ports, the condition of power flow inside the three-port DC-DC converter is more complicated than that inside the DAB. Through changing the phase-shift angle among different AC equivalent output

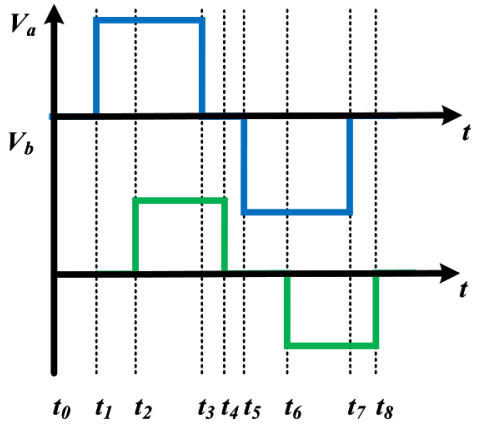

FIGURE 13. Equivalent AC output voltage waveforms on both sides.

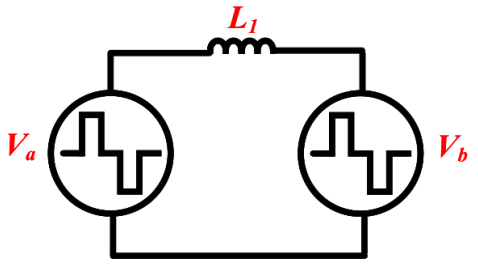

FIGURE 14. Equivalent circuit of three-port DC-DC converter.

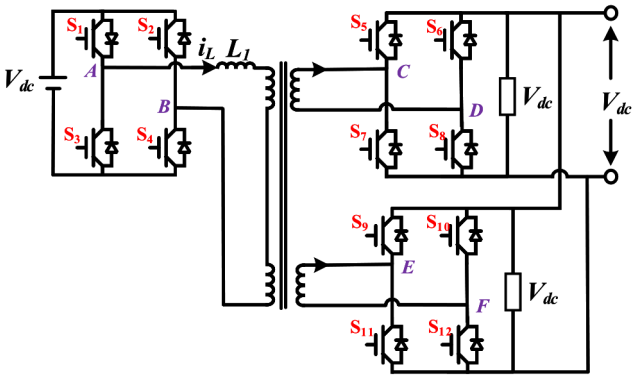

FIGURE 15. Switch table voltage equalization module status.

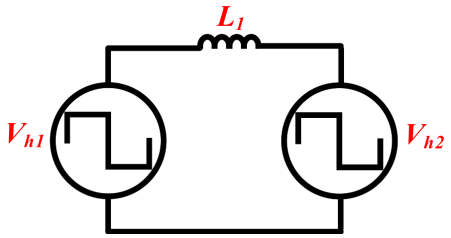

FIGURE 16. Equivalent circuit of three-port DC-DC converter in case 3.

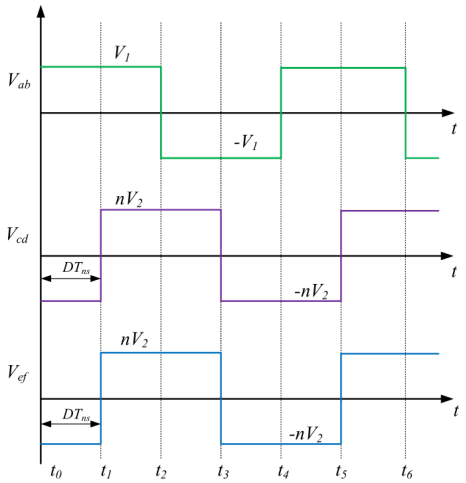

FIGURE 17. AC equivalent output voltage (1) V_{ab}: on the primary side (2) V_{cd}: output port 1 (3) V_{ef}: output port 2.

voltages, the direction and amplitude of power flow can be controlled precisely. That is to say, from the perspective of entire topology, the operation states and basic control principles are definitely different even having the same equivalent circuit. Moreover, the introduction of inner phase-shift angle is to decrease the value of backflow power under EPS control of DAB, resulting in lower power losses further. However, the phase-shift angles between the input port and the output port 1 and between the input port and the output port 2 are defined as θ_1 and θ_2 respectively. For EPS control of three-port DC-DC converter, the power flow and AC equivalent voltage are manipulated by not only inner phase-shift angle but the difference between θ_1 and θ_2, where several important variables mentioned in many papers such as backflow power and transmission power can be controlled in same way. The detailed configuration of three-port DC-DC converter is shown in Fig.15.

The AC equivalent output voltage of full-bridge is square waveform. Input port or output port is composed of a full-bridge topology, a linked inductor and high-frequency transformer (HFT). Without any phase-shift angle inside this topology, input port can be equivalent to square waveform V_{ab}. At the same time, output port can be equivalent to square waveform V_{cd} and V_{ef} respectively. The phase displacement between V_{ab} and V_{cd} is same as that between V_{ab} and V_{ef}. As a result, there is no power exchange between these two output ports. The phase-shift ratio between V_{ab} and V_{cd} is same as that between V_{ab} and V_{ef}, which is denoted as D.

The specific configuration of equivalent circuit is demonstrated in Fig.16 apparently. Likewise, the AC equivalent voltage waveforms are elaborated in Fig.17.

According to the analysis in Fig.17, the secondary side of this topology can be equivalent to a square waveform. The amplitude and direction of power flow can be determined by phase-shift ratio D between the AC equivalent voltage on the primary side and the secondary side.

When it comes to the conventional control scheme, the single-phase-shift (SPS) control is the common used control method. However, the uncontrollable backflow power and enormous current stress are the main problem occurring in

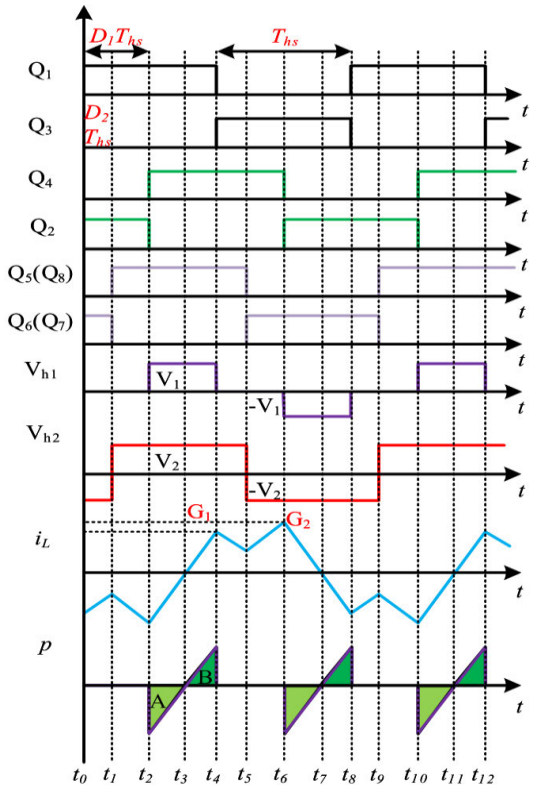

FIGURE 18. AC equivalent output voltage (1) V_{ab}: on the primary side (2) V_{cd}: output port 1 (3) V_{ef}: output port 2.

operation. Subsequently, the extended-phase-shift (EPS) control is introduced to decrease the backflow power and current stress substantially. The operation states of this three-port DC-DC converter under EPS control are described in Fig.18 apparently.

The negative part A of transient power represents the value of backflow power. The sum of A and B represents the value of transmission power. The transmission power, backflow power and current stress are displayed as follows.

$$p_{backflow} = \frac{1}{T_{hs}} \int_0^{t_3} V_{h1} \, |i_L| \, dt \tag{17}$$

$$p = \frac{1}{T_{hs}} \int_0^{T_{hs}} V_{h1} i_L dt \tag{18}$$

$$i_{L\max} = \max\{G_1, G_2\} \tag{19}$$

With the variation of inner phase-shift ratio D_1, the negative part of transient power decreases substantially, which means the drop of backflow power.

III. MMC SUB-MODULE CAPACITANCE VOLTAGE EQUALIZATION ALGORITHM

I Regarding the voltage equalization of the sub-modules of the modular multi-level converter, the most direct idea is to control the charge and discharge of the sub-module capacitors

Instruction Cycle	1		2		3		4		5		6	
	1	0	1	0	1	0	1	0	1	0	1	0
SM1	1	1	0	1	0	1	1	1	1	1	1	1
SM2	1	1	1	1	0	1	0	1	1	1	1	1
SM3	1	1	1	1	1	1	0	1	0	1	1	1
SM4	0	1	1	1	1	1	1	1	0	1	0	1
SM5	0	1	0	1	1	1	1	1	1	1	0	1
SM6	1	1	0	1	0	1	1	1	1	1	1	1
SM7	1	1	1	1	0	1	0	1	1	1	1	1
SM8	1	1	1	1	1	1	0	1	0	1	1	1
SM9	0	1	1	1	1	1	1	1	0	1	0	1
SM10	0	1	0	1	1	1	1	1	1	1	0	1

FIGURE 19. Switch table voltage equalization module status.

in different states to ensure that the voltages of each capacitor are balanced. The logic of sorting algorithm based on the direction of the bridge arm current and the capacitor voltage is as follows:

(1) According to the quasi-square-wave modulation algorithm and the current quasi-square-wave cycle state, determine the number of sub-modules that need to be inserted into the bridge arm at the current moment n;

(2) Real-time acquisition and sorting of the capacitor voltage of the bridge arm sub-module;

(3) Control the switching state of the bridge arm sub-module according to the current direction. When the bridge arm current is greater than 0, that is, the current flows into the input sub-module to charge the module capacitance. Otherwise, it discharges the module capacitance. Therefore, when the bridge arm current is positive, the n sub-modules with the lowest capacitor voltage value are inserted in; when the bridge arm current is negative, the n sub-modules with the highest capacitor voltage value are inserted in.

This method has small capacitance voltage fluctuations, good voltage equalization effect and strong applicability. It can be more convenient to increase the number of modules or expand to multi-port applications. The disadvantages are: 1. When the number of modules is large, the controller needs to collect a large amount of data. The sampling cost and the controller's calculation pressure are relatively high; 2. Real-time sampling needs to use a higher sampling frequency and switching frequency to ensure that the effect of voltage equalization is High-frequency MMC will greatly increase the switching loss of the device.

In view of the problems of the voltage equalization method based on voltage sequencing and current direction judgment, consider using the sub-module cycle switching method to perform voltage equalization, so as to avoid a large amount of sampling and sequencing.

The square wave modulated switch meter capacitor voltage equalization is the simplest. Taking 10 sub-modules of one bridge arm as an example, it takes 10 cycles to complete a voltage equalization. Regardless of the redundancy of the sub-modules, the voltage equalization is shown in Fig.19:

Among them, 1 means that the submodule is in the input state. 0 means that the submodule is in the removal state.

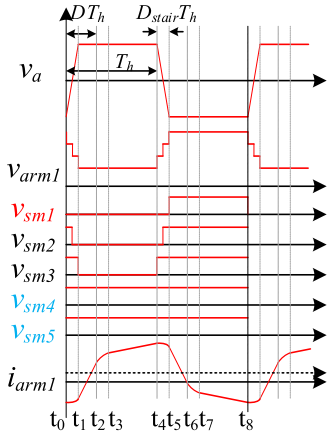

FIGURE 20. Quasi-square wave bridge arm 1 module waveform.

In 10/6 modulation, the equalization period can be shortened from 10 to 5 by symmetrical arrangement.

For quasi-square-wave modulation, due to the step transition time, a single-square-wave cycle cannot be simply divided into the first half cycle and the second half cycle. Due to the characteristics of the quasi-square-wave modulation method with a wide gain range, taking bridge arm 1 as an example, the switching states of each module of the MMC in a quasi-square-wave period are allocated as shown in Fig.20.

State 1: As shown by v_{sm1} in Fig.20, it is only switched on during the high-level phase of the quasi-square-wave cycle;

State 2: As shown in v_{sm2} and v_{sm3} in Fig.20, on the basis of state 1, gradually increase the investment time of the two stages of the ascending stage and the descending stage. The number of levels in each sub-module is fixed. From high level to low level, the on-time of each small state increases by two single-stage steps.

State 3: As shown by v_{sm4} and v_{sm5} in Fig.20, it is switched on during the entire quasi-square-wave period.

When the sub-module is turned on, the bridge arm current flowing through the sub-module capacitance begins to charge or discharge it. Therefore, in a sampling cycle, the current integral within conduction period of the sub-module is the change in the charge of the module capacitance in that cycle. The amount of change may cause the module voltage oscillations.

The bridge arm current mainly includes circulating current flowing through the bridge arm and half of the AC output current:

$$\begin{cases} i_{arm1} = i_{arm4} = \dfrac{1}{2} i_L + i_{cir} \\ i_{arm2} = i_{arm3} = -\dfrac{1}{2} i_L + i_{cir} \end{cases} \tag{20}$$

$$i_{cir} = \frac{P}{2V_{Mdc}} \tag{21}$$

Based on this, the charge change in each state of the sub-module in a quasi-square-wave period can be obtained:

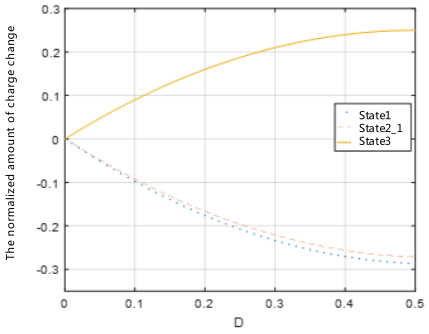

FIGURE 21. One cycle charge change of each state module.

$$Q_{state1} = \frac{V_{Mac}T_h^2}{4L}(2kD^2 + kD_{stair}^2 - 2kDD_{stair} - 2Dk) + \frac{V_{Mac}T_h^2}{2L}Jk[D(1-D) - \frac{D_{stair}^2}{24}](1 - D_s) \tag{22}$$

$$Q_{state2\_q} = \frac{V_{Mac}T_h^2}{4L}(2kD^2 + kD_{stair}^2 - 2kDD_{stair} - 2Dk) + \frac{V_{Mac}T_h^2}{2L}Jk[D(1-D) - \frac{D_{stair}^2}{24}] \times (1 - D_s + \frac{2q}{q_{stair}}D_{stair}) \tag{23}$$

$$Q_{state3} = \frac{V_{Mac}T_h^2}{2L}Jk[D(1-D) - \frac{D_{stair}^2}{24}] \tag{24}$$

In the formula: J——MMC AC voltage gain,.

The relationship curve between the normalized amount of charge change of each bridge arm sub-module and the phase shift angle D can be drawn, as shown in Fig.21:

It can be seen from Fig.21 that the charge change is negative in state 1 and state 2. And the charge change of each sub-module in state 1 and state 2 is relatively close; when the sub-module is in state 3, the charge change of the module is positive. In the voltage equalization algorithm of the switch meter, the two states can be regarded as one state, thereby reducing the length of the voltage equalization cycle.

Every two sub-modules are divided into a group as a sub-module group, that is, a total of n/2 sub-module groups. Each sub-module group is sampled. The two sub-modules in each sub-module group adopt a cyclic switching mode. The specific pressure equalization principles are as follows:

(1)At the beginning of a near-square wave period, collect the voltages of each sub-module group and sort them

(2) According to the order of voltage from high to low, extract one of the four sub-module groups with the highest voltage The sub-modules are put into state 1, state 2_1∼ state 2_3 in turn during the near-square wave period, and the remaining 6 sub-modules are put into state 3.

(3) Re-sampling the voltage and at the beginning of the next near-square wave period Sequencing.

(4) In each sub-module group, the two sub-modules adopt a cyclic switching mode, that is, they are in the discharging and charging state in turn to achieve voltage balance between the two sub-modules.

(5) When a certain sub-module group is integrated When the voltage is higher than a certain threshold, in the near square wave period, the two sub-modules are in state 1 or state 2_1, so that the voltage of the sub-module group drops rapidly.

(6) When the modulation mode is changed, step 2 needs to be performed Flexible adjustment.

For example, in 10/4 modulation, the two sub-modules in the sub-module group with the highest voltage are in state 1 or state 2_1, and the remaining 4 sub-module groups are sorted by voltage, and one of the sub-modules is extracted and made in turn. In the near square wave cycle, the input state is state 1, state 2_2∼ state 2_5, and the input state of the remaining 4 sub-modules is state 3.

The above is the grouping capacitor voltage equalization principle combining voltage sorting and switching table. This voltage equalization method integrates the characteristics of voltage sequencing and switching tables, and has a certain voltage correction capability.

The cyclic switching can be completed within 2 to 3 near square wave cycles, and it can greatly reduce the number of sampling links and the amount of sequencing calculations. And each quasi-square-wave cycle only needs to be sampled and be equalized once, which will not increase the switching frequency.

Combining the voltage sorting principle with the grouping capacitor voltage equalization principle of the switch table, this voltage equalization method integrates the characteristics of voltage sequencing and switching tables, which has a certain voltage correction capability.

The cyclic switching can be completed within 2 to 3 quasi-square-wave cycles. It can greatly reduce the number of sampling links and the amount of sequencing calculations.

IV. DC TRANSFORMER SOFT-SWITCHING ANALYSIS

The loss of power electronic equipment mainly includes switching loss, conduction loss and magnetic loss. Among them, switching loss accounts for a heavier proportion of devices with higher frequencies. The realization of soft switching can significantly reduce switching losses and improve the efficiency of power electronic devices.

First analyze the soft switching performance of the MMC side. In the traditional MMC structure of the converter valve, only half of the devices that can achieve zero voltage turn-on (ZVS-ON) are usually used. The rest of the devices work is in the hard-switching state, resulting in severe switching losses. Although the medium voltage side of the DC transformer studied in this article adopts the MMC structure, the control method is different from the converter valve MMC. The control method is also different. So it is necessary to analyze its soft switching performance in detail.

Fig.19 shows the two state switching processes of the MMC sub-module. When the current flows in (capacitor charging), the voltage of the T_2 tube is 0 at the moment of state switching, which can realize ZVS-OFF; the current flows through the freewheeling diode of the upper tube T_1. So the upper tube T_1 can realize ZVS-ON. When the current flows out, the upper transistor T_1 and the lower transistor T_2 both bear the capacitor voltage at the moments of turn on and turn off. Respectively, they are in a hard switching state. In the same way, when the sub-module is switched from on to off, the ZVS of the two switches can be realized when the current flows out, and it is hard to switch when the current flows in.

According to the current at each time in formula mentioned above, the soft switching range of the MMC side device can be obtained:

$$\begin{cases} k \le \dfrac{1-D_{stair}}{D_{stair}-2D+1+2J[D(1-D)-\dfrac{D_{stair}^2}{24}]}; \\ k \le \dfrac{1-D_{stair}}{3D_{stair}-2D+1+2J[D(1-D)-\dfrac{D_{stair}^2}{24}]} \\ k \le \dfrac{1-D_{stair}}{D_{stair}-2D+1-2J[D(1-D)-\dfrac{D_{stair}^2}{24}]}; \\ k \le \dfrac{1-D_{stair}}{3D_{stair}-2D+1-2J[D(1-D)-\dfrac{D_{stair}^2}{24}]} \end{cases} \tag{25}$$

The soft switching range of cascaded H-bridge can be obtained by similar analysis:

$$\begin{cases} k \ge \dfrac{1-2D+D_{stair}}{D_{stair}+1} \\ k \ge \dfrac{1-2D-D_{stair}}{D_{stair}+1} \end{cases} \tag{26}$$

Combining formulas (25) and (26), the curve of the soft switching range shown in Fig.23 can be obtained.

The orange area in the middle is the range where all the components of the DC transformer can achieve soft switching. The black dashed line is the power transmission curve at different values of k. It can be seen that when $k \neq 1$, soft switching cannot be realized under light load. The closer the power is to full load, the easier it is to realize soft switching. Therefore, during the working process of the DC transformer, light load operation should be avoided as much as possible and the voltage matching operation should be ensured as much as possible.''

V. DC TRANSFORMER MULTI-PORT POWER CHARACTERISTICS

In the DC distribution network, the low-voltage side needs to be adapted to DC buses of different voltage levels according to different types of loads, such as rail traction power, data center, residential building power supply, etc. In order to connect the medium-voltage DC bus with each low-voltage bus, it can be realized by a multi-port DC transformer, as shown

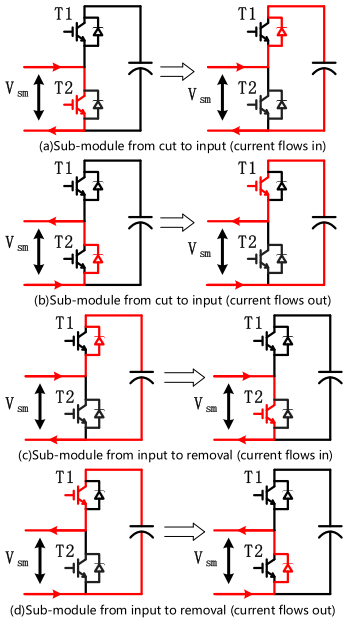

FIGURE 22. Sub-module operation state switching.

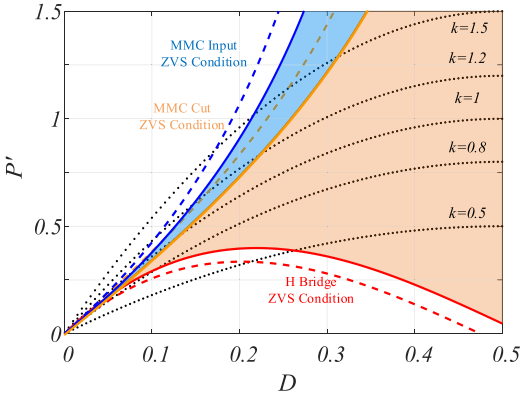

FIGURE 23. DC transformer soft switching range.

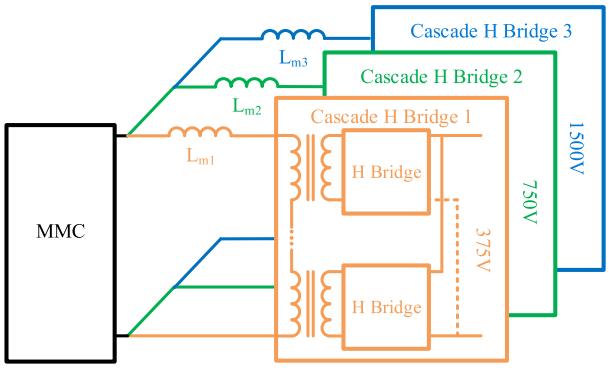

FIGURE 24. Multi-port DC transformer structure.

in Fig.24. In the AC link, multiple low-voltage side cascaded H bridges are led to realize single-end to multi-end DC conversion.

For DC transformers with single-pole input and multi-port output, load imbalance is a relatively common situation under actual working conditions. In extreme cases, some ports may

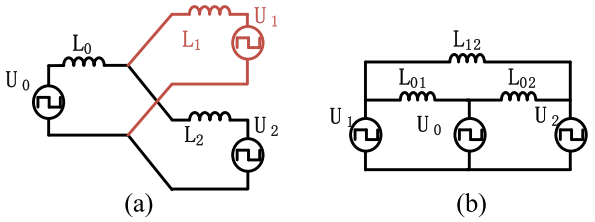

FIGURE 25. (a) Equivalent circuit of dual-port output;(b) Equivalent circuit after star-delta transformation.

even be unloaded and some ports may be overloaded. Analyzing with dual-port output, there are similar conclusions for multiple ports. The equivalent circuit of the dual-port output is shown in Fig.25.

Fig.25(b) is the equivalent circuit. In order to facilitate the calculation of the equivalent impedance between the various ports of the impedance, the equivalent circuit after star-delta transformation is performed. The equivalent reactance between each AC source is expressed by the following formula:

$$\begin{cases} L_{01} = L_0 + L_1 + L_0L_1/L_2 \\ L_{02} = L_0 + L_2 + L_0L_2/L_1 \\ L_{21} = L_2 + L_1 + L_2L_1/L_0 \end{cases} \tag{27}$$

Among them, when L_0 is 0, the value of L_{21} will be infinite, that is, ports 1 and 2 cannot transfer energy to each other. According to Fig.25(b), the three-port DC transformer can be analyzed as a phase-shift control for three power independent transmissions. Suppose the phase shift angles (radians) of U_1 and U_2 are θ_1 and θ_2 respectively. According to the power transmission expression of phase shift control, the power transmission formula between the three ports can be obtained:

$$\begin{cases} P_{01} = \dfrac{U_0U_1}{\omega L_{01}}\theta_1(1 - \dfrac{\theta_1}{\pi}) \\ P_{02} = \dfrac{U_0U_2}{\omega L_{02}}\theta_2(1 - \dfrac{\theta_2}{\pi}) \\ P_{21} = \dfrac{U_2U_1}{\omega L_{21}}(\theta_1 - \theta_2)(1 - \dfrac{\theta_1 - \theta_2}{\pi}) \end{cases} \tag{28}$$

When the load is unbalanced, adjusting the phase shift angle with the output voltage of the two ports as the control target can also achieve voltage stability. In a steady state, the actual power consumed on the load of port 1 and port 2 is $UOUT_2/R_1$ and $UOUT_2/R_2$, which are denoted as PR_1 and PR_2. Regardless of the device loss during power transmission, the power transmission between the three ports should conform to the power consumption on the load as:

$$\begin{cases} P_{R1} = P_{01} + P_{21} \\ P_{R2} = P_{02} - P_{21} \end{cases} \tag{29}$$

When the load of the two ports is unbalanced, the transmission power P_{21} between the two ports will play the role of peak-shaving and valley-filling. Energy will be transferred from the port with lower load demand to the port with higher

load demand, so when the port moves. When the phase angle reaches the maximum phase shift angle, the port can transmit more energy than a single DAB. The actual phase shift angle of a port with a smaller load will be greater than the required phase shift angle when a single DAB transmits the same energy, so that the port with a small load can avoid running in a light load state.

VI. SIMULATION VERIFICATION

Verification of case 1:

With the number of voltage level increasing and SMs increasing, the frequency of the carriers should be limited to a certain range to avoid the devastating impact on shape of AC output voltage. In this case, the modulation ratio m is chosen as a value of 10.

Under equal CPS-PWM control, the voltage waveform of MMC in both phase A and B and the AC output waveform on the primary side are illustrated in Fig.26 apparently.

The circuit parameters in case 1 is designed in table 1.

TABLE 1. Simulation parameters in case 1.

Modulation ratio	10
DC bus voltage on the medium voltage side	400V
Bridge arm sub-module capacitance	470μF
Power inductor	100μH
Bridge arm inductance	10μH
AC frequency	500Hz
Low voltage side DC bus voltage on lower arm	50V
Low voltage side H bridge capacitor	1mF
Low voltage DC side load R	1Ω

As is shown in Fig.26, under the equal CPS-PWM control, the results of the AC output voltage in single phase or on the primary side in theoretical analysis are verified. For each period when output voltage keeps constant, the time slot among these periods stays the same.

Under unequal CPS-PWM control, the voltage waveform of MMC in both phase A and B and the AC output waveform on the primary side are illustrated in Fig.27 apparently. As a result, the simulation is in accordance with the theoretical analysis.

The specific parameters of MMC are shown in table 2.

As is shown in Fig.27, under the unequal CPS-PWM control, the results of the AC output voltage in single phase or on the primary side in theoretical analysis are verified.

Verification of case 2: In view of the above DC transformer structure and modulation strategy, a simulation is built in Matlab/Simulink. Each bridge arm of the medium-voltage side MMC consists of 10 half-bridge sub-modules, and the low-voltage side cascaded H-bridge consists of 6 H-bridges plus transformers. The simulation parameters are shown in Table 3.

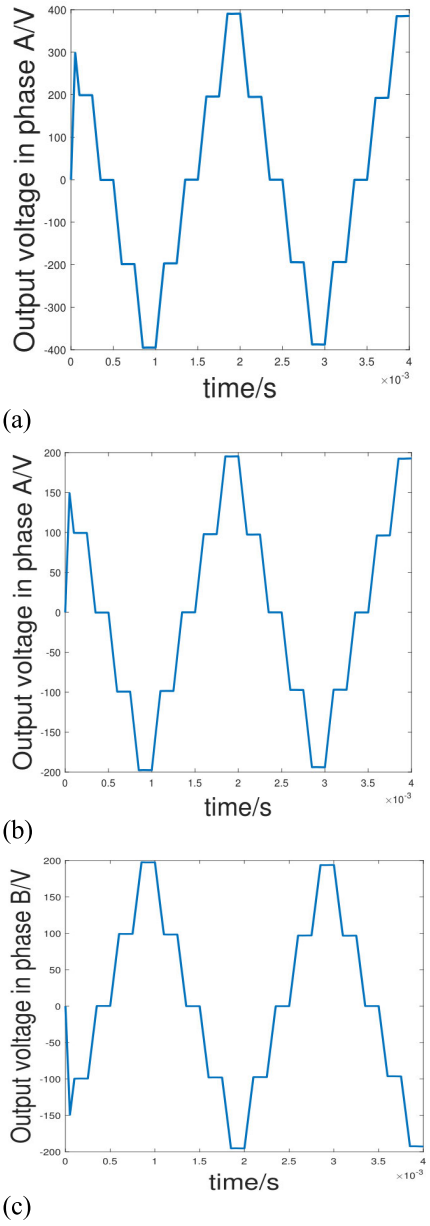

FIGURE 26. AC equivalent output voltage under equal CPS-PWM control (a) on the primary side (b) in phase A (c) in phase B.

Both the MMC of the DC transformer and the cascaded H-bridge adopt near square wave modulation. The AC link voltage level of the DC transformer is shown in Table 4. Among them, s and n are the MMC modulation ratios, and B_stage is the cascaded full bridge's step-level layer.

The voltage waveforms of the AC link of the DC transformer are shown in Fig.28, which are the near square waveforms on the MMC side and the cascaded H-bridge side.

The low-voltage side DC output voltage is shown in Fig.29 and is stable at 750V, and the fluctuation range is within ±5V, that is, within ±1%.

The waveforms of the three voltage equalization methods are shown in Fig.30. From left to right, they are the voltage equalization algorithm based on voltage sequencing

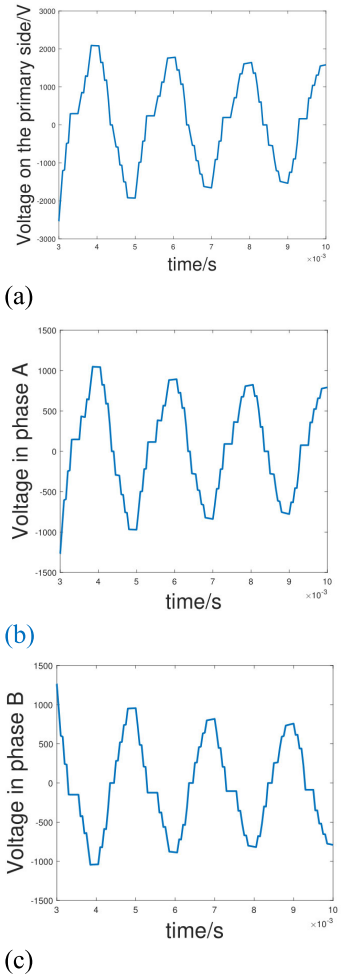

FIGURE 27. AC equivalent output voltage under unequal CPS-PWM control (a) on the primary side (b) in phase A (c) in phase B.

TABLE 2. Simulation parameters in case 1.

Modulation ratio	10
DC bus voltage on the medium voltage side	2kV
Bridge arm sub-module capacitance	470μF
Power inductor	100μH
Bridge arm inductance	10μH
AC frequency	500Hz
Low voltage side DC bus voltage on lower arm	50V
Low voltage side H bridge capacitor	1mF
Low voltage DC side load R	1Ω

and current direction judgment, the cyclic switching voltage equalization algorithm based on the switch table, and the combination of voltage sequencing and cyclic switching. The voltage equalization waveform of the grouping capacitor voltage equalization algorithm.

Among them, the voltage equalization algorithm based on voltage sorting has the best effect, and the fluctuation

TABLE 3. Simulation parameters.

Interval	u_0
DC bus voltage on the medium voltage side	20kV
Bridge arm sub-module capacitance	470μF
Power inductor	100μH
Bridge arm inductance	10μH
AC frequency	5kHz
Low voltage side DC bus voltage	750V
Low voltage side H bridge capacitor	1mF
Low voltage DC side load R	1Ω
Near square wave step time	15μs

TABLE 4. AC side voltage level.

s	n	U_a	B_ stage	U_b
10	6	-1/4 U_{Mdc}	0	-60/9U_{Ldc}
9	7	-1/8 U_{Mdc}	1	-40/9 U_{Ldc}
8	8	0 U_{Mdc}	2	-20/9 U_{Ldc}
7	9	1/8 U_{Mdc}	3	0 U_{Ldc}
6	10	1/4 U_{Mdc}	4	20/9 U_{Ldc}
			5	40/9 U_{Ldc}
			6	60/9 U_{Ldc}

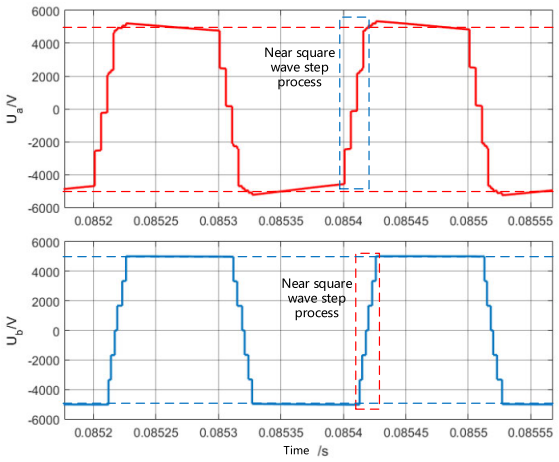

FIGURE 28. Quasi-square wave modulation AC side voltage.

amplitude is about ±25V; the cycle switching voltage equalization algorithm based on the switch meter has a poor effect, the fluctuation amplitude is about ±75V, but the voltage equalization frequency is low; The fluctuation amplitude of the grouping capacitor voltage equalization algorithm combining voltage sorting and cyclic switching is about ±75V, and it has a better voltage equalization effect and a lower voltage equalization frequency.

For the case of dual-port output, the two low-voltage ports are 1500V and 750V, and the port loads are 0.8Ω and

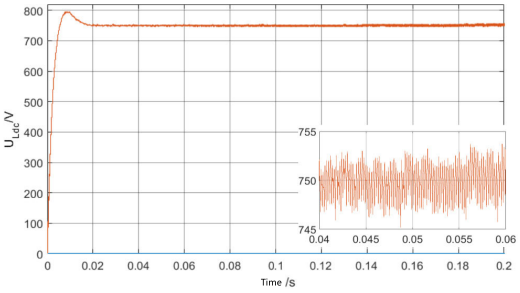

FIGURE 29. DC output waveform.

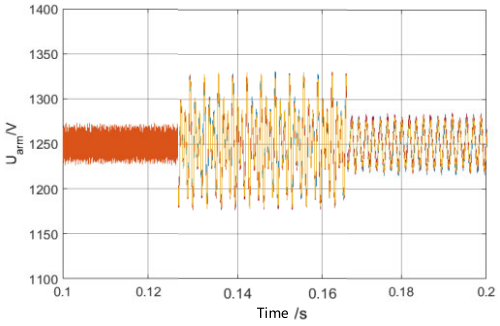

FIGURE 30. DC output waveform.

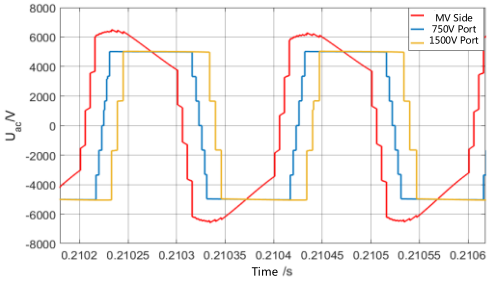

FIGURE 31. Multi-ports AC waveform.

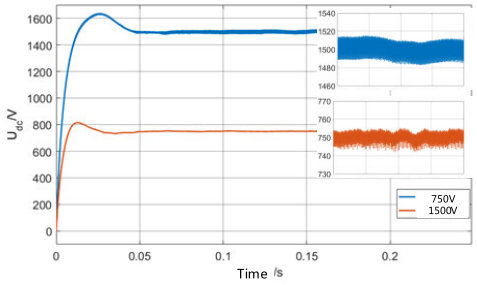

FIGURE 32. Multi-ports DC output waveform.

0.25Ω. The AC and DC waveforms are shown in Fig.31 and Fig.32 respectively.

Verification of case 3: the simulation results are shown in Fig.33 concerning with the comparisons between the SPS control and EPS control. The power characteristics and current characteristics of DAB under EPS control with the variations of D_1 and D_2 are also shown in Fig.33.

According to the description of Fig.33, with the increase of inner phase-shift ratio D_1 and the unchanged outer phase-shift ratio D_2, the negative part of transient power decreases

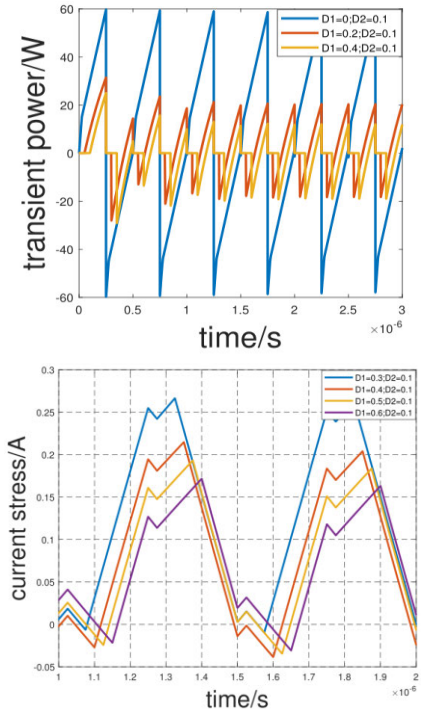

FIGURE 33. The simulation results of three-port DC-DC converter under EPS control.

substantially, which means the drop of backflow power. At the same time, the peak values of current stress reduce gradually as well.

VII. CONCLUSION

In this paper, aiming at the medium and low voltage DC distribution network, combining the MMC and ISOP-DAB structure, several multi-port DC transformer structure and its control strategy are proposed. The descriptions of multi-port converter are divided into three cases. The medium voltage side of this topology has a higher voltage bearing capacity, and its modularity makes it highly reliable. The output side of the low-voltage side cascaded H-bridge is connected in parallel to increase the output current.

First of all, case 1 presents the DC-DC converter made up of input port based on MMC and two output ports based on cascaded H bridges. The basic control scheme of primary side contains equal CPS-PWM control and unequal CPS-PWM control. Secondly, case 2 elaborates a novel topology consisting of input side based on MMC and four output ports based on cascaded H bridges. In order to reduce the voltage stress on the AC side and improve the phase shift transmission, both MMC and cascaded H-bridges adopt near-square wave modulation to reduce voltage stress. Aiming at the problem of high insulation pressure of the high-frequency transformer in the ISOP-DAB structure, the amplitude of the AC side voltage is reduced through a wide gain range modulation method, thereby reducing the insulation level of a single high-frequency transformer and reducing the design difficulty. For the MMC side capacitor voltage equalization strategy, the two

voltage equalization strategies are combined, and a grouped capacitor voltage equalization strategy combining voltage sequencing and cyclic switching is proposed, which has a better voltage equalization effect, less sampling information, and sampling. Case 3 introduces three-port DC-DC converter based on cascaded H bridges, which operates under extended-phase-shift (EPS) control.

For the case of multi-port output, the power transmission characteristics of the multi-port DC transformer are analyzed. In order to verify the feasibility of the topology and the effectiveness of the control strategy, the simulation verification is carried out in Matlab/Simulink, which is more compatible with the theoretical analysis.

This article analyzes and researches DC transformers based on MMC and cascaded H-bridges. Currently, a test prototype is being built. In the future, further in-depth research on fault ride-through, redundant control, and various actual operating conditions will be conducted through laboratory prototypes. To explore the feasibility of large-scale application of DC transformers with this structure in medium and low voltage DC distribution networks.

REFERENCES

[1] National Development and Reform Commission, "The 12th five-year plan for renewable energy development," *Solar Energy*, vol. 16, pp. 6–19, 2012.

[2] National Energy Administration, "Twelfth five-year Plan for wind power development," *Solar Energy*, vol. 20, pp. 7–18, 2012.

[3] National Energy Administration, "'Twelfth five-year plan' of solar power development," *Solar Energy*, vol. 18, pp. 6–13, 2012.

[4] D. Jovcic, "Step-up DC–DC converter for megawatt size applications," *IET Power Electron.*, vol. 2, no. 6, pp. 675–685, Nov. 2009.

[5] L. Jianguo *et al.*, "Switched capacitor access type dual active phase shift converter suitable for DC microgrid," *Proc. CSEE*, vol. 37, no. 17, pp. 4922–4930, 2017.

[6] L. Jianguo *et al.*, "Switched capacitor access type DC transformer suitable for medium and high voltage DC power grids," *J. Electr. Eng. Technol.*, vol. 033, no. 004, pp. 817–825, 2018.

[7] L. Zixin *et al.*, "Research on power electronic transformer for medium and high voltage intelligent distribution network," *Power Grid Technol.*, vol. 37, no. 09, pp. 2592–2601, 2013.

[8] J. Ke, F. Tao, C. Miao, W. Congbo, and B. Tianshu, "Line protection scheme of LCC-MMC hybrid DC distribution system," *J. Electr. Eng. Technol.*, vol. 36, no. 3, pp. 1–10, 2021, doi: 10.19595/j.cnki.1000-6753.tces.200003.

[9] W. Xinxin *et al.*, "Topological research on DC/DC converters for DC convergence of Yuanhai wind farm," *Chin. J. Electr. Eng.*, vol. 37, no. 03, pp. 837–848, 2017.

[10] G. Zhou, M. Jun, D. Ran, G. Rui, and F. Guangyao, "Modular multi-level DC transformer for DC distribution network based on extended phase shift control," *J. Electr. Eng. Technol.*, vol. 34, no. 13, pp. 2770–2781, ,2019.

[11] Y. Zhu, S. Shi, F. Wang, F. Zhuo, S. Cheng, and H. Yi, "Quasi square wave modulation with voltage transformation ability applied to modular multilevel DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 3050–3054, doi: 10.1109/ECCE.2018.8557397.

[12] S. Shi, F. Zhuo, S. Cheng, R. Ding, and Z. Zhao, "Research on multi-phase topology of F2F DC transformer and the control method," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia (ICPE, ECCE Asia)*, Busan, South Korea, 2019, pp. 1395–1400.

[13] S. Shi, F. Zhuo, Y. Zhu, S. Cheng, and F. Wang, "Research on control strategy of MMC DC power electronic transformer based on DAB mode," *IET Gener., Transmiss. Distrib.*, vol. 14, no. 21, pp. 4694–4702, Nov. 2020.

[14] B. Wang, Y. Liu, D. Lu, K. Yue, and R. Fan, "Transmission line fault location in MMC-HVDC grids based on dynamic state estimation and gradient descent," *IEEE Trans. Power Del.*, early access, Aug. 3, 2020, doi: 10.1109/TPWRD.2020.3013755.

[15] J. Mei, R. Ge, P. Zhu, G. Fan, B. Wang, and L. Yan, "An adaptive reclosing scheme for MMC-HVDC systems based on pulse injection from parallel energy absorption module," *IEEE Trans. Power Del.*, early access, Aug. 10, 2020, doi: 10.1109/TPWRD.2020.3015311.

[16] S. Yang, W. Xiang, M. Zhou, W. Zuo, and J. Wen, "A single-end protection scheme for hybrid MMC HVDC grids considering the impacts of the active fault current-limiting control," *IEEE Trans. Power Del.*, early access, Aug. 19, 2020, doi: 10.1109/TPWRD.2020.3017895.

[17] H. Xiao, K. Sun, J. Pan, and Y. Liu, "Operation and control of hybrid HVDC system with LCC and full-bridge MMC connected in parallel," *IET Gener., Transmiss. Distrib.*, vol. 14, no. 7, pp. 1344–1352, Apr. 2020.

[18] S. Yang, W. Xiang, and J. Wen, "An improved DC fault protection scheme independent of boundary components for MMC based HVDC grids," *IEEE Trans. Power Del.*, early access, Oct. 7, 2020, doi: 10.1109/TPWRD.2020.3029308.

[19] F. Z. Dejene, M. Abedrabbo, G. Bergna, J. Beerten, and D. Van Hertem, "Design of robust MMC controls considering HVDC grid protection: Small signal-based tuning," *IEEE Trans. Power Del.*, early access, Jan. 12, 2021, doi: 10.1109/TPWRD.2021.3051166.

[20] Y. Li, T. An, D. Zhang, X. Pei, K. Ji, and G. Tang, "Analysis and suppression control of high frequency resonance for MMC-HVDC system," *IEEE Trans. Power Del.*, early access, Jan. 8, 2021, doi: 10.1109/TPWRD.2021.3049973.

[21] J. Liu, D. Dong, and D. Zhang, "A hybrid modular multilevel converter family with higher power density and efficiency," *IEEE Trans. Power Electron.*, early access, Jan. 29, 2021, doi: 10.1109/TPEL.2021.3055690.

[22] S. Haq, S. P. Biswas, M. K. Hosain, M. A. Rahman, M. R. Islam, and S. Jahan, "A modular multilevel converter with an advanced PWM control technique for grid-tied photovoltaic system," *Energies*, vol. 14, no. 2, p. 331, Jan. 2021.

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