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A Temperature Stable Amplifier Characteristics of AlGa_N/Ga_N HEMTs on 3C-SiC/Si

ARIJIT BOSE¹, DEBALEEN BISWAS¹, SHIGEOMI HISHIKI², SUMITO OUCHI², KOICHI KITAHARA², KEISUKE KAWAMURA², AND AKIO WAKEJIMA¹, (Member, IEEE)

¹Department of Electrical and Mechanical Engineering, Nagoya Institute of Technology, Nagoya 466-8555, Japan

²SiC Division, Air Water Inc., Azumino 399-8204, Japan

Corresponding authors: Arijit Bose (arijeetbosu@gmail.com) and Debaleen Biswas (debaleenbiswas5@gmail.com)

ABSTRACT A high temperature stable amplifier characteristics for L-band or 2 GHz was studied using AlGa_N/Ga_N high electron mobility transistors (HEMTs) on 3C-SiC/Si substrate. A crack free, high quality AlGa_N/Ga_N heterostructure on a 6-inch Czochralski (Cz)-Si substrate was realized by metal oxide chemical vapor deposition (MOCVD). The epitaxial structure comprises an 8 μm thick nitride layer and a 1 μm thick 3C-SiC intermediate layer. The fabricated AlGa_N/Ga_N HEMT achieved excellent electron transport characteristics along with a comparable cutoff frequency (f_T) of 4.8 GHz for 2 μm gate length device. Temperature dependent S-parameter measurement of open pad structures achieved outstanding temperature stability up to 125 °C. Continuous wave power measurements showed a 2 GHz continuous wave power density of 2 W/mm, a maximum power added efficiency (PAE) of 47% along with a linear gain of 17.2 dB for class A amplifier operation. Moreover, at elevated temperature of up to 125 °C, the minimal power performance degradation was mainly attributed to the intrinsic property of the device, thus elimination of RF leakage from the buffer or epitaxial layers at high temperatures was confirmed.

INDEX TERMS Ga_N-on-Si HEMT, thick nitride layer, 3C-SiC intermediate layer, high temperature, f_T , g_m , open pad, P_{out} .

I. INTRODUCTION

In the field of high power and high frequency semiconductor device technologies, gallium nitride (Ga_N) has emerged as one of the most promising candidates for the past decades because of its high breakdown field and the high electron saturation velocity [1]–[3]. A high sheet carrier density of 2 dimensional electron gas (2DEG) is formed at AlGa_N/Ga_N interface due to the piezoelectric and spontaneous polarization, which makes AlGa_N/Ga_N heterostructure high electron mobility transistors (HEMTs) highly suitable for the above high frequency and high power electronics applications [4]. For RF applications of Ga_N HEMTs, typically SiC substrates are used owing to its certain advantages, such as high thermal conductivity and very low lattice mismatch to Ga_N [5], [6]. However, availability in small size and high market price of those substrates hinder wide applications. In response to

the above constraints, the cost-effective Ga_N-on-Si device technology can be an excellent alternative. However, it is difficult to grow a Ga_N film on Si due to high thermal and lattice mismatch which generate large tensile stress resulting in dislocation and huge cracks in the epi-structure [7], [8]. To overcome these challenges, different approaches were implemented, such as the use of an AlN layer, a strained layer superlattice (SLS) structure, an InAlN buffer layer and a SiC intermediate layer on Si substrate [9]–[17]. In this work, we opted for a high quality 3C-SiC intermediate layer between Ga_N and Si to achieve a crack-free, high quality Ga_N film on Si. The thermal and lattice mismatch between Ga_N and Si can be minimized by 3C-SiC intermediate layer which can also prevent the melt back reaction [18]. In the case of high-resistivity Si (HR-Si), the intrinsic carrier density significantly increases at high temperature and these carriers generate huge RF loss [19]. However, at high temperature, there is also a possibility of generation of charge carriers in the buffer layers for Ga_N devices on low resistivity (LR-Si)

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substrates. The generation of these charge carriers results in the degradation of the device performance [20]. Another problem with LR-Si is that it generates large parasitic capacitance which also deteriorates the high frequency performance of the device. Hence, the generation of charge carriers and the effect of low resistivity need to be eliminated to effectively use GaN-on-Si HEMTs in RF applications. It is already reported that the effect of low resistivity Si (LR-Si) substrate can be eliminated by using a thick nitride layer [21]. Taking that into consideration, we also used a very thick nitride layer on Si to give the device a better temperature stability by suppressing the generation of charge carriers at high temperature. In addition, significant output power performance is also needed to be confirmed in order to use the device for the commercial RF applications, such as cellular base stations or radars. Hence, detailed investigation of the temperature impact on the RF performance of GaN HEMTs is necessary for deep understanding of thermal stability to establish their feasibility in next-generation commercial RF applications. There are several reported studies on the temperature impact on microwave performance in high periphery GaN HEMTs [22]–[27], however there are no reports available on the temperature dependent detailed DC and RF performance analysis of thick GaN HEMTs on 3C-SiC/Si structure.

In this study, we used a thick nitride layer of $8\ \mu\text{m}$ on Si to get a significant RF performance. The 2DEG property of AlGaN/GaN heterostructure exhibited excellent mobility of $2110\ \text{cm}^2/\text{V}\cdot\text{s}$ with a sheet resistance of $280\ \Omega/\square$. Small-signal characteristics achieved a cutoff frequency of $4.8\ \text{GHz}$ for a device with gate length (L_g) of $2\ \mu\text{m}$ and gate width of $2 \times 50\ \mu\text{m}$. Temperature dependent S-parameter of the open pad structures confirmed the suppression of generation of charge carriers, thus very low RF leakage at the high temperature of up to $125\ ^\circ\text{C}$. At room temperature, the device achieved a PAE of 47% while delivering a $2\ \text{W}/\text{mm}$ output power along with a $17.2\ \text{dB}$ of maximum linear gain at drain and gate bias of $+22.5$ and $-1.5\ \text{V}$, respectively. The primitive study of the device performance of the reported GaN on 3C-SiC/Si structure was reported in [21]. Present Study on high temperature stable amplifier performance established the overall effectiveness of the reported structure.

II. GROWTH AND FABRICATION

A high quality, crack free AlGaN/GaN heterostructure with thick nitride layer was grown by metal oxide chemical vapor deposition (MOCVD) on a commercially prepared, low resistive 3C-SiC / Cz-Si substrate of 6-inch diameter. AlGaN/GaN HEMTs were fabricated on the above epitaxial structure. A cross-sectional view of the fabricated device is depicted in Fig. 1. The epitaxial stack comprises a $1\ \mu\text{m}$ thick 3C-SiC intermediate layer on 6-inch Cz-Si substrate, a $2\ \mu\text{m}$ thick III-N buffer layer containing Al, a $6\ \mu\text{m}$ thick GaN layer and a $23\ \text{nm}$ thick AlGaN barrier layer. Typically, the Al mole fraction in AlGaN/GaN heterostructure is in the range of 15-30% for barrier thickness of 15-30 nm [28]–[30]. In this work, an Al composition of 26% was used in the

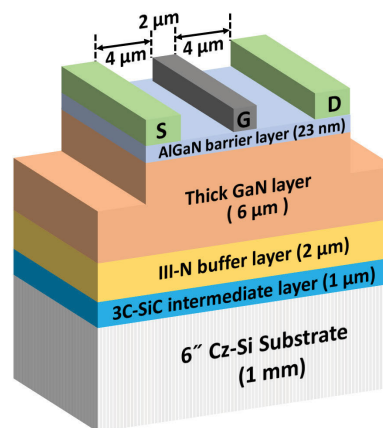


FIGURE 1. The cross-sectional structure of the fabricated AlGaN/GaN HEMT on 6-inch Cz-Si with $8\ \mu\text{m}$ thick nitride and $1\ \mu\text{m}$ thick 3C-SiC intermediate layer. The S, G, and D stand for source, gate, and drain respectively. Gate to source (L_{gs}), gate (L_g) and gate to drain (L_{gd}) lengths were 4, 2, $4\ \mu\text{m}$, respectively.

AlGaN barrier layer to achieve high electron mobility and sheet carrier density. The thick GaN layer is a combination of carbon doped (C-GaN) and unintentionally doped (u-GaN) regions where the thickness of the u-GaN region is approximately one-tenth of the total GaN layer. The Carbon doping concentration in the C-GaN region was measured to be $< 10^{19}\ \text{cm}^{-3}$. The high quality nitride epitaxial layer was realized with 5 mm edge exclusion. We defined the substrate displacement by SORI, which we stably controlled at less than $50\ \mu\text{m}$. Afterwards, room temperature Hall measurements were performed on the epitaxial structure to estimate the electron transport parameters, such as mobility (μ), two-dimensional electron gas (2DEG) carrier concentration (N_s), and 2DEG sheet resistance (R_{sh}). The measured μ was $2110\ \text{cm}^2/\text{V}\cdot\text{s}$ which was translated from the obtained R_{sh} of $280\ \Omega/\square$ and N_s of $1.06 \times 10^{13}\ \text{cm}^{-2}$. However, at high temperature, a significant increment of phonon concentration causes increased scattering which lowers the mobility and increases the sheet resistance of the epitaxial structure significantly [31]–[33] which slightly degrades the DC and RF performance of the device.

For the device fabrication, firstly BCl_3 plasma-based reactive ion etching (RIE) was used to get approximately 300-nm deep mesa isolation. The source and drain areas were precisely defined by UV photo-lithography technique. Ohmic contacts were formed by using rapid thermal annealing (RTA) at $850\ ^\circ\text{C}$ for 30 seconds in N_2 environment right after depositing the Ti/Al/Ni/Au metal stack by electron beam (e-beam) evaporation. Finally, a Ni/Au metal composite was deposited using e-beam evaporation to form the gate electrodes.

III. RESULTS AND DISCUSSION

A. DC CHARACTERISTICS

Fig. 2 (a) depicts the DC (I_d - V_d) characteristics of the fabricated AlGaN/GaN HEMT on 3C-SiC/Si. The drain voltage

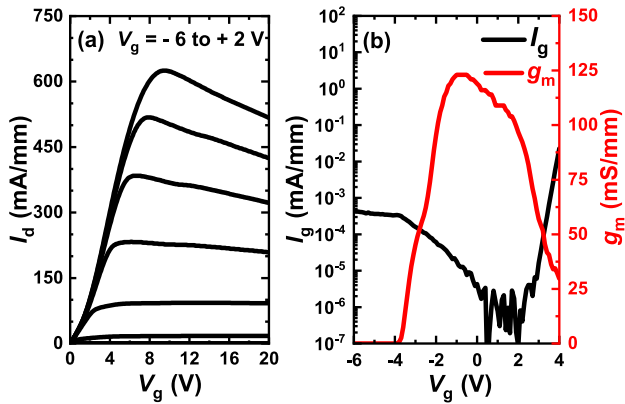


FIGURE 2. (a) Static I_d - V_d characteristics of the device where gate voltage (V_g) was varied from -6 V to $+2$ V in 1 V increments. (b) I_g - g_m characteristics of the device at $V_d = +10$ V and V_g was swept from -6 V to $+4$ V. The device dimension was $L_{gs}/L_g/L_{gd} = 4/2/4$ μm .

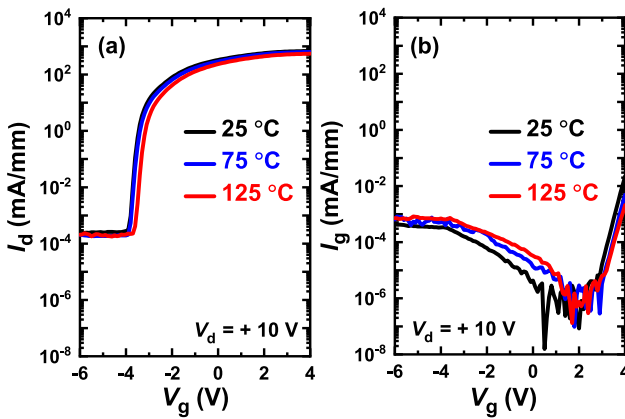


FIGURE 3. Transfer (a) I_d - V_g , and (b) I_g - V_g characteristics of the device where V_g was varied from -6 V to $+4$ V and V_d was fixed at $+10$ V. The device dimension was $L_{gs}/L_g/L_{gd} = 4/2/4$ μm .

(V_d) was varied from 0 to $+20$ V and the gate bias (V_g) was swept from -6 to $+2$ V in 1 V increments. The device attained a drain current density (I_d) of 625 mA/mm at $V_g = +2$ V with a specific on resistance ($R_{on,sp}$) of 1.1 $\Omega\text{-cm}$. The transfer characteristics were measured at $V_d = +10$ V. A gate leakage current density (I_g) of $\sim 4.5 \times 10^{-4}$ mA/mm and a peak transconductance ($g_{m,max}$) of 123 mS/mm at $V_g = -1$ V were attained, displayed in Fig. 2 (b). The threshold voltage (V_{th}) was -2.8 V. The transfer characteristics of the device with varying temperature are shown in Fig. 3 (a) and (b). From Fig. 3 (a), it can be seen that the off-state leakage current is significantly stable even at 125 $^{\circ}\text{C}$. In Fig. 3 (b), temperature dependent I_g - V_g characteristics are shown. The V_d was fixed at $+10$ V, for both the I_d - V_g and I_g - V_g characteristics.

Temperature dependency of g_m was measured for temperature range of 25 to 125 $^{\circ}\text{C}$ with a step of 25 $^{\circ}\text{C}$. In Fig. 4 (a), g_m at 25, 75, and 125 $^{\circ}\text{C}$ are shown where a gradual decrement of g_m was observed. It is mainly because of degraded 2DEG mobility with temperatures due to phonon scattering

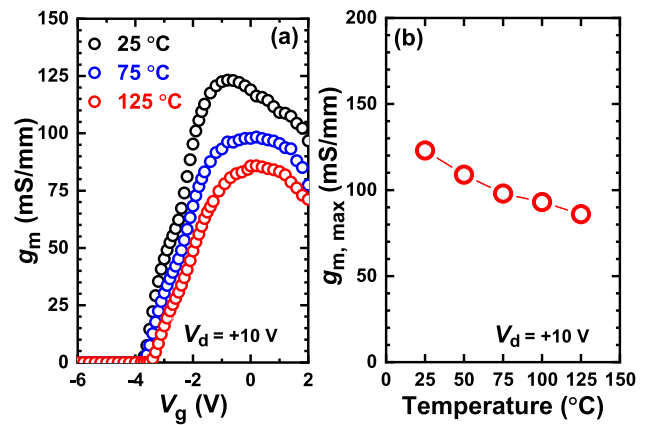


FIGURE 4. (a) Temperature dependent transconductance density (g_m) at 25, 75, and 125. (b) Measured $g_{m,max}$ at 25, 50, 75, 100, and 125 $^{\circ}\text{C}$.

phenomenon, as discussed earlier. In addition, electron saturation velocity also decreases at high temperatures along with an increment in device non-linearity [33]. For the above reason, peak transconductance was reduced to 86 mS/mm and $R_{on,sp}$ was increased to 1.54 $\Omega\text{-cm}$ at 125 $^{\circ}\text{C}$. In Fig. 4 (b), the values of maximum g_m densities at every temperature points were plotted. The threshold voltages at all the temperature points remained almost constant because of the invariant 2DEG density at AlGaN/GaN interface even at high temperatures. At 125 $^{\circ}\text{C}$, V_{th} was -2.5 V which is almost the same as the room temperature V_{th} of -2.8 V. From the above results, we observed that the degradation of the DC performance was quite low and consistent with temperature. Therefore, the temperature dependency of 2DEG properties is solely responsible for the above. Moreover, at high temperatures there is a possibility of high leakage from the buffer or epitaxial layers due to generation of charge carriers which hugely affects the RF performance of the device. However, in our case, a very small detrimental high temperature effect on DC performance primitively indicates no buffer leakage even at a high temperature of 125 $^{\circ}\text{C}$.

B. SMALL-SIGNAL CHARACTERISTICS

Small-signal RF characteristics of the device with L_g and gate width (W_g) of 2 and 2×50 μm , respectively and their temperature dependency were characterized by a P5004A vector network analyzer. On-wafer temperature dependent S-parameters were evaluated in the frequency range of 0.5 to 20 GHz and the temperature was varied from 25 to 125 $^{\circ}\text{C}$ with a 25 $^{\circ}\text{C}$ interval. In Fig. 5 (a) and (b), unilateral Mason's gain (U) and small-signal current gain ($|H_{21}|$) vs frequency were plotted at 25, 75, and 125 $^{\circ}\text{C}$. The cutoff frequency (f_T) and a maximum frequency of oscillation (f_{max}) were estimated from $|H_{21}|$ and U, respectively. Evaluated values of f_T and f_{max} at room temperature were 4.8 and 10 GHz, respectively under $g_{m,max}$ biasing condition of $V_g = -1$ V and $V_d = +10$ V. The f_T of our device is well comparable with the previously reported results of GaN HEMTs on different

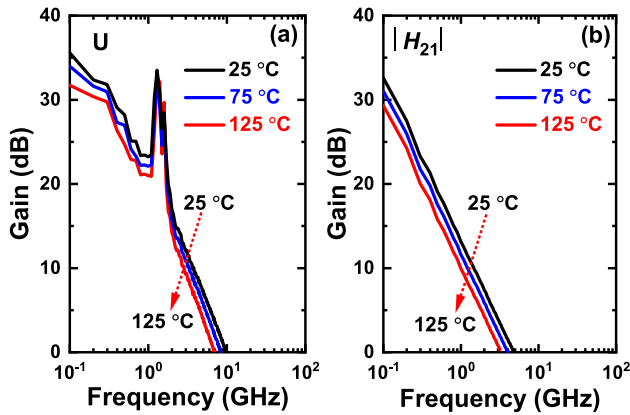


FIGURE 5. (a) Temperature dependent Mason's unilateral gain (U), and (b) current gain $|H_{21}|$ vs frequency. U and $|H_{21}|$ were plotted at 25, 75, and 125 °C for 2 μm gate length device at $V_d = +10\text{ V}$ and $V_g = -1\text{ V}$.

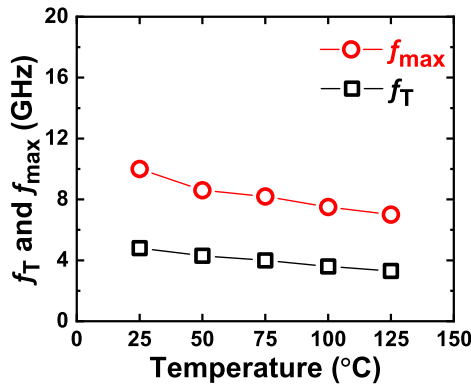


FIGURE 6. f_T and f_{max} at 25, 50, 75, 100, and 125 °C for the 2 μm gate length device at $V_d = +10\text{ V}$ and $V_g = -1\text{ V}$.

substrates, following the relationship $f_T \propto L_g^{-1}$ [21]. The estimated values of f_T and f_{max} at all temperatures are plotted in Fig. 6 where it can be seen that f_T and f_{max} were slightly deteriorated with increasing temperatures. The degradation of f_T is also associated with deterioration of 2DEG likewise the DC performance at high temperatures. Because f_T is an intrinsic property like g_m and their relationship is shown in Eq. 1, [34], [35] where C_{gg} is the total gate capacitance. C_{gg} can also be expressed as $(C_{\text{gs}} + C_{\text{gd}})$, where C_{gs} and C_{gd} represent intrinsic gate-to-source and gate-to-drain capacitances, respectively.

$$f_T = \frac{g_m}{2\pi C_{\text{gg}}} = \frac{g_m}{2\pi(C_{\text{gs}} + C_{\text{gd}})} \quad (1)$$

To confirm the dependence of f_T on g_m , we extracted g_m at every temperature point using Eq. 1 and compared with the measured g_m from DC characteristics. For the evaluation of g_m from f_T , C_{gg} was taken as 0.43 pF, extracted using the small-signal equivalent circuit model of Dambrine *et al.* [36]. Moreover, to gain a better understanding of the achieved microwave characteristics, we also extracted temperature dependent small-signal equivalent circuit parameters. The

extracted temperature dependent intrinsic and extrinsic parameters showed minimum temperature sensitivity except for the intrinsic g_m and input resistance (R_i) and the trend of these parameters agrees with Ref. [25]. The extracted values of intrinsic g_m and R_i at room temperature were 148 mS/mm and 19.9 Ω , whereas at 125 °C, it were 106 mS/mm and 28.4 Ω , respectively. The comparison between g_m measured from DC characteristics, extracted from S-parameters and calculated from Eq. 1, is presented in Fig. 7. It can be seen that both the g_m measured from DC characteristics and calculated from Eq. 1, are very closely comparable which confirmed that the small degradation in small-signal performance was mainly due to the 2DEG properties of the AlGaIn/GaN interface. If there was a generation of charge carriers at high temperatures, the g_m values were not be comparable owing to high leakage through the epitaxial layers. In addition, the extracted intrinsic g_m from S-parameters also consistent with our measurement results. Thus, suppression of RF leakage at high temperatures was successfully attained and significant temperature stability was observed in the reported GaN HEMT on 3C-SiC/Si.

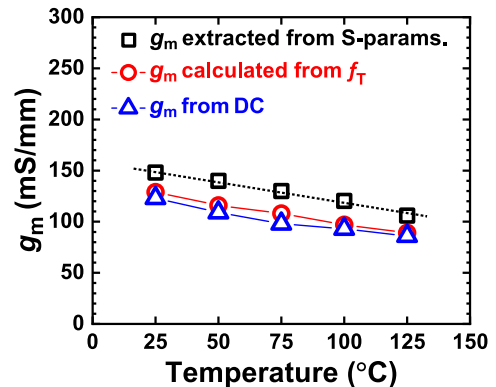


FIGURE 7. A Comparison between extracted g_m from S-parameters, calculated g_m from Eq. 1, and measured peak g_m from DC characteristics with varying temperature.

Further, loss evaluation at high temperatures was analyzed by temperature dependent on-wafer S-parameter measurements on the open pad structures in 0.5 to 20 GHz frequency range. In the same previous way, the temperature was varied from 25 to 125 °C in 25 °C increments. Very low and unaltered S-parameter (S_{11}) of the open pad structures were observed from Fig. 8, where S_{11} at 25, 75, and 125 °C are represented. The above observation also indicates thermal stability of the device. Hence, it can be said that the thick nitride layer efficiently suppressed the increment of charge carrier density at high temperature and there was no evidence of leakage from the epitaxial layers of the device.

C. LOAD-PULL MEASUREMENTS

Continuous wave (CW) on-wafer RF power measurements were carried out using a load-pull measurement system at 2 GHz fundamental frequency on the device with L_g and W_g

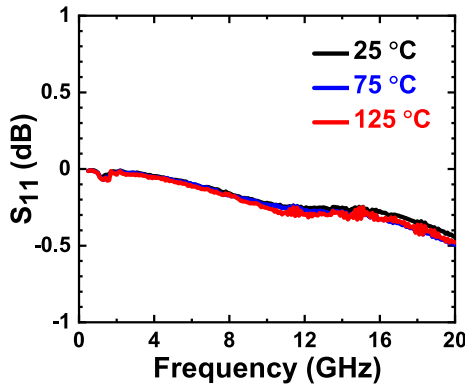


FIGURE 8. S_{11} of the open pad structures at 25, 75, and 125 °C in the frequency range of 0.5 to 20 GHz.

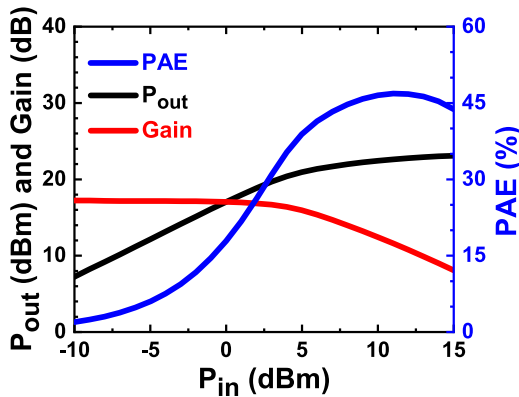


FIGURE 9. CW power measurement of the AlGaIn/GaN HEMT with L_g of 2 μm and W_g of 2 \times 50 μm at 2 GHz fundamental frequency. The biasing conditions for optimum PAE were $V_d = +22.5$ V and $V_g = -1.5$ V.

of 2 and 2 \times 50 μm , respectively. The gate was biased at -1.5 V for class A amplifier operation and V_d was varied from + 10 to + 30 V. Input and output impedances were matched for the optimum PAE. At $V_d = +22.5$ V, the input (P_{in}) vs output power (P_{out}) response exhibited a maximum PAE of 47% while delivering 23.1 dBm output power with a maximum linear gain of 17.2 dB, displayed in Fig. 9. The associated drain efficiency (D.E) was calculated to be 51.5%, which almost similar to the output efficiency of an ideal class A amplifier which is 50%. Drain bias dependency of PAE and P_{out} is shown in Fig. 10, where the output power and PAE saturated at V_d of + 22.5 V and slightly deteriorated beyond that. We assume that, current collapse beyond drain bias of + 22.5 V is the reason for the small degradation of P_{out} and PAE. RF output power of a class A amplifier follows the equation 2, where P_{out} is proportional to maximum drain voltage swing or ($2 \times V_d$) and maximum drain current swing (I_{max} or $2 \times I_d$).

$$P_{out} = \frac{1}{8} \times 2V_D \times I_{max} \quad (2)$$

Using Eq. 2, P_{out} was calculated for 10, 15, 17.5, 20, and 22.5 V drain bias taking I_{max} as drain current at $V_g = 0$ V.

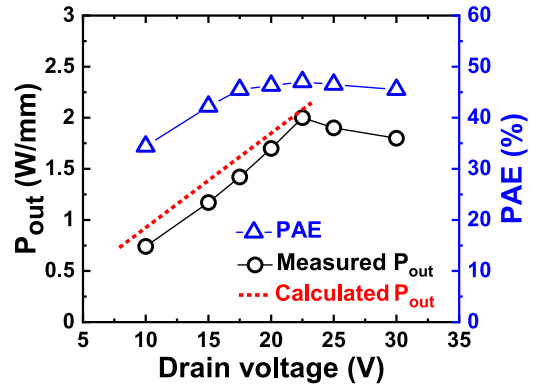


FIGURE 10. Drain bias dependency of P_{out} and PAE where V_d was varied from + 10 to + 30 V and V_g was -1.5 V. The red line is the calculated P_{out} from Eq. 2 at each drain biasing point upto $V_d = +22.5$ V.

Extracted data was compared with P_{out} obtained from CW power measurement. As represented in Fig. 10, both the P_{out} up to + 22.5 V showed excellent comparability and continuity.

Temperature dependent power performance of the device was also evaluated. The biasing was set at optimum conditions for maximum PAE and output power, which were $V_d = +22.5$ V and $V_g = -1.5$ V. The temperature was varied from 25 to 125 °C in a 25 °C increment. P_{out} , gain, and PAE vs P_{in} characteristics at 25, 75, and 125 °C, are shown in Fig. 11 (a) and (b). With increasing temperature, a small degradation of gain, P_{out} and PAE was observed. As in our case, as the drain bias was fixed at + 22.5 V, there was no change in the voltage swing which means the decrement of P_{out} is mainly because of the deterioration of I_d . It is already discussed that, a significant increment of phonon concentration at high temperature causes increased scattering which crucially degrades the mobility of the epitaxial structure, thus degrades the I_d . Moreover, we calculated P_{out} at every

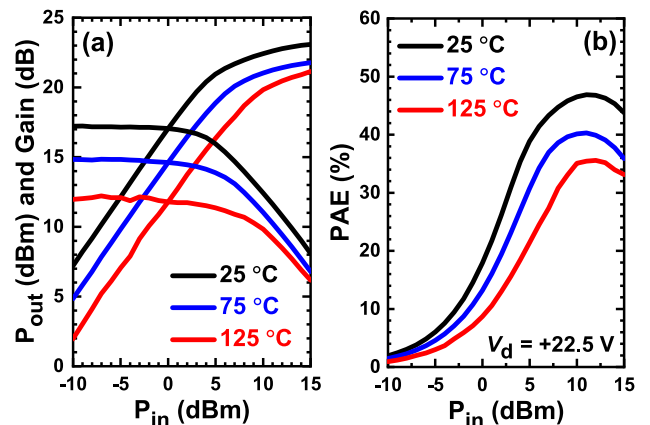


FIGURE 11. (a) Temperature dependent P_{out} and gain, and (b) Temperature dependence of PAE at $V_d = +22.5$ V and $V_g = -1.5$ V of the device with $L_g = 2$ μm and $W_g = 2 \times 50$ μm . The temperature was varied from 25 to 125 °C with a step of 25 °C.

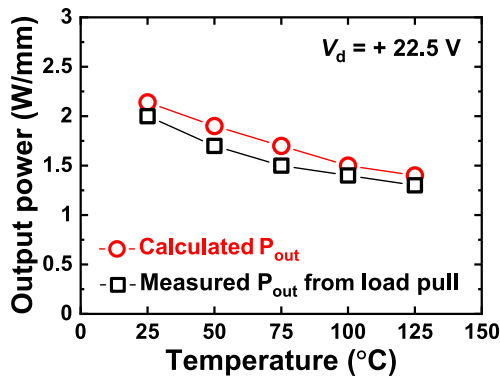


FIGURE 12. A Comparison between evaluated P_{out} from temperature dependent load pull measurement and calculated P_{out} from Eq. 2 at each temperature point.

TABLE 1. Comparison of P_{out} and PAE with previously reported results.

References	$\Delta P_{out} / \text{temp}$ (K^{-1})	$\Delta \text{PAE} / \text{temp}$ (K^{-1})	Frequency (GHz)
Present Work	0.0035	0.002	2
Ref. [26]	0.002	0.0013	3
Ref. [27]	0.004	—	2

temperature point using Eq. 2, where V_d was fixed at +22.5 V and I_d was taken for $V_g = 0$ V. The calculated P_{out} at each temperature point was also compared with the P_{out} measured from load pull, as depicted in Fig. 12. Excellent comparability between the calculated and measured P_{out} strongly confirmed that the slightly degraded power performance was strongly due to the temperature dependency of drain current. It further confirms that there was no buffer or substrate leakage from the device and the possibility of charge carrier increment at high temperature was also eliminated. A comparative study of the decremental rate of P_{out} and PAE is shown in Table. 1 [26], [27]. The rate of change of P_{out} and PAE with temperature, denoted as $\Delta P_{out} / \text{temp}$ and $\Delta \text{PAE} / \text{temp}$, respectively are calculated by taking the rate of decrement for 1 K temperature change, which can be demonstrated as Eq. 3.

$$\Delta P_{out}/\text{temp} = \frac{P_{out}(RT) - P_{out}(HT)}{P_{out}(RT)} / \Delta T \quad (3)$$

In Eq. 3, $P_{out}(RT)$ is the output power at room temperature, $P_{out}(HT)$ is the output power at the highest temperature, and ΔT is the difference between the highest and room temperature. $\Delta \text{PAE} / \text{temp}$ is also calculated in the same way as $\Delta P_{out} / \text{temp}$. The above data also demonstrates the comparable amplifier characteristics of our device.

IV. CONCLUSION

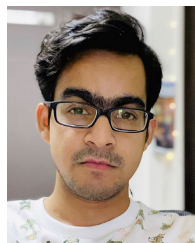
We observed a significant and high temperature stable amplifier performance in GaN HEMTs on 3C-SiC/Si by introducing an 8 μm thick nitride layer, grown via a 3C-SiC intermediate layer. Temperature dependent small-signal characteristics showed excellent stability even at a high temperature of up to 125 °C. At room temperature, the device

achieved a well comparable f_T of 4.8 GHz for a 2 μm gate length device. Very low and identical S_{11} of the open pad structures were observed in the temperature range of 25 to 125 °C which confirmed the suppression of generation of charge carriers at high temperature. From room temperature CW power measurements, a maximum output power of 2 W/mm along with a PAE of 47% and a 17.2 dB of maximum linear gain were obtained. Comparative study of gain and power performance further confirmed that the detrimental effect of high temperature on DC and RF characteristics was mainly because of the intrinsic property i.e. mobility of the epitaxial structure. Summing up all the results, it can be concluded that the presented GaN HEMT on 3C-SiC/Si showed excellent stable amplifier characteristics by suppressing any sort of leakage through the epitaxial layers. Hence, this work emphasizes on detailed investigation of the thermal impact on both DC and RF performance of thick GaN HEMT on 3C-SiC/Si which can be an outstanding candidate for next generation commercial RF applications as it can deliver significant RF performance, as well as cost effectiveness.

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ARIJIT BOSE was born in West Bengal, India, in 1992. He received the bachelor's degree in physics from the University of Calcutta, India, and the master's degree in instrumentation (applied physics) from Jadavpur University, India. He is currently pursuing the Ph.D. degree with the Department of Electrical and Mechanical Engineering, Nagoya Institute of Technology, Japan. He also worked as a Project Student at the Saha Institute of Nuclear Physics, Kolkata, India. His research interests include Gallium nitride (GaN) based semiconductor device technology and its applications in high-power and high-frequency domain.



DEBALEEN BISWAS was born in Krishnanagar, West Bengal, India, in 1989. He received the B.Sc. degree (Hons.) from the Abhedananda Mahavidyalaya, under the affiliation of The University of Burdwan, India, the M.Sc. degree from the University of Calcutta, India, and the Ph.D. degree from the University of Calcutta, in 2017, all in physics. He started his research work at the Saha Institute of Nuclear Physics, Kolkata, as a Research Fellow. In 2018, he joined the Nagoya Institute of Technology (NITech), Japan, as a Postdoctoral Researcher. His current research interests include GaN-based devices for high-power and high-frequency applications.



power and high frequency application.

SHIGEOMI HISHIKI was born in Chiba, Japan, in 1977. He received the B.S. degree in science from Nihon University, Japan, in 2000, the M.S. degree in chemical engineering from the University of Yamanashi, Japan, in 2002, and the Ph.D. degree in engineering from Kyoto University, Kyoto, Japan, in 2006. He is currently a Senior Assistant Manager with Air Water Inc., Azumino, Japan. His research interests include GaN based semiconductor device fabrication process for high



he moved to the Advanced Technology Research Laboratories, Nippon Steel Corporation, Yamaguchi, Japan, where he was a Senior Researcher and was engaged in establishing commercial production processes of large-diameter separation-by-implanted-oxygen (SIMOX)-SOI wafers. From 2001 to 2007, he was a Senior Researcher with Siltronic Japan Corporation, Yamaguchi, and his research themes were defect control and electrical characterization for the following semiconductor materials, SIMOX, strained-Si-on-insulator (s-Si-OI), Ge-on-insulator (Ge-OI), and ion-beam-synthesized-SiC (IBS-SiC). In 2008, he became the General Manager of the Division of Research and Development, Air Water Inc., Osaka, and Nagano, Japan, and since then, he has been engaged in the research and development of 3C-SiC/Si and GaN/3C-SiC hetero-epitaxy. In 2018, he became a Visiting Professor with the Global Innovation Center (GIC), Kyushu University, where his research themes have been defect control and doping technology development of 3C-SiC crystal for high-temperature operation MOSFETs.

KEISUKE KAWAMURA was born in Tokyo, Japan, in 1968. He received the B.S. degree in applied physics from The University of Tokyo, Tokyo, in 1992, and the Ph.D. degree in material science and engineering from Kyushu University, Fukuoka, Japan, in 2006. In 1992, he joined the Electronic Research Laboratories, Nippon Steel Corporation, Japan, where he was engaged in process optimization and characterization of thin-film-Si-on-insulator (TFSOI)-MOSFETs. In 1995,



his current research interest includes GaN epitaxial growth and crystal evaluation.

SUMITO OUCHI was born in Hokkaido, Japan, in 1987. He received the M.S. degree in electrical and electronic engineering from Mie University, Japan, in 2012. He is currently an Assistant Manager with Air Water Inc., Azumino, Japan. His current research interest includes GaN epitaxial growth and crystal evaluation.



His current research interests include GaN HEMTs for microwave wireless power transfer and 6G cellular base station amplifiers.

KOICHI KITAHARA was born in Kitakyushu, Fukuoka, Japan, in 1966. He received the M.S. degree in electrical and electronic engineering from the Kyushu Institute of Technology, Japan, in 1992. He is currently the Manager of Air Water Inc., Azumino, Japan. His current research interest includes 3C-SiC epitaxial growth on Si wafer.



he spent an academic year at the Georgia Institute of Technology, Atlanta, where he worked on antenna design for ultra-wideband (UWB) communication and UWB signal simulation. In 2010, he joined the Nagoya Institute of Technology, where he was engaged in the research of GaN-HEMTs. His current research interests include GaN HEMTs for microwave wireless power transfer and 6G cellular base station amplifiers.

AKIO WAKEJIMA (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from Osaka University, Osaka, Japan, in 1992, 1994, and 2007, respectively. In 1994, he joined NEC Corporation, Japan, where he had been engaged in research and development of III-V compound semiconductor devices for microwave and millimeter-wave applications. He was then an Assistant Manager of the Photonic and Wireless Devices Research Laboratories, NEC Corporation. From 2002 to 2003,

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