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Implementation of Optimization-Based PI Controller Tuning for Non-Ideal Differential Boost Inverter

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ABSTRACT The demand for renewable energy to sustain today's vulnerability towards depleting fossil fuels is a crucial agenda for research. Various inverter topologies have been proposed to convert renewable sources into a usable form. But output THD, additional filtering components at line frequency (leading to bulky circuitry), lower efficiency, etc., are some of the limitations faced in all those topologies. This paper aims to change a voltage source inverter's traditional behavior, which generates lesser output voltage with higher THD. The paper proposes a closed-loop non-ideal differential boost inverter (DBI) employing a PI controller. The optimization techniques such as, genetic algorithm (GA) and bacterial foraging optimization algorithm (BFOA) are incorporated to accentuate the PI controller's performance to produce a better response during line and load disturbance conditions with reduced THD. DBI performance is evaluated on a laboratory prototype with different loading conditions. A comparison between the algorithms and the previous topologies from the literature survey has also been provided to validate this research's claims. This paper's required simulation study is carried out using MATLAB, and real-time validation is carried out using dSPACE 1104 with sampling time of one μs.

INDEX TERMS Average modeling, bacterial foraging optimization algorithm (BFOA), differential boost inverter (DBI), genetic algorithm (GA), small signal modeling, tuning of PI controller.

NOMENCLATURE

R_0	Load resistor
S_1 to S_4	Bidirectional IGBT switches
d, $\hat{d}$	Large signal and small signal duty cycles
D	Steady-state duty cycle
v_0, $\hat{v}_0$	Large signal and small signal output voltages
V_0	Steady-state output voltage
V_M	Peak value of output voltage
v_g, $\hat{v}_g$	Large signal and small signal input voltages
V_g	Steady-state input voltage
i_g	Source current
v_{C_1}, $\hat{v}_{C_1}$	Large and small signal capacitor-1 voltages
V_{C_1}, V_{C_2}	Steady-state capacitor-1 and capacitor-2 voltages
v_{C_2}, $\hat{v}_{C_2}$	Large and small signal capacitor-2 voltages
i_z, $\hat{i}_z$	Large and small signal load currents
I_Z	Steady state load current
i_{L_1}, $\hat{i}_{L_1}$	Large and small signal inductor-1 currents
I_{L_1}, I_{L_2}	Steady state inductor-1 and inductor-2 currents
i_{L_2}, $\hat{i}_{L_2}$	Large and small signal inductor-2 currents
i_{C_1}, i_{C_2}	Capacitor-1 and capacitor-2 currents
r_{ON}	Resistance during on-time of switch
r_{L_1}, r_{L_2}	Internal resistances of high frequency inductors
k_P, k_I	PI controller parameters
t_r, t_s	Rise time and settling time
P_0	Peak overshoot
E_{SS}	Steady-state error

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I. INTRODUCTION

Inverters are a great addition to the power electronics world due to their ability to convert DC renewable sources' energy to AC usable form. Generally, the DC to AC

TABLE 1. State-of-the-art in boost inverter.

Topology	Ref.	Power rating (W)	Input voltage (V)	Output voltage (V)	Voltage gain	Switching frequency (kHz)	Control/ modulation technique	No. of active devices	No. of memory elements	% THD
Hybrid energy storage system	[1]	50	24	60	2.5	20	SMC	8	8	-
Grid-connected fuel cell system	[5], [6]	1000	42	220	5.23	20	DLC	7	9	4
Active buck–boost inverter	[2]	500	100 – 200	110	0.55-1.1	20	SPWM	8	2	-
Boost inverter	[7]	1000	50	220	4.4	20	DLC	4	4	5.70
DBI	[8]	44	25	42	1.68	50	DLM	4	4	6.29
Inverse Watkins–Johnson	[9]	-	53	140	2.6	10	SPWM	6	4	-
Switched-capacitor DBI	[10]	250	60	325	5.4	50	SPWM	8	6	6.1
Single-stage sine-wave inverter	[11]	4.84	16	22	1.375	10	SPWM	4	4	10.80
Boost inverter	[3], [12]	270	96	180	1.875	20	SMC	4	4	-
Boost inverter	[13]	175	55	270	4.9	20	VMC	4	4	2.35
GA-based tuning of PI controller for boost inverter	[14]	220	60	311	5.18	20	VMC	4	4	2.97
BFOA-based tuning of PI controller for boost inverter	[15]	55	36	155	4.3	20	VMC	4	4	4.22

boost converters can be broadly classified into three categories: (i) single-phase grid-connected battery-super capacitor hybrid energy storage system [1], (ii) active buck-boost full-bridge inverter [2], and (iii) boost-inverter [3]. Here the main challenges faced lie in the development of a low-cost, high-efficiency, high gain, and low THD topology, with small size power conversion system. On this note, the use of a differential boost inverter (DBI) is of choice. A DBI topology employs a single-stage power conversion from DC to AC. It uses differential boost converters, which are being controlled by two positive DC biased clamping sinusoidal references which are out of phase-shifted. The differences in the output of the converters produce an AC output voltage [3]. The possibility of generating higher AC output voltage from a comparatively lower input DC voltage, employing a single power conversion stage, is advantageous.

The DBI topology used in the literature comprises four ports (two power ports and two signal ports) [4]. The unregulated input and the regulated output represent two power ports, whereas the controlled input (duty cycle) and the sensed feedback signals represent two signal ports. TABLE 1 summarizes various attributes of DBIs, such as control strategies, modulation techniques, switching frequencies, etc. It is to mention here that the topologies compared in the table have different voltage, power ratings and are used for various applications. Further, the control technique employed uses many control parameters and feedback, leading to complexity in design. The use of diversifying control techniques in those studies is mainly because of their applications. The voltage mode control (VMC) technique is simple and well established whereas, the other control techniques such as sliding mode control (SMC) and double loop control (DLC) are primarily appreciated for their control mechanism's added flexibility. But, they have some lacunae. The SMC [1], [3], [12] and DLC [5], [6], [7] techniques require a minimum of four feedbacks for a fixed input voltage, and the number may further increase for the increase in feedback parameters as well as the multiple-input case. In [8], VMC and dynamic linearizing modulator (DLM) for DBI achieve stabilized output for a wide range of frequencies. Further, the feedbacks may drastically increase in number, or complexity may increase under the line and load disturbance conditions. A proper selection of the controller parameters in the case of VMC can tackle the issues described above. It is further to highlight that most of the above studies used the mathematical modeling of only one-half of the DBI, which indicates that the complete structure is not mathematically analyzed for the non-ideal case. As a result, the selection of controller parameters will be difficult under real-time disturbance conditions.

A close inspection on the DBI literature reveals that,

(i) The use of mathematical models is only applied for a second-order system, i.e., for one-half of the DBI [4].
(ii) A forth order mathematical modeling employed in [13], though accounts for non-ideal cases; stability analysis is not carried out.
(iii) The topologies in [1], [3] [5]–[7], [10], [12] have employed intricate control strategies involving more control parameters leading to a bulky structure.
(iv) An intuitive way of determining controller parameters by comparing multiple optimization algorithms has never been suggested in the literature.

Following the above research gaps in the literature, this research aims to provide a perfect DBI topology solution via mathematical modeling of the fourth-order non-ideal DBI system. The paper's significant contributions are listed underneath.

(i) The controller parameters' selection is taken from the root locus plot, and the parameters' range values are confirmed from the stability region in the plot.
(ii) The controller parameters are tuned in the confirmed stability region using optimization techniques, genetic algorithm (GA), and bacterial foraging optimization algorithm BFOA) to achieve a high-quality output sine wave with lower THD under line and load disturbances.
(iii) The outcome is experimentally tested to be stable under the line and load disturbance conditions.

(iv) The obtained results under different voltage levels, power values, and load types using an experimental set-up attest to the proposed scheme's suitability for a real-time application.

The research flowchart for the proposed topology of the non-ideal boost inverter scheme is elucidated in Fig. 1 for better clarity.

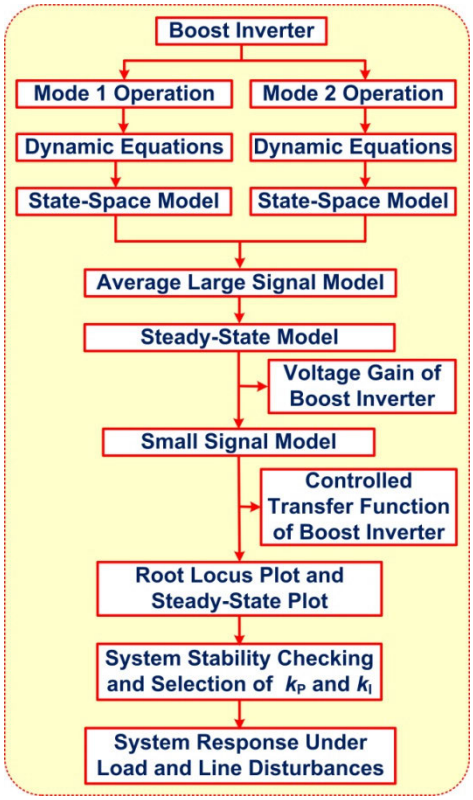


FIGURE 1. Research flow for the proposed work.

II. OPERATING MODES OF DBI

A. DESCRIPTION OF DBI

The DBI topology (refer to Fig. 2) consists of four IGBT switches, two high-frequency inductors, and two DC capacitors. The assumptions in modeling are: (i) use of non-ideal component, (ii) continuous converter current, (iii) inductance $L_1 = L_2$, and capacitance $C_1 = C_2$.

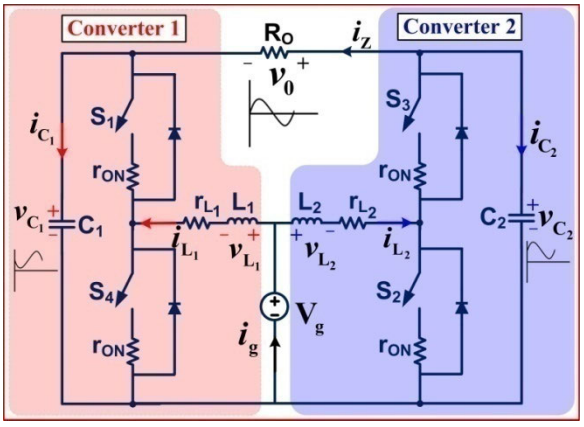


FIGURE 2. Traditional DBI circuit for non-ideal case.

B. DBI OPERATIONAL MODES

There are two modes of operation for the DBI, Mode 1, and Mode 2, which are respectively portrayed in Fig. 3 and Fig. 4. In each mode, two of the switches are in the on state and remaining in the off state.

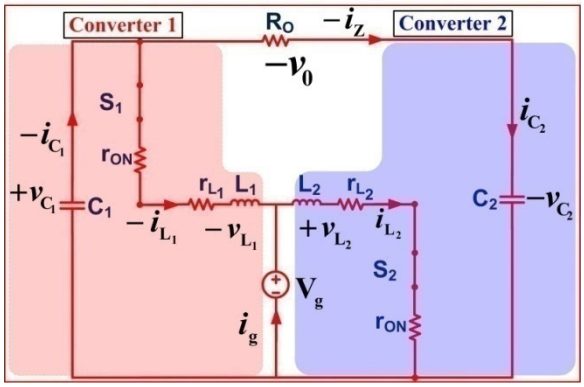


FIGURE 3. Mode 1 operation (S_1 and S_2 are ON) of DBI.

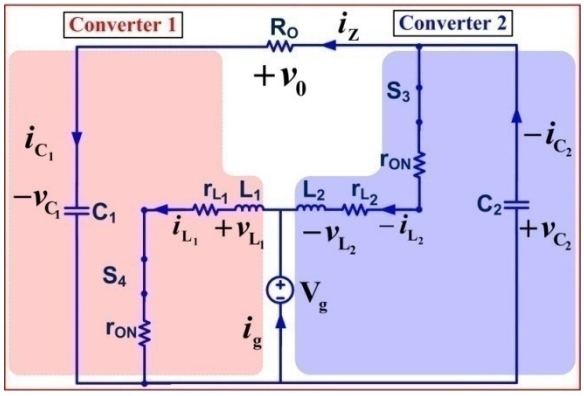


FIGURE 4. Mode 2 operation (S_3 and S_4 are ON) of DBI.

Detailed dynamic equations and state-space models for the operational modes of the DBI can be found in [13]. From the state-space model, the average model is formed. The non-ideal state-space equations related to the average model, the steady-state model, the small-signal model, and the controlled transfer functions are as detailed under:

1) AVERAGE MODEL

The DBI's average state-space model [13] as derived from Fig. 3 and 4 is as follows.

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} -r/L_1 & 0 & -d/L_1 & 0 \\ 0 & -r/L_2 & 0 & (d-1)/L_2 \\ d/C_1 & 0 & -1/RC_1 & 1/RC_1 \\ 0 & (1-d)/C_2 & 1/RC_2 & -1/RC_2 \end{bmatrix}$$

$$\times \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ 0 \\ 0 \end{bmatrix} [v_g] \tag{1}$$

$$[v_O] = \begin{bmatrix} 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \tag{2}$$

2) STEADY-STATE MODEL

By equating the differential terms to zero in (1), the resulting steady-state model help deriving the converter voltage gains and duty cycles as formulated under.

$$g_1 = \frac{V_{C_1}}{V_g} = \frac{D^3R - 2D^2R + DR + r}{\left(D^4 - 2D^3 + D^2\right)R + \left(2D^2 - 2D + 1\right)r} \tag{3}$$

$$D_1 = \frac{\sqrt{\left(g_1^2 - 2g_1 + 1\right)R^2 - 8g_1^2rR} - \left(g_1 + 1\right)R}{2g_1R} \tag{4}$$

$$g_2 = \frac{V_{C_2}}{V_g} = \frac{-D^3R - D^2R + r}{\left(D^4 - 2D^3 + D^2\right)R + \left(2D^2 - 2D + 1\right)r} \tag{5}$$

$$D_2 = \frac{\sqrt{\left(g_2^2 - 2g_2 + 1\right)R^2 - 8g_2^2rR} - \left(g_2 - 1\right)R}{2g_2R} \tag{6}$$

The voltage gain of the DBI can be obtained as the difference of the voltage gains "g_2" and "g_1" as in (3) and (5), respectively. Further, the ideal voltage gains and duty cycles can easily be obtained by substituting the value of "r" set to zero in (3) through (6).

3) SMALL-SIGNAL MODEL

The DBI circuit in Fig. 2 comprises non-linear switches. To control DBI during line and load disturbance cases, it must operate the voltage gain in the linear region where a small elemental length helps tune the output voltage with respect to the duty cycle. On this note, an establishment of a small-signal model is vital.

$$\begin{bmatrix} \dot{\hat{i}}_{L_1} \\ \dot{\hat{i}}_{L_2} \\ \dot{\hat{v}}_{C_1} \\ \dot{\hat{v}}_{C_2} \end{bmatrix} = \begin{bmatrix} -r/L_1 & 0 & -D/L_1 & 0 \\ 0 & -r/L_2 & 0 & (D-1)/L_2 \\ D/C_1 & 0 & -1/RC_1 & 1/RC_1 \\ 0 & (1-D)/C_2 & 1/RC_2 & -1/RC_2 \end{bmatrix} \times \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix} + \begin{bmatrix} 1/L_1 & -V_{C_1}/L_1 \\ 1/L_2 & -V_{C_2}/L_2 \\ 0 & -I_{L_1}/C_1 \\ 0 & -I_{L_2}/C_2 \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{d} \end{bmatrix} \tag{7}$$

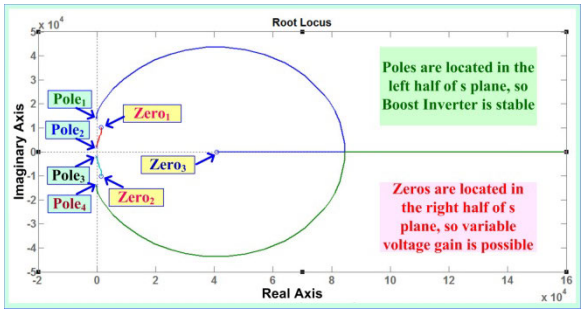


FIGURE 5. Root locus plot of closed-loop DBI.

$$\begin{bmatrix} \hat{v}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix} \tag{8}$$

4) CONTROLLED TRANSFER FUNCTION

The controlled transfer function as the ratio between $\hat{v}_0$ (in (8)) and $\hat{d}$ (in (7)) is given in (9). The detailed formulation can be found in Appendix.

$$H(s) = \frac{\hat{v}_O(s)}{\hat{d}(s)} \tag{9}$$

III. OPTIMIZATION OF PI CONTROLLER PARAMETERS

The closed-loop controlled transfer function model of DBI has three zeros and four poles, located respectively in the RHS and LHS of the s-plane (refer to Fig. 5), demonstrating the non-minimum phase characteristic [16]. Such a feature helps get a variable output voltage on the load side. The selection of controller parameters from the Root Locus plot is detailed underneath.

$$k = k_P + \frac{k_I}{s} \Rightarrow k = k_P\left(\frac{s+a}{a}\right), \tag{10}$$

where,

$$a = \frac{k_I}{k_P}. \tag{11}$$

A. CLOSED LOOP DBI

The closed loop DBI block diagram is shown in Fig. 6. The converter 1 switches S_1 and S_4 (refer to Fig. 2) are turned on by control inputs u_1 and u_4 respectively. Similarly, the converter 2 switches S_2 and S_3 (refer Fig. 2) are triggered respectively by control inputs u_2 and u_3. The output voltage is controlled by VMC technique. The reference voltages for the converters are expressed as,

$$V_{C_2} = V_{DC} + \left(\frac{V_M}{2}\right)\sin\theta, \tag{12}$$

$$V_{C_1} = V_{DC} + \left(\frac{V_M}{2}\right)\sin\left(\theta - 180^0\right), \tag{13}$$

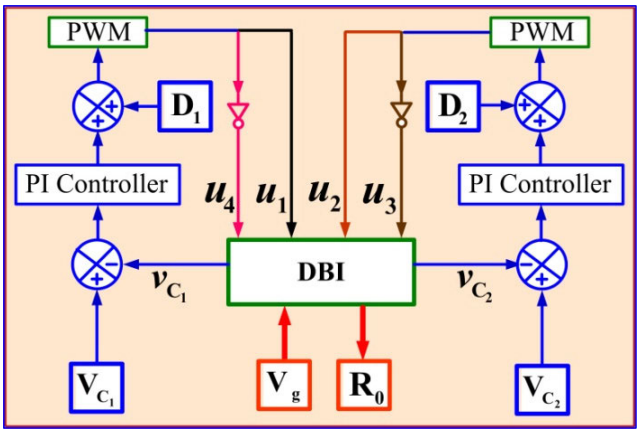


FIGURE 6. Block diagram of closed-loop DBI for non-ideal case.

where the DC component, $V_{DC} > V_g + \left(\frac{V_M}{2}\right)$ help obtain a perfect sinusoidal output voltage waveform.

Finally, the output voltage is obtained as difference of (12) and (13) and can be expressed as,

$$V_0 = V_{C_2} - V_{C_1} = V_M \sin\theta. \tag{14}$$

For an easy understanding, the closed-loop duty cycle generation technique is detailed in Fig. 7 for an ideal case. A double edge carrier PWM technique has been employed to obtain the duty cycle for the DBI.

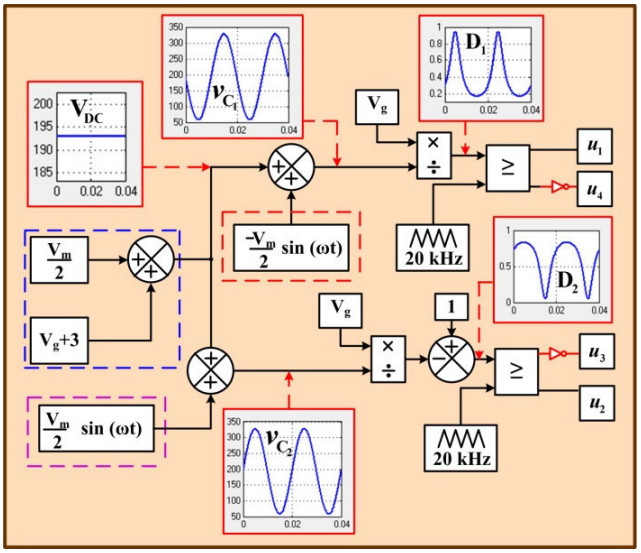


FIGURE 7. SPWM implementation using double edge carrier wave.

For real-time implementation of the closed loop non-ideal DBI, (3)-(6) are used for the steady-state voltage gain and duty cycle generation.

B. GA-BASED TUNING OF PI CONTROLLER

This control strategy is based on "survival of the fittest." It aims to eliminate the weakest members from a gene pool, resulting in a more robust future generation. This strategy has been previously applied on a novel boost DC-DC converter [17] and a buck-boost feedback controller design [10]. It is also used in reducing harmonic contents in a multi-level converter [16]. The design flow of the GA is explained in Fig. 8.

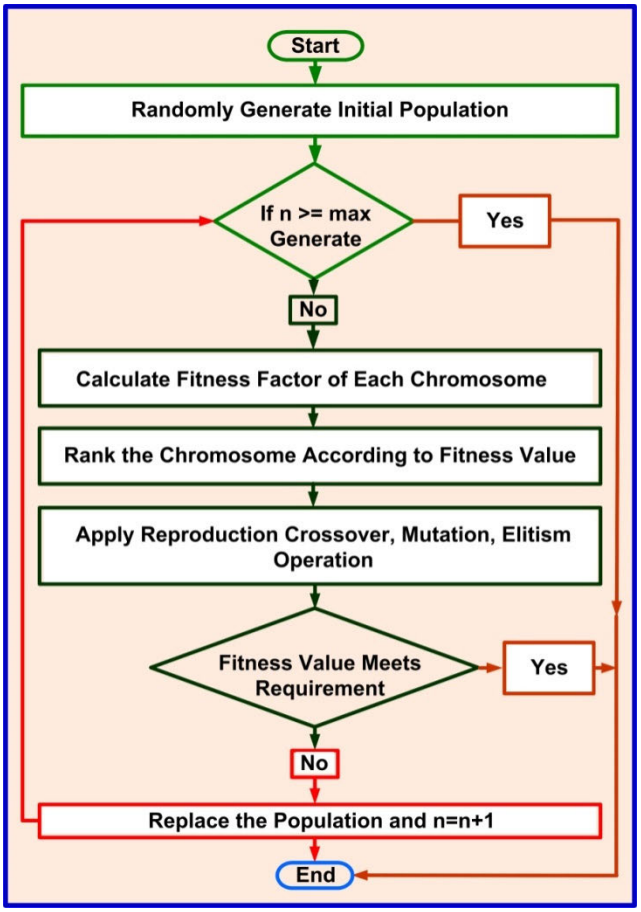


FIGURE 8. Generalized GA-based design flow for parameter tuning.

Here, the objective is to accomplish rapid turn on and turn off, i.e., by minimizing the values of transient parameters t_r, t_s, P_0, and E_{SS} [17]. On this note, a GA-based optimization is carried out with the following parameter specifications:

(i) Population size of 75,

(ii) Chromosome structure is binary coding, and

(iii) Reproduction is probabilistic crossover followed by mutation. Multi-point crossover is applied with ten iterations.

The objective function is given as,

$$\text{Min } F = (1 + t_r)\,(1 + t_s)\,(1 + P_0)\,(1 + E_{SS})\,, \tag{15}$$

subjected to, $\varphi_{(\text{Lower})} \leq \varphi \leq \varphi_{(\text{Upper})}$, where $\varphi = \{k_P, k_I\}$.

The range of values of k_P and k_I to be used as upper and lower limits in the GA, are taken from the root locus plot (refer Fig. 5) and are listed down.

$$k_P\,(\text{Min}) = 0.000001, \text{ and } k_P\,(\text{Max}) = 0.0001$$
$$k_I\,(\text{Min}) = 0.0000001, \text{ and } k_I\,(\text{Max}) = 0.00001$$

The final values of k_P and k_I are found to be 0.00003 and 0.000008 respectively which are obtained through GA-based tuning (performed using MATLAB) to stabilize the DBI output voltage. Fig. 9 shows the control strategy involved in the GA-based tuning of the PI controller for the rapid prototype control of DBI using dSPACE 1104.

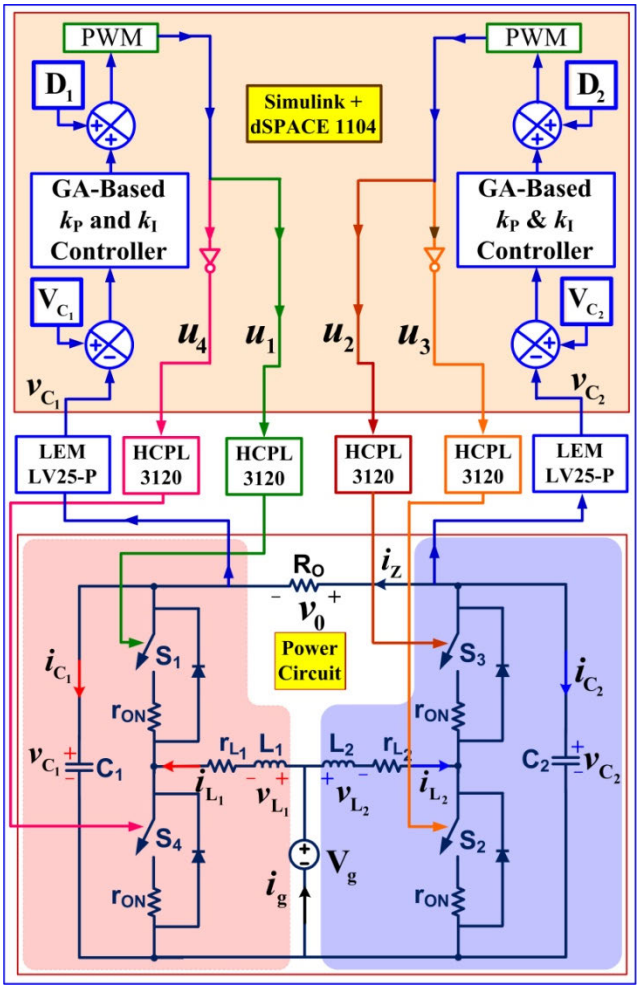


FIGURE 9. Block diagram of GA-based tuning of the PI controller used for the closed-loop DBI.

C. BFOA BASED TUNING OF PI CONTROLLER

The BFOA is based on the strategy of ''elimination and dispersal.'' While foraging, a bacterium tries to garner maximum energy while searching for nutrients and communicates with other bacteria. It essentially follows a chemotactic movement while solving a problem utilized in this algorithm [18]. The block diagram of the BFOA-based tuning of the PI controller to control the DBI is shown in Fig. 10. The flow of the BFOA control strategy is similar to that of Fig. 9 but by replacing both the blocks namely ''GA-Based k_P and k_I Controller'' by ''BFOA-Based k_P and k_I Controller''. It is to mention that, the parameter tuning process using BFOA (as discussed in Fig. 10) is more involved as compared to GA-based design flow as discussed in Fig. 8. This leads to more computational time compared to GA-based tuning. The strategy is utilized to tune the PI controller, which in turn controls the DBI. The dotted boundary box in the figure refers to the complete control unit functioning with MATLAB and dSPACE 1104. The voltage sensor output acts as the sensing voltage (for duty cycle calculation) through dSPACE 1104 analog ports.

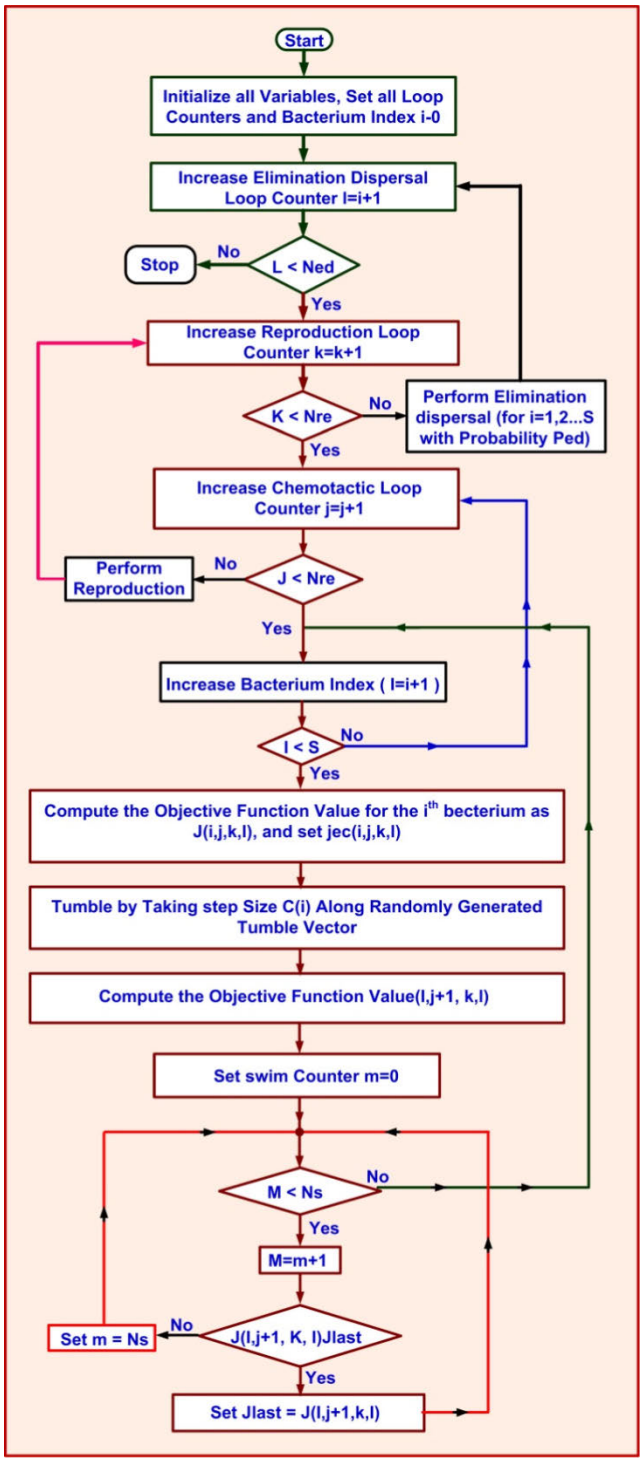


FIGURE 10. Generalized BFOA-based design flow for parameter tuning.

The PWM signal is collected from the slave I/O port in the dSPACE. The population size and the number of iterations are ten. The chemotactic size and the reproductive loop size are four, the elimination and dispersal loop size is two, the swim length is four, and the dispersal probability is 0.2. The objective function and constraint are the same as in (15).

IV. RESULTS AND DISCUSSIONS

This Section consists of four subsections to help manifest and validate the paper's purpose claimed so far. The first one discusses the traditionally controlled DBI employing a PI controller. Different voltage rating results have been showcased as stages. Stage 1 is performed at low voltage levels to observe the converter's behavior in the event of disturbances. In stage 2, results depict standard 220 V operations. The detailed analysis of GA and the BFOA-based tuning of the PI controller for better results are elucidated respectively in subsections IV (B) and IV (C). Hardware results implementing the algorithms are also given in these two subsections. Finally, the fourth subsection compares the THD results obtained by employing the algorithms and their influence on producing a better output from the DBI. A detailed comparison between the traditional topologies in the literature survey and the proposed topology has been provided. The required simulation is carried out using MATLAB-Simulink. The hardware setup for validating the closed-loop DBI claimed in this model is shown in Fig. 11.

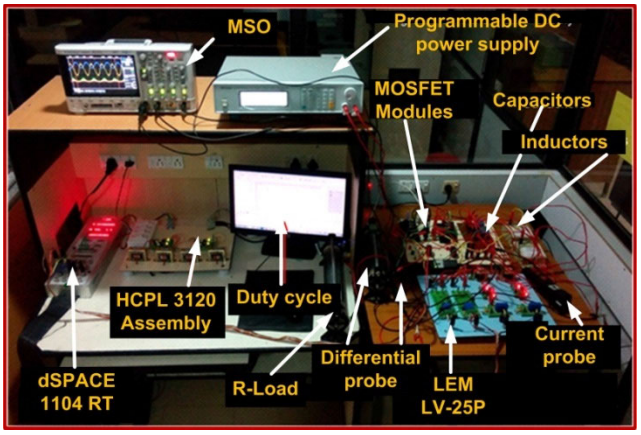


FIGURE 11. Hardware setup of DBI using dSPACE 1104.

A. NON-IDEAL DBI EMPLOYING A PI CONTROLLER

TABLE 2 shows the stage 1 design parameters used to determine the DBI's performance with resistive and motor load under various load combinations. The relevant results are also provided in Fig. 12 (a)-(c). The expected phase shift as obtained in Fig. 12 (a) and (b) indicates the DBI's smooth performance under boosted gain. Further, in Fig. 12 (c), it is noteworthy that the load voltage is stable under load disturbance conditions. TABLE 3 shows the design parameters for the stage 2 result analysis. Fig. 13 (a) depicts the hardware results obtained for the DBI under study. The obtained AC

TABLE 2. Stage 1 specifications.

Parameter	Value
Input DC voltage, V_g	24 V
Output AC voltage, V_o	72 V (Max. value)
Reference sine wave frequency	50 Hz
Switching frequency, f_s	20 kHz
Inductors, L_1 and L_2	500 µH
Parasitic resistance in series with inductor	0.1 Ω
Capacitors, C_1 and C_2	20 µF
Dual IGBT modules, S_1 to S_4	CM75DU-12H
Switch on-time resistance	1 mΩ
Load resistor, R	220 Ω
Universal motor load rating	220 V
Real-time interfacing kit	dSpace-1104
Voltage sensor, LEM LV 25-P	500 V

TABLE 3. Stage 2 specifications.

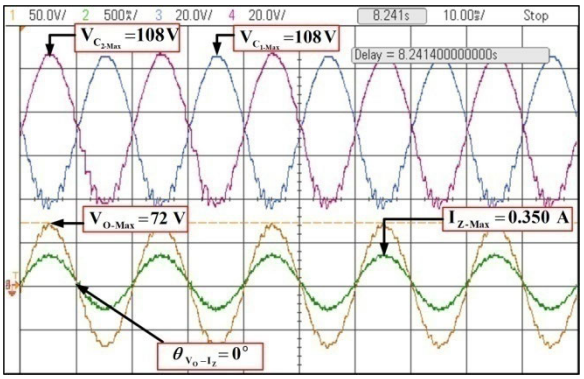
Parameter	Value
Input DC voltage, V_g	48 V
Output AC voltage, V_o	308 V (Max. value)
Reference sine wave frequency	50 Hz
Switching frequency, f_s	20 kHz
Inductors, L_1 and L_2	700 µH
Parasitic resistance in series with inductor	0.1 Ω
Capacitors, C_1 and C_2	10 µF
Dual IGBT modules, S_1 to S_4	CM75DU-12H
Switch on-time resistance	1 mΩ
Load resistor, R	220 Ω
Real-time interfacing kit	dSpace-1104
Voltage sensor, LEM LV 25-P	500 V

RMS output voltage is almost equal to 220V. Finally, the THD value is indicated in Fig. 13 (b).

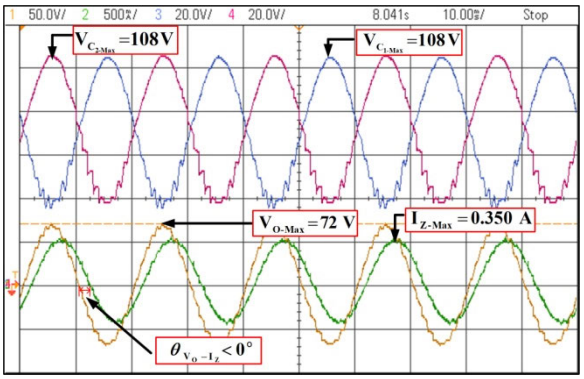
B. GA-BASED TUNING OF PI CONTROLLER

The GA-based closed loop DBI (refer to Fig. 9) is successfully implemented in Fig. 11. The design parameters involved in the GA-based tuning of the PI controller used for DBI is presented in TABLE 4. The hardware result for the resistive load is shown in Fig. 14 (a), whereas for the motor load, it is given in Fig. 14 (b). Fig. 14 (c) shows that even under load disturbance, the system's output voltage regains its stability within one cycle. Fig 14 (d) indicates that the output voltage of DBI reached the steady-state in less than a cycle under input transient condition.

The input voltage is rapidly changed from 0 V to the rated value to incorporate a transient environment. Even then, the output voltage attains stability in a cycle, and this proves the claim of improved settling time due to the usage of the GA



(a)



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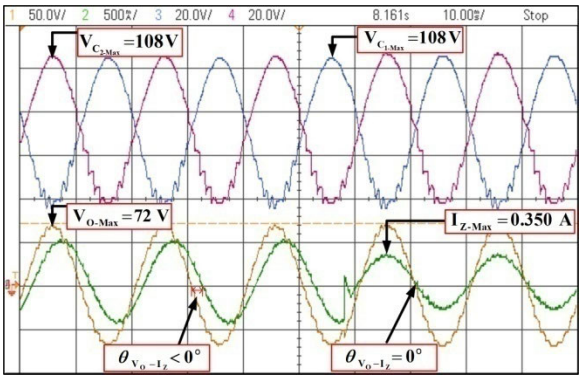
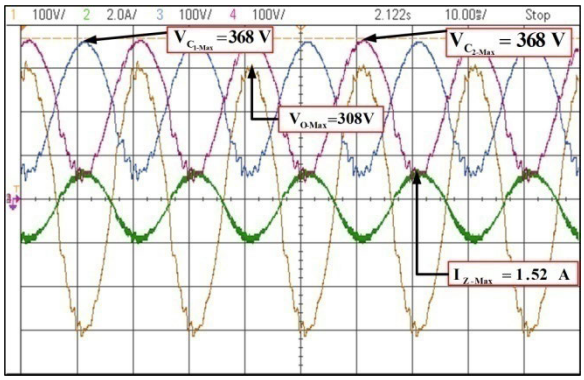
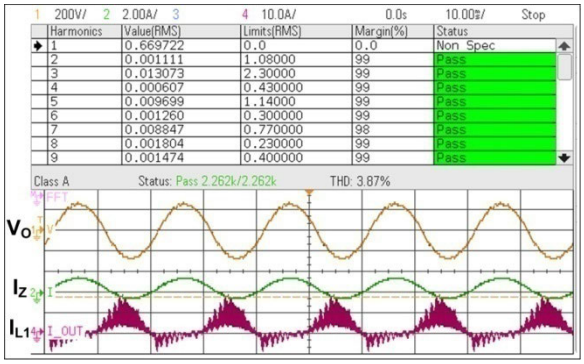


(c)

FIGURE 12. Stage 1 steady-state testing with (a) Resistive load, (b) Motor load, (c) Load disturbance test.



(a)



(b)

FIGURE 13. (a) V_0, V_{C1}, V_{C2} and I_Z as obtained from the DBI, (b) Graph of steady-state results of V_0, I_Z, and I_{L1} during stage 2 operation.

TABLE 4. Specifications for GA-based PI controlled DBI.

Parameter	Value
Input DC voltage, V_g	24 V
Output AC voltage, V_o	48 V (Max. value)
Reference sine wave frequency	50 Hz
Switching frequency, f_s	20 kHz
Inductors, L_1 and L_2	500 µH
Parasitic resistance in series with inductor	0.1 Ω
Capacitors, C_1 and C_2	20 µF
Dual IGBT modules, S_1 to S_4	CM75DU-12H
Switch on-time resistance	1 mΩ
Load resistor, R	220 Ω
Universal motor load rating	220 V
Real time interfacing kit	dSpace-1104
Voltage sensor, LEM LV 25-P	500 V

algorithm. Even when the line disturbance was introduced the integral and proportional constants generated by the GA algorithm forced the response to become stable as shown in Fig. 14 (e). The THD result obtained after tuning the PI controller of the DBI with GA is given in Fig. 14 (f).

C. BFOA -BASED TUNING OF PI CONTROLLER

The design parameter for the BFOA-based PI controller for the DBI is provided in TABLE 5.

Fig. 15 (a) results showcase the steady-state capacitor voltages along with the output current and voltage waveforms. Fig. 15 (b) shows line disturbance response. Even after incorporating the line disturbance, due to the stepping down of the input voltage from 36 V to 33 V (line disturbance), the current waveform stabilizes in just 20 ms due to BFOA controlling in the PI controller. In Fig. 15 (c), load disturbance is depicted by a sudden load change from a unity power factor to a lagging power factor, which has negligible

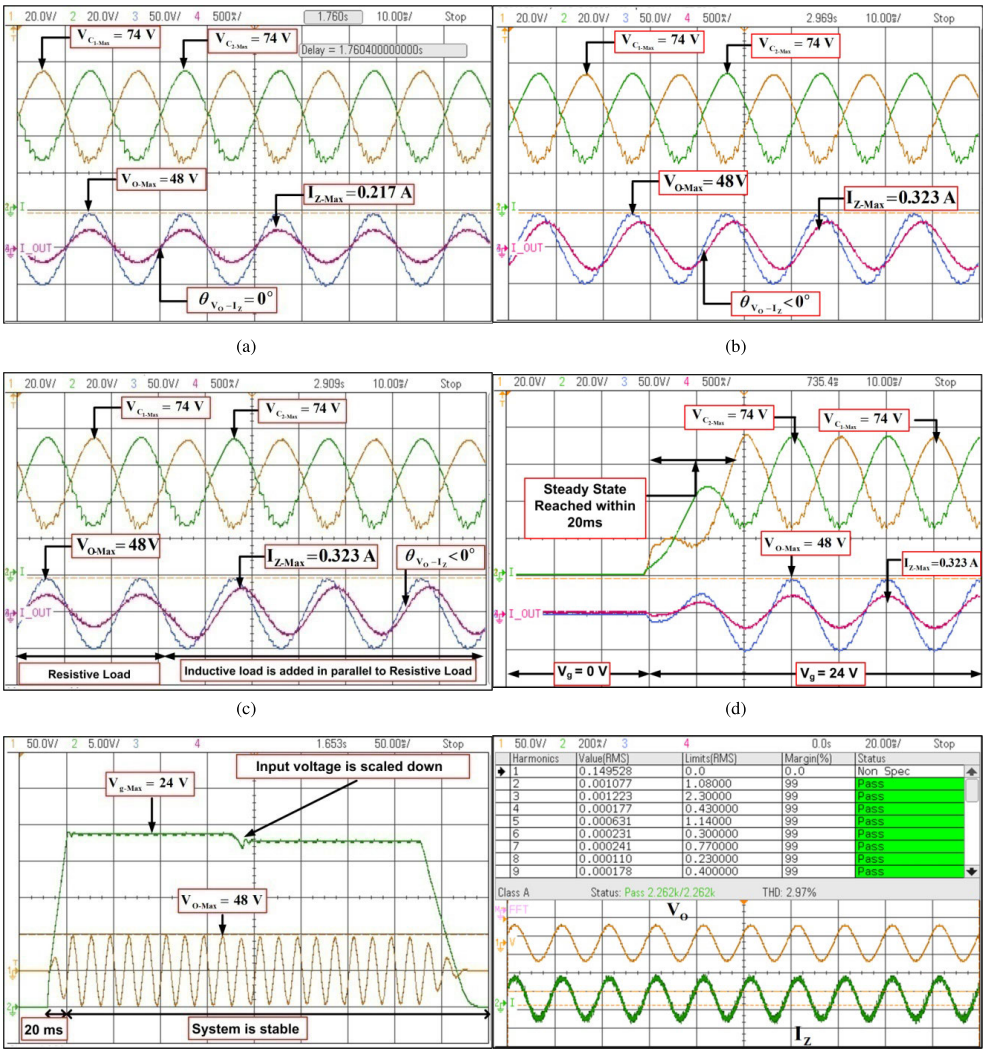


FIGURE 14. GA-based DBI steady-state response for (a) Resistive load, (b) Motor load, (c) Load disturbance, (d) Transient response, (e) Supply voltage regulation and transience, (f) THD results for resistive load.

TABLE 5. Specifications for BFOA-based PI controlled DBI.

Parameter	Value
Input DC voltage, V_g	36 V
Output AC voltage, V_o	155.5 V (Max. value)
Reference sine wave frequency	50 Hz
Switching frequency, f_s	20 kHz
Inductors, L_1 and L_2	200 µH
Parasitic resistance in series with inductor	0.1 Ω
Capacitors, C_1 and C_2	20 µF
Dual IGBT modules, S_1 to S_4	CM75DU-12H
Switch on-time resistance	1 mΩ
Load resistor, R	220 Ω
Universal motor load rating	220 V
Real time interfacing kit	dSpace-1104
Voltage sensor, LEM LV 25-P	500 V

influence on the voltage waveform. In contrast, the current waveform attains stability again in just 20 ms indicating the advantage of using the BFOA technique to control the PI

TABLE 6. System response for traditional PI, GA-based PI and BFOA-based PI.

Dynamic response specifications	Traditional method (k_P = 0.00001, k_I = 0.000001)	GA (k_P = 0.00023, k_I =0.000008)	BFOA (k_P = 0.000053, k_I = 0.000009)
t_r	5.61 ms	5.62 ms	5.5 ms
t_s	18.5 ms	17 ms	16.9 ms
P_0	0	0	0
E_{SS}	0.513 V	0.414 V	0.402 V

controller used in the DBI. Even during turn on and turn off, the waveforms attained are smooth and within the desirable range, as depicted by Fig. 15 (d). THD response is shown in Fig. 15 (e).

D. FURTHER DISCUSSIONS AND COMPARISONS

As manifested by the hardware results, a DC to AC conversion was achieved. A close-loop circuit was implemented

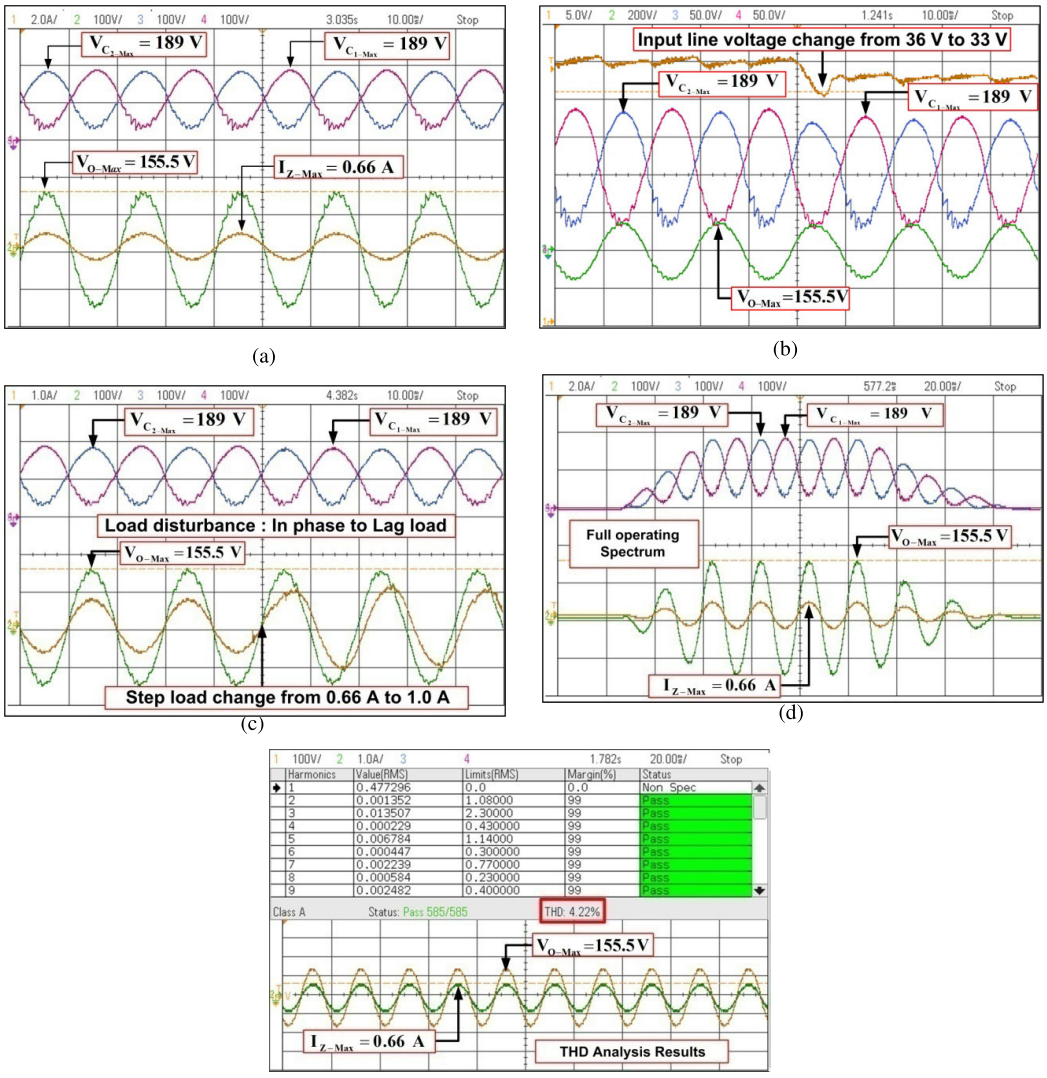


FIGURE 15. (a) Capacitor voltages, Output current and output voltages obtained in the steady-state, (b) Line disturbance response, (c) Load disturbance response, (d) Transient response during turn on and turn off, (e) THD analysis.

successfully, and the performance was enhanced by incorporating the GA and BFOA algorithms. A better response was obtained by reducing the rise time, settling time, maximum overshoot, and the steady-state error, as shown in TABLE 6. The THD values were less than 5% which complies with Class-A IEEE standard 519-2014. Also, the response during line and load disturbances reached a steady state in significantly less time. Thus, the result complies with the claims made at the beginning of this research.

V. CONCLUSION

The voltage gain and the THD results so obtained comply with the claims made at the beginning of this research. The modeling of the proposed DBI is done for the non-ideal case, thus, providing the expected result. Despite the incorporation of load disturbance, the output waveforms attain stability in just one cycle due to the GA and BFOA algorithms' addition to tune the PI controller. A detailed benefit of this addition has been highlighted. Also, in stages, hardware results for different ratings have been given to prove the versatile applications in which this inverter can be used. A future prospectus for this topology would be to extend it as a three-phase inverter to cater to the higher power demands used in industrial devices.

APPENDIX
FORMULATION OF CONTROLLED TRANSFER FUNCTION

The transfer function in (9) can be derived as,

$$\frac{\hat{v}_O(s)}{\hat{d}(s)} = \frac{(q_1x_4 + q_2x_3 + q_3x_2 + q_4x_1)}{s^4 + n_1s^3 + n_2s^2 + n_3s + n_4}$$

where,

$$q_1 = -s^3 - m_{20}s^2 + m_{17}s - m_{21}s + m_{18}s - m_{22} + m_{19}$$
$$q_2 = s^3 - m_{14}s^2 + m_{11}s^2 - m_{15}s + m_{12}s - m_{16} + m_{13}$$
$$q_3 = -m_8s^2 - m_9s + m_7 - m_{10}$$
$$q_4 = m_1s^2 - m_4s + m_2s - m_5 + m_3$$

$$
\begin{aligned}
n_1 &= -k_6 - k_3 + k_{10} - k_1 \\
n_2 &= -k_7k_9 - k_4k_8 + (k_3 + k_{10} + k_1)k_6 - k_2k_5 \\
&\quad +(k_{10} + k_1)k_3 + k_1k_{10} \\
n_3 &= (k_3 + k_1)k_7k_9 + (k_4k_6 + k_1k_4)k_8 \\
&\quad +((-k_{10} - k_1)k_3 - k_1k_{10})k_6 \\
&\quad +(k_2k_3 + k_{10}k_2)k_5 - k_1k_{10}k_3 \\
n_4 &= k_1k_3k_7k_9 + (k_2k_4k_5 - k_1k_4k_6)k_8 \\
&\quad +k_1k_{10}k_3k_6 - k_{10}k_2k_3k_5 \\
m_1 &= k_5, m_2 = (-k_3 - k_{10})k_5, m_3 = -k_4k_5k_8 + k_{10}k_3k_5 \\
m_4 &= k_5k_9, m_5 = -k_3k_5k_9, m_6 = k_7k_8, m_7 = -k_1k_7k_8 \\
m_8 &= k_8, m_9 = -k_6k_1k_8, m_{10} = (k_6k_1 - k_2k_5)k_8 \\
m_{11} &= -k_3 - k_{10} - k_1, \\
m_{12} &= -k_4k_8 + (k_{10} + k_1)k_3 + k_1k_{10} \\
m_{13} &= k_1k_8 - k_1k_{10}k_3, m_{14} = k_9, m_{15} = (-k_3 - k_1)k_9 \\
m_{16} &= k_1k_3k_9, m_{17} = k_7, m_{18} = (-k_3 - k_1)k_7 \\
m_{19} &= k_1k_3k_7, m_{20} = -k_6 - k_3 - k_1 \\
m_{21} &= (k_1 + k_3)k_6 - k_2k_5 + k_1k_3, \\
m_{22} &= -k_1k_3k_6 + k_2k_3k_5 \\
k_1 &= {}^{-\mathrm{r}}\!/_{\mathrm{L}_1}, k_2 = {}^{-\mathrm{D}}\!/_{\mathrm{L}_1}, k_3 = {}^{-\mathrm{r}}\!/_{\mathrm{L}_2}, k_4 = {}^{(\mathrm{D}-1)}\!/_{\mathrm{L}_2}, \\
k_5 &= {}^{\mathrm{d}}\!/_{\mathrm{C}_1}, k_6 = {}^{-1}\!/_{\mathrm{RC}_1}, k_7 = {}^{1}\!/_{\mathrm{RC}_1}, k_8 = {}^{(1-\mathrm{D})}\!/_{\mathrm{C}_2}, \\
k_9 &= {}^{1}\!/_{\mathrm{RC}_2}, k_{10} = {}^{-1}\!/_{\mathrm{RC}_2}, x_1 = {}^{-\mathrm{V}_{\mathrm{C}_1}}\!/_{\mathrm{L}_1}, \\
x_2 &= {}^{\mathrm{V}_{\mathrm{C}_2}}\!/_{\mathrm{L}_2}, \\
x_3 &= {}^{\mathrm{I}_{\mathrm{L}_1}}\!/_{\mathrm{C}_1}, x_4 = {}^{-\mathrm{I}_{\mathrm{L}_2}}\!/_{\mathrm{C}_2}
\end{aligned}
$$

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