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Mitigation of Complex Non-Linear Dynamic Effects in Multiple Output Cascaded DC-DC Converters

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ABSTRACT In the modern world of technology, the cascaded DC-DC converters with multiple output configurations are contributing a dominant part in the DC distribution systems and DC micro-grids. An individual DC-DC converter of any configuration exhibits complex non-linear dynamic behavior resulting in instability. This paper presents a cascaded system with one source boost converter and three load converters including buck, Cuk, and Single-Ended Primary Inductance Converter (SEPIC) that are analyzed for the complex non-linear bifurcation phenomena. An outer voltage feedback loop along with an inner current feedback loop control strategy is used for all the sub-converters in the cascaded system. To explain the complex non-linear dynamic behavior, a discrete mapping model is developed for the proposed cascaded system and the Jacobian matrix's eigenvalues are evaluated. For the simplification of the analysis, every load converter is regarded as a fixed power load (FPL) under reasonable assumptions such as fixed frequency and input voltage. The eigenvalues of period-1 and period-2 reveal that the source boost converter undergoes period-2 orbit and chaos whereas all the load converters operate in a stable period-1 orbit. The proposed configuration eliminates the period-2 and chaotic behavior from all the load converters and is also validated using simulation in MATLAB/Simulink and experimental results.

INDEX TERMS Bifurcation, chaos, DC-DC power converters, non-linear dynamical systems.

I. INTRODUCTION

DC-DC converters are the inescapable components of modern DC distribution systems. The non-linear behavior of those individual converter circuits is thoroughly carried out in the studies of power electronics circuits presented in reference [1], [2]. The time-varying behavior of those converter circuits is because of the low and high-frequency oscillations that result in multiple period bifurcations and chaos phenomena [3]. In the modern era of technology, most of the consumer devices are comprised of DC-DC converter circuits that necessitate the design engineers to mainly focus on the elimination of sub-harmonics [4]. So, it is important to go through the studies of the non-linear dynamics of those converter systems. The main advantages of the DC distribution systems include simplicity in the connectivity with renewable sources, higher efficiency, and a wide range of choices for the design parameters. The reliability and stability of DC power converters are the main issues that come across when they are used in the distribution systems. The design and stability of a single converter can be easily carried out. However, the main stability issues arise in a DC distribution system when the interaction of sub-converters takes place [5].

The DC converters connected in a cascaded style is the basic form in a DC distribution system where various renewable energy sources deliver power to a shared DC bus and all the load converters take power from that bus [6]. Hence, it is the need of the hour to study the reliability and stability of cascaded DC-DC converter systems. The studies have proven that the non-linear dynamic effect is due to the cascaded configuration in the DC-DC converter systems [7]–[9]. These studies are only suitable for small-signal analysis about the stability of DC converter systems. Some models such as FPLs, impedance calculation criteria, and Thevenin network

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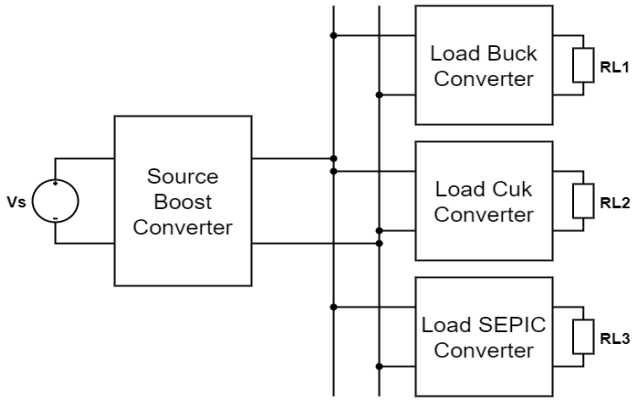

FIGURE 1. Block diagram of the proposed cascaded system.

have been developed for large-scale systems [10]–[12]. However, the study of the stability issues about the non-linear dynamic behavior of cascaded DC converter systems is less explored. This paper presents the non-linear dynamic behavior of a cascaded converter system having one source and three load converters and proposes remedial measures to avoid non-linear effects.

Over the past few decades, the complex non-linear behavior of individual converters such as a boost, buck, Cuk, buck-Boost, SEPIC, and flyback converter has been studied. Using the average and discrete mapping model, the eigenvalues at the equilibrium point are evaluated and examined for the stability behavior [13]–[18]. The main problem associated with the analysis using the averaged model is that the period-doubling bifurcation cannot be estimated because the switching frequency of the converter under analysis is completely neglected [19]. Several complex non-linear dynamic studies such as Niemark-Sacker bifurcation, border collision bifurcation, discrete mapping model, slow and fast scale instabilities, and chaos are available in the literature, but they are only used in the studies of single DC-DC converter circuits with stand-alone operation [20]–[23]. Those bifurcation studies are not used in the investigation of the non-linear dynamic behavior of cascaded DC-DC converter systems whose behavior is dependent on the load converters. Therefore, this paper presents the investigation of the complex non-linear bifurcation phenomena for the cascaded DC-DC converter systems.

The block diagram of the proposed systems to improve the complex bifurcation phenomena of the cascaded multiple outputs DC-DC converter systems that are part of a large DC distribution system is shown in Fig. 1. The simulation of every individual sub-converter of the cascaded system is carried out and the complex bifurcation phenomena of the cascaded converter systems are studied in detail. Section 2 presents the implementation of the cascaded converter system along with the control scheme used for all sub-converters. In section 3, the results of the simulation of the individual converter and for the complete cascaded system are presented. Section 3 also shows the results in the form of inductor current waveforms obtained from the real hardware circuit board. Section 4 describes the discrete mapping model of the proposed simplified cascaded converter system with FPLs in detail. The Jacobian matrix's eigenvalues are used to explain the unstable behavior of the cascaded system. Finally, in section 5, the results are summarized, and a conclusion is drawn which confirms that by decreasing the input source voltage, the system undergoes period-2 phenomena which finally turns into chaos if the input voltage is further decreased and hence the system stability weakens. When the system becomes unstable, some of the eigenvalues are out of the unit circle that severely affects the performance of the source boost converter in the cascaded system. This paper provides an efficient way to get rid of the complex non-linear dynamic behavior in the cascaded DC distribution systems and in DC micro-grids that have multiple output configurations.

II. IMPLEMENTATION OF CASCADED CONVERTER SYSTEM

The schematic diagram of the cascaded system with multi-output converters is presented in Fig. 2. The source boost converter in the cascaded system at the first stage takes DC input and its output becomes the input to all the sub-converters on the load side. The load side converters include a buck converter, a Cuk converter, and a SEPIC converter. All the converters in the cascaded system are controlled individually with the same control technique which is shown in Fig. 3. The control technique used for all the sub-converters in the cascaded converter system comprises an outer voltage feedback loop and an inner current feedback loop. Furthermore, the voltage loop contains a resistive divider circuit, an error amplifier with a compensation network, and one protection circuit with offset-divided protection property. The resistive divider circuit steps down the output capacitor voltage of every sub-converter and feeds to the inverting input of the error amplifier. The protection circuit with offset divided property offsets the voltage by dropping the voltage across two diodes. The voltage is then divided by a ratio of 3:1 with Rd and 2Rd which is further fed to the inverting input of the comparator. This configuration of using diodes confirms that there is no switching pulse when the converter is operating under no-load condition. In the current feedback loop, the current is subjected to a gain which is then fed to the comparator's non-inverting input. The output of the comparator is connected to the R input of the R-S latch whereas the S input of the latch is fed with a clock source with period T. The control scheme operates as follows: When the current feedback level reaches the voltage feedback level, the output of the comparator circuit applies a reset signal to the R-S latch which turns OFF the MOSFET switch. When the switch is turned OFF, the current and the voltage feedback levels begin to fall, and hence, the output of the comparator is not asserted. Hence, it lifts the reset signal of the R-S latch and the output of the R-S latch is set by the clock source with period T which directly turns ON the MOSFET, and the voltage and current feedback increases again. This process continues indefinitely,

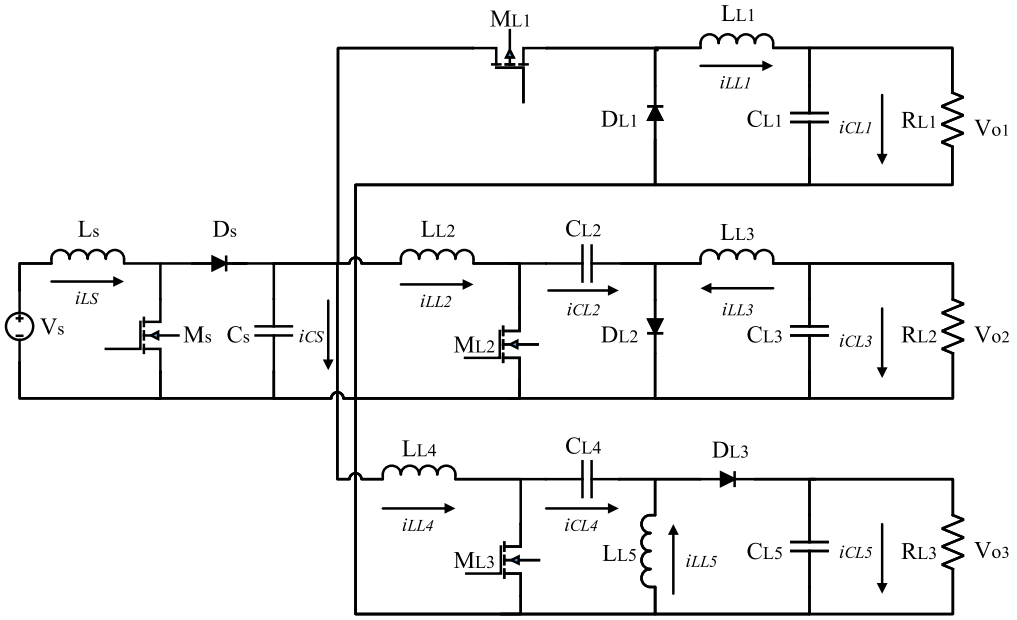

FIGURE 2. Circuit diagram of the proposed cascaded converter system.

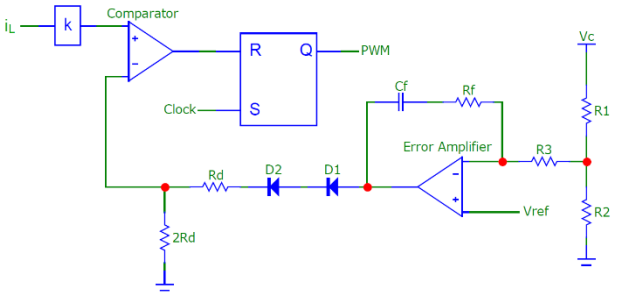

FIGURE 3. Circuit diagram of feedback controller implemented for every sub-converter in the cascaded system.

and the reference voltage can be calculated as:

$$V_{ref} = \frac{R_2}{R_1 + R_2} \times V_C \tag{1}$$

III. STABILITY ANALYSIS USING SOFTWARE SIMULATIONS AND HARDWARE IMPLEMENTATION

The parameters used for the simulation study are presented in Table 1. For simulation purposes, the source boost converter is designed for an input voltage of 35 V and an output voltage of 50 V which acts as the bus voltage for all the load converters. However, the converters can be designed for any other voltage range. The initial values of all the energy storing elements are set to zero and each converter has been simulated individually at rated power and designed input voltage. The inductor current and capacitor voltage waveform for every individual converter in the cascaded converter system at the rated input voltage is obtained by simulating the system in MATLAB/Simulink and is shown in Fig. 4.

From Fig. 4, it can be found that all the converters operate in stable period-1 orbit when they are subjected to the input voltage equal to the rated value. However, when the input

TABLE 1. Component values for the converters in the cascaded system.

Parameter	Boost	Buck	Cuk	SEPIC
V_S (V)*	35	50	50	50
D	0.3	0.36	0.3243	0.5902
L_1 (mH)	1.225	2.074	2.1113	5.7637
C_1 (uF)	28.8	12.34	27.39	11.38
L_2 (mH)	-	-	1.013	8.2983
C_2 (uF)	-	-	13.03	11.38
R (Ω)	83.33	32.4	48	648
V_O (V)	50	18	24	72
P_O (W)	30	10	12	8

*The parameter V_S for the load converters represents the bus voltage which is also the output of the source boost converter.

source voltage for every individual converter is decreased from the rated value, the converters undergo period-2 orbit which severely affects their stability. The period-2 behavior of every individual converter is shown in Fig. 5. After the verification of period-2 orbit from the simulation of every individual converter, the complete cascaded converter system is simulated at the source input voltage of 35 V, and the inductor currents are shown in Fig. 6. We have seen from Fig. 6 that all the sub-converters of the cascaded system are operating in a stable period-1 orbit. As the input voltage of the source boost converter is decreased to 25 V, the source boost converter undergoes period-2 orbit however all the load converters continue operating in period-1 orbit with stable behavior. This phenomenon is shown in Fig. 7. Since, for any DC-DC converter, almost all the practical applications require a specific operating point at equilibrium. Therefore, the designed system should behave accurately around that equilibrium point within a certain tolerance band. As seen from Fig. 7, it is clear that the proposed converter enters period-2 orbit at 25 V which confirms that it has a tolerance

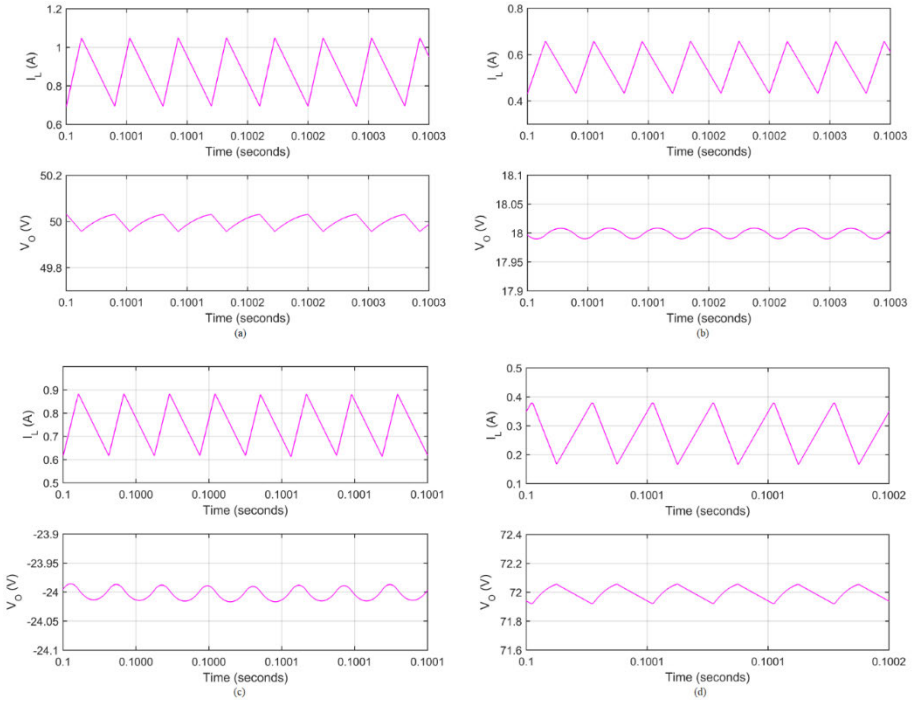

FIGURE 4. Inductor current ripple and output voltage ripple waveforms of stable period-1 operation for a) boost converter at $V_S = 35$ V b) buck converter at $V_S = 50$ V c) Cuk converter at $V_S = 50$ V d)SEPIC converter at $V_S = 50$ V.

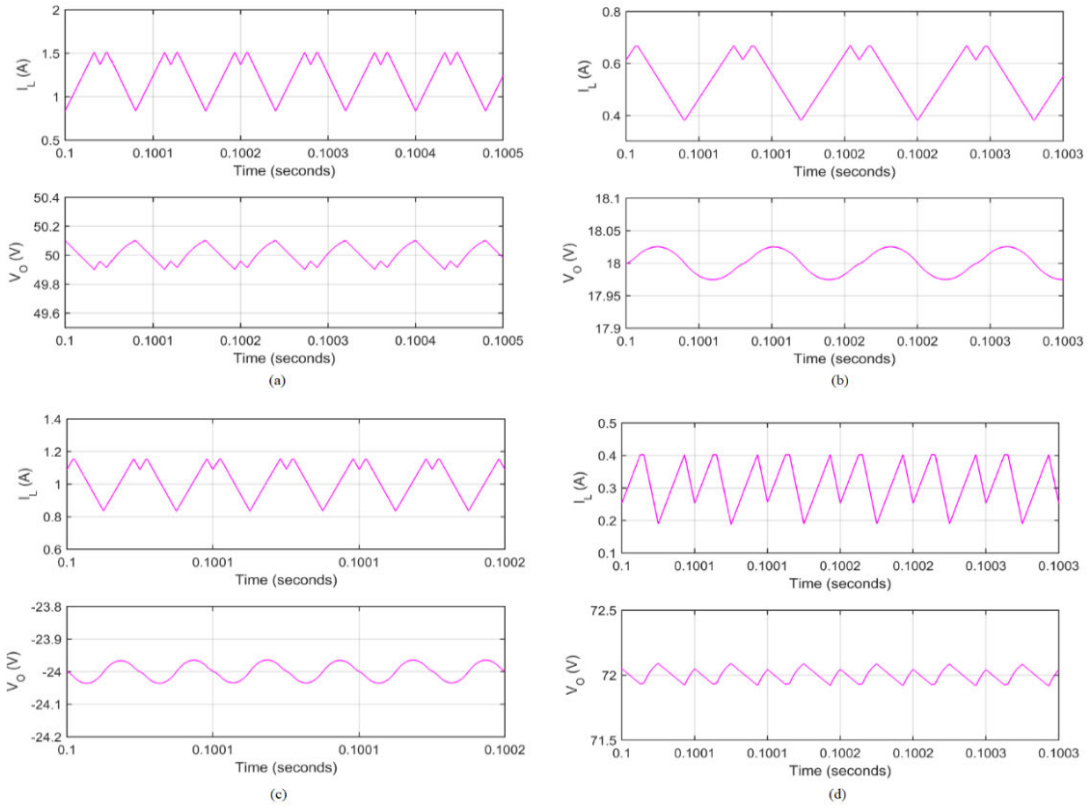

FIGURE 5. Inductor current ripple and output voltage ripple waveforms of period-2 operation for a) boost converter at $V_S = 25$ V b) buck converter at $V_S = 36$ V c) Cuk converter at $V_S = 24$ V d) SEPIC converter at $V_S = 40$ V.

band for input voltage as 10 V and within this tolerance band, the converter operates linearly under stable period-1 orbit. The inductor current waveform of the source boost converter for a step variation in the input voltage from 25 V to 35 V at

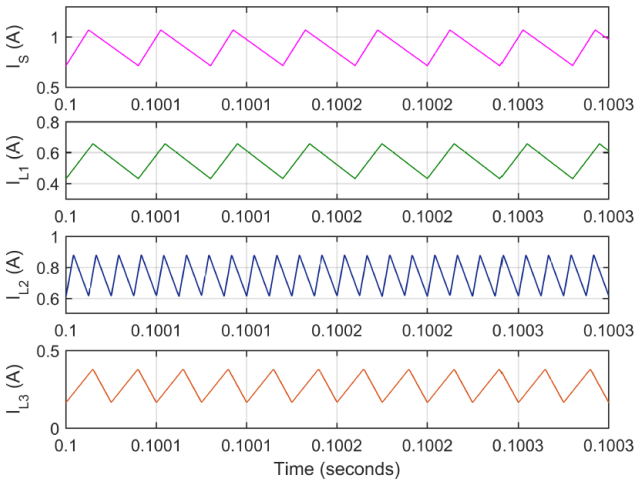

FIGURE 6. Inductor current waveforms of all the converters of the cascaded system at $V_S = 35$ V.

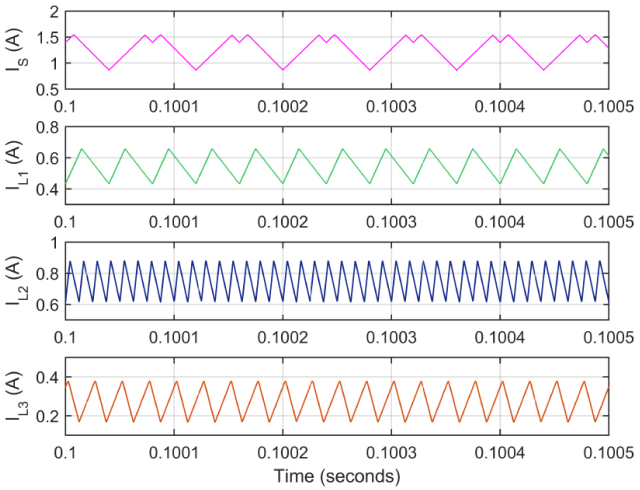

FIGURE 7. Inductor current waveforms of all the converters of the cascaded system at $V_S = 25$ V.

t = 0.1 s and then again 35 V to 25 V at t = 0.15 s is plotted in Fig. 8. The inductor current waveform at t = 0.1 s and t = 0.15 s is zoomed-in and shown separately within the same figure. It can be seen from Fig. 8 that before t = 0.1 s, the input voltage is set at 25 V and hence, the inductor current of the source boost converter undergoes period-2 phenomenon. From t = 0.1 s to t = 0.15 s, the input voltage is kept constant at 35 V which confirms that the inductor current exhibits period-1 behavior. After t = 0.15 s, the input voltage is again stepped down to 25 V and the inductor current again exhibits period-2 behavior. However, it is confirmed that the inductor current waveforms for all the load converters are having period-1 behavior.

Since in the simulation studies, the influences and disturbances from the external environment do not occur, it is necessary to consider the effect of external disturbances and influences on the system behavior. So, for the verification of the simulation results, a hardware printed circuit board (PCB) is developed using the UC3842, fixed frequency current mode

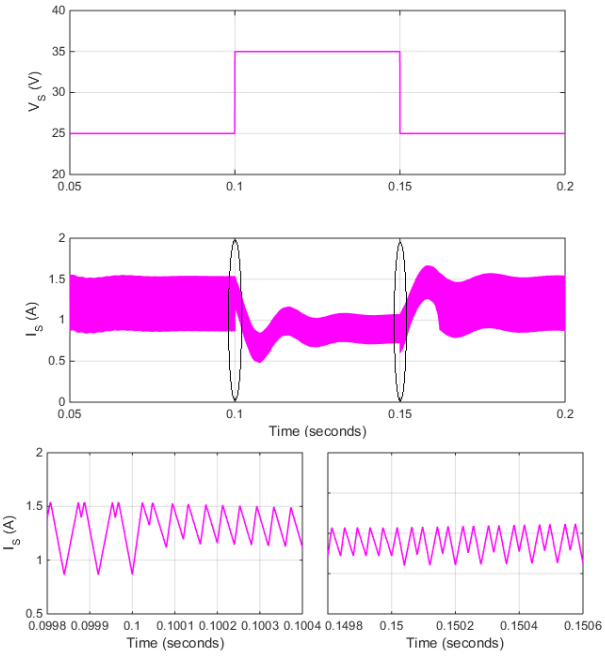

FIGURE 8. Inductor current waveform of source boost converter for step change in the input voltage verifying non-linear incident effects.

pulse width modulation (PWM) control integrated circuit (IC) and is shown in Fig. 9(a). The internal diagram of the IC depicts a similar circuit as developed for the control scheme of every individual converter in the cascaded system. In the design of the hardware circuit, an N-channel MOSFET STD20NF20 having very small internal resistance, high current, and low gate charge is used which ensures fast switching. The inductor current waveform for the input voltage of 35 V and 25 V is obtained using a digital storage oscilloscope and is shown in Fig. 9(b) and Fig. 9(c) respectively. When the input voltage of the source boost converter is further decreased from 25 V, the source boost converter exhibits fast and slow scale instability behavior with all the load converters still operating in the stable period-1 state. This phenomenon is depicted in Fig. 9(d).

IV. BIFURCATION AND CHAOS ANALYSIS

The simulation studies presented in the previous section show that every load converter in the proposed cascaded system works in the stable period-1 orbit and is independent of the state and dynamic behavior of the source boost converter which may undergo period-2 orbit depending on the input voltage of the system. This section explains the instability phenomena regarding the simulation and experimental studies using the best suitable model. The discrete mapping model is developed that best describes the instability and dynamic behavior of the converters in the proposed cascaded system with multiple output configurations.

A. SIMPLIFICATION OF THE SYSTEM AND DISCRETE MAPPING MODEL

If all the components used in the cascaded converter system are assumed to be ideal, then every load converter can be

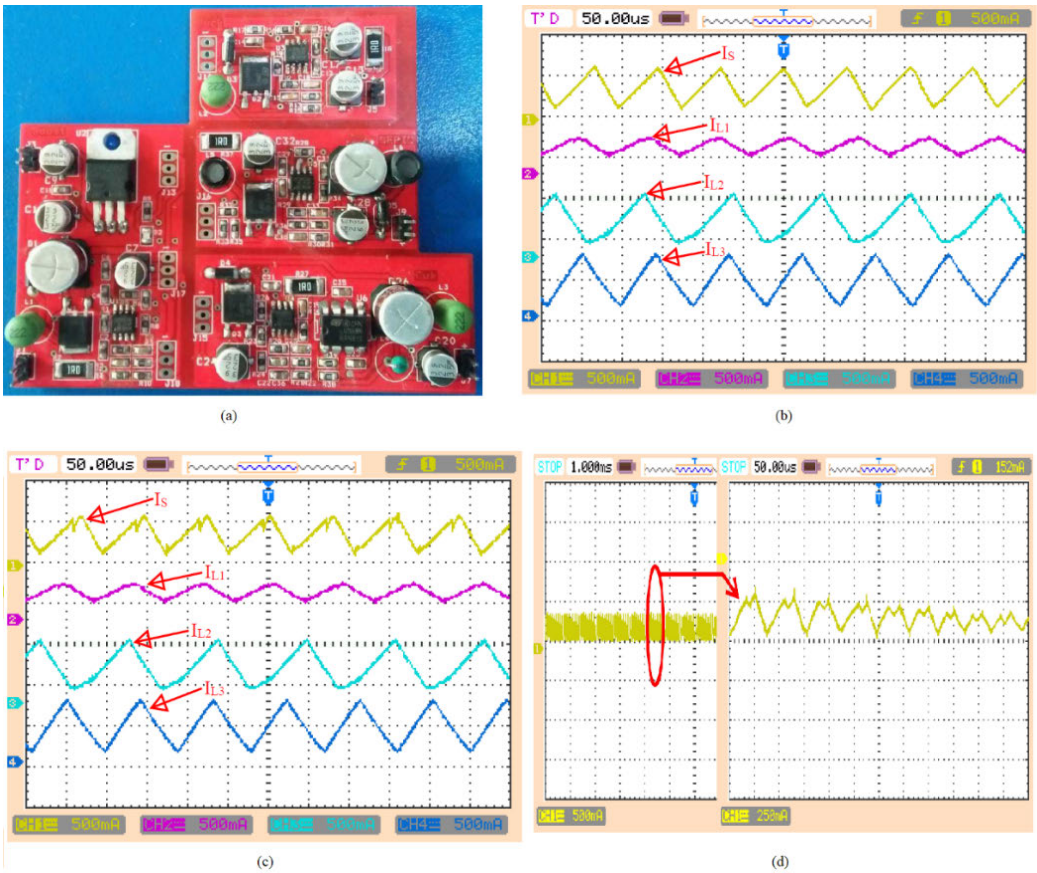

FIGURE 9. Experimental hardware implementation and resulting waveforms a) Hardware circuit prototype board b) Inductor current waveforms at $V_S = 35$ V c) Inductor current waveforms at $V_S = 25$ V d) Inductor current waveform for source boost converter at $V_S < 25$ V.

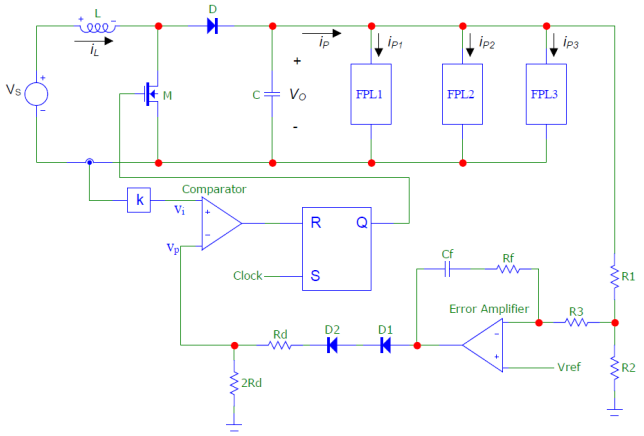

FIGURE 10. Schematic diagram of the simplified cascaded converter system by using FPLs.

regarded as an FPL at a suitable switching frequency and input voltage range. This assumption is well supported by the simulation and experimental results of the previous section because all the load converters remain in stable period-1 orbit irrespective of the mode of operation and dynamic behavior of the source boost converter. The load buck, Cuk, and SEPIC converters are modeled as FPL1, FPL2, and FPL3 respectively which makes the overall cascaded converter system simplified as shown in Fig. 10.

The output power of an FPL_i (where i = 1, 2, and 3 for the buck, Cuk, and SEPIC converter respectively) is given as:

$$P_i = \frac{V_{oi}^2}{R_{Li}} \tag{2}$$

Now, the input current of FPL_i can be given as,

$$i_{Pi} = \frac{P_i}{v_o} \tag{3}$$

$$I_{Pi} = \frac{P_i}{V_o} \tag{4}$$

where (4) is the steady-state representation of (3).

The rate of change of input current with respect to v_{DC} using

(3) is given as:

$$\frac{\partial i_{Pi}}{\partial v_o} = -\frac{P_i}{V_o^2} \tag{5}$$

By integrating (5) and inserting into (4), we get:

$$i_{Pi} = -\frac{P_i}{V_o^2} v_o + \frac{2P_i}{V_o} \tag{6}$$

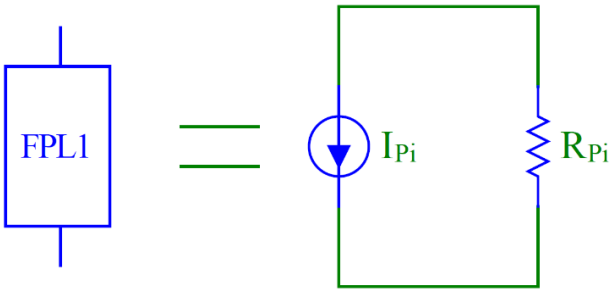

FIGURE 11. Simplified FPL model used for analysis.

TABLE 2. Circuit parameters for FPLS.

Parameter	FPL1	FPL2	FPL3
I_{Pi} (A)	0.4	0.48	0.32
R_{Pi} (kΩ)	-250	-208.3	-312.5

Equation (6) shows that the current flowing through any FPL can be approximated by a negative resistance and a fixed current source. That is,

$$R_{Pi} = \frac{v_o^2}{P_i} \tag{7}$$

$$I_{Pi} = \frac{2P_i}{V_o} \tag{8}$$

The above two equations are transformed into a circuit diagram in the steady-state and are shown in Fig. 11. Table 2 shows the calculated parameters for all the FPLs using (7) and (8).

The state-space representation of the simplified system for the kth control cycle by assigning the state variables as $X = \left[i_L v_O v_f\right]^T$ can be given as:

$$\dot{x} = \begin{cases} A_1 x + B_1, & kT \le t \le (k + d_k)\, T \\ A_2 x + B_2, & (k + d_k)T \le t \le (k + 1)\, T \end{cases} \tag{9}$$

where d_k is the duty ratio. The matrices A_1 and A_2 in the (9) can be written as:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\left(\frac{1}{R_{P1}} + \frac{1}{R_{P2}} + \frac{1}{R_{P3}}\right)\frac{1}{C} & 0 \\ 0 & \frac{R_2}{(R_1 + R_2)\, R_3 C_f} & 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ -\frac{1}{C} & -\left(\frac{1}{R_{P1}} + \frac{1}{R_{P2}} + \frac{1}{R_{P3}}\right)\frac{1}{C} & 0 \\ 0 & \frac{R_2}{(R_1 + R_2)\, R_3 C_f} & 0 \end{bmatrix}$$

and the vectors B_1 and B_2 are:

$$B_1 = B_2 = \begin{bmatrix} \frac{V_S}{L} \\ -\frac{I_{P1} + I_{P2} + I_{P3}}{C} \\ -\frac{V_{ref}}{R_3 C_f} \end{bmatrix}$$

The discrete mapping model is the best match for the converters in power electronics. There are various reasons for this match, however, the main reason is that a digital control system can be designed very easily using the sampled data model. The discrete mapping model focuses on the cycle-to-cycle behavior of the DC-DC converter system. Using the switching intervals described in equation (9) for ON and OFF time respectively, the sample data model for the simplified system presented in Fig. 10 can be given as:

$$\begin{aligned} x\,(kT + T) = {} & e^{A_2(1-d_k)T} e^{A_1 d_k T} x\,(kT) \\ & + e^{A_2(1-d_k)T} \int_0^{d_k T} e^{A_1 t} B_1 dt \\ & + \int_0^{(1-d_k)T} e^{A_2 t} B_2 dt \end{aligned} \tag{10}$$

Using the control period number in subscript for easiness, we obtain the following:

$$\begin{aligned} f\,(X_k) = X_{k+1} = {} & e^{A_2(1-d_k)T} e^{A_1 d_k T} x\,(kT) \\ & + e^{A_2(1-d_k)T} \int_0^{d_k T} e^{A_1 t} B_1 dt + \int_0^{(1-d_k)T} e^{A_2 t} B_2 dt \end{aligned} \tag{11}$$

Now, referring to Fig. 10, the reference voltage of the outer voltage loop (inverting terminal voltage of the comparator) can be given as:

$$v_p = \frac{1}{2}(V_{ref} - v_f - R_f i_f - 2V_D) \tag{12}$$

where V_D represents the voltage drop across the diode. In matrix notation:

$$v_p = M_p X + \frac{1}{3}\left[V_{ref}\left(1 + \frac{R_f}{R_3} - 2V_D\right)\right] \tag{13}$$

where,

$$M_p = \left[0 \; -\frac{R_2 R_f}{3R_3\,(R_1 + R_2)} \; -\frac{1}{3}\right] \tag{14}$$

The reference voltage for the inner current loop (non-inverting terminal voltage of the comparator) can be written as:

$$v_i = k i_s \tag{15}$$

where i_s is the source current (also known as the inductor current in the case of a boost-converter). In matrix notation:

$$v_i = M_i X \tag{16}$$

where,

$$M_i = \left[k \; 0 \; 0\right]$$

Using (13) and (16), the switching condition can be stated as:

$$s(d_k, X_k) = v_i - v_p = (M_i - M_p)\left(e^{A_1 d_k T} X_k + \int_0^{d_k T} e^{A_1 t} B_1 dt\right) - \frac{1}{3}\left[V_{ref}\left(1 + \frac{R_f}{R_3} - 2V_D\right)\right] \quad (17)$$

The above switching condition equation can be used to determine the duty ratio d_k for the k^{th} cycle. Once, the duty cycle is calculated using (17), it can be plugged into (11) and the solution can be obtained using the iterative approach. The Jacobian matrix for the proposed system whose discrete mapping model is given by the (11) can be stated as:

$$J(d_k, X_k) = \frac{\partial X_{k+1}}{\partial X_k} - \frac{\partial X_{k+1}}{\partial d_k}\left(\frac{\partial s}{\partial d_k}\right)^{-1} \frac{\partial s}{\partial X_k} \quad (18)$$

and the roots of the characteristic equation (18) gives the eigenvalues,

$$\det[\lambda I - J(d_k, X_k)] = 0 \quad (19)$$

By setting the equilibrium points for period-1 orbit as $X_Q = \left[I_{SQ} V_{OQ} V_{fQ}\right]^T$ and for period-2 orbit as $X_{Q2} = \left[I_{SQ2} V_{OQ2} V_{fQ2}\right]^T$ and $X^*_{Q2} = \left[I^*_{SQ2} V^*_{OQ2} V^*_{fQ2}\right]^T$, the resulting equations can be given as:

$$Period - 1 \begin{cases} f(X_Q) = X_Q \\ s(D_Q, X_Q) = 0 \end{cases} \quad (20)$$

$$Period - 2 \begin{cases} f(X_{Q2}) = X_{Q2} \\ f(X^*_{Q2}) = X^*_{Q2} \\ s(D_{Q2}, X_{Q2}) = 0 \\ s(D^*_{Q2}, X^*_{Q2}) = 0 \end{cases} \quad (21)$$

Hence, using (17), the duty ratio d_k is obtained and inserted into (11).

B. EIGENVALUES CALCULATION FROM THE SYSTEM OF EQUATIONS AND BIFURCATION DIAGRAM

The system of equations for the discrete mapping model of the simplified cascaded system is iterated with the initial state vector as $X_0 = [2500]^T$ for a range of input voltage values and the plot of the bifurcation diagram is shown in Fig. 12. The Jacobian matrix for the simplified cascaded system is obtained from the discrete mapping model and is presented in equation (18). By developing the Jacobian matrix, the system is again iterated, and the eigenvalues are obtained using the period-1 and period-2 conditions given by the equations (20) and (21). The eigenvalues of the simplified cascaded system of Fig. 10 for period-1 (λ_1) and period-2 (λ_2) orbits are shown in Table 3. The eigenvalues for period-1 at a source voltage of 35V are plotted in Fig. 13 and the eigenvalues for period-2 at a source voltage of 25V are plotted in Fig. 14.

It can be seen from the plots of the eigenvalues that one of the eigenvalues for period-2 is outside the unit circle which

TABLE 3. Eigenvalues of the period-1 and period-2 orbits.

V_S (V)	λ_1	λ_2
35	0.8633, 0.9507 ± j0.0231	0.8738, 0.9770, 0.9891
25	0.9512, 0.9705, 0.8759	1.3526, 0.9715, 0.8754

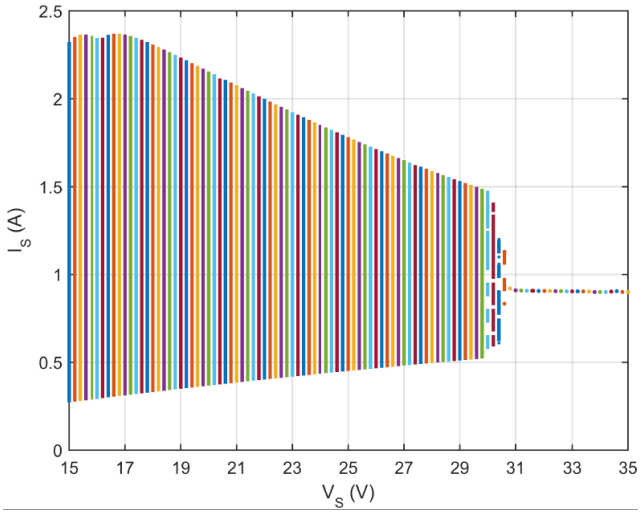

FIGURE 12. Bifurcation diagram of the proposed system iterated from state X_0.

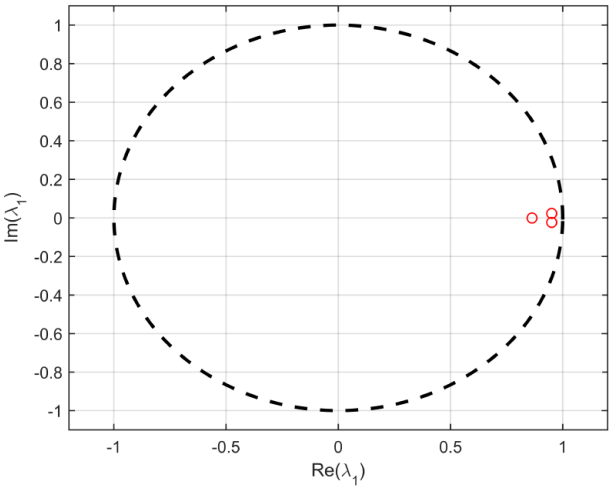

FIGURE 13. Eigenvalues of period-1 orbit.

indicates the non-linear behavior of the source boost converter as the voltage is decreased. The results obtained from the simulation, mathematical model, and hardware circuit are the same. When a DC-DC converter is regulated accurately at a specific equilibrium point with its fast enough dynamic response for a given practical application, it can be thought to operate as an FPL when all the components are considered ideal. Therefore, it can be generalized from the above analysis which simplifies the cascaded DC-DC converter system with suitable assumptions that the discrete mapping model is a suitable model for the analysis of bifurcation phenomena

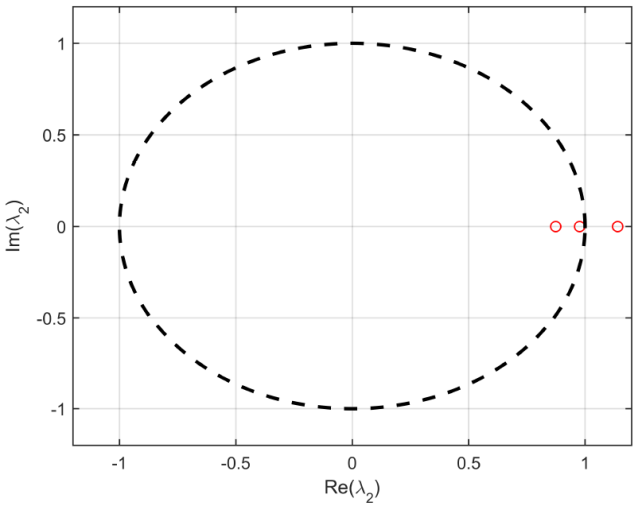

FIGURE 14. Eigenvalues of period-2 orbit.

in the cascaded multiple outputs DC-DC converter systems having any configuration.

The theoretical and experimental study presented in this paper provides adequate support for the modeling of modern renewable energy sources where input voltage varies with time. The proposed structure of the converters and investigations can be applied in DC distribution and DC microgrids with multiple input-output configurations to improve the stability and eliminate the complex non-linear dynamic behavior of load converters in the system.

V. CONCLUSION

This paper presents a configuration of the cascaded multiple output DC-DC converters to eliminate complex non-linear dynamic behavior and improve the stability when subjected to varying source voltage. The proposed cascaded DC-DC converter system consists of one source boost converter, one load Buck converter, one load Cuk converter, and a SEPIC converter. All the converters in the proposed system are engaged with a current-mode controller with a compensation network technique in which an outer voltage feedback loop and an inner inductor current feedback loop are used along with an offset divided voltage protection circuit and an RS-latch. The simulation and experimental results reveal that the source boost converter undergoes period-2 orbit and ultimately chaos when the input voltage of the source boost converter is decreased. However, it is verified that all the converters that are acting as a load in the proposed system continue to operate in the stable period-1 orbit and the input voltage of the source boost converter does not affect their stability. The discrete mapping model is developed by considering all the load converters as FPLs because of their stable behavior which also generalizes it for other types of converters. The Jacobian matrix is developed using the data of the discrete mapping model and the eigenvalues are obtained which are close to 1. So, by decreasing the input source voltage, the eigenvalues move out of the unit circle which results in period-2 behavior of the system that severely affects the stability of the whole cascaded converter system. The proposed structure makes load converters in the system insensitive towards input voltage variation which has been demonstrated analytically and using experimental results.

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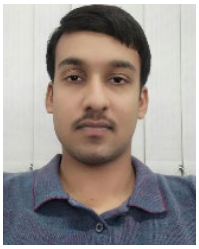

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