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The Generation Mechanism and Elimination Strategy of Narrow- and Error-Pulse for Cascaded H-Bridge NL-PWM Modulation

JIE MU[1], ZHIXUAN HE[1], (Student Member, IEEE), YONGHAI XU[1], (Member, IEEE), XUEYIN ZHANG[2], AND YUNBO LONG[1]

[1]State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China
[2]Nanjing NR Electric Company Ltd., Nanjing 211111, China

Corresponding author: Yonghai Xu (yonghaixu@263.net)

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ABSTRACT There is a wide application prospect of Nearest level pulse width modulation (NL-PWM) in cascaded H-bridge (CHB) converter, however, it will produce narrow- and error-pulse in the process of implementation, which has a negative impact on CHB efficiency, output voltage quality and safe operation of power devices. In this paper, the NL-PWM strategy is improved based on *round* function to solve the narrow pulse of traditional NL-PWM, and a step wave delay update strategy is proposed to solve the error-pulse of NL-PWM. This paper analyzes the basic principle of improved NL-PWM and its ability to avoid narrow pulse of power device, shows the harmonic characteristics of improved NL-PWM, analyzes the generation mechanism of error pulse, and calculates the error of output voltage caused by the proposed step wave delay update strategy. The correctness of theoretical analysis and the effectiveness of the proposed method are verified by simulation and experiment. The research shows that the improved NL-PWM can effectively prevent narrow pulse while maintaining good harmonic characteristics, and the proposed step wave delay update strategy can avoid error pulse and has little impact on the output of NL-PWM.

INDEX TERMS Cascade H-bridge, NL-PWM, error pulse, narrow pulse, harmonic characteristics.

I. INTRODUCTION

Cascaded H-bridge (CHB) converter is a widely used multilevel topology, and it is a research hotspot in the field of high-voltage and high-power converters [1]. CHB has many advantages, such as simple structure, excellent harmonic characteristics, easy modularization, high reliability and easy realization of redundant design, etc. [2], [3]. CHB multilevel converter is widely used in motor drive [4], new energy power generation [5], [6], active filter [7], flexible power transmission [8], static var compensator [9], power electronic transformer [10]–[13] and other fields.

Modulation strategy is the key technology of multilevel converters. It plays an important role in the output waveform quality, system reliability, working efficiency and service life of the converter, and has a great effect on the output power balance of each sub-module (SM) of CHB. At present, the modulation strategies used in CHB are mainly divided into the following three categories. The first type is high-frequency PWM modulation, which includes carrier phase shift PWM (CPS-PWM) [14], [15], level-shifted PWM(LS-PWM) [16], [17] and space vector PWM(SVPWM) [18]. The second type is nearest level modulation (NLM) [19], which is based on fundamental frequency modulation. And the last one is NL-PWM, which is a combination of high frequency PWM modulation and fundamental frequency modulation [20]. CPS-PWM has been widely studied because of its high equivalent switching frequency, good waveform quality and balanced switching frequency distribution. Compared with CPS-PWM, LS-PWM has better harmonic characteristics and can reduce the switching times. However, it needs additional equalization control, which has high control complexity and cannot achieve equivalent switching frequency doubling. SVPWM has high voltage utilization and good

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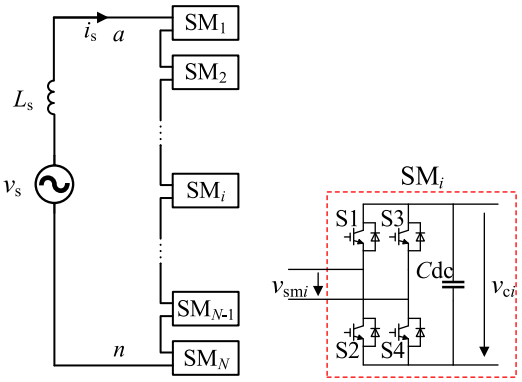

FIGURE 1. Topology of CHB.

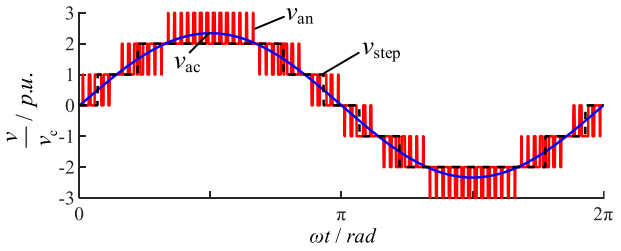

FIGURE 2. NL-PWM modulation principle.

waveform quality, but its voltage vector increases rapidly with the increase of the number of levels, and the modulation process is complicated. NLM adopts a step wave to approximate the sine reference voltage, which has the advantages of low switching frequency, simple voltage equalization control and small switching loss. It is widely used in high-voltage application, but when the number of levels is small, its dynamic response capability and the waveform quality are poor [21].

Reference [20] proposed the NL-PWM method for CHB, also known as hybrid pulse width modulation (HPWM), which combines the advantages of high frequency PWM and fundamental frequency modulation. In NL-PWM, only one SM in each bridge arm works in high-frequency PWM mode, and the other SMs output step waves. While retaining the advantages of NLM, it has the characteristics of less low-frequency harmonic content of PWM and higher waveform quality. NL-PWM uses voltage sorting method to implement voltage balancing control. The voltages of SMs are sampled and sorted in each voltage balancing period, and the output level of the SMs is controlled according to the sorting results and the bridge arm current direction. The output voltage quality of NL-PWM is compared with CPS-PWM in [22], proving that the output voltage quality of NL-PWM is better than that of CPS-PWM. However, in traditional NL-PWM method, the amplitude of the PWM reference voltage is equal to the amplitude of the triangular carrier voltage, and the SM working in the PWM mode will generate the narrow pulse. This may cause the switch devices failing to turn on or turn off, increase switching loss of devices, and even cause the switching device to be overheated and burned under long-term operation [23], [24]. In practical application, elimination technology of narrow pulse is required to eliminate these impacts. In addition, error pulses with incorrect level will appear during the implementation of NL-PWM, which has a negative impact on the output voltage quality and converter efficiency. The generation mechanism and elimination methods of error pulses have not been studied yet.

In view of the above problems, this paper is organized as follows. Section II analyzes the generation mechanism of the narrow pulse in traditional NL-PWM, proposes an improved NL-PWM based on *round* function to avoid the generation of the narrow pulse of the power device, and analyzes harmonic characteristics of the improved NL-PWM. Section III analyzes the generation mechanism of NL-PWM error pulse and its influence on the output voltage, proposes a step wave delay update strategy to eliminate the error pulse, and the error of the NL-PWM output voltage caused by the step wave delay update strategy is also analyzed in this section. The theoretical research is verified through simulation in section IV. Section V builds a CHB prototype to verify the correctness of the theoretical analysis. Finally, section VI summarizes the research work of this paper and makes an outlook for the next work.

II. NL-PWM NARROW PULSE AND ELIMINATION STRATEGY

A. NL-PWM NARROW PULSE GENERATION MECHANISM

The topology of CHB is shown in Fig. 1, which is composed of N full bridge SMs cascaded. In Fig. 1, L_s represents the AC filter inductance, v_s is grid voltage, i_s is grid current, v_{smi} and v_{ci} are the output voltage and capacitor voltage of the ith-SM respectively. Under stable operation, the capacitor voltages of each SM are equal, that is, $v_{c1} = v_{c2} = \ldots = v_c$.

NL-PWM is a modulation strategy that combines NLM and PWM. For the bridge arm with N SMs, $N-1$ SMs use NLM to output the step wave voltage v_{step}, and the remaining one SM outputs the PWM voltage v_{PWM}. The step wave voltage and the PWM voltage can be superimposed to get the $2N+1$ level output voltage v_{an} which is close to the sine reference wave.

$$v_{an} = v_{step} + v_{PWM} \tag{1}$$

Taking v_c as the reference voltage, the output voltage waveform of the bridge is shown in Fig. 2. In the figure, v_{ac} is the sinusoidal reference voltage, and its expression is

$$v_{ac} = MNv_c \cos(\omega_r t + \theta_r) = MNv_c \cos y \tag{2}$$

where, M is the modulation ratio; N is the number of SMs in the bridge arm; ω_r, θ_r are the frequency and initial phase of the sinusoidal reference voltage, respectively.

Under the normalization condition, the PWM reference voltage is obtained by subtracting the sinusoidal reference voltage v_{ac} and the step wave voltage v_{step}. The step wave voltage and PWM reference voltage of the traditional NL-PWM method are shown in Fig. 3. At the jumping point of the step wave, the value of the PWM reference voltage is

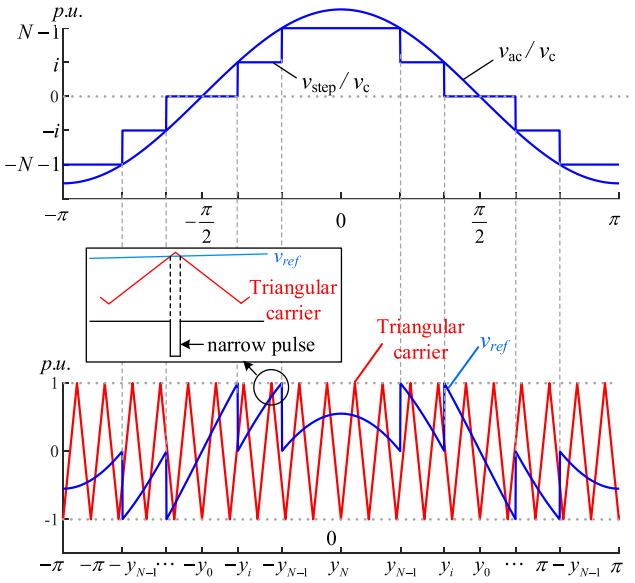

FIGURE 3. Step wave voltage and PWM reference voltage of traditional NL-PWM.

equal to the carrier amplitude, and PWM narrow pulse will appear due to full modulation. In practice, it is necessary to use elimination methods such as modulation wave limiting and switching device delay on-off to avoid the generation of narrow pulse. But these methods will inevitably distort the modulation wave and affect the waveform quality.

B. THE IMPROVED NL-PWM

If the phase of the step wave jumping point can be adjusted, the amplitude of the PWM reference voltage will be changed, thereby the narrow pulses can be avoided. For this reason, an improved NL-PWM modulation using *round* function to generate a step wave is proposed in this paper. The expression of the step wave voltage v_{step} is

$$v_{\text{step}} = round(v_{\text{ac}}/v_{\text{c}}) \cdot v_{\text{c}} \tag{3}$$

where, $round(\cdot)$ represents *round* function.

Taking v_{c} as the reference voltage, the PWM reference voltage of the improved NL-PWM can be expressed as

$$v_{ref} = \frac{v_{\text{ac}} - v_{\text{step}}}{v_{\text{c}}} = \frac{v_{\text{ac}}}{v_{\text{c}}} - round(v_{\text{ac}}/v_{\text{c}}) \tag{4}$$

The reference voltage of PWM is separated by step wave jump point, and its waveform is segmented sawtooth shape. As shown in Fig. 4, it can be expressed as the sum of N parts

$$v_{ref}(i) = \begin{cases} NM\cos y - i + 1, \\ y \in (-y_{i-1}, -y_i) \cup (y_i, y_{i-1}) \\ NM\cos y + i - 1, \\ y \in [\pi - y_{i-1}, \pi - y_i] \cup [-(\pi - y_i), -(\pi - y_{i-1})] \end{cases} \tag{5}$$

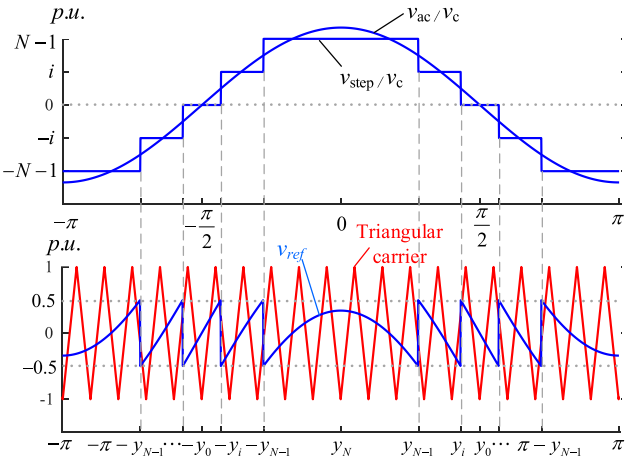

FIGURE 4. Step wave voltage and PWM reference voltage of improved NL-PWM.

In Fig. 4, the step wave jumping point can be expressed as

$$y_i = \begin{cases} 0, & i > NM + 1/2 \\ \arccos(\dfrac{i - 1/2}{NM}), & 0 < i \le NM + 1/2 \\ \dfrac{\pi}{2}, & i = 0 \end{cases} \tag{6}$$

As shown in Fig. 4, the value of the PWM reference voltage at the step wave jumping point of the improved NL-PWM is only 0.5, regardless of the value of M. There is no narrow pulse due to the equal amplitude of the PWM reference voltage and the triangular carrier. The amplitude of v_{ref} at the 0 and π radian in the fundamental frequency cycle is $1 - N(1 - M)$. When the frequency of triangular carrier $f_{\text{c}} = 3000\text{Hz}$ and $N = 5$, only if M is greater than 0.994, the narrow pulse with the width less than $10\mu\text{s}$ will be generated. As the number of SMs increases, the value of M will continue to increase. If the converter modulation ratio is too high, it will affect the output of inductive reactive power, and this situation is relatively rare. Therefore, narrow pulse can be avoided without additional elimination technology using the improved NL-PWM.

According to the theory of double Fourier transform, the Fourier series expression of the improved NL-PWM output voltage can be obtained

$$\begin{aligned} v_{\text{an}} &= v_{\text{step}} + v_{\text{PWM}} \\ &= NMv_{\text{c}}\cos y + \sum_{m=2,4,6}^{\infty} \sum_{n=\pm1,\pm3,\pm5}^{\pm\infty} [A_{mn}\cos(mx + ny)] \\ &= NMv_{\text{c}}\cos\omega_r t \\ &\quad + \sum_{m=2,4,6}^{\infty} \sum_{n=\pm1,\pm3,\pm5}^{\pm\infty} [A_{mn}\cos(m\omega_c t + n\omega_r t)] \end{aligned} \tag{7}$$

where, the expression of A_{mn} is (8), as shown at the bottom of the next page.

NL-PWM outputs PWM voltage and step wave voltage at the same time, which belongs to unbalanced modulation,

TABLE 1. Voltage balancing method of improved NL-PWM.

Value of v_{ac}	Value of i_s	Output of SMs		
		SMs with Low Voltage	SM with Middle Voltage	SMs with High Voltage
$v_{ac}\geqslant 0$	$i_s\geqslant 0$	$+v_c$	PWM	0
$v_{ac}\geqslant 0$	$i_s<0$	0	PWM	$+v_c$
$v_{ac}<0$	$i_s\geqslant 0$	0	PWM	$-v_c$
$v_{ac}<0$	$i_s<0$	$-v_c$	PWM	0

so it is necessary to equalize the voltage of each SM. The improved NL-PWM uses voltage sorting method to realize the voltage balancing of SMs. The output voltage of SMs is determined by the value of v_{ac}, i_s and the voltage of the SMs. The specific voltage balancing method of the proposed improved NL-PWM is shown in Table 1.

The power loss of a modulation strategy is mainly caused by the switching of the power devices. In order to reduce the loss of the improved NL-PWM, the switching time of voltage balancing can be set at the step wave jump point. Voltage balancing switching of traditional NL-PWM is carried out in each PWM carrier period. Compared with traditional NL-PWM, the improved NL-PWM can effectively reduce the number of additional switches generated by voltage balancing switching while ensuring the voltage balancing effect, so the power loss of improved NL-PWM is smaller. In addition, NL-PWM method outputs PWM voltage and step wave voltage at the same time. Only one SM works in high-frequency PWM mode, and the other SMs work in fundamental frequency mode. Therefore, the power device switching frequency and power loss of improved NL-PWM is much smaller than that of conventional strategies such as CPS-PWM.

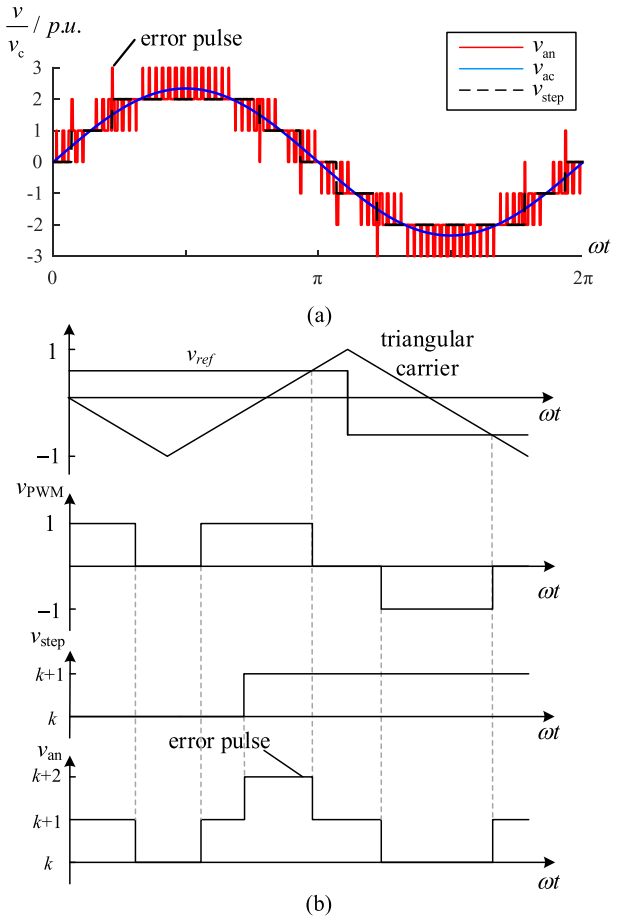

FIGURE 5. The error pulse of NL-PWM and its generating mechanism (a: NL-PWM error pulse; b: generation mechanism of error pulse).

III. NL-PWM ERROR PULSE AND ELIMINATION STRATEGY

A. NL-PWM ERROR PULSE AND ITS GENERATION MECHANISM

NL-PWM error pulse and its generation mechanism are shown in Fig. 5. In Fig. 5(b), v_{PWM} is the PWM output voltage under unipolar frequency double modulation. v_{step} is the step wave voltage; v_{an} is the CHB output voltage after the step wave and the PWM wave are superimposed. Because each SM of NL-PWM may work in PWM mode, but the number of ePWM channels of DSP is limited, the controller architecture of FPGA + DSP is usually adopted in practical application. The step wave level and PWM level are calculated and generated by DSP, and the distribution between different SMs

$$A_{mn}=\begin{cases} NMv_c-\frac{4v_c}{\pi}\sum_{i=1}^{N-1}\sin y_i,\ m=0,n=1 \\ -\frac{4v_c}{n\pi}\sum_{i=1}^{N-1}\sin ny_i,\ m=0,n=3,5,7\ldots \\ \frac{8v_c}{m\pi^2}\sum_{i=1}^{N}\cos\frac{mi\pi}{2}\left\{\begin{array}{l}\sin\frac{k\pi}{2}J_k(\frac{m\pi NM}{2}) \\ \sum_{k=1,3,5\ldots}^{\infty;k\neq\pm n}[\frac{\sin(n+k)y_{i-1}-\sin(n+k)y_i}{n+k} \\ \quad+\frac{\sin(n-k)y_{i-1}-\sin(n-k)y_i}{n-k}] \\ +\sum_{k=1,3,5\ldots}^{\infty;k=\pm n}\sin\frac{k\pi}{2}J_k(\frac{m\pi NM}{2}) \\ \quad[y_{i-1}-y_i+\frac{\sin 2ky_{i-1}-\sin 2ky_i}{2k}]\end{array}\right\} \\ m=2,4,6,\ldots,n=\pm1,\pm3,\pm5,\ldots \end{cases} \tag{8}$$

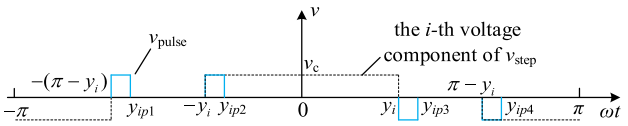

FIGURE 6. Equivalent pulse voltage.

is realized by FPGA. The step wave level and PWM level are calculated by DSP, and the distribution of the two between different SMs is implemented by FPGA. In the implementation process, the step wave usually updates its reference value through DSP in a control interrupt, and the corresponding SM outputs the step wave voltage through FPGA after the interruption. While PWM usually adopts asymmetric regular sampling [33], the modulation wave is updated in the control interrupt, but the PWM trigger pulse is loaded and generated at the peak and valley value of PWM triangular carrier. When step wave voltage jumps, the reference voltage of PWM wave will have a step change, but the step wave and PWM modulation wave cannot be updated synchronously due to the loading mechanism of PWM, which will lead to the generation of error pulse.

In the presence of error pulse, the NL-PWM output voltage can be equivalent to the superposition of the correct NL-PWM output voltage and the pulse voltage with the value of $\pm v_c$ as shown in Fig. 6.

In Fig. 6, y_{ipk} $(k = 1, 2, 3, 4)$ is the end time of the error pulse corresponding to the i-th step wave component, and its value can be calculated according to the carrier frequency, modulation ratio, number of bridge arm modules and the value of y_i. The pulse voltage can be expanded by Fourier series:

$$v_{\text{pulse}} = \sum_{n=1,3,5\ldots}^{\infty} \left((P_{1n} + 8\sin ny_i)\cos ny + P_{2n}\sin ny\right) + \sum_{n=2,4,6\ldots}^{\infty} \left(P_{1n}\cos ny + P_{2n}\sin ny\right) \quad (9)$$

where

$$P_{1n} = \frac{v_c}{n\pi}\sum_{i=1}^{N-1}\left(\sin ny_{ip1} + \sin ny_{ip2} - \sin ny_{ip3} - \sin ny_{ip4} + 4\sin ny_i\right)$$

$$P_{2n} = \frac{v_c}{n\pi}\sum_{i=1}^{N-1}\left(\sin ny_{ip1} + \sin ny_{ip2} - \sin ny_{ip3} - \sin ny_{ip4}\right)$$

$$Q_n = -\frac{v_c}{n\pi}\sum_{i=1}^{N-1} \times \left(\cos ny_{ip1} + \cos ny_{ip2} - \cos ny_{ip3} - \cos ny_{ip4}\right)$$

The Fourier series expression of output voltage can be expressed as (10) according to (7) and (9) with the error pulse consideration.

$$v_{\text{an}} = \sqrt{(NMv_c + P_{11})^2 + Q_1^2}\cos\left(\omega_r t - \varphi_{p1}\right) + \sum_{n=3,5,7}^{\infty}\sqrt{P_{1n}^2 + Q_n^2}\cos\left(n\omega_r t - \varphi_{pn}\right) + \sum_{n=2,4,6}^{\infty}\sqrt{P_{2n}^2 + Q_n^2}\cos\left(n\omega_r t - \varphi_{pn}\right) + \sum_{m=2,4,6}^{\infty}\sum_{n=\pm1,\pm3,\pm5}^{\pm\infty}\left[A_{mn}\cos\left(m\omega_c t + n\omega_r t\right)\right] \quad (10)$$

B. STEP WAVE DELAY UPDATE STRATEGY

According to the generation mechanism of error pulse, in order to solve the problem, it is necessary to make the loading time of the step wave level and PWM level as consistent as possible. Since the time required for each execution of DSP control interrupt is not fixed, it is difficult to adjust the end time of control interrupt. Therefore, the end time of control interrupt cannot be corresponding to the peak and valley time of PWM triangular carrier. In order to solve the problem of error pulse, this paper proposes a step wave delay update strategy. In the case that PWM adopts asymmetric regular sampling, the step wave is properly delayed within half of the carrier cycle, so that the step wave voltage and PWM voltage can be updated synchronously, and the problem of error pulse can be solved.

The step wave delay update strategy sets the end time of the control interrupt earlier than the peak and valley time of the PWM triangular carrier to complete the update of the step wave reference value. At the same time, an interrupt is set at the peak and valley time of the PWM triangular carrier, and the step wave voltage will complete the loading and output at this interrupt to realize the synchronous loading of the step wave and the PWM wave. Due to hardware delay and other reasons, the time when the step wave voltage changes do not completely correspond to the peak and valley value of PWM carrier. If the delay is too long, the error pulse will still appear. Therefore, it is necessary to analyze the allowable range of the delay time.

The SM working in the PWM mode adopts unipolar frequency multiplication modulation, and the reference voltage amplitude of the improved NL-PWM is 0.5 at the step wave jump point, so the PWM output voltage is 0 within the range of 1/8 carrier period from the peak and valley values of the triangular carrier. Therefore, the delay time t_d needs to satisfy the following condition

$$|t_d| < \frac{1}{8f_c} \quad (11)$$

where, f_c is the frequency of the triangular carrier. When the above condition is satisfied, even if the change time of step wave voltage does not completely correspond to the peak and valley value of PWM carrier, there will not be error pulse in the output voltage of NL-PWM, as shown in Fig. 7.

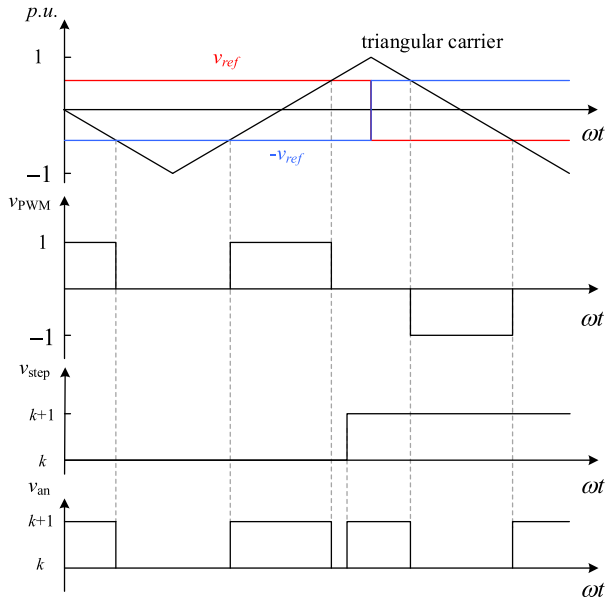

FIGURE 7. Elimination mechanism of error pulse of NL-PWM.

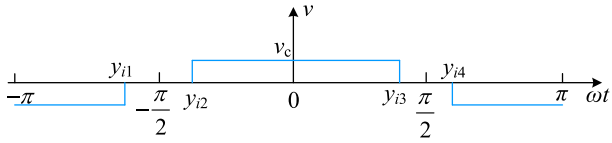

FIGURE 8. Decomposition of step wave.

The step wave can be regarded as the superposition of $N-1$ components with amplitude $\pm v_c$. After using the step wave delay update strategy, the schematic diagram of the i-th voltage component is shown in Fig. 8. In the figure, y_{ik} $(k = 1, 2, 3, 4)$ is the phase of the k-th jumping point of the voltage component, and

$$\begin{aligned} y_{i1} &= -(\pi - y_i) + y_{ei1} \\ y_{i2} &= -y_i + y_{ei2} \\ y_{i3} &= y_i + y_{ei3} \\ y_{i4} &= \pi - y_i + y_{ei4} \end{aligned} \tag{12}$$

The expression of y_i is shown in (6). $y_{eik} = t_{eik}/0.02^*2\pi$ is the phase delay of the k-th jumping point of the voltage component. t_{eik} is the delay time of the jumping point, and the value of t_{eik} meets the following requirement:

$$0 \le t_{eik} \le \frac{1}{2f_c} \tag{13}$$

The Fourier series expression of the step wave voltage v_{step1} after using the step wave delay update strategy is

$$v_{\text{step1}} = \sum_{n=1}^{\infty} (C_n \cos ny + D_n \sin ny) \tag{14}$$

where

$$C_n = -\frac{v_c}{n\pi} \sum_{i=1}^{N-1} (\sin ny_{i1} + \sin ny_{i2} - \sin ny_{i3} - \sin ny_{i4})$$

$$D_n = \frac{v_c}{n\pi} \sum_{i=1}^{N-1} (\cos ny_{i1} + \cos ny_{i2} - \cos ny_{i3} - \cos ny_{i4})$$

Using the step wave delay update strategy, it can be obtained that the output voltage expression of NL-PWM is

$$\begin{aligned} v_{\text{an}} = &\sqrt{(NMv_c + C_1 + A_{01})^2 + D_1^2} \cos(\omega_r t - \varphi_{d1}) \\ &+ \sum_{n=2,4,6}^{\infty} \sqrt{C_n^2 + D_n^2} \cos(n\omega_r t - \varphi_{dn}) \\ &+ \sum_{n=3,5,7}^{\infty} \sqrt{(C_n + A_{0n})^2 + D_n^2} \cos(n\omega_r t - \varphi_{dn}) \\ &+ \sum_{m=2,4,6}^{\infty} \sum_{n=\pm1,\pm3,\pm5}^{\pm\infty} [A_{mn} \cos(m\omega_c t + n\omega_r t)] \end{aligned} \tag{15}$$

where, the expression of A_{mn} is shown in (8), and the expression of φ_{dn} is

$$\varphi_{dn} = \begin{cases} \arctan \dfrac{D_1}{NMv_c + C_1 + A_{01}}, & n = 1 \\ \arctan \dfrac{D_n}{C_n}, & n = 2, 4, 6 \cdots \\ \arctan \dfrac{D_n}{C_n + A_{0n}}, & n = 3, 5, 7 \cdots \end{cases} \tag{16}$$

It can be obtained from (10) and (15) that, when using the step wave delay update strategy to eliminate the error pulse voltage, the NL-PWM output voltage expression is

$$\begin{aligned} v_{\text{an}} = &\sqrt{(NMv_c + C_1 + A_{01} + P_{11})^2 + (D_1 + Q_1)^2} \\ &\times \cos(\omega_r t - \varphi_1) \\ &+ \sum_{n=2,4,6}^{\infty} \sqrt{(C_n + P_{2n})^2 + (D_n + Q_n)^2} \cos(n\omega_r t - \varphi_n) \\ &+ \sum_{n=3,5,7}^{\infty} \sqrt{(C_n + A_{0n} + P_{1n})^2 + (D_n + Q_n)^2} \\ &\times \cos(n\omega_r t - \varphi_n) \\ &+ \sum_{m=2,4,6}^{\infty} \sum_{n=\pm1,\pm3,\pm5}^{\pm\infty} A_{mn} \cos(m\omega_c t + n\omega_r t) \end{aligned} \tag{17}$$

The delay of the step wave will cause errors between the amplitude and phase of the fundamental component of the actual output voltage and the theoretical value, which will have a negative impact on the output voltage. If the error is too large, it means that the method is not feasible. According to (17), for a CHB with 2-8 SMs, when the carrier frequency $f_c = 3000$Hz and $M = 0.9$, the amplitude error δ and phase delay φ_{dn} of the fundamental frequency component of output voltage after using step wave delay update strategy are shown in Fig. 9. It can be seen from the figure that the amplitude error δ of the fundamental frequency component

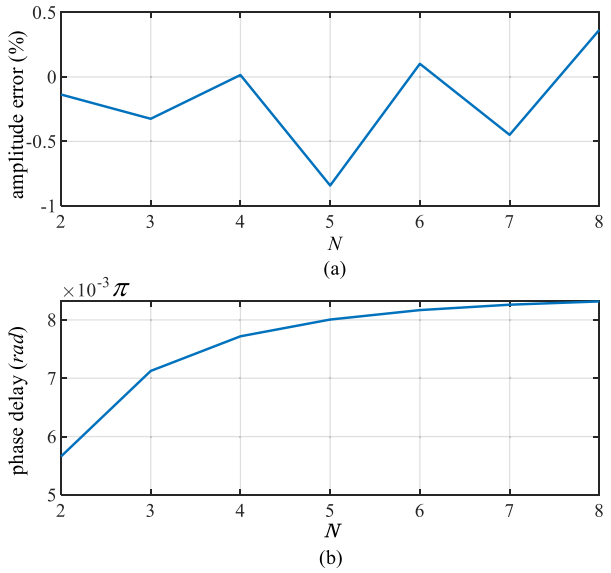

FIGURE 9. Error of fundamental frequency component of output voltage (a: amplitude error; b: phase delay).

of the NL-PWM output voltage caused by step wave delay update strategy is less than 0.9%, and the phase delay φ_{dn} is less than $9 \times 10^{-3}\pi$. The errors can be ignored in practical application.

IV. SIMULATION ANALYSIS

A. SPECTRUM ANALYSIS OF PROPOSED NL-PWM METHOD

Based on the results of theoretical analysis, the spectrums and THDs of NL-PWM are analyzed when $N = 2$, $M = 0.78$, and $f_c = 3000$Hz.

According to (7) and (8), the spectrum of improved NL-PWM is shown in Fig. 10(a), and the spectrum of traditional NL-PWM [22] is shown in Fig. 10(b). As can be seen from Fig. 10, the THDs (2^{nd}-255^{th} harmonics) of improved NL-PWM and traditional NL-PWM are 33.6% and 34.58% respectively, and the harmonic characteristics of improved NL-PWM are better than traditional NL-PWM with the same number of SMs.

According to (10), the spectrum of NL-PWM with the presence of error pulse is shown in Fig. 11. We can see from Fig. 11 that the THD (2^{nd}-255^{th} harmonics) of the NL-PWM output voltage after superimposing the error pulse is 35.53%. Comparing Fig. 10(a) and Fig. 11, it can be seen that the error pulse will increase the harmonic content of the low frequency and reduce the NL-PWM output voltage. Therefore, it is necessary to adopt reasonable method to eliminate the adverse effects of error pulse.

According to (17), when using step wave delay update strategy to eliminate error pulse, the spectrum of NL-PWM is shown in Fig. 12. Comparing Fig. 11 and Fig. 12, we can see that the proposed step wave delay update strategy can reduce the NL-PWM output voltage THD (2^{nd}-255^{th} harmonics) to 34.53%, effectively eliminating the adverse effects caused by error pulse.

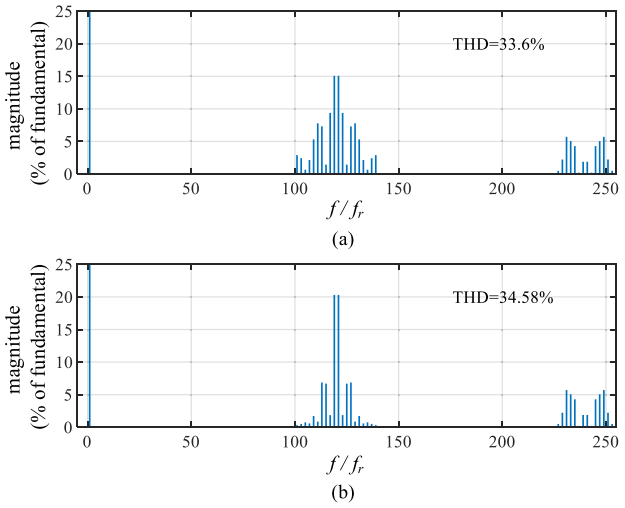

FIGURE 10. Spectrums and THDs of output voltages under 5 level (a: Improved NL-PWM; b: Traditional NL-PWM).

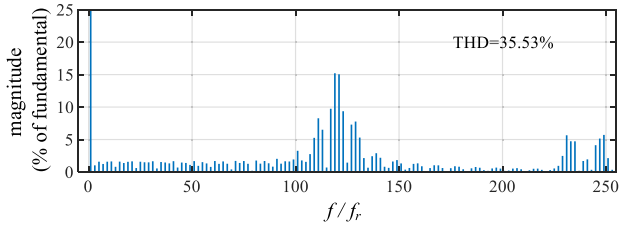

FIGURE 11. Spectrums and THDs of output voltages with error pulses under 5 level.

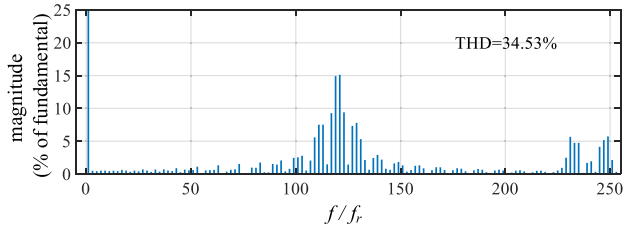

FIGURE 12. Spectrums and THDs of output voltages after eliminating error pulses under 5 level.

B. VERIFICATION OF THEORETICAL ANALYSIS

In order to verify the effectiveness of proposed NL-PWM methods, a CHB model is established in PSCAD/EMTDC and main parameters of the model are shown in Table 2.

Fig. 13 and Fig. 14 show the output voltage simulation waveforms and their enlarged waveforms at the step wave jumping point of traditional NL-PWM and improved NL-PWM, respectively. From the two figures, it can be seen that the pulse width of the traditional NL-PWM is about 3μs at the jumping point, which has a narrow pulse problem.

TABLE 2. Parameters of simulation model.

Parameters	Values
AC grid voltage U/kV	10
Sub-module voltage v_c/kV	5.23
Modulation ratio M	0.78
Number of bridge arm sub modules N	2
Sub-module capacitance C/μF	2750
PWM carrier frequency f_c/Hz	3000

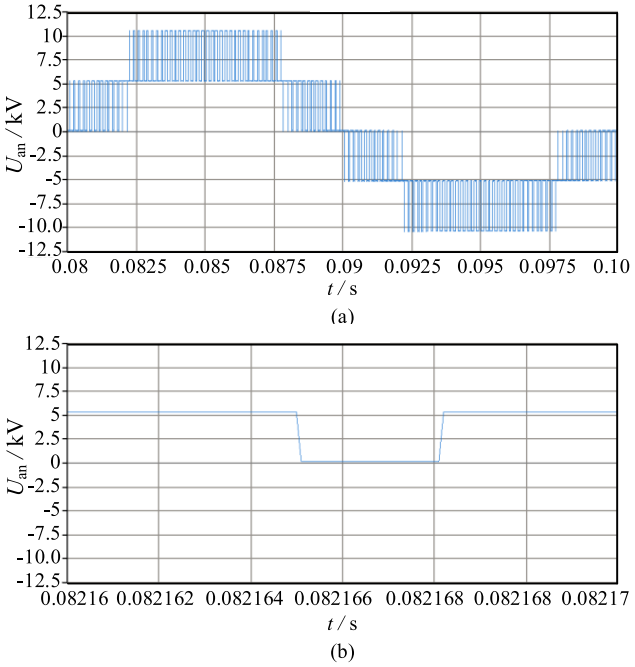

FIGURE 13. Simulation results of output voltage of traditional NL-PWM (a: output voltage waveform; b: waveform amplification at the jumping point).

Whereas, a pulse width of about 40μs occurs for the improved NL-PWM with narrow pulse disappearing. Also, the THDs (2^{nd}-255^{th} harmonics) of improved NL-PWM and traditional NL-PWM are 33.69% and 34.56% respectively. The harmonic characteristics of improved NL-PWM are better than that of traditional NL-PWM.

The improved NL-PWM output voltage waveform under asymmetric regular sampling is shown in Fig. 15. Comparing Fig. 5(a) and Fig. 15, we can see that the position of the NL-PWM error pulse is consistent with the theoretical analysis, which proves the correctness of the error pulse generation mechanism. Before and after the error pulse is eliminated, the spectrums of NL-PWM are shown in Fig. 16. It can be seen that the output voltage of NL-PWM has a higher low-frequency harmonic content in the presence of the error pulse, and the THD (2^{nd}-255^{th} harmonics) content is 36.21%. After using the step wave delay update strategy, the THD (2^{nd}-255^{th} harmonics) content of the output voltage is reduced to 34.48%. The step wave delay update strategy can effectively eliminate the adverse effects caused by the error pulse and improve the output voltage quality of NL-PWM.

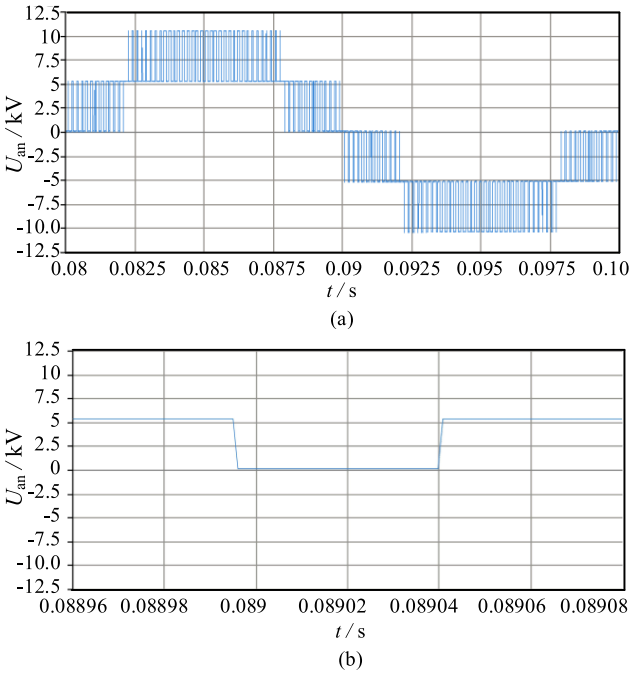

FIGURE 14. Simulation results of output voltage of improved NL-PWM (a: output voltage waveform; b: waveform amplification at the jumping point).

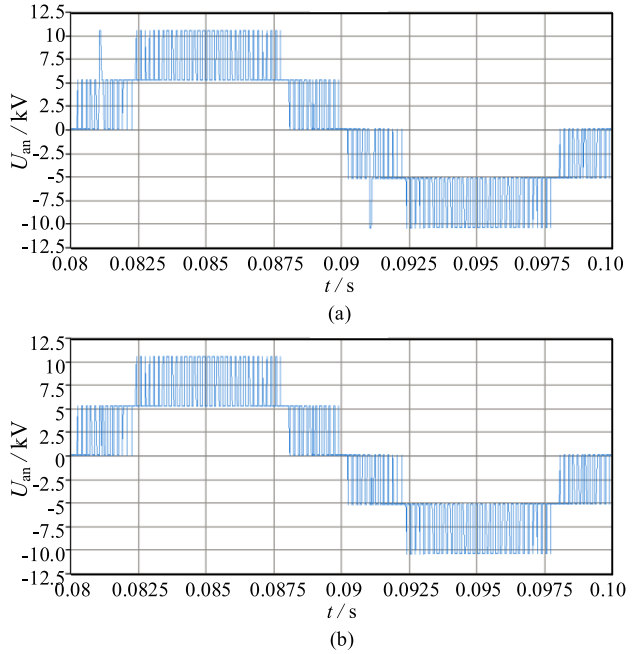

FIGURE 15. Simulation results of output voltage of NL-PWM under asymmetric regular sampling (a: before eliminating error pulse; b: after using step wave delay update strategy).

In addition, comparing Fig. 11, Fig. 12 and Fig. 16, it can be seen that after error pulse is eliminated, the simulation results of the output voltage spectrum are consistent with the

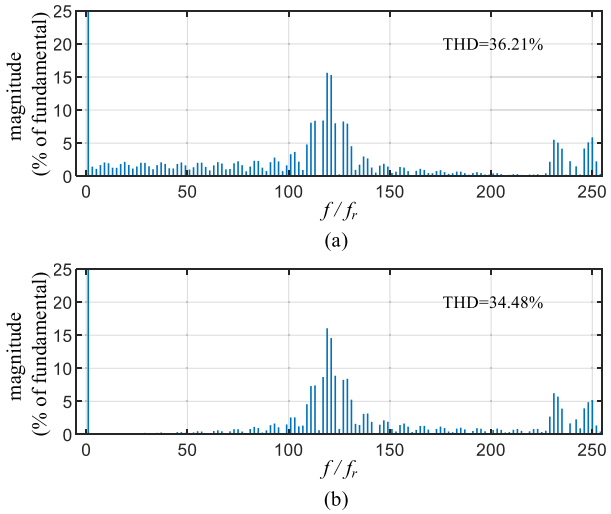

FIGURE 16. Simulation results of spectrums and THDs of output voltage before and after eliminating error-pulse (a: before eliminating the error pulse; b: after eliminating the error pulse).

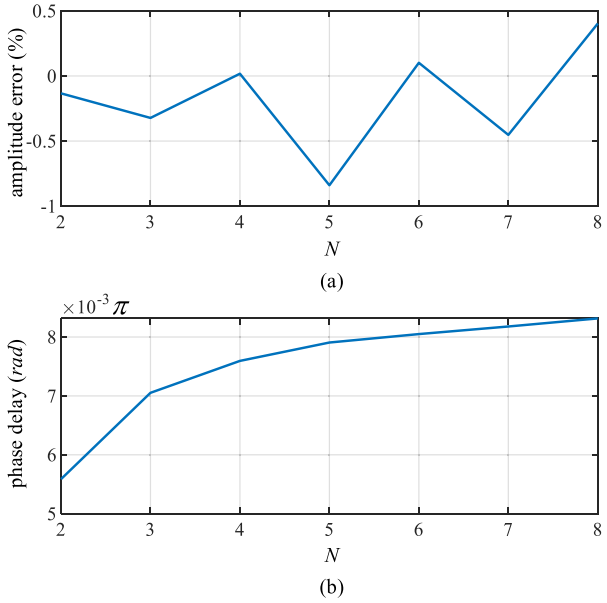

FIGURE 17. Simulation results of the error of fundamental frequency component of output voltages (a: amplitude error; b: phase delay).

theoretical analysis results, which proves the correctness of the theoretical analysis.

In order to study the error of NL-PWM caused by step wave delay update strategy, a CHB with 2-8 SMs is built under the condition of modulation ratio $M = 0.9$. When the step wave jumping point is delayed to the peak and valley value of triangular carrier, the amplitude error and phase delay of the fundamental frequency component of NL-PWM relative to the sinusoidal modulation wave are shown in Fig. 17. Comparing Fig. 9 and Fig. 17, we can see that the theoretical analysis of the error of the step wave delay update strategy is correct. Fig. 18 shows the simulation result of the fundamental error of the output voltage due to asymmetric regular sampling before eliminating the error pulse. Comparing Fig. 17 and Fig. 18, it can be seen that before the error pulse is eliminated, the fundamental frequency component of the output voltage has an error within $\pm 1\%$ in terms of amplitude. The step wave delay update strategy does not significantly increase the amplitude of the fundamental component of the output voltage. In terms of the phase delay of the fundamental wave of the output voltage, the delay update of the step wave improves the phase delay, but the phase delay φ_1 is less than $9 \times 10^{-3}\pi$ after the error pulse is eliminated. The influence can be ignored in practical application.

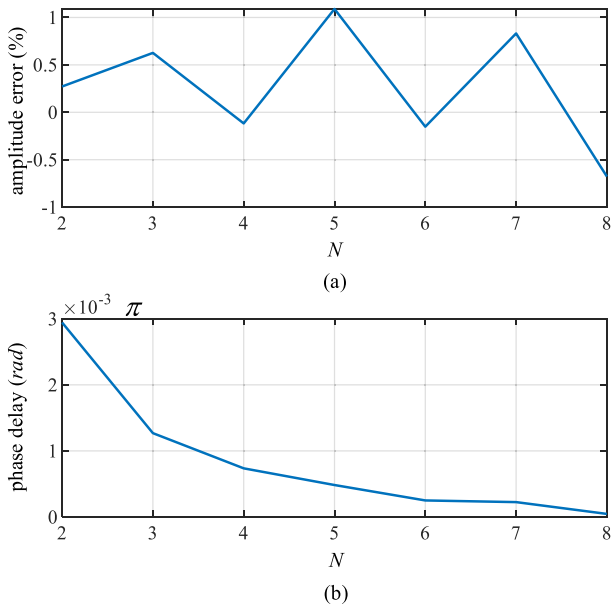

FIGURE 18. Simulation results of the error of fundamental frequency component of output voltages before eliminating error-pulse (a: amplitude error; b: phase delay).

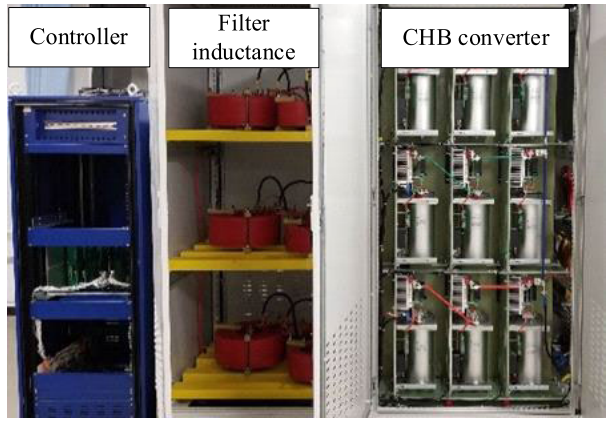

FIGURE 19. Prototype of MMC.

V. EXPERIMENTAL VERIFICATION

In order to verify the feasibility of the proposed NL-PWM narrow-and error-pulse elimination method in the actual system, this paper built a three-phase CHB prototype as shown in Fig. 19 for experimental verification.

TABLE 3. Parameters of prototype.

Parameters	Values
AC grid voltage U/V	100
AC grid frequency f_r/Hz	50
Number of bridge arm sub modules N	2
Bridge arm inductance/mH	1.5
Sub-module capacitance C/μF	2600
Sub-module voltage v_c/V	52
Rated power P_N/kW	2
PWM carrier frequency f_c/Hz	3000
Modulation ratio M	0.78

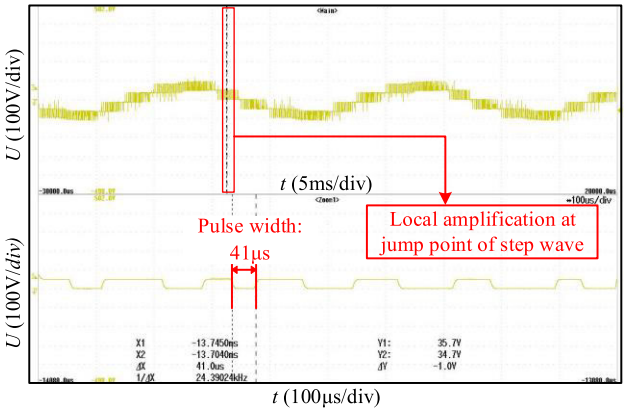

FIGURE 20. Experimental results of output voltage and narrow pulse with the improved NL-PWM.

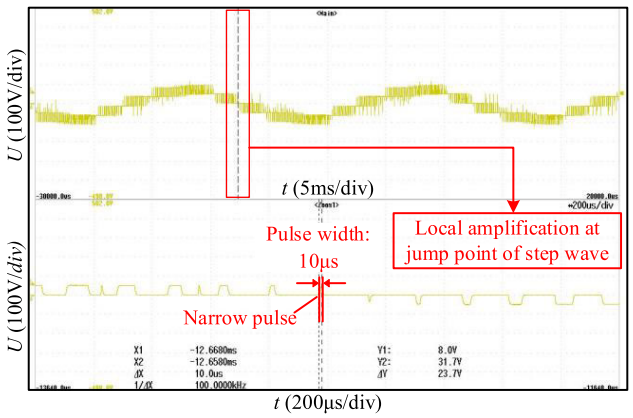

FIGURE 21. Experimental results of output voltages and narrow pulses with the traditional NL-PWM.

The main parameters of the prototype are shown in Table 3. The AC side of the CHB prototype is connected to the AC power grid, and the DC side is connected to a resistor to simulate a DC load.

Fig. 20 and Fig. 21 show the phase voltage experimental results of the improved NL-PWM and the traditional NL-PWM, as well as the local amplified waveforms in the case of narrow pulse at the jumping point. The waveforms in the lower half of the figures are the amplification of the waveform in the red box in the upper half of each figures. In order to ensure the safety of the experiment, the narrow pulse less than 10μs will be delayed to 10μs. It can be seen from

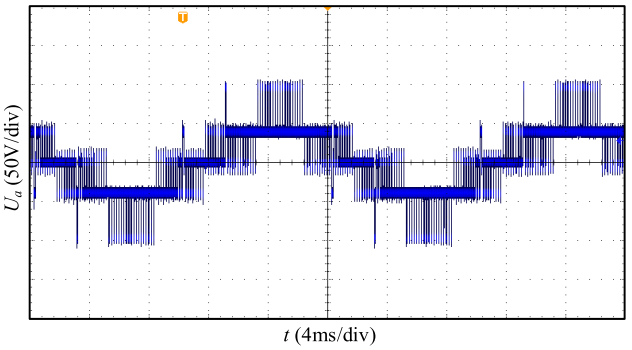

FIGURE 22. Experimental results of output voltage without eliminating error pulse.

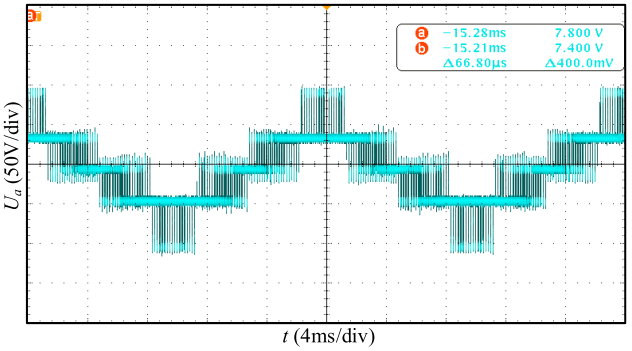

FIGURE 23. Experimental results of output voltage after eliminating error pulse.

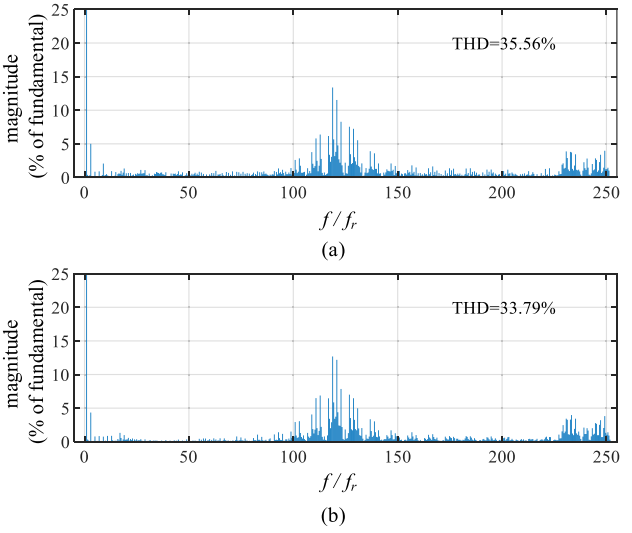

FIGURE 24. Experimental results of spectrums and THDs of output voltage before and after eliminating error pulse (a: before eliminating the error pulse; b: after eliminating the error pulse).

Fig. 20 that the PWM pulse width at the step wave jumping point of the traditional NL-PWM method is only 10μs, and there is a narrow pulse. In practical application, additional control is needed to eliminate narrow pulse. And in Fig. 21, the PWM pulse width at the jumping point of the improved NL-PWM is 41μs, and there is no narrow pulse generated by voltage sharing switching.

Fig. 22 and Fig. 23 show the experimental results of the phase voltage before and after the error pulse is eliminated, respectively. Comparing Fig. 5(a) and Fig. 22, it can be seen that the position of NL-PWM error pulse is consistent with the theoretical analysis. Comparing Fig. 22 and Fig. 23, it can be seen that the error pulse shown in Fig. 22 does not exist at the corresponding position of the output voltage waveform shown in Fig. 23, and the error pulse elimination effect is obvious, which can explain the correctness of the NL-PWM error pulse theoretical analysis and the effectiveness of the delayed update strategy in eliminating error pulse. After the error pulse is eliminated, the CHB phase voltage THD (2^{nd}-255^{th} harmonics) is reduced from 35.56% to 33.79%, and the frequency spectrum is shown in Fig. 24. Comparing Fig. 11, Fig. 12, Fig. 16 and Fig. 24, it can be seen that the experimental results of the phase voltage spectrum are basically consistent with the simulation and theoretical analysis results, proving that the proposed step wave delay update strategy has good results in practical application. Also, the THD (2^{nd}-255^{th} harmonics) of traditional NL-PWM in Fig. 20 (error pulse is eliminated) is 34.22%, and the harmonic characteristics of improved NL-PWM are better than that of traditional NL-PWM.

VI. CNOCLUSION

Aiming at the problem of narrow- and error-pulse in the implementation of NL-PWM, this paper proposed an improved NL-PWM based on the *round* function and a step wave delay update strategy. Through theoretical analysis, simulation and experimental verification, the following conclusions can be drawn:

(1) The improved NL-PWM based on the *round* function can avoid the narrow pulse of traditional NL-PWM while maintaining good harmonic characteristics.

(2) The step wave delay update strategy can effectively solve the problem of error pulse in NL-PWM, and it has a little negative impact on the output voltage of NL-PWM.

This paper focuses on CHB converter. The next step is to study the implementation methods of NL-PWM in other converter topologies such as MMC to further improve the application scope and practical engineering application value of NL-PWM.

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JIE MU was born in Hengshui, Hebei, China, in 1997. He received the B.S. degree in electrical engineering and automation from North China Electric Power University, where he is currently pursuing the M.S. degree. His research interests include multilevel converter and solid-state transformer.

ZHIXUAN HE (Student Member, IEEE) was born in Tangshan, Hebei, China, in 1996. He graduated from the School of Electrical Engineering, Hebei University of Technology, in 2019. He is currently pursuing the master's degree with North China Electric Power University. His major is planning photovoltaic and power electronic transformers in active distribution networks.

YONGHAI XU (Member, IEEE) was born in Henan, China, in 1966. He received the B.S. degree from Tsinghua University, Beijing, China, in 1989, the M.S. degree from North China Electric Power University, Beijing, in 1992, and the Ph.D. degree from the Harbin Institute of Technology, Harbin, China, in 2002, all in electrical engineering.

He is currently a Professor with the School of Electrical and Electronic Engineering, North China Electric Power University. His research interests include power quality analysis and control, solid-state transformer, and new energy power systems.

XUEYIN ZHANG was born in Luzhou, Sichuan, China, in May 1992. He received the B.S. degree in smart grid information engineering and the Ph.D. degree in electric engineering from the School of Electrical and Electronic Engineering, North China Electric Power University (NCEPU), Beijing, China, in 2015 and 2020, respectively.

He was a Visiting Scholar with the FREEDM Systems Center, The North Carolina University, North Carolina, USA, from 2018 to 2019. He is currently working with Nanjing NR Electric Company Ltd., Nanjing, China. His research interests include multilevel converter and solid-state transformer.

YUNBO LONG was born in Yunnan, China, in 1980. He received the B.S. degree in electrical engineering, the M.S. degree in electric machine and electric appliance, and the Ph.D. degree power system and its automation from North China Electric Power University (NCEPU), Beijing, China, in 2002, 2006, and 2015, respectively.

Since 2006, he has been working with NCEPU. He is also a member of the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources. His research interests include power quality and multilevel converter.