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Discrete Modeling and Period-Adding Bifurcation of DC–DC Converter Feeding Constant Power Load

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ABSTRACT In this work, an including the switched evolution process discrete model of a DC–DC converter feeding a switched constant power load is proposed based on the Poincaré mapping rule and matrix exponent method. Numerical simulations of the bifurcation scheme based on the proposed discrete model reveal the period-adding bifurcation structures of the system as multiple devils' staircases. Further, the calculation of the stable regions of the multiple-period orbits of the nested period-adding bifurcation structures are illustrated. The experimental results verify the validity of the discrete model and analytical accuracy of the period-adding bifurcation characteristics of the system. The proposed model solves the difficulties associated with discrete modeling for power electronic nonlinear switched systems. The introduction of the switched evolution process in the proposed discrete model provides a specific mathematical model for studying the influence of the switched evolution process on the dynamics of power electronic nonlinear switched systems. This study is expected to be a foundation for the theory and further research on such power electronic nonlinear switched systems.

INDEX TERMS Chaos, constant power load, DC–DC converter, discrete model, period-adding bifurcation.

I. INTRODUCTION

Cascaded DC–DC converters have a wide range of applications in distributed power systems comprising a variety of renewable energy [1], [2]. In these systems, the rear converters can often be treated as the constant power loads (CPLs) on the front converter [3], [4]. The CPL exhibits a negative incremental impedance [5], [6], which tends to destabilize the systems, consequently inducing strong nonlinearities [7], such as bifurcation and chaos, in the entire cascaded DC–DC converter system. These nonlinear behaviors of the DC–DC converters feeding CPLs may cause unstable operation in renewable energy systems. Therefore, it is necessary to study the mechanisms of their nonlinear behaviors. Besides the analyzing and controlling of the instability for DC–DC converters feeding CPLs shown in [1]–[6], the non-linear behaviours of these systems have also attracted wide attention in recent years [7]–[10].

In [7] the stability and the low-scale bifurcation phenomena at the equilibrium point of a power factor correction converter feeding a CPL were studied by a low-frequency small-signal model. But the more complex nonlinear phenomenon in the system, such as the fast-scale instability like period-doubling bifurcation and chaos, cannot be revealed by this low-frequency small-signal model. In [8] the stability, Hopf bifurcation and catastrophic bifurcation phenomena of a Buck converter feeding a CPL in a photovoltaic-battery hybrid power system were investigated based on the small and large-signal models. In [9] the stability and the complex non-linear behaviours of a DC–DC bidirectional converter feeding a CPL in an islanding microgrid were studied by the reduced large-signal model. To simplify the nonlinear term in the study model, the CPL was equivalently linearized as a negative resistance with constant resistance at the equilibrium point both in [8] and [9]. According to the electrical characteristics of CPL, it can be known that this equivalent model is not suitable for studying the global bifurcation characteristics of the system other than the equilibrium points. Previous studies have shown that the discrete mapping model was suitable for the study of the global bifurcation analyses of power electronics systems [10]–[14]. In [12] a new discrete-time model was proposed to investigate the bifurcation behavior

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of the boost converter feeding a CPL in the transportation system. However, there are too many intermediate variables and procedures involved in the modeling method, which cause the discrete model too complex for practical. In [13] and [14] the discrete mapping model for one source boost converter (SBC) paralleled with multi-CPLs was established. The bifurcation behaviors and the coexisting fast-scale and slow-scale instabilities of the system were analyzed in these two papers. In these two works, the CPL was equivalent to the circuit composed of a constant current source parallel with a negative resistance at the steady-state, but this equivalent circuit could not reflect the real dynamics of CPL perfectly. Therefore, the discrete mapping proposed in [13] and [14] cannot precisely describe the dynamics of a DC–DC converter feeding with CPLs.

Moreover, the reported literature on switched systems has shown that the switched evolution processes may influence the dynamic characteristics of the switched systems [15], [16].

As a typical switched system, the dynamics and stability of a DC–DC converter feeding a CPL are obviously affected by the switched evolution processes. However, very few existing models on power electronic switched nonlinear systems discuss the switching evolution process; hence, the dynamic characteristics obtained from these models cannot reflect the influence of the switched evolution process on the system characteristics. To study this influence in detail, a specific mathematical model of the switched evolution process is needed in the model of the power electronic switched nonlinear system.

To overcome the problem that the equivalent model of CPL is only applicable to the equilibrium point in above-given models and the modeling difficulty of the switched evolution processes of power electronic system, a discrete model including the switched evolution process for DC–DC converters feeding switched CPLs (SCPLs) is established in this work. Here, the so-called SCPL is a CPL that may exhibit switching behaviors such as hopping, removal, or cut-in under different conditions [17], e.g., a constant power electrical brake system [18].

The remainder of this paper is organized as follows. Section 2 presents the system model and state equations of a buck converter feeding an SCPL. Section 3 proposes the new discrete model including the switched evolution process for DC–DC converters feeding an SCPL. Section 4 presents the simulation results based on the proposed discrete model and discusses the period-adding bifurcation of the system. The results of the experiments are discussed in Section 5. Finally, the conclusions are presented in Section 6.

II. MATHEMATICAL MODEL OF A BUCK CONVERTER FEEDING AN SCPL

This study considers a buck converter feeding an SCPL as an example to discuss the modeling method to include the switched evolution process in the discrete model of the power electronic switched nonlinear system. The schematic of a buck converter feeding an SCPL is shown in Fig. 1.

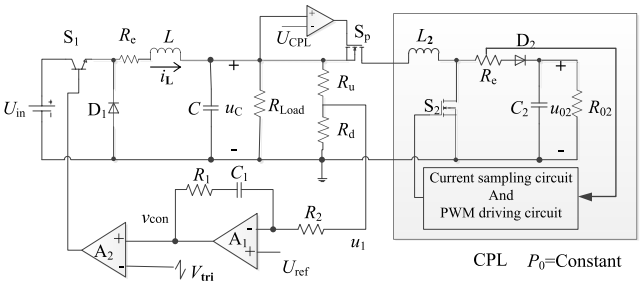


FIGURE 1. Buck converter feeding an SCPL.

The front converter in the schematic is a voltage-controlled continuous conduction mode (CCM) buck converter, and the rear cascaded SCPL is modeled using a dual-loop controlled CCM boost converter that is controlled by switch S_p. The starting reference and output voltages of the CPL are U_{CPL} and $u_{02}(t)$ respectively. The other circuit components are as follows: U_{in} is the primary voltage source, L is the inductance, C is the capacitance, R_e is the integrated equivalent impedance of the power supply and cable, R_{Load} is a resistive load, R_u and R_d are the sampling resistors, $r = R_d/(R_u + R_d)$ is the voltage sampling coefficient, $u_C(t)$ and $i_L(t)$ are the capacitor voltage and inductor current, respectively. The PI controller in the system is composed of R_1, R_f, C_f, and operational amplifier A_1, and its input and output voltages are $u_1 = ru_C$ and $v_{con}(t)$ respectively. Further, U_{ref} is the reference voltage. $v_{con}(t)$ is defined as

$$v_{con}(t) = k_P(u_1 - u_{ref}) + k_I \int_0^T (u_1 - u_{ref})dt + u_{ref} \quad (1)$$

where three control parameters of PI controller are described as $k_P = R_1/R_f$, $k_I = 1/C_fR_f$, $k_r = R_d/(R_u + R_d)$.

The sawtooth ramp voltage is described as follows:

$$V_{tri}(t_1) = V_L + (V_M - V_L)^* t/T \quad (2)$$

where T is the control period, and V_M and V_L are the peak and valley voltages of $V_{tri}(t)$ respectively.

The state variables of the system are sampled once at the beginning of each clock cycle. It is assumed that the converter will experience m ($m = 1, 2$) switching modes (SMs) in one cycle, where the switching rules are as follows. First, at the beginning of each switching period, the system operates in SM1, where switch S_1 is on and diode D_1 is off. Then, when $v_{con}(t) < V_{tri}(t)$, S_1 is turned off and D_1 is turned on, with the system operating in SM2.

The state equations of the converter are derived as follows: When $v_{con}(t) \geq V_{tri}(t)$, the system operates in SM1, and the state equations are

$$F_{S1j}(u_C, i_L, b(u_C)) : \begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(U_{in} - u_C) \\ \dfrac{du_C}{dt} = \dfrac{1}{C}(i_L - \dfrac{u_C}{R_{Load}} - b(u_C) \cdot \dfrac{P_0}{u_C}) \end{cases} \quad (3)$$

Here, $b(u_C)$ is the control function of S_p. When $b(u_C) = 0$, S_p is off, and the CPL is cut off; here, $j = 1$, so (3) can be expressed as F_{s11}. Otherwise, when $b(u_C) = 1$, S_p is on, and the CPL is operational; here, $j = 2$ and (3) can be expressed as F_{s12}.

In SM2, when $v_{con}(t) < V_{tri}(t)$, S_1 is off and D_1 is on, and the state equations are given as follows.

$$F_{S2j}(u_C, i_L, b(u_C)) : \begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(-u_C) \\ \dfrac{du_C}{dt} = \dfrac{1}{C}(i_L - \dfrac{u_C}{R_{Load}} - b(u_C) \cdot \dfrac{P_0}{u_C}) \end{cases} \tag{4}$$

Here, the meaning of $b(u_C)$ is the same as that in (3). When $b(u_C)$ is equal to 1 or 0, (4) can be expressed as F_{s21} or F_{s22} respectively.

III. MODELING THE DISCRETE MODEL WITH SWITCHED EVOLUTION PROCESS FOR BUCK CONVERTER FEEDING AN SCPL

Based on the circuit diagram of the buck converter feeding the SCPL, as shown in Fig. 1, the modeling method for the approach including the switched evolution process of the discrete model of the power electronic switched nonlinear system is described in this section. According to previous studies, the discrete model including the switched evolution process of a DC–DC converter feeding a SCPL can be established by connecting different piecewise local mappings according to the Poincaré mapping rule [19]–[21] and matrix exponent method [14]. Hence, the different piecewise local mappings are derived in detail as follows.

A. LINEAR SMOOTH PIECEWISE LOCAL MAPPING OF DC–DC CONVERTER FEEDING A RESISTOR

For smooth piecewise states when the converter feeds a resistor, the system can be modeled discretely using the existing model as follows [14]:

$$\begin{aligned} X_{k+1} &= F_{Mi1}(X_k, \Delta t_1) \\ &= e^{A_1 \Delta t_1} X_k + (e^{A_1 \Delta t_1} - I) A_1^{-1} B_{1i} U_{in} \end{aligned} \tag{5}$$

Here, X means the state variables matrix of the system and $X = [i_L u_C]^T$, Δt_1 is the working time, $e^{A_1 \Delta t_1}$ is the state transition matrix of the system that can be obtained accurately by the Cayley–Hamilton theorem [22], A_1 and B_{1i} are coefficient matrixes and expressed as follows

$$A_1 = \left[\frac{\partial F_{Si0}}{\partial X}\right] = \left[\frac{\partial F_{Si0}}{\partial i_L} \quad \frac{\partial F_{Si0}}{\partial u_C}\right] = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_{Load} C} \end{bmatrix},$$

$$B_{1i} = \left[\frac{\partial F_{Si0}}{\partial U_{in}}\right] \quad i = 1, 2,$$

$$\therefore B_{11} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \quad B_{12} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

where, the subscript i represents different SMs of the former buck converter, i.e., $i = 1$ corresponds to SM1 and $i = 2$ corresponds to SM2.

B. NONLINEAR SMOOTH PIECEWISE LOCAL MAPPING OF DC–DC CONVERTER FEEDING A CPL

Unlike the linear differential equations of a DC–DC converter feeding a resistor, the state equations of the converter feeding a CPL are nonlinear. Previous studies have shown that it is necessary to approximately linearize the nonlinear differential equation of the system in advance, such that the discrete model of the system can be established using the exponential matrix method [14], [16], [21]. Based on this, the discrete local mapping of a DC–DC converter feeding a CPL is derived as follows.

For the convenience of discussion, use $F(t, X)$ to represent the right side nonlinear functions of (3) and (4) at first. According to the Newton method [19], [20], $F(t, X)$ can be approximately linearized as follows

$$F_L(t, X) = F(t, \varphi(t_0)) + A_2(t)\,[X - \varphi(t_0)] + O(t, X) \tag{6}$$

where $X = [i_L u_C]^T$, $F_L(t, X)$ is the linearized function of $F(t, X)$, $\varphi(t_0) = [i_L(t_0)\ u_C(t_0)]^T$ is an arbitrary solution of the system at any running time t_0, $O(t, X)$ is the higher order term that can be omitted, and $A_2(t)$ is the coefficient matrix whose elements $a_{ij}(t)$ can be obtained by the following expression.

$$a_{ij}(t) = \left.\frac{\partial F(t, X)}{\partial X_i}\right|_{X=\varphi(t_0)} \quad i, j = 1, 2. \tag{7}$$

Through solving (6) exactly with the matrix exponent method [19], [20], [23] and omitting its higher-order term $O(t, X)$ at the same time, the general smooth piecewise discrete mapping of DC–DC converter feeding a CPL can be obtained as follows

$$\begin{aligned} X_{n+1} &= F_{Mi2}(X_n, \Delta t) \\ &= e^{A_2 \Delta t}(X_n - \varphi(t_0)) + (e^{A_2 \Delta t} - I) A_2^{-1} F(\Delta t, \varphi(t_0)) \end{aligned} \tag{8}$$

where $A_2(t) = [a_{ij}(t)]$ is the coefficient matrix of $A(t)$ when $X = \varphi(t_0)$ and $e^{A_2 \Delta t}$ is the state transition matrix of the system.

C. DISCRETE MODEL OF THE SWITCHED EVOLUTION PROCESS

On the basis of the modeling method of the impact oscillator [15], [19],[21], [23], the discrete mapping of the switched evolution process for a DC–DC converter feeding an SCPL was derived in detail in our previous work [17]. Thus, the discrete mapping of the

switched evolution process is used directly and rewritten as [17], [19], [20]

$$\begin{aligned} &P_{ZDM} : X_{ZDM} \\ &= F_{ZDM}(i_{Lk}, u_{Ck}) \\ &= \begin{cases} i_{LZDM} = i_{Lk} - F_2(X^*)\sqrt{2a^*}\sqrt{-\dfrac{\partial H(X)}{\partial X}\Delta i_L} = i_{Lk} \\ u_{CZDM} = u_{Ck} - F_2(X^*)\sqrt{2a^*}\sqrt{\left|-\dfrac{\partial H(X)}{\partial X}\Delta u_C\right|} \end{cases} \\ &= X_{Ck} - F_2(X^*)\sqrt{2a^*}\sqrt{\left|-\frac{\partial H(X)}{\partial X}(X_{Ck} - X^*)\right|} \end{aligned} \tag{9}$$

where $X = [i_L u_C]^T$, $\Delta X = [\Delta i_L \Delta u_C]^T$, $\Delta i_L = i_L - i_L = 0$, $\Delta u_c = (v_{con}(t^*) + (1-k_P)U_{ref})/k_P - u_C$, $v_{con}(t^*)$ is calculated as $v_{con}(t^*) = V_{tri}(t^*)$, $X^* = [(v_{con}(t^*) + (1-k_P)U_{ref})/k_P \; i_L(t_n)]$ is the switched point, and $H(X)$ is the switching function. The expression of a^* is given as

$$\begin{aligned} a^* &= (F_i^T H_{XX} + H_X F_{iX})F_i(X^*) \\ &= m_1 \cdot \frac{U_{in}}{LC} - \frac{CR_{Load}^2 + L}{LC^2R_{Load}^2}u_C^* - \frac{2b(u_C)P_0}{C^2R_{Load}u_C} \\ &\quad + m_2 \cdot \left(\frac{1}{C^2R_{Load}} + \frac{b(u_C)P_0}{C^2u_C^2}\right)i_L^* - \frac{b(u_C)P_0^2}{C^2u_C^3} \end{aligned} \tag{10}$$

where $m_1 = 1$ and $m_2 = 1$ when the system is in SM1, $m_1 = 0$ and $m_2 = 1$ when the system is in SM2, and $m_1 = 0$ and $m_2 = 0$ when the system is in SM3; $b(u_C) = 0$ if the switching S_P is stopped before mode switching and 1 otherwise.

Different mappings of the switched evolution process of the system can be obtained under different working modes according to (9) and (10).

For example, when the system state is in SM1 and the load is switched from a resistor to CPL in parallel with resistor, the mapping of the switched evolution process of the system can be obtained according to (9) and (10) as follows:

$$\begin{aligned} &X_{ZDM1} \\ &= F_{ZDM1}(X_k, \Delta t, b) \\ &= (e^{A_1\Delta t_1}X_k + (e^{A\Delta t_1} - I)A_1^{-1}B_1U_{in}) - F_{S12}(X_1^*)\sqrt{2a_1^*} \\ &\quad \cdot \sqrt{\left|-H_X(e^{A_1\Delta t_1}X_k + (e^{A\Delta t_1} - I)A_1^{-1}B_1U_{in} - X_1^*)\right|} \end{aligned} \tag{11}$$

where a^* and $H(X)$ aregiven as

$$\begin{aligned} a^* &= (F_{S11}^T H_{XX} + H_X F_{S11X})F_{S11}(X^*) \\ &= \frac{U_{in}}{LC} - \frac{CR_{Load}^2 + L}{LC^2R_{Load}^2}U_{CPL} + \frac{1}{C^2R_{Load}}i_L \end{aligned} \tag{12}$$

$$H(X) = u_C - U_{CPL} \tag{13}$$

D. BOUNDARY VOLTAGES AND WORKING MODES

A DC–DC converter system will undergo different SMs and load modes (LMs) in a switching period under different initial values. Hence, the system will have different discrete models for different initial values. To establish the discrete model of the system, the SMs and LMs of the system in a switching period must be exactly determined in advance. Previous studies [14], [17] have shown that these SMs and LMs can be exactly determined by comparing the initial values of u_C to the boundary voltages of the system. Therefore, deriving the boundary voltages is of importance for the discrete modeling of the system. The boundary voltages of the system can be derived as follows.

1) U_{BC1} IS THE SWITCHED BOUNDARY VOLTAGE OF CPL IN SM1

It is assumed that the system is in SM1 and feeding a resistor at the beginning of the switching period, with initial value $u_C(0) = U_{BC1}$. Under this condition, after one switching period, u_C increases to $u_C = U_{CPL}$, and the switch S_p is turned on for the CPL at time $t = T$. This means that the LM of the system is switched from a resistor to CPL in parallel with the resistor in one switching period for the initial value $u_C(0) = U_{BC1}$. This initial value U_{BC1} is called the switched boundary voltage of CPL in SM1. From (10) and the condition $u_C(T) = U_{CPL}$, the expression for U_{BC1} can be obtained as follows:

$$U_{BC1} = (U_{CPL} - (e^{A_1T} - I)A_1^{-1}B_1U_{in})e^{-A_1T} \tag{14}$$

2) U_{BS1} IS THE SWITCHED BOUNDARY VOLTAGE FOR MODE SWITCHING

It is supposed that the system starts from the initial value of $u_C(0) = U_{BS1}$ in SM1 at the beginning of the switching period, and under this initial condition, the output voltage of the PI controller $v_{con}(t)$ is equal to $V_{tri}(t)$ at time T, i.e., $v_{con}(T) = V_{tri}(T)$. Then, the output of A2 would move toward low voltage, which would cause S_1 to turn off and the system to switch to SM2. Here, U_{BS1} is the switched boundary voltage for mode switching. Note that U_{BS1} is larger than U_{BC1}, i.e., when switching from SM1 to SM2, the system feeds a CPL. Therefore, under the initial value condition of $u_C(0) = U_{BS1}$, the system undergoes the following two states in a switching period: the system state is SM1 and feeds a resistor; the system state is SM1 and feeds a resistor in parallel with the CPL. U_{BS1} can be obtained by the following steps. First, according to the conditions of the system described by (10), when $t < \Delta t_1$ and $u_C(\Delta t_1) = U_{CPL}$, the following expression is obtained:

$$\begin{bmatrix} U_{CPL} \\ i_{L1} \end{bmatrix} = e^{A_1\Delta t_1}\begin{bmatrix} U_{BS1} \\ i_{L0} \end{bmatrix} + (e^{A\Delta t_1} - I)A_1^{-1}B_1U_{in} \tag{15}$$

Second, according to (15) and the condition $v_{con}(T) = V_{tri}(T)$. The expression Δt_1 can be obtained as

$$\Delta t_1 = T - \frac{V_M - u_{ref} - k_P(k_rU_{CPL} - u_{ref})}{k_I(k_rU_{CPL} - u_{ref})} \tag{16}$$

where $k_r = R_d/(R_d + R_u)$.

Lastly, U_{BS1} can be obtained numerically using (15) and (16).

3) U_{BC2} IS THE SWITCHED BOUNDARY VOLTAGE OF CPL IN SM2

In this case, it is assumed that the system starts from the initial value $u_C(0) = U_{BC2}$ and undergoes the following states: working in SM1 and feeding resistor only, working in SM1 and feeding CPL in parallel with resistor, and working in SM2 and feeding CPL in parallel with resistor. In this switching period, u_C first increases and then decreases, finally settling at $u_C(T) = U_{CPL}$ at the end of the switching period. This initial value U_{BC2} is called the switched boundary voltage of CPL in SM2 and can be obtained as follows. First, under the condition $u_C(\Delta t_1) = U_{CPL}$, the state of the system working in SM1 and feeding a resistor is described by (15). Second, by inserting (2), (15), $v_{con}(\Delta t_1 + \Delta t_2) = V_{tri}(\Delta t_1 + \Delta t_2)$, and $\Delta t = \Delta t_2$ in (9), the state equation of the system working in SM1 and feeding a CPL in parallel with the resistor within Δt_2 is obtained as

$$\begin{bmatrix} u_{C2} \\ i_{L2} \end{bmatrix} = e^{A_1 \Delta t_2}\left(\begin{bmatrix} U_{CPL} \\ i_{L1} \end{bmatrix} - \varphi(t_0)\right) + (e^{A_1 \Delta t_2} - I)A_1^{-1} \times F_{S1}(\Delta t_2, \varphi(t_0), 1) \quad (17)$$

Third, inserting (2), (17), $u_C(T) = U_{CPL}$, and $\Delta t = \Delta t_3 = T\text{-}(\Delta t_1 + \Delta t_2)$ in (9), the state equation of the system working in SM2 and feeding a CPL in parallel with a resistor is obtained as

$$\begin{bmatrix} U_{CPL} \\ i_{L3} \end{bmatrix} = e^{A_2(T-\Delta t_1-\Delta t_2)}\left(\begin{bmatrix} u_{C2} \\ i_{L2} \end{bmatrix} - \varphi(t_0)\right) + (e^{A_2(T-\Delta t_1-\Delta t_2)} - I)A_1^{-1} \times F_{S2}((T - \Delta t_1 - \Delta t_2), \varphi(t_0), 1) \quad (18)$$

According to (1), (2), and condition $v_{con}(T) = V_{tri}(T)$, the expression of Δt_2 can be obtained as

$$\Delta t_2 = \frac{V_M - u_{ref} - k_P(k_r U_{CPL} - u_{ref})}{k_I(k_r U_{CPL} - u_{ref})} \quad (19)$$

Lastly, U_{BC2} can be obtained numerically using (15)-(19).

4) WORKING MODE

It can be observed from the above description that when the initial values belong to a certain boundary region, the system undergoes the same SMs and LMs during different switching periods. Therefore, the working states of the system between different boundary regions can be defined as the following working modes (WMs).

WM F_1: if $u_C(0) < U_{BC1}$, the system will undergo SM1 and feed only a resistor in a given switching period.

WM F_2: if $U_{BC1} < u_C(0) < U_{BS1}$ in a given switching period, the system remains in SM1 but undergoes two LMs, i.e., the load of the system switches from a resistor to a CPL in parallel with a resistor at the time $u_C \geq U_{CPL}$.

WM F_3: if $U_{BS1} < u_C(0) < U_{BC2}$ in a switching period, the system undergoes the following states: remaining in SM1 with the LMs switching from only a resistor to a CPL in parallel with a resistor; remaining in SM2 and feeding a CPL in parallel with a resistor.

WM F_4: if $U_{BC2} < u_C(0) < U_{BS2}$ in a switching period, the system undergoes the following states: remaining in SM1 with the LMs switching from only a resistor to a CPL in parallel with a resistor; remaining in SM2 with the LMs switching from a CPL in parallel with a resistor to only a resistor.

5) MODELING THE SWITCHED EVOLUTION PROCESS INCLUDED IN THE DISCRETE MODEL

The local smooth mappings of the system under different SMs and LMs are defined by P_i as follows:

P_1: in SM1 and feeding only a resistive load.

P_2: in SM1 and feeding a CPL in parallel with a resistive load.

P_3: in SM2 and feeding a CPL in parallel with a resistive load.

P_4: in SM2 and feeding only a resistive load.

The global Poincaré mapping P of the system can be described as follows [19]–[21]:

$$P = P_{i+1} \circ P_{ZDMi} \circ P_i \circ \cdots \circ P_{ZDM1} \circ P_1 \quad (20)$$

When the system is in different WMs, there will be different P_i and P_{ZDMi} included in (20). According to (20), the discrete model with switched evolution process of a DC–DC converter feeding a SCPL can be described as

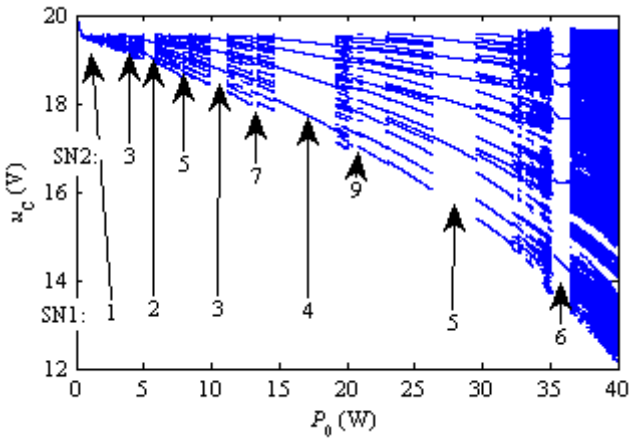
$$\begin{aligned} X_{n+1} &= X_{Mi} = G_{Mi}(X_n) \\ &= F_{i+1}(F_{ZDMi}(F_i(\cdots, F_1(\Delta t_1, b_1), \Delta t_i, b_i)), \\ &\quad \times \Delta t_{i+1}, b_{i+1}) \end{aligned} \quad (21)$$

where F_{ZDMi} are the discrete models of the switched evolution processes of the systems in (9) and (11), and F_i are the different local smooth piecewise discrete models of the systems in (5) and (8).

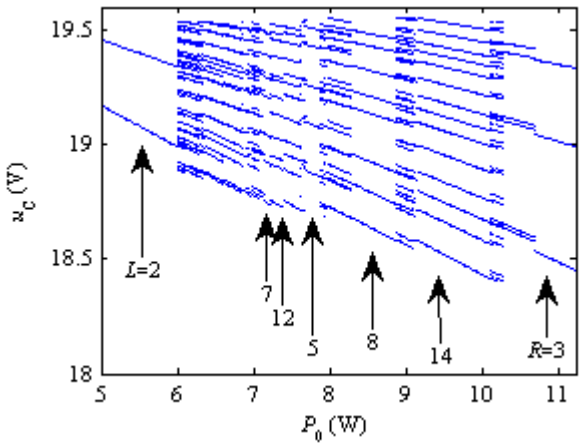
IV. PERIOD-ADDING BIFURCATION STRUCTURE

A DC–DC converter feeding a CPL is rich in nonlinear dynamics, such as low-frequency bifurcation [7], Hopf bifurcation, Catastrophic bifurcation [8], Saddle-node bifurcation, T-singularity bifurcation [9], border collision bifurcations [10], period-doubling bifurcation, coexistence of fast-scale and slow-scale instabilities state and chaos, Neimark-Sacker bifurcation [13], [14], etc. Besides, a period adding bifurcation of a buck converter feeding an SCPL were studied by numerical simulation and preliminary theoretical analysis based on the proposed model.

In the numerical simulations, P_0 is considered as the bifurcation parameter and varies in the range of $P_0 \in$ [0 W, 40 W]. The values of the remaining parameters used in the simulation are as follows: $U_{in} = 30$ V, $C = 67$ μF, $L = 1$ mH, $C_1 = 5 \times 10^{-3}\mu$F, $R_e = 0.3$ Ω, $R_u = 90$ kΩ, $R_d = 10$ kΩ, $R = 20$ Ω, $R_2 = 9$ kΩ, $U_{ref} = 0.88$ V, $U_{CPL} = 8.84$ V, and $U_M = 1$ V.



(a)



(b)

FIGURE 2. Bifurcation diagrams of u_C with P_0 as the bifurcation parameter: (a) global bifurcation diagram; (b) local enlargement of bifurcation diagram.

A. BIFURCATION STRUCTURE

Based on (21), the numerical bifurcation diagram of u_C for $P_0\epsilon$ [0 W, 40 W] is as shown in Fig. 2(*a*).

With the increasing of P_0, there are abundant bifurcation phenomena, e.g., state jumping, period-doubling bifurcation, Periodic Windows, Coexistence of periodic orbits, period adding bifurcation, weak chaos, and chaos, displayed in the bifurcation scheme. Where the state jumping is one of typical phenomenon of border collision bifurcation. The period-doubling bifurcation is a traditional bifurcation phenomenon of smooth piecewise. Both border collision bifurcation and period-doubling bifurcation may lead to weak chaos and chaos of the system. The phenomenon of coexistence of periodic orbits is caused by the fact that when two stable periodic orbits collide on the boundary, the regions two periodic orbits do not separate immediately, but overlap in a certain region, leading to the coexistence of the two stable periodic attractors in this region [24], as shown in figure 2.

In addition, there is a typical monotonically increasing periodic sequence named SN1 nested among the global bifurcation in Fig. 2(a). SN1 spans from the orbits of cycle-1 to cycle-6 in increments of $\Delta k = 1$ in the range $P_0\epsilon$ [0 W, 40 W]. Here, the sequence SN1 are conventional devils' staircases whose periodic numbers can be obtained by the well-known Farey addition rule [25]. Moreover, there are many different periodic orbits nested between any two periodic orbits of SN1, and that the periodic numbers of these periodic orbits are obtained by adding such two periodic orbits of SN1 via a certain period-adding rule. This bifurcation is called period-adding bifurcation (PAB) [26], which is a typical bifurcation phenomenon of the switched system [27]. The reason for this bifurcation phenomenon is that the unstable periodic orbits collide on the boundary and result in the topology changing and the merging cascade of the periodic orbits [28]. As shown in Fig.2, there is another set of monotonically increasing periodic sequence named SN2. It can be seen from Fig.2, SN2 is nested in the interval of cycle-1 to cycle-5 of SN1 and which spans from the cycle-3 to cycle-9 orbits in increments of $\Delta k = 2$. Every periodic orbit of SN2 is nested in two adjacent periodic orbits of SN1 and whose periodic number is equal to the sum of such two periodic orbits of SN1. The PBA sequence SN2 is a conventional devil's staircase and also obey the well-known Farey addition rule.

However, the other multiperiodic orbits nested in SN1 are multiple devils' staircases; their periodic numbers cannot be obtained from the Farey addition rule directly [29] but can be obtained by following rule [22], [29], [30]:

$$K_{PABSi} = nL + mR \tag{22}$$

Here, k_{PABSi} are the periodic numbers of the nested multiperiodic orbits, L and R denote the left and right orbits of any two adjacent periodic orbits of SN1 respectively, and n and m are natural numbers.

According to (22), the periodic numbers of SN2 can be obtained as $K_{\mathrm{PABS2}} = L + R$, for $n = m = 1$. This means that sequence SN2 and the nested multiperiodic orbits are obtained via the period-adding rule; therefore, sequences SN1 and SN2 as well as the nested multiperiodic orbits comprise the PABS.

It can be seen from Fig. 2(a) that as P_0 increases, the system states tend to diverge, and the PABS orbits nested within SN1 gradually become more complex. After period 5 of SN1, the multiperiodic orbits of SN2 are no longer present in the bifurcation structure, and intermittent chaotic orbits are observed among the nested orbits. Moreover, after the cycle 6 orbit, there is a short period-doubling bifurcation that sharply transitions to chaos, and the PABS orbits are no longer present in this chaos region.

Fig. 2(b) displays the PABS between the cycle - 2 and 3 orbits of SN1 in detail. As shown in Fig. 2(b), there are several multiperiodic orbits such as cycle - 5, 7, 8, 14, etc. It can be known from the analysis above that these multiperiodic orbits are all PABS orbits brought about by the adding

of the cycle 2 and 3 orbits, and their periodic numbers can be obtained by (22). Thus, the periodic number of cycle - 5 is $L+R=2+3=5$ and its function can be described as $f_L \cdot f_R$; the periodic number of cycle - 7 is $L+(L+R)=2+5=7$ and its function can be described as $f_L \cdot (f_L \cdot f_R)$; the periodic number of cycle - 8 is $(L+R)+R=5+3=8$ and its function can be described as $(f_L \cdot f_R) \cdot f_R$; the periodic number of cycle - 14 is $L+L+(L+R)+(L+R)=2+2+5+5=14$ and its function can be described as $f_L \cdot f_L \cdot (f_L f_R) \cdot (f_L \cdot f_R)$.

The PABS described above is a special phenomenon of the switched discontinuous system [22], [24]–[29] that is caused by the boundary collision of the discontinuous system. Because of the presence of two different types of switched boundaries, the SM and LM were switches, and a DC–DC converter feeding a SCPL displays a more complex PABS than a normal discontinuous system.

Lastly, many orbits interlacing phenomena also can be observed among the PABS orbits, in these conditions two adjacent periodic orbits of the PABS will coexist in a longer interval. The positions of the periodic points are shifted when the system parameters change, resulting in interlacing of the various adjacent periodic orbits of the PABS.

In short, Fig.2 (a) and (b) indicate the influence of SCPL on the nonlinear dynamics of a DC–DC converter feeding with an SCPL by bifurcation scheme. As shown in Fig. 2(a) and (b), with the varying of SCPL's power, the system exhibits complex dynamics, such as the period-adding bifurcation, period-doubling bifurcation, orbits interlacing, chaos, etc.

B. CALCULATION OF STABILITY REGION

In this section, the PABS cycle-5 orbit nested within the cycle-2 and cycle-3 orbits of SN1 are considered as an example to illustrate the calculation of the stable regions of different periodic orbits of the PABS.

It is observed from the analysis of the bifurcation scheme that the PABS cycle-5 orbit comprises the cycle-2 and cycle-3 orbits of SN1, and the periodic number of this PABS orbit can be obtained from (22) as $k=2+3$. Moreover, the mapping of this PABS cycle 5 orbit comprises the mappings of the cycle 2 and 3 orbits as follows. According to the working principle of the system, there are two mappings of the cycle 2 orbits:

$$P_{C2} = P_2 \circ P_1 \tag{23}$$

Or

$$P_{C2} = P_1 \circ P_2 \tag{24}$$

According to (21), P_{C2} is described as follows:

$$\begin{aligned} X_2 &= F_{\mathrm{L}}(X_n) \\ &= F_{M12}(F_{ZDM1}(F_{M11}(X_n, \Delta t_1), 0, 1), \Delta t_2) \end{aligned} \tag{25}$$

Or

$$\begin{aligned} X_2 &= F_{\mathrm{L}}(X_n) \\ &= F_{M11}(F_{ZDM1}(F_{M12}(X_n, \Delta t_1), 0, 1), \Delta t_2) \end{aligned} \tag{26}$$

There are also two mappings of the cycle 3 orbits:

$$P_{C3} = P_3 \circ P_2 \circ P_1 \tag{27}$$

Or

$$P_{C3} = P_4 \circ P_3 \circ P_2 \tag{28}$$

According to (21), P_{C3} can be described as

$$\begin{aligned} X_5 &= F_R(X_n) \\ &= F_{M21}(F_{ZDM2}(F_{M12}(F_{ZDM1}(F_{M11}(X_n, \Delta t_1), \\ &\quad \times \Delta t_1, 0), \Delta t_2), \Delta t_2, 1), \Delta t_3) \end{aligned} \tag{29}$$

$$\begin{aligned} X_3 &= F_R(X_n) \\ &= F_{M22}(F_{ZDM3}(F_{M21}(F_{ZDM2}(F_{M11}(X_n, \Delta t_1), \\ &\quad \times \Delta t_1, 1), \Delta t_2), \Delta t_2, 1), \Delta t_3) \end{aligned} \tag{30}$$

The mappings of the cycle 5 orbits are obtained as

$$P_{C5} = P_{C2} \circ P_{C3} \tag{31}$$

Or

$$P_{C5} = P_{C3} \circ P_{C2} \tag{32}$$

If there exists a stable region for a periodic orbit, then there exists a fixed point where the following expressions are workable

$$X_S = F_R(F_L(X_S)) \tag{33}$$

Or

$$X_S = F_L(F_R(X_S)) \tag{34}$$

and

$$\begin{cases} f_L(X_S) < X^* \\ f_R(X_S) > X^* \end{cases} \tag{35}$$

Using (27) – (35), the stable region of the cycle-5 orbit comprising the cycle-2 and cycle-3 orbits according to the period-adding theory is numerically obtained as $P_0 \in [7.7, 7.9]$ W. This stable region is in good agreement with that shown in Fig. 2. Similarly, the stable regions of the orbits of cycle - 2, 3, 4, 5 and 6 of SN1 can be obtained as [4.9 W, 6.0 W], [10.6 W, 11.3 W], [14.6 W, 18.9 W], [26.3 W, 29.3 W] and [35.3 W, 36.3 W] respectively according to the above numerical method. These stable regions are in good agreement with those shown in Fig. 2. The stable regions of other cycle-*nLmR* orbits also can be obtained by using the above numerical method.

C. COMPARISON WITH OTHER WORKS

In this section, a comparison is made between the presented work and previous ones.

Compared with the large and small signal models used in papers [7]–[9], the discrete model proposed in the presented work was more suitable for the global bifurcation analysis of DC–DC converters feeding CPLs not just the bifurcation analysis of equilibrium points.

Compared with the complex discrete model proposed in paper [12], the discrete model proposed in this paper has a clearer physical meaning that can better predict the dynamic characteristics of the system in different parameter intervals.

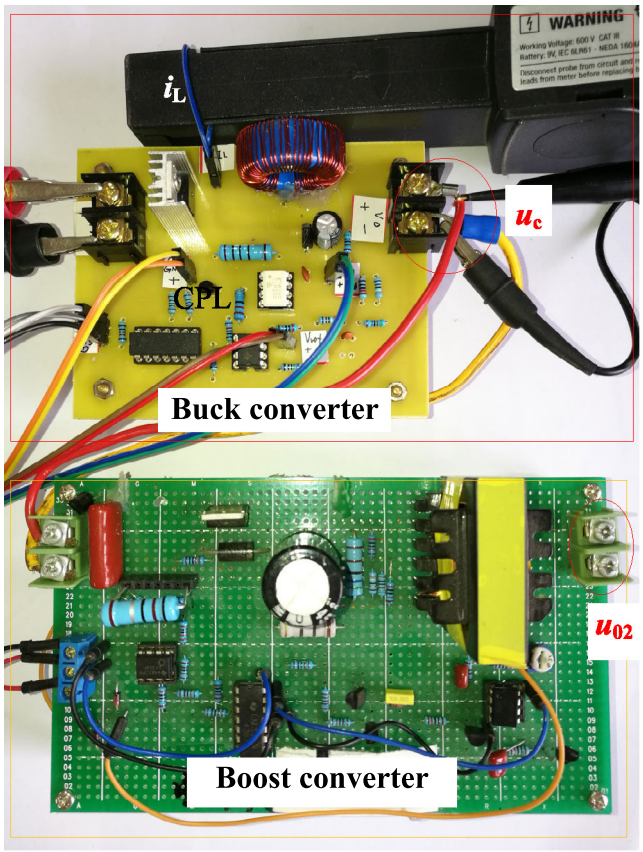


FIGURE 3. Experimental setup.

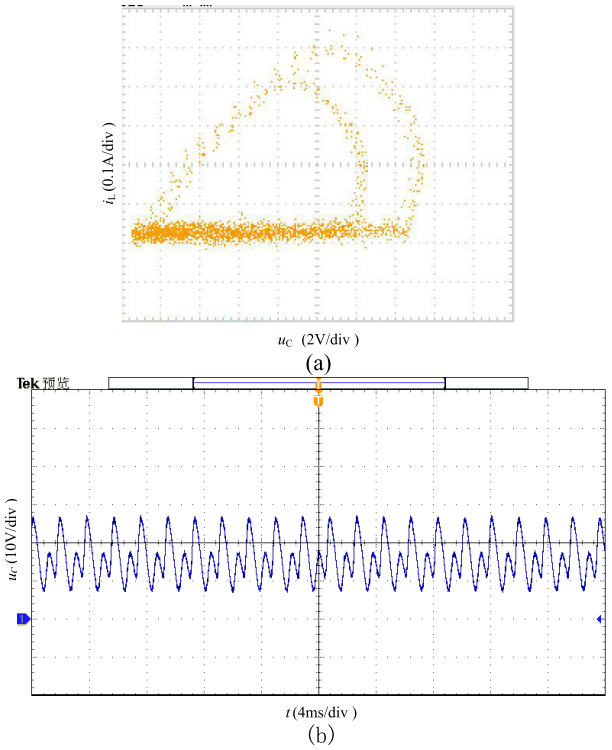


FIGURE 4. Experimental results of cycle-2 at $P_0 = 5.8$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

Compared with the equivalent model of CPL proposed in papers [13] and [14], the discrete model of this paper obtained through approximately linearizing the nonlinear differential state equation at an arbitrary solution can reflect the dynamic characteristics of CPL in a broader scope including the steady and unsteady states.

In addition, the switching evolution process included in the model of this paper was not included in the models of papers [7]–[9], [12]–[14]. Therefore, based on the model of this paper, more abundant nonlinear behaviors of DC–DC converters feeding CPLs can be simulated, such as monotone increasing period sequence and period adding bifurcation as shown in Fig. 2.

Above all, for the nonlinearity analyzes of DC–DC converters feeding CPLs, the discrete model of this paper not only has a broader range but also can reflect more abundant bifurcation phenomenon than the previous models.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed discrete model and validate PABS analysis, an experimental setup of a buck converter feeding an SCPL was constructed in the laboratory, shown in Fig. 3 [17].

The main DC–DC converter of the experimental setup is a PI scheme voltage-mode-controlled Buck converter and the SCPL is a dual-loop controlled Boost converter. Where the major components of circuit design are as follows: IRF840 and TLP250 are used as switching device and gate drive circuit for S_1, MUR20100 is used as diode D_1, two LM311 are used as amplifiers A_1 and A_2 respectively, IRFP460 and TL949 are used as switching device and gate drive circuit for S_2, APT30D60B is used as diode D_2. The other related parameters of the experimental circuit are presented as follows: $U_{\text{in}} = 30$ V, $C = 67$ μF, $L = 1$ mH, $C_1 = 5 \times 10.3$ μF, $R_{\text{e}} = 0.3$ Ω, $R_{\text{u}} = 90$ kΩ, $R_{\text{d}} = 10$ kΩ, $R_{\text{Load}} = 20$ Ω, $R_2 = 9$ kΩ, $U_{\text{ref}} = 0.88$ V, $U_{\text{CPL}} = 8.84$V, and $U_{\text{M}} = 1$ V, $L_2 = 1$ mH, $C_2 = 600$ μF, $R_{\text{O2}} = 50$ Ω, $f_{\text{B}} = 5$ kHz, $D_{\text{B}} = [0.45, 0.66]$, $U_{\text{ref2}} = 2.5$ V, $R_{\text{u2}} = 150$ kΩ, $R_{\text{d2}} = 10$ kΩ, $K = 0.2$, $R_3 = 15$ kΩ, $R_{\text{W2}} = 10$ kΩ.

The phase portraits of $i_L(t)$-$u_C(t)$ and the time waveform of $u_C(t)$ under several P_0 values were measured with the experimental platform, as shown in Figs. 4 to 9.

As shown in Fig.2, the cycle-2 and cycle-3 orbits are two periodic orbits of the sequence SN1 and appear in two different regions of $P_0\epsilon$ [4.9 W, 6 W] and $P_0\epsilon$ [10.6 W, 11.3 W] respectively. To verify the existence of these two orbits, experiment was carried out in these two regions and the results were shown in Figs. 4 and 5.

Fig. 4 (a) and (b) show the cycle-2 phase portrait of $i_L(t) - u_C(t)$ and the time waveform of $u_C(t)$ respectively at $P_0 = 5.5$ W, which is in good agreement with that of the system in the region $P_0\epsilon$ [4.9 W, 6 W] shown in the numerical simulation of the bifurcation scheme based on the proposed discrete model.

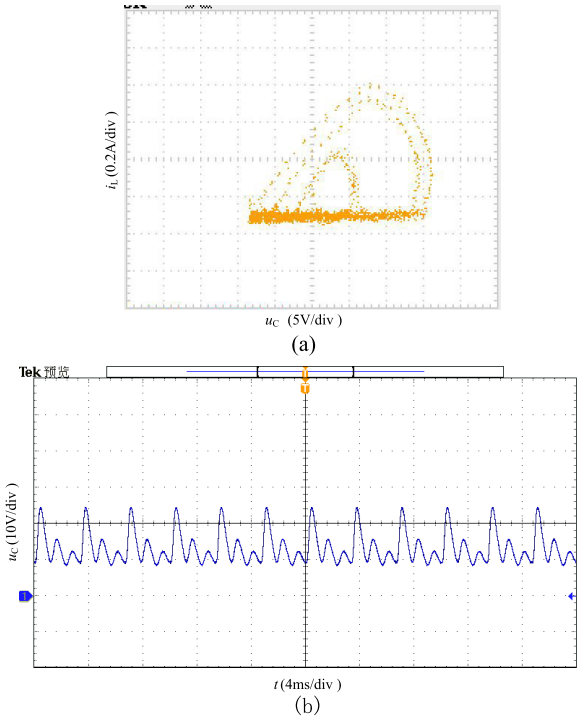


FIGURE 5. Experimental results of cycle-3 at $P_0 = 10.6$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

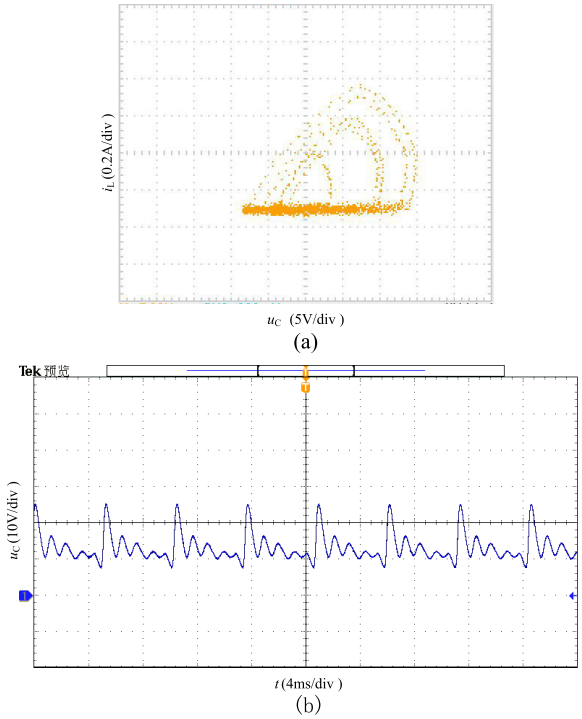


FIGURE 6. Experimental results of cycle-5 at $P_0 = 7.8$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

Fig. 5 (a) and (b) show the cycle-3 phase portrait of $i_L(t) - u_C(t)$ and the time waveform of $u_C(t)$ respectively at $P_0 = 10.6$ W, which is in good agreement with that of the system in the region $P_0 \epsilon$ [10.6 W, 11.3 W] shown in the

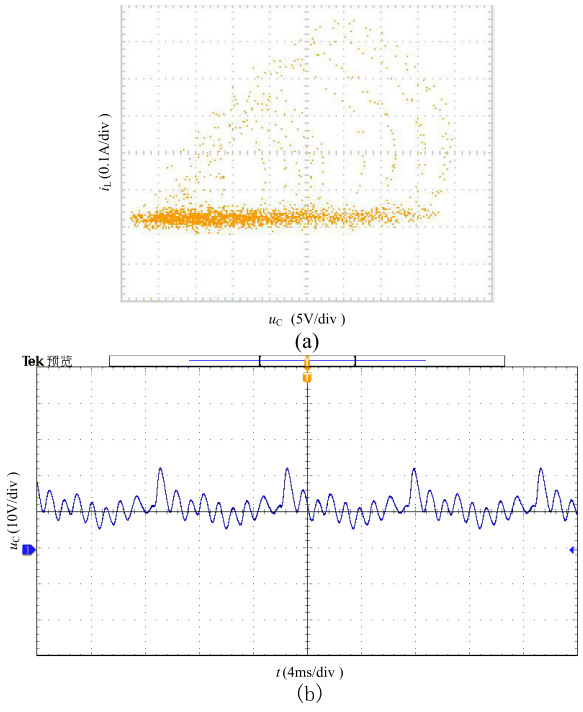


FIGURE 7. Experimental results of cycle-9 at $P_0 = 20.6$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

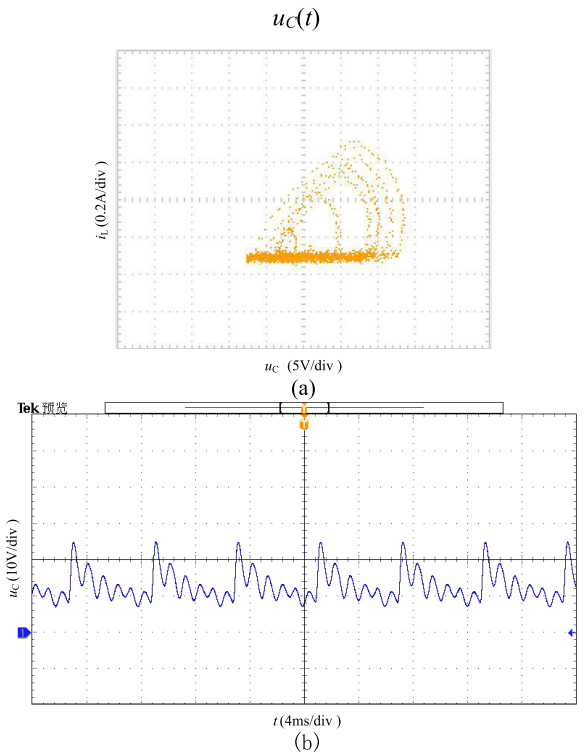


FIGURE 8. Experimental results of cycle-6 at $P_0 = 36$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

numerical simulation of the bifurcation scheme based on the proposed discrete model.

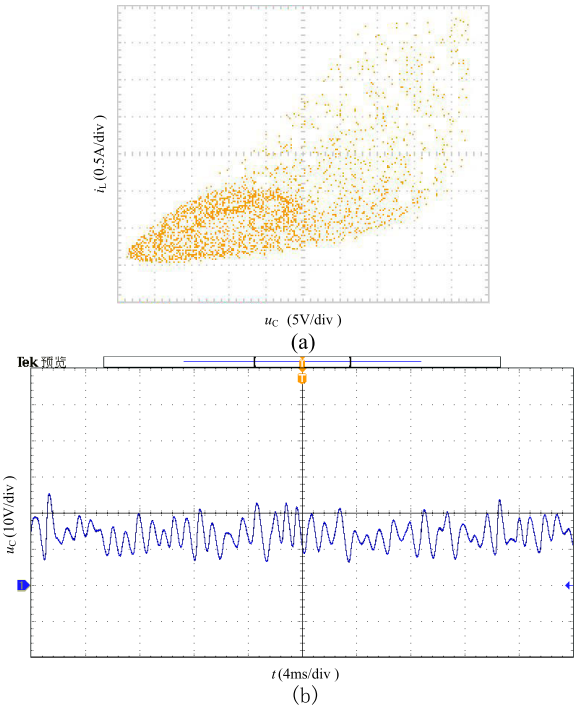


FIGURE 9. Experimental results of chaos at $P_0 = 38$ W (a) the phase portraits of $i_L(t) - u_C(t)$ (b) the time waveform of $u_C(t)$.

Therefore, the experimental results shown in Figs. 4 and 5 verify the existence of the cycle-2 and cycle-3 orbits of the sequence SN1.

According to the analysis of section 4, there is a PAB cycle-5 orbit produced by the period adding rule $k = 2 + 3$ nested between the cycle-2 and cycle-3 orbits in region of $P_0 \in$ [7.7 W, 7.9 W]. The experiment was carried out to verify the existence of this orbit and the results were shown in Fig.6.

Fig. 6 (a) and (b) show the cycle-5 phase portrait of $i_L(t)$-$u_C(t)$ and the time waveform of $u_C(t)$ respectively at $P_0 = 7.8$ W, which is in good agreement with that of the system in the region $P_0 \in$ [7.7 W, 7.9 W] shown in the numerical simulation of the bifurcation scheme based on the proposed discrete model.

Thus, the experiment results of Fig.6 verify the existence of this PAB cycle-5 orbit.

In addition, three other orbits shown in the bifurcation scheme are also verified by experiments as follows.

One is the PAB cycle-9 orbit existing in the region $P_0 \in$ [20.3 W, 20.9 W], which is produced by the adding of cycle-4 and cycle-5 orbits of SN1 according to the rule of $K = L + R$.

Fig. 7 (a) and (b) show the cycle-9 phase portrait of $i_L(t)$-$u_C(t)$ and the time waveform of $u_C(t)$ at $P_0 = 20.6$ W, which is in good agreement with that of the system in the region $P_0 \in$ [20.3 W, 20.9 W] shown in the numerical simulation of the bifurcation scheme based on the proposed discrete model.

Thus, the experiment results of Fig.7 verify the existence of this PAB cycle-9 orbit.

Another is the cycle-6 orbit existing in the region of $P_0 \in$ [35.3 W, 36.3 W], which is one of the periodic orbits of SN1. Fig. 8 (a) and (b) show the cycle-6 phase portrait of $i_L(t) - u_C(t)$ and the time waveform of $u_C(t)$ at $P_0 = 36$ W, which is in good agreement with that of the system in the region $P_0 \in$ [35.3 W, 36.3 W] shown in the numerical simulation of the bifurcation scheme based on the proposed discrete model.

Therefore, the experiment results of Fig.8 verify the existence of this cycle-6 orbit of SN1.

The last one is the chaotic orbit in the region of $P_0 \in$ [36.5 W, 40 W]. Fig. 9 (a) and (b) show the chaotic phase portrait of $i_L(t) - u_C(t)$ and the time waveform of $u_C(t)$ at $P_0 = 38$ W, which is in good agreement with that of the system at

$P_0 = 38$ W shown in the numerical simulation of the bifurcation scheme based on the proposed discrete model.

That is to say the experiment results of Fig.9 verify the existence of chaotic orbit.

It can be known that from the above analysis of the experimental results of Figs. 4, 5 and 8 verify the existence of the sequence SN1, the experimental results of Figs. 6 and 7 verify the existence of PBA orbits, all the experimental results verify the correctness of the bifurcation scheme. Therefore, it can be concluded that the validity of the proposed model and the correctness of the analysis of PAB in this work are confirmed by the experimental results.

VI. CONCLUSION

In this paper, a novel discrete model including the switched evolution process of a DC–DC converter feeding a switched constant power load (SCPL) is proposed. The period-adding bifurcation structure (PABS) of the power electronic nonlinear switched system is studied via numerical simulations based on the proposed discrete model. The PAB behavior of the system is demonstrated to be dependent on the border collision bifurcations, whereby the areas in the parameter spaces leading to specific PABS cycles are obtained numerically. The experimental results verify the effectiveness of the proposed discrete model and validate the PABS analysis. This work has two innovative contributions: (1) Approximately linearizing the nonlinear differential state equation of the system on an arbitrary solution which provides a novel way for discrete modeling of nonlinear power electronics cascade system. (2) Deducing the mathematical model of the switching evolution process provides a reference for describing the switching evolution process of the power electronics system. In this sense, the proposed model overcomes the problem of the previous equivalent model of CPL is only applicable to the steady-state and the modeling difficulty of the switched evolution processes of power electronic system.

In the future, the influence of the switched evolution process on the dynamics of power electronic switched nonlinear cascade systems will be analyzed qualitatively and quantitatively in detail based on the discrete model with the switched evolution process proposed in this paper.

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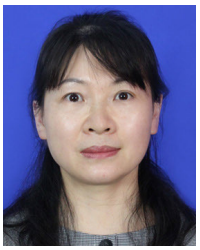

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