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300 mA LDO Using 0.94 μA I_Q With an Additional Feedback Path for Buffer Turn-off Under Light-Load Conditions

INHO JEON, TIAN GUO, AND JEONGJIN ROH, (Senior Member, IEEE)
Department of Electrical Engineering, Hanyang University, Ansan 15588, South Korea

Corresponding author: Jeongjin Roh (jroh@hanyang.ac.kr)

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ABSTRACT This paper proposes a 300 mA low-dropout (LDO) regulator using an I_Q of only 0.94 μA, which has the advantage of minimizing power consumption in the standby mode of a battery-based system. The LDO uses a source follower buffer with dynamic biasing to maintain loop stability and load transient response performance. Under light-load conditions, the buffer enters a fully-off state because there is a sub-nA bias current. Therefore, the LDO uses a dual output operational transconductance amplifier (DO-OTA) for operation under light-load conditions. The second output of the DO-OTA for light-load operation in the LDO forms an additional feedback path instead of the fully-off buffer. The second output of the DO-OTA is designed to consume a current lower than the bias current of the buffer while operating. Furthermore, the buffer in the LDO is designed for operation above 5 mA I_L. While the buffer is operating, the dynamic biasing current of the buffer is used as the second output of the DO-OTA. The second output of the DO-OTA has lower output impedance characteristics than its main output, so the LDO can secure loop stability under light-load conditions by lowering the DC gain. As a result, the LDO exhibits load transient response performance up to 300 mA by using a minimal I_Q under the no-load condition. The LDO is based on a 180 nm bipolar-CMOS-DMOS (BCDMOS) process and covers an area of approximately 256 $\times$ 143μm^2. The measured I_Q is 0.94 μA under the no-load condition with a maximum load current of 300 mA.

INDEX TERMS LDO regulator, DO-OTA, adaptive biasing, dynamic biasing, source follower, low-I_Q, power management integrated circuit (PMIC).

I. INTRODUCTION

Several electronic products, such as battery-powered laptops, tablets, smartphones, and smartwatches, include blocks for various functions, such as application processor (AP), display drivers, camera modules, sensors, and memory. High-efficiency DC-DC converters are mainly used for blocks with significant power consumption, such as AP, display devices, and memory. Besides, LDOs are used for blocks that consume relatively little power, such as sensors, ADCs, and are sensitive to noise. As such, efficient power management is possible by using power management integrated chips (PMICs) that are suitable for each block. Thus, it is possible to improve performance by increasing device usage time and mitigating heat generation.

Recently, LDOs have been classified into two categories: capacitor-less and capacitor-based. Capacitor-less LDOs have the ability to supply low power without using an off-chip capacitor and are likely to have lower output voltage noise characteristics compared to capacitor-based LDOs due to structural limitations. Further, research suggests that they show higher power supply rejection (PSR) under low I_Q conditions and can achieve excellent load transient characteristics [1]–[3]. An LDO with a digital conduction feedback structure is even in development [4]–[6].

Capacitor-based LDOs still have considerably low-noise characteristics by employing large external capacitors and can provide larger loads than capacitor-less LDOs.

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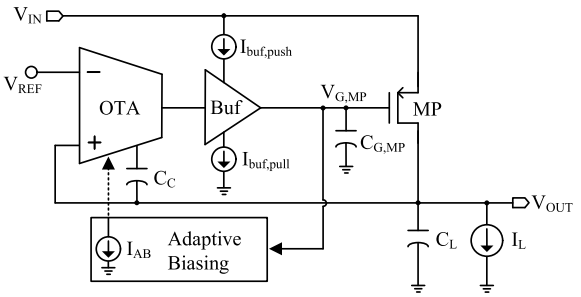

FIGURE 1. Conventional LDO regulator with adaptive biasing block.

By employing a separate fast-feedback loop, the loop bandwidth under heavy-load conditions can be improved to achieve increased bandwidth under the loading current of the LDO [7]–[9]. To increase the lifetime of battery systems, an adaptive bias current generator has been used to limit the use of I_Q under light-load conditions [10], [11].

Capacitor-based LDOs have difficulty maintaining stable performance due to two low frequency poles. As shown in Fig. 1, a conventional LDO has a buffer to ensure stability by splitting one low frequency pole into two high frequency poles via a source follower buffer. Also, an adaptive biasing block has been used in LDOs for larger bias current in the operational transconductance amplifier (OTA) to increase bandwidth under heavy-load conditions [12], [13]. In addition, loop stability can be guaranteed by generating a zero through the feed-forward capacitor C_C. A general design for raising the transient response of the output voltage while utilizing a source follower buffer has been proposed [14]–[16].

In this paper, a capacitor-based LDO is proposed. Using a large power transistor that can withstand a heavy-load current may limit the improvements offered to loop stability of an LDO under light-load conditions. Under light-load conditions, a feedback path is constructed through the second output of a dual output operational transconductance amplifier (DO-OTA) instead of the main output with the buffer stage. The second output of the DO-OTA has lower output impedance characteristics than its main output, so the proposed LDO can provide loop stability under light-load conditions by lowering the DC gain. The buffer in the LDO is designed for operation above 5 mA I_L; while the buffer is operating, the dynamic biasing current of the buffer is used as the second output of the DO-OTA. As a result, the LDO exhibits an load transient response performance up to 300 mA by using a minimal I_Q under the no-load condition.

The LDO design guarantees an output of up to 300 mA with a 0.94 μA I_Q under the no-load condition while achieving faster transient performance than previous implementations. Section II outlines the application of the proposed LDO and compares it with the conventional source follower buffer. This section also discusses how the corresponding transient response could be improved. Further, Section III presents the circuit diagram of the proposed LDO and analyzes the stability. Section IV compares the proposed LDO to other known LDOs. Finally, Section V concludes the paper.

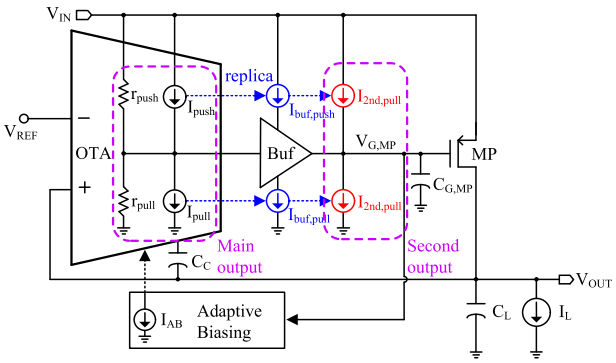

FIGURE 2. Proposed LDO regulator.

II. DESIGN OF THE PROPOSED LDO

The structure of the proposed LDO is shown in Fig. 2. The LDO is designed to minimize the I_Q of the buffer by applying a DO-OTA in the structure of a conventional LDO. It also receives adaptive biasing I_{AB} to the OTA. Through this, the LDO can improve the transient response characteristics with only low I_Q under light-load conditions. I_{push} and I_{pull} represent the main outputs of the DO-OTA, and r_{push} and r_{pull} represent the corresponding output resistances. I_{AB}, I_{push}, and I_{pull} show dynamic characteristics according to the load current in addition to the response from the output voltage according to the input signal of the OTA. By mirroring I_{push} and I_{pull}, the buffer bias current is applied dynamically as $I_{buf,push}$ and $I_{buf,pull}$. As a result, the performance of the transient response at the buffer stage is improved.

The proposed LDO uses a DO-OTA, which serves to minimize the I_Q. The width of the buffer receiving adaptive biasing should remain above a certain level as the load current increases, requiring a sufficient bias current for buffer operation. However, as the bias current increases, it generates unnecessary I_Q under light-load conditions. To solve this problem, the second output of the DO-OTA is placed in parallel with the buffer to prevent unnecessary bias current consumption of the buffer under light-load conditions and to minimize I_Q across the loop control through the second output of the DO-OTA. The LDO is composed of the second output through $I_{2nd,push}$ and $I_{2nd,pull}$. Low-I_Q operation of the LDO is possible only when the amount of current used by the second output of the DO-OTA is lower than the bias current required for the buffer to be in the saturation region. This is compared to the current consumption through the designed DO-OTA and the buffer check magnitude for the full schematic shown in Fig. 5.

The proposed LDO is designed to have a power transistor and buffer with sufficiently large widths to supply a load of 300 mA. Due to the structural constraints inherent to a conventional LDO, it is difficult to guarantee adequate phase margins under light-load conditions. Section III describes how the phase margin characteristics are guaranteed under the light-load conditions in the LDO.

The copied current of the power transistor, MP_S in the adaptive biasing block, is utilized mainly to adjust the loop

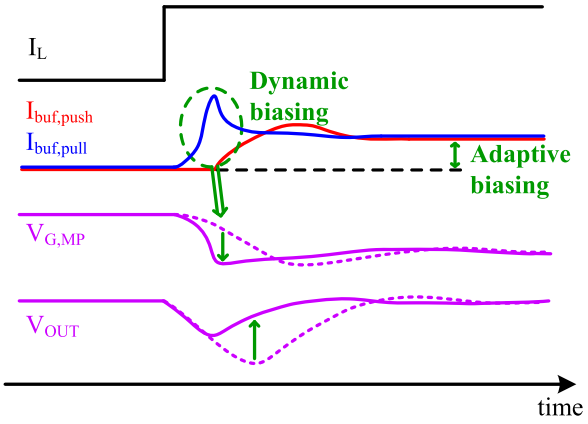

FIGURE 3. Transient improvement of the dynamic biasing buffer.

stability as well as improve the transient response through changes in the output resistance of the buffer according to the load current. I_{AB} generated by MP_S is supplied to the tail current of the OTA. This is reflected in the output component of OTA such that the current component of MP_S can be used in the source follower buffer. MP_S has a copy ratio of approximately 1/4000 of MP and is not influential due to a sub-threshold current generation of 25 nA based on a light load of approximately 100 μA; however, 300 mA is used as the dynamic bias current source for the OTA with a current generation of approximately 75 μA.

Changes in $I_{buf,push}$ and $I_{buf,pull}$ according to the load transient can improve the gate voltage response speed of the MP. The simulation results that could improve the undershoot voltage and transient response performance of the output voltage are shown in Fig. 3. Dynamic biasing increases as I_{AB} in Fig. 2 increases with an increase in I_L. $I_{buf,pull}$ current increases faster than $I_{buf,push}$ due to the OTA's gain characteristics. This is designed to improve the response speed of the output voltage of the LDO by increasing the slewing of $C_{G,MP}$, as described in (1) and (2):

$$\Delta V_{G,MP} = \frac{I_{buf,push} - I_{buf,pull}}{C_{G,MP}} \tag{1}$$

$$|\Delta V_{OUT}| \propto |\Delta V_{G,MP}|. \tag{2}$$

The feedback loop of the proposed LDO is shown in Fig. 4. $v_d (= V_{OUT} - V_{REF})$ is the small-signal differential input of the OTA. M1 and M16 transfer G_m current to the DO-OTA outputs. The main output of the DO-OTA used in the LDO is designed to have a cascode class-AB output structure in M2, M3, M11, and M17. M2 and M17 are designed as I_{push} and I_{pull} in Fig. 2. We implemented $I_{buf,push}$ and $I_{buf,pull}$ as current sources of the source follower buffer through M18 and M19, which copy M2 and M17, respectively. They also form the second output of the DO-OTA in parallel with the buffer through M19 and M20.

In Fig. 4(a), the increase in V_{OUT} under light-load conditions lowers the $V_{G,M2}$ of the OTA output terminal due to the increase in feedback signal v_d. At this time, the decrease in $V_{G,M2}$ increases the main output of the DO-OTA. Subsequently, because the effect of the common source stage of M8 is augmented, there is a decrease in $V_{G,M2}$ as $V_{D,M18}$ decreases. As shown in Fig. 4(c), M18 enters the triode region at 5 mA or less. Below 5 mA, V_{GS} and V_{DS} of M18 decrease together, and I_{M18} decreases at sub-nA levels. The width of M8 is designed to be 60 μm to supply a 300 mA load current. M18 entering the triode region causes M8 to fall into the sub-threshold region. As the load current increases, I_{M18} increases steadily. As shown in Fig. 4(b), the design enables weak inversion of M8 from a load current above 5 mA [18]. From the point when the source follower buffer M8 begins its operation, the feedback loop is controlled by the relatively low output impedance of M8.

In conclusion, the operating state of M8 is determined by the 5 mA load current. Thus, a feedback loop is established to control the second output of the DO-OTA and M8 of the source follower buffer according to the load current.

TABLE 1. Simulated I_Q of the schematics under the no-load condition.

Component	Current (nA)
I_{M9}, I_{M10}	160
I_{M14}, I_{M15}	40
I_{M13}, I_{M16}	40
I_{M12}, I_{M17}	40
I_{M19}	240
I_{REF} for V_{B1}, V_{B2}	120
Total current	920

III. LDO IMPLEMENTATION

The proposed LDO regulator is shown in Fig. 5(a). The main OTA of the designed circuit, which has two G_m stages, is taken from [22]. Transistors M4 and M7 in the main G_m stage receive a differential voltage input and convert it into a current. At this time, the current is converted into voltage by the diode-connected transistors M14 and M15. The converted voltage is received by transistors M9 and M10. M9 and M10 finally generate the G_m boosting terminal. The sum of the current generated in the main G_m terminal and G_m boosting terminal is converted into voltage by M13 and M16. This voltage is copied to M12 (M2) and M17 and transferred to the class-AB output terminal. The OTA can minimize the current consumption through the MP's current mirror (MN_2) when the load current is small. The G_m of the OTA increases as the load current increases, thereby improving the transient response of the LDO.

Table 1 lists the results of I_Q simulation under the no-load condition shown in Fig. 5(a). M10 and M16 boost the OTA transconductance at a 4:1 ratio. M2 and M17 are copied from the current mirrors of M1 and M16 respectively. They are the main output of the DO-OTA and are connected to the gate of the M8 buffer. M19 and M20 are the second output of the DO-OTA and are connected to the gate of the MP. M18 is the bias current of M8 and copies the M1 current. M1, M16, M18, M19, and M20 are configured under the

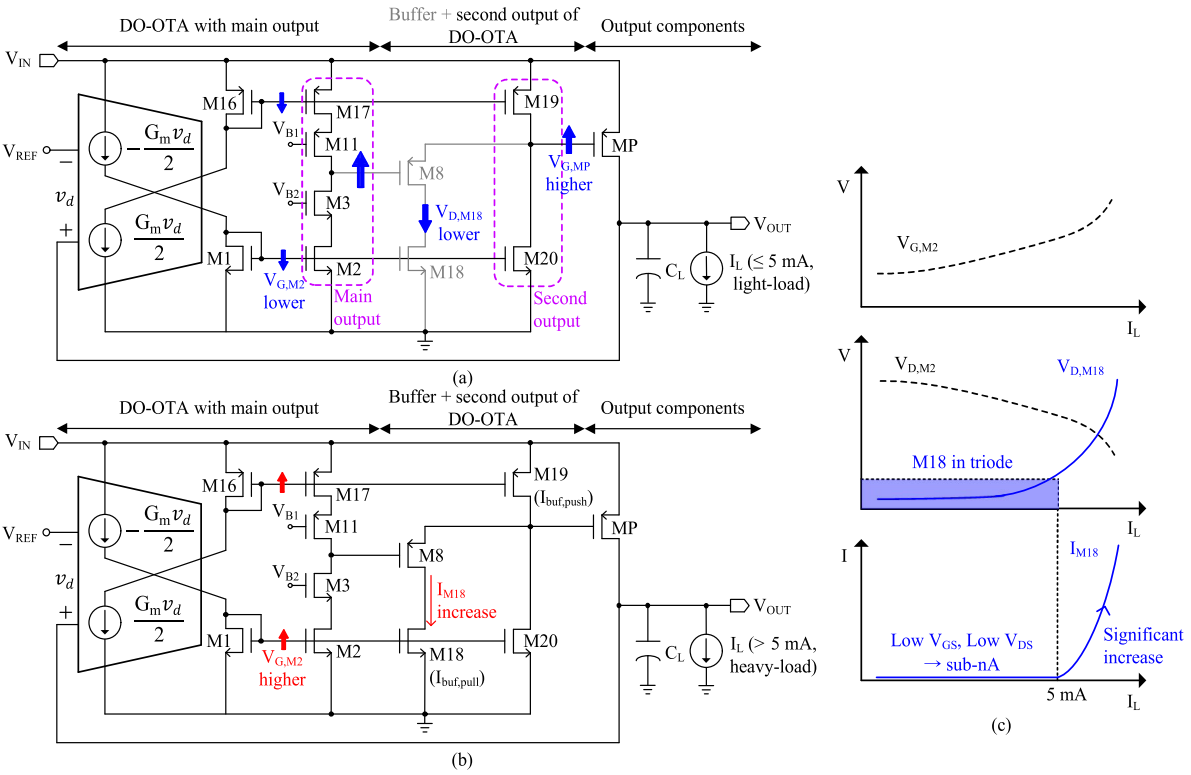

FIGURE 4. Feedback loop of the proposed LDO regulator (a) under light-load conditions and (b) at over 5 mA load. (c) V_G, V_D, and I_{M18} versus I_L.

copy ratio M1:M18+M20 = M16:M19 = 1:6. Under the no-load condition, the current in MP_S occurs at sub-nA levels. Therefore, the current of MP_S can be omitted from the total I_Q. The total I_Q under the no-load condition of the proposed LDO is calculated as $I_{B1} + I_{M12} + I_{M17} + I_{M19} = 0.92\,\mu$A.

The width of M8 is determined with consideration of dynamic biasing under max-load conditions. If a sufficiently large width is not secured, the value of $V_{GS,M8}$ is very large under the maximum loading current. Thus, the maximum loading current range of the LDO can be limited outside the output swing range of the OTA. Therefore, the size of M8 is designed to be 60 μm in which so that the swing range of the OTA is not limited. Furthermore, to drive a transistor of that size, a bias current of at least 1 μA is required, which is low-I_Q and can burden the design. The second output of the DO-OTA consumes 0.16 μA under the no-load condition. This consumes significantly less total quiescent current than an LDO that uses a bias current in the buffer.

The proposed LDO is designed to have two modes depending on load current changes. As mentioned in Section II, when the load current is low, $V_{D,M18}$ decreases and M18 moves to the deep triode region. M8 is almost turned off due to its large width but small current of M18. The buffer does not work in this case, so M19 and M20 work as the second output of the DO-OTA. The second output of the DO-OTA drives the MP and forms a feedback loop of the LDO. The output impedance driving $V_{G,MP}$ is $r_{o19} \parallel r_{o20}$.

When the load current increases over 5 mA, $V_{D,M18}$ increases, and M18 enters the weak inversion region and then the saturation region. The output impedance driving the $V_{G,MP}$ is in parallel with the second output of the DO-OTA and source follower output impedance. In general, $1/g_{m8} \ll r_{o19} \parallel r_{o20}$. The source follower M8 drives $V_{G,MP}$, and the main output of the DO-OTA and M8 form a feedback loop of the LDO.

Fig. 5(b) shows the buffer stage of a conventional LDO, where M21 has six transistors in parallel. In comparison to the proposed LDO, M21 of this buffer stage is the combination of M18 (four transistors in parallel) and M20 (two transistors in parallel). Upon applying this change, the second output of the DO-OTA is removed in the proposed LDO. The LDO applied according to Fig. 5(b) works the same as a conventional LDO with adaptive biasing block. The stability of the LDO in Fig. 5(b) was compared with that of the proposed LDO.

In conclusion, open-loop stability is improved by using a large source follower buffer suitable for the maximum load current. Under light-load conditions, the buffer is not used, thus minimizing I_Q and securing open-loop stability.

A. STABILITY ANALYSIS

Fig. 6 shows the feedback loop of the proposed LDO regulator according to the load current. This is a simplified small-signal block diagram based on Fig. 4 to find the transfer function. Here, G_m and g_{mp} represent the transconductance of the OTA and MP, respectively. R_{O1} and R_{O2} represent the output

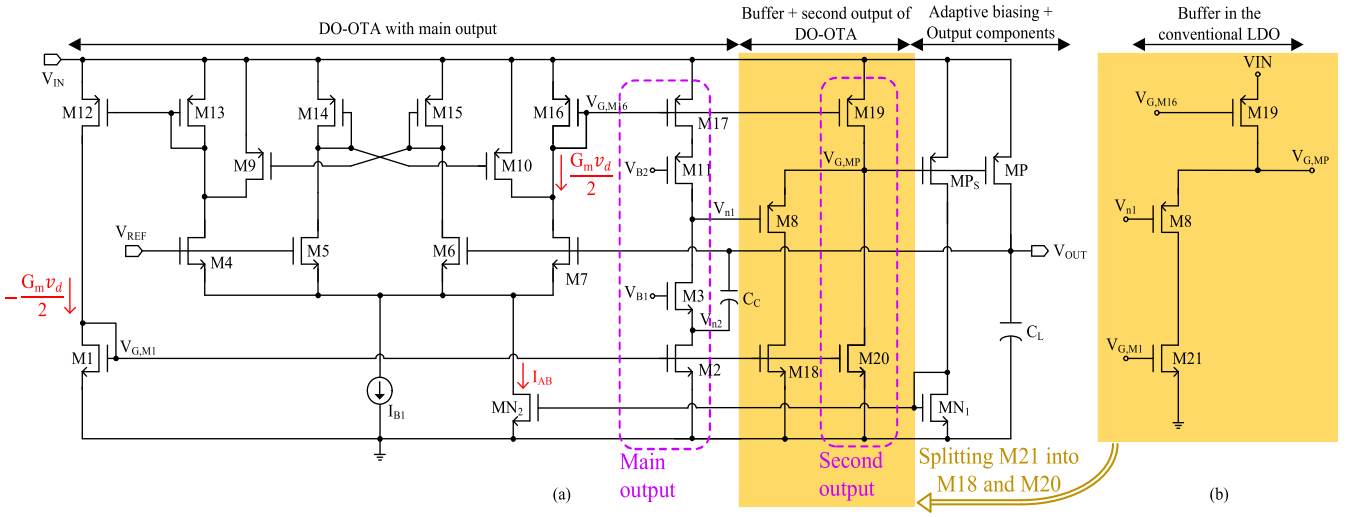

FIGURE 5. Schematics of the (a) proposed LDO regulator and (b) buffer stage in a conventional LDO.

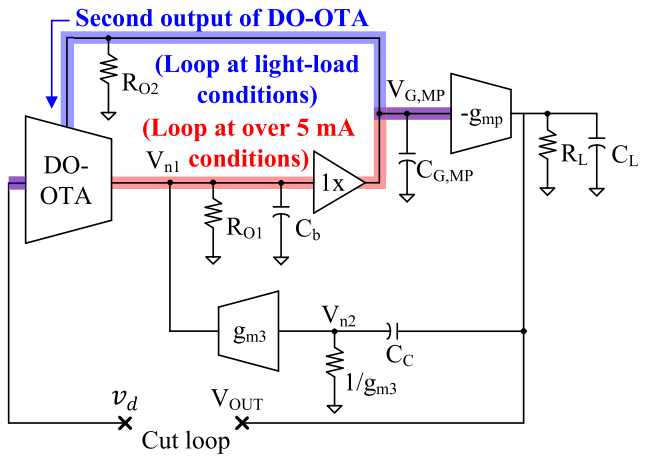

FIGURE 6. Small-signal block diagram of the proposed LDO regulator.

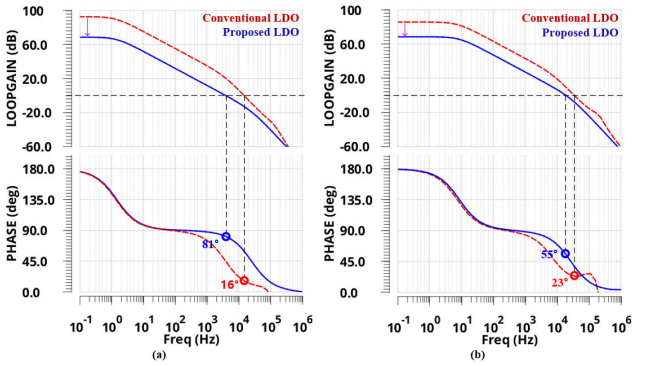

FIGURE 7. Simulation results of the loop gain/phase of the conventional/proposed LDO regulator with a load current of (a) 10 μA and (b) 100 μA.

impedance of the main and second outputs of the DO-OTA, respectively. In addition, it is composed of g_{m3}, which is the transconductance of the current buffer stage of M3, and MP, which is a pass device.

Fig. 7 shows the open-loop characteristics of the conventional LDO and proposed LDO under the load conditions of 10 and 100 μA. The conventional LDO compared in Fig. 7 is the same as that in Fig. 5(b). For C_C, 10.5 pF is used for both LDOs. The conventional LDO is designed to secure a swing range of V_{n1} by increasing the widths of the MP and M8 to accommodate 300 mA loading. Therefore, the two non-dominant poles occurring at the V_{n1} and $V_{G,MP}$ nodes move at low-frequency. As a result, the phase margins become 16° and 23°, respectively, making it difficult to ensure LDO stability. Phase margin compensation is possible by increasing C_C, but the transient response performance may deteriorate due to an excessive phase margin under heavy-load conditions. The proposed LDO is looped through the second output of the DO-OTA path under light-load conditions. Therefore, the dominant pole of the output stage and non-dominant pole by $V_{G,MP}$ occur. At this time, the phase margin is compensated by lowering the DC gain of the second output of the DO-OTA [23]. In addition, the number of non-dominant poles is reduced compared to in a conventional LDO, and the proposed LDO can guarantee loop stability under light-load conditions with phase margins of 81° and 55°, respectively.

Under light-load conditions, the buffer enters the cutoff state due to a low bias current. At this time, the output impedance of the second output of the DO-OTA is relatively low, driving the MP instead of the buffer. Based on this, the transfer function under light-load conditions is as follows:

$$T(s)|_{I_L\simeq 0} = \frac{-G_m g_{mp} R_{O2} R_L}{(1+sC_L R_L)\left(1+sC_{G,MP}R_{O2}\right)} = \frac{1}{\left(1+\frac{s}{p_{-3dB}\,|\,I_L\simeq 0}\right)\left(\frac{s}{p_{nd}\,|\,I_L\simeq 0}\right)}, \quad (3)$$

where there are two poles, $p_{-3dB\,|\,I_L\simeq 0} = 1/(C_L R_L)$ and $p_{nd\,|\,I_L\simeq 0} = 1/(C_{G,MP}R_{O2})$. R_{O2} is designed to be lower than that of the main output of the DO-OTA, so $p_{nd|IL\simeq 0}$ is located

at a high frequency and under light-load conditions. The high resistance value of R_{O1} is due to the very low frequency pole that occurs and can be stabilized using a one-pole system.

As the load current increases, the buffer enters a saturation region due to an increase in adaptive biasing, and the MP is driven through the buffer, resulting in a change in the main feedback loop. Equations (4)-(6) represent Kirchoff's current law in each branch as follows:

$$G_m V_{IN} + g_{m3} V_{n2} = \frac{V_{n1}}{R_{O1} \parallel \frac{1}{sC_b}} \tag{4}$$

$$g_{mp} V_{n1} = \frac{V_{OUT}}{R_L \parallel \frac{1}{sC_L}} + \frac{V_{OUT} - V_{n2}}{\frac{1}{sC_C}} \tag{5}$$

$$\frac{V_{OUT} - V_{n2}}{\frac{1}{sC_C}} = g_{m3} V_{n2}. \tag{6}$$

Through (4)-(6), V_{n1} and V_{n2} can be summarized as follows:

$$V_{n1} = -\frac{\frac{1}{R_L \parallel \frac{1}{sC_L}} + \frac{g_{m3} sC_C}{g_{m3} + sC_C}}{g_{mp}} V_{OUT} \tag{7}$$

$$V_{n2} = \frac{sC_C}{g_{m3} + sC_C} V_{OUT}. \tag{8}$$

Here, (7) and (8) are applied to (4) and the transfer function of the LDO occurs as represented by (9) under heavy-load conditions. Thus the two poles $p_{-3dB\,|\,I_L \gg 0} = 1/(g_{mp} C_C R_{O1} R_L)$ and $p_{nd\,|\,I_L \gg 0} = (g_{mp} C_C)/(C_b C_L)$ appear.

$$\begin{aligned} T(s)|_{I_L \gg 0} &\approx \frac{-G_m g_{mp} R_{O1} R_L \left(1 + s\frac{C_C}{g_{m3}}\right)}{1 + s g_{mp} C_C R_{O1} R_L + s^2 C_b C_L R_{O1} R_L + s^3 \frac{C_b C_C C_L R_{O1} R_L}{g_{m3}}} \\ &\approx \frac{-G_m g_{mp} R_{O1} R_L (1 + s\frac{C_C}{g_{m3}})}{\left(1 + s\frac{1}{g_{mp} C_C R_{O1} R_L}\right)\left(1 + s\frac{C_b C_L}{g_{mp} C_C}\right)\left(1 + s\frac{C_C}{g_{m3}}\right)} \\ &= \frac{-G_m g_{mp} R_{O1} R_L}{\left(1 + s g_{mp} C_C R_{O1} R_L\right)\left(1 + s\frac{C_b C_L}{g_{mp} C_C}\right)} \\ &= \frac{-G_m g_{mp} R_{O1} R_L}{\left(1 + \frac{s}{p_{-3dB\,|\,I_L \gg 0}}\right)\left(\frac{s}{p_{nd\,|\,I_L \gg 0}}\right)}. \end{aligned} \tag{9}$$

Fig. 8(a) shows the open-loop characteristics according to load current under a 1.8 V input, 1.6 V output, and 1μF output capacitor. Under light-load conditions of 100 μA and 1 mA, it is possible to confirm loops through the second output of the DO-OTA, which appear in the form of a one-pole system. Under the load conditions of 10 and 300 mA, the feedback loop changes from the second output of the DO-OTA to the path of the main OTA and the buffer. Through C_C across the main output of the DO-OTA, it can be seen that phase compensation is achieved at zero in the high-frequency region.

The change of phase margin according to increased load current via different process corners and temperatures [24] can be seen in Fig. 8(b). It can be inferred that the feedback loop changes in the corresponding section due to the change

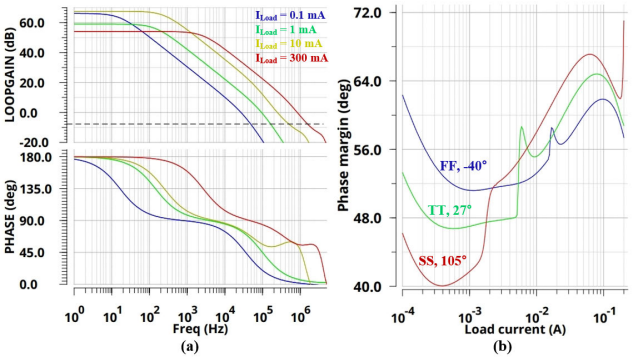

FIGURE 8. (a) Simulation results of the loop gain/phase of the proposed LDO regulator with a load current of 100 μA, 1 mA, 10 mA, and 300 mA. (b) Phase margin as the load current increases versus the process corner/temperature.

TABLE 2. Worst phase margins under different load conditions according to process corner/temperature.

Temperature	FF	SF	FS	SS
-40 °C	51.8°	48.4°	47.5°	43.7°
27 °C	49.6°	47.5°	44.9°	41.6°
105 °C	48.2°	50.3°	41.8°	40.8°

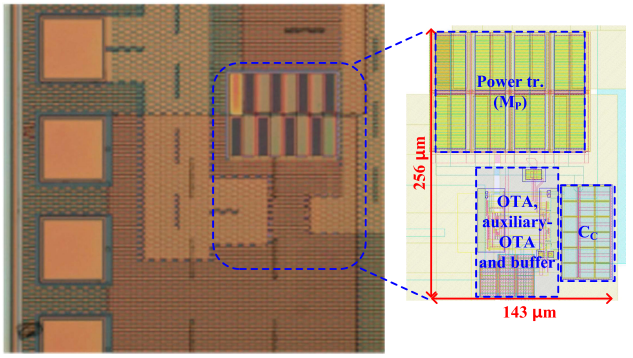

FIGURE 9. Chip micrograph and layout.

in the state of the buffer around 5 mA based on the TT corner at 27 °C. In addition, it can be confirmed that the operation change of the buffer according to the load current guarantees AC stability. Also, Table 2 shows the worst phase margins under different load conditions according to process corner/temperature. When considering the worst conditions of the SS corner at 105 °C, it is confirmed that a phase margin of 40° is guaranteed.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The chip micrograph of the designed LDO regulator is shown in Fig. 9. It is designed with a 180 nm BCDMOS process, and the actual area, excluding pads, is approximately 0.037 mm^2. The LDO has an output range of approximately 1.2-1.6 V and can supply up to approximately 300 mA of current. 1 μF is used for the output capacitor.

Fig. 10 shows the measurement results for I_Q under the no-load condition using five chip samples. Along with the measurement of I_Q, we measured ΔV_{OUT} under the conditions of

TABLE 3. Recent LDO performance comparison.

	[26]	[7]	[25]	[13]	[20]	[21]	[10]	This Work
Year	2012	2015	2017	2017	2018	2020	2020	2020
Technology (μm)	0.35	0.18	0.13	0.18	0.25	0.18	0.055	0.18
Chip Area (mm^2)	0.044	0.024	0.1825	0.0285	0.108	0.1245	0.042	0.037
Input Voltage V_{in} (V)	3.3	1.2	1.05-2.0	1.4	1.5-3.3	2	0.8	1.4-1.8
Output Voltage V_o (V)	3.0	1.0	1	1.2	1.0-3.0	1.8	0.6	1.2-1.6
Dropout Voltage (mV)	300	200	29.7	200	240	200	200	200
Max Load Current (mA)	200	100	300	50	150	600	10	300
I_Q (μA)	147-314	135.1	14-120	1.6-200	1.24-100	30-700	0.016-	0.94-255
Max Current Efficiency (%)	99.8	99.86	99.96	99.6	99.93	99.88	99.99	99.92
Load Regulation (mV/mA)	0.45	0.075	0.006	0.1	-	0.0083	1.05	0.1
Line Regulation (mV/V)	34	22.7	0.44	5.5	-	0.23	0.5	5.33
Output Capacitor C_o (μF)	0.3	1	1	1	1-47	1	1	1
Undershoot voltage (mV)	100	25	56	24	135	15.6	70	96
Overshoot voltage (mV)	110	7.5	24	5	65	15.4	0	37
$\Delta I_{O,max}$ (mA)	110	100	300	50	150	600	10	300
FOM (ps)*	765	439	12.44	18.5	7.4	2.58	11.4	1.39

* $FOM = C_{LOAD} * \Delta V_{OUT} * I_Q / I^2_{Load,max}$

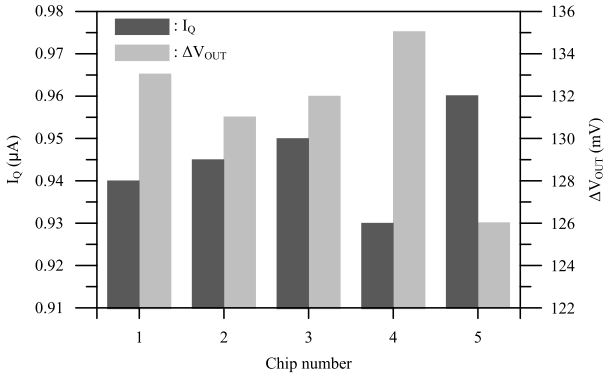

FIGURE 10. Measured no-load I_Q of 5 chips with corresponding peak-to-peak output voltage ΔV_{OUT}.

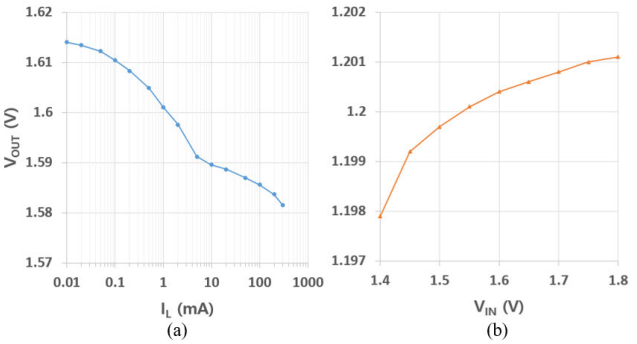

FIGURE 11. Measured (a) load and (b) line regulation of the proposed LDO regulator.

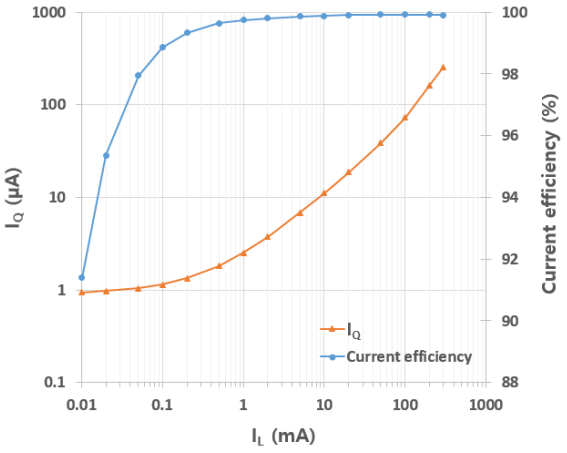

FIGURE 12. Measured quiescent current and current efficiency of the proposed LDO regulator.

$V_{IN} = 1.8$ V and $V_{OUT} = 1.6$ V. ΔV_{OUT} recorded the peak-to-peak output voltage according to the response in the load transient state of 0.1 μA to 300 mA. In Table 3, its value is based on the measurement result of sample 1, which has an intermediate value.

Fig. 11(a) shows the measured load regulation of the proposed LDO regulator under the conditions of $V_{IN} = 1.8$ V and $V_{OUT} = 1.6$ V. Below a 5 mA load current, the change of the feedback loop is shown in the load regulation. It is confirmed that the load regulation is weak when minimizing the consumption of I_Q of the LDO under light-load conditions, but the load regulation in the total load current range is 0.1 mV/mA, showing good characteristics.

Fig. 11(b) shows the measured line regulation of the proposed regulator when the input voltage changes from 1.4 to 1.8 V under the conditions of $V_{OUT} = 1.2$ V and $I_{LOAD} = 300$ mA. A 3.2-mV variation in the output voltage was observed. Thus, the line regulation is 5.33 mV/V.

Fig. 12 shows the measured quiescent current and current efficiency of the proposed regulator. The total quiescent current varied from 0.94 and 255 μA as the load current changed. Thus, the maximum current efficiency is 99.92 % at $I_L = 300$ mA.

The transient response result for the input/output voltage change is shown in Fig. 13. It was measured under an I_Q

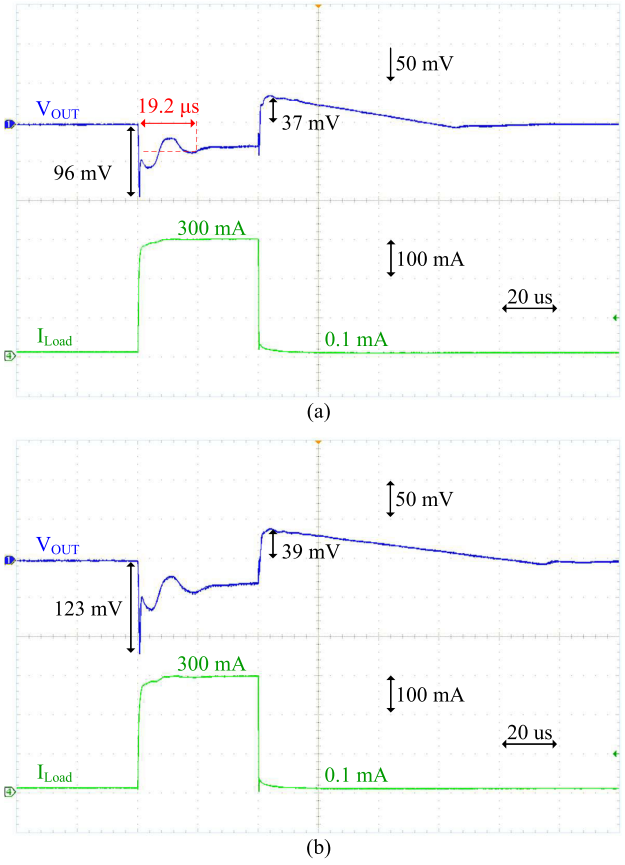

FIGURE 13. Measured output transient response under (a) $V_{IN} = 1.8$ V, $V_{OUT} = 1.6$ V and (b) $V_{IN} = 1.5$ V, $V_{OUT} = 1.2$ V.

of 0.94 μA and it was confirmed that it is possible to measure upto 300 mA loading of a 100 ns slope. This occurs upto approximately 96 mV under the conditions of $V_{IN} = 1.8$ V and $V_{OUT} = 1.6$ V. This V_{OUT} can recover to a tolerable error limit of $\pm 1\,\%$ within 19.2 μs during I_L transitions of 0.1 to 300 mA. In the other case, it is like a slewing that is not included in the transient response [19], [20].

Table 3 shows a performance comparison of LDOs using several recent capacitors. The proposed LDO is capable of regulating 300 mA in an off-chip capacitor LDO with only sub-1 μA standby current under the no-load condition. In addition, $FOM(= C_{LOAD} * \Delta V_{OUT} * I_Q/I^2_{Load,max})$ is 1.39 ps. This is substantially better than previously reported results. The proposed LDO operates with the sub-μA I_Q, which is much lower than existing LDOs that can load more than 100mA [21]. It is clear that our proposed design supplies larger loading current than existing LDOs and exhibits excellent characteristics, even with regulation.

V. CONCLUSION

In this paper, an LDO with a low I_Q using the second output of a DO-OTA was described. To implement this, adaptive biasing was used for the OTA, and dynamic biasing was used for the source follower. Techniques such as arranging a buffer and second output of the DO-OTA in a parallel structure were applied. Through this approach, we proposed a design that minimizes the standby current of the LDO by eliminating unnecessary biasing consumption of the buffer under light-load conditions. The proposed LDO can drive a load of up to 300 mA with a no-loading standby current of only approximately 0.94 μA under a dropout voltage of 200 mV, and the AC stability within the loading range was verified to power the battery. Our design could contribute to minimizing the leakage current in the standby state of the system and can play the role of a regulator that covers a loading of 300 mA or more.

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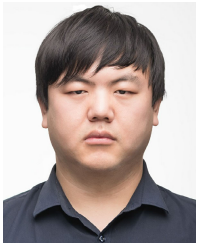
INHO JEON received the B.S. and M.S. degrees in electrical and electronic engineering from Hanyang University, Ansan, South Korea, in 2012 and 2014, respectively, where he is currently pursuing the Ph.D. degree. His current research interests include power management integrated circuits and mixed-signal integrated circuits.



TIAN GUO received the B.S. degree from the Tianjin University of Technology, in 2014, and the M.S. degree in electrical and electronic engineering from Hanyang University, Ansan, South Korea, in 2017, where he is currently pursuing the Ph.D. degree. His current research interests include power management integrated circuits and mixed-signal integrated circuits.

JEONGJIN ROH (Senior Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from The Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from The University of Texas at Austin, in 2001. From 1990 to 1996, he was with the Samsung Electronics, Giheung, South Korea, as a Senior Circuit Designer for mixed-signal products. From 2000 to 2001, he was with the Intel Corporation, Austin, TX, USA, as a Senior Analog Designer for delta-sigma data converters. In 2001, he joined the Faculty of the Hanyang University, Ansan, South Korea. His research interests include power management integrated circuits and oversampled delta-sigma converters.