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Polycrystalline-Silicon-MOSFET-Based Capacitorless DRAM With Grain Boundaries and Its Performances

SANG HO LEE[1], WON DOUK JANG[2], (Student Member, IEEE), YOUNG JUN YOON[3], JAE HWA SEO[2], HYE JIN MUN[1], MIN SU CHO[1], JAEWON JANG[1], (Member, IEEE), JIN-HYUK BAE[1], AND IN MAN KANG[1], (Member, IEEE)

[1]School of Electronic and Electrical Engineering, Kyungpook National University, Daegu 702-201, South Korea
[2]Samsung Electronics Company Ltd., Hwasung-si 445-701, South Korea
[3]Korea Multi-Purpose Accelerator Complex, Korea Atomic Energy Research Institute, Gyeongju 38180, South Korea

Corresponding author: In Man Kang (imkang@ee.knu.ac.kr)

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ABSTRACT In this work, a capacitorless one-transistor dynamic random access memory (1T-DRAM) based on a polycrystalline silicon (poly-Si) metal–oxide–semiconductor field-effect transistor was designed and analyzed through a technology computer-aided design (TCAD) simulation. A poly-Si thin film was utilized within the device because of several advantages, including its low fabrication cost and the feasibility of its use in high-density three-dimensional (3D) memory arrays. An asymmetric dual-gate structure is proposed to perform the write "1" operation and achieve high retention characteristics. The proposed 1T-DRAM cell demonstrates a high sensing margin of 8.73 μA/μm and a high retention time of 704.4 ms compared to previously reported 1T-DRAMs, even at a high temperature. In addition, the effect of grain boundaries on the memory performance of the proposed device was investigated, and the results validated the excellent reliability of its retention characteristics even in the presence of grain boundaries (>64 ms at $T = 358$ K).

INDEX TERMS Polycrystalline silicon, one-transistor dynamic random access memory, grain boundaries, metal–oxide–semiconductor field-effect transistor, one transistor dynamic random access memory, dual-gate.

I. INTRODUCTION

Capacitorless one-transistor dynamic random access memory (1T-DRAM) has attracted a great deal of attention as a substitute for conventional one-transistor one-capacitor (1T-1C) DRAM. Given the difficulty of capacitor fabrication, the researchers have proposed the 1T-DRAM, which eliminate the need for capacitor altogether as a substitute for the conventional DRAM. The 1T-DRAM does not use an external capacitor, and instead relies on the principle of floating body effect. 1T-DRAMs have the advantage of simple fabrication and excellent compatibility with logic devices [1]–[11]. However, the smaller dimensions of these devices tend to limit their retention characteristics because of the stronger electric field between the body and the source/drain junctions. The stronger electric field increases the recombination/generation rate of excess holes and the down-scaled 1T-DRAMs have the short retention time [12]. Therefore, 3D memory arrays can be a solution to increase the retention time of 1T-DRAMs. 1T-DRAMs based on polycrystalline silicon (poly-Si) have attracted attention due to the feasibility of obtaining high-density 3D memory arrays. Poly-Si-based transistors have previously been employed in 3D memory technology because of their significant advantages related to integrated fabrication technology [13]–[15].

In this work, a poly-Si metal–oxide–semiconductor field-effect transistor (MOSFET) based 1T-DRAM cell with an asymmetric dual-gate structure, to realize superior

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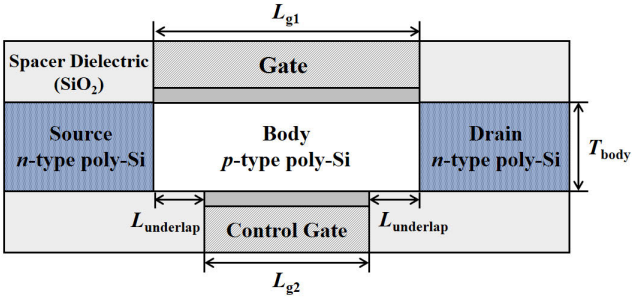

FIGURE 1. Schematic view of the proposed poly-Si MOSFET-based 1T-DRAM cell with asymmetric dual-gate structure.

memory performance, was investigated through a technology computer-aided design (TCAD) simulation. The memory performance characteristics of the proposed 1T-DRAM cell, namely, its sensing margin and retention time, were obtained and analyzed based on parameters calibrated against the experimental data in [13] to ensure high accuracy. Moreover, the effect of grain boundaries (GBs) within the poly-Si layers on the reliability of the device was investigated.

II. DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 1 shows a schematic view of the poly-Si- MOSFET-based 1T-DRAM cell with an asymmetric dual-gate structure to realize high memory performance. The main gate is used to perform both the conventional MOSFET operation and the program operation, while the control gate is employed to perform the program, erase, and hold operations. Furthermore, an underlap structure is proposed to reduce the electric field in the depletion region between the body and the source/drain region, resulting in an increase in the retention time. The work-functions of the main gate (WF_{MG}) and the control gate (WF_{CG}) are 4.85 and 5.3 eV, respectively. Poly-Si can be used as a material of the main gate. Additionally, Ni and Ir can be used as materials of the control gate [16], [17]. Due to the high work-function of the control gate, the energy band diagram near the control gate is raised, thus creating a sufficient potential well for hole storage in the body.

The main gate length (L_{g1}) is 70 nm, the control gate length (L_{g2}) is 50 nm and the gate dielectric (HfO_2) thicknesses (T_{ox}) are 3 nm each. The doping concentrations of the source, body, and drain regions are 1×10^{20} cm^{-3} (n-type), 1×10^{18} cm^{-3} (p-type), and 1×10^{20} cm^{-3} (n-type), respectively. The device parameters for the proposed devices are summarized in Table 1. The geometric parameters of the cell, including its underlap length ($L_{underlap}$) and body thickness (T_{body}), are regarded as the main design variables, given that they have a critical influence on the cell's memory characteristics. The device design and analysis were performed using the Sentaurus TCAD simulation tool. In the simulation, the Fermi–Dirac statistical model, the nonlocal band-to-band tunneling (BTBT) model, the Shockley-Read-Hall (SRH) recombination model, the Auger recombination model, the trap-assisted-tunneling (TAT) model, the doping-dependent and field-dependent mobility models, the bandgap narrowing model, and the quantum confinement effect were all considered to maximize the simulation accuracy [18]. Furthermore, the trap distribution in the GBs of the poly-Si was calibrated using the experimental data in [13], which is shown in Fig. 2(b). In Fig. 2(b), the GB had four trap states, depending on the energy level: acceptor-like shallow trap, acceptor-like deep trap, donor-like shallow trap, and donor-like deep trap. As shown in Fig. 2(a), the simulation results show a good agreement with the measured data using the calibrated parameters and the experimental data in [13].

TABLE 1. Device parameters of the proposed 1t-dram used for simulation.

Parameter	Values
Main gate length (L_{g1})	70 nm
Underlap length ($L_{underlap}$)	0 nm -20 nm
Body thickness (T_{body})	7 nm -15 nm
Gate dielectric (HfO_2) thickness (T_{ox})	3 nm
Source/Drain doping concentration	n-type, 1×10^{20} cm^{-3}
Body doping concentration	p-type, 1×10^{18} cm^{-3}
Main gate work-function (WF_{MG})	4.85 eV
Control gate work-function (WF_{CG})	5.3 eV

TABLE 2. Operating bias scheme for memory performance.

	Write "1" (Program)	Write "0" (Erase)	Read	Hold
Main gate voltage (V_{GS1})	2.0 V	0.0 V	1.0 V	0.0 V
Control gate voltage (V_{GS2})	−1.7 V	0.3 V	0.0 V	−0.1 V
Drain voltage (V_{DS})	0.0 V	−0.5 V	0.5 V	0.0 V

III. RESULTS AND DISCUSSIONS

Fig. 3 shows the transient characteristics of the proposed 1T-DRAM cell. The operating bias of the 1T-DRAM performance is summarized in Table 2. Program operation was performed using the BTBT mechanism. During the erase operation, the holes that accumulated at the control gate side of the body region drifted toward the drain region because of the absence of a potential barrier. As shown in the figure, the proposed 1T-DRAM cell obtained a high sensing margin

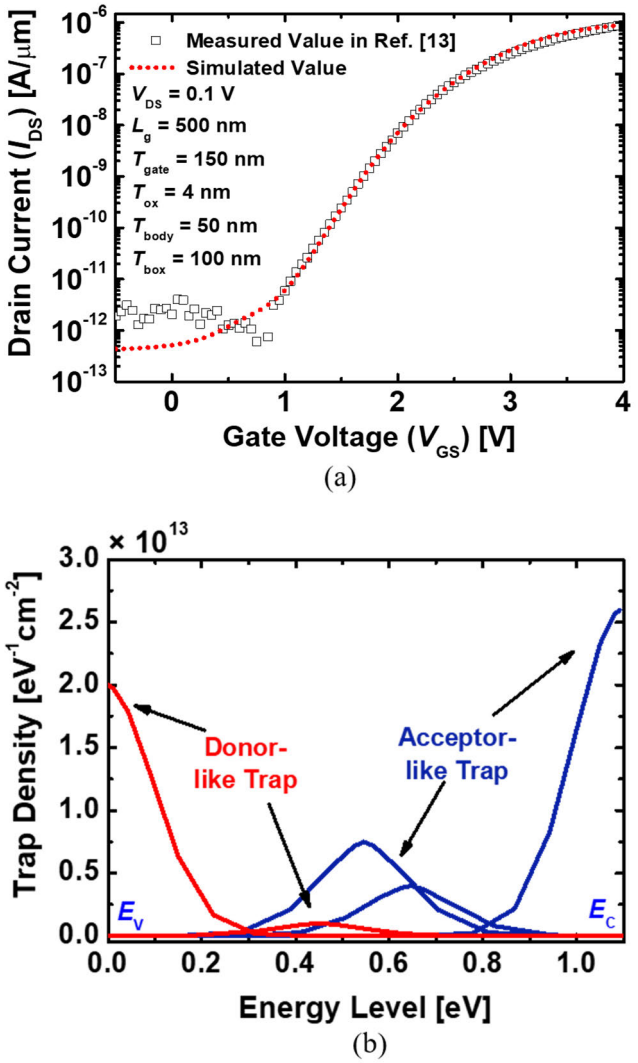

FIGURE 2. (a) Transfer characteristics of the simulation result with the calibrated parameters and the experimental data in [13]. (b) GB trap distribution calibrated using the experimental data in [13].

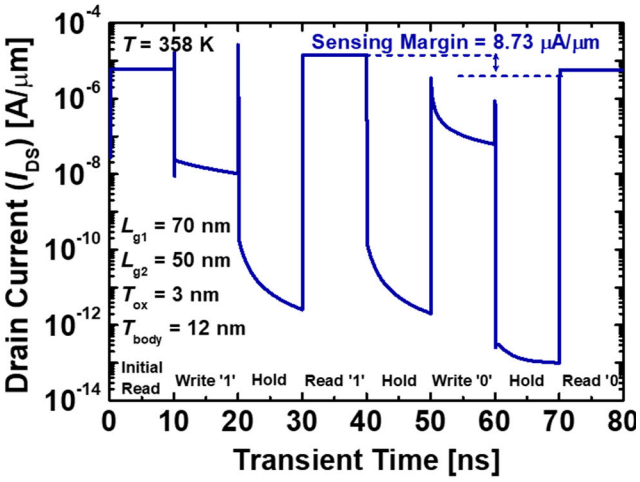

FIGURE 3. Transient characteristics of the proposed 1T-DRAM cell.

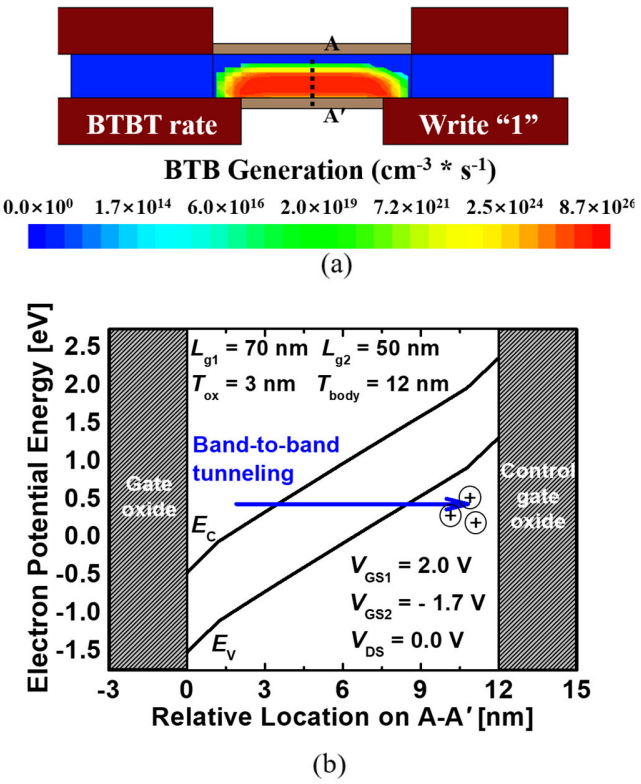

FIGURE 4. (a) Contour map of the BTBT rate and (b) energy band diagram of the proposed poly-Si MOSFET-based 1T-DRAM cell in the program operation. The energy band is extracted at the center of the body region.

of 8.73 μA/μm at $T = 358$ K. In the proposed device, the electrical characteristics of the body region critically affect the memory performance. Therefore, various geometric and electrical parameters, including L_{underlap}, T_{body}, and the hold bias of the control gate ($V_{\text{GS2\_H}}$), were modulated to optimize the device performance.

Fig. 4(a) shows the program operation carried via the BTBT mechanism in the vertical direction between the main gate and the control gate. The tunneling-based program operation is used considering that the tunneling mechanism requires less power consumption compared to that used by the impact ionization mechanism. Furthermore, during the program operation, static-power dissipation can be avoided because there is no bias at the drain region. As shown in Fig. 4(b), by applying a positive bias of 2.0 V at the main gate and a negative bias of −1.7 V at the control gate, BTBT occurs and holes tunnel from the main gate side to the control gate side in the same direction as the electric field, which enhances the tunneling rate. The excess holes accumulate at the control gate side of the body region due to the potential well, which facilitates hole storage, formed by the high work-function of the control gate.

Fig. 5(a) and (b) depict both the contour map of the hole density and the energy band diagram of the proposed 1T-DRAM cell in states "1" and "0", respectively. Since

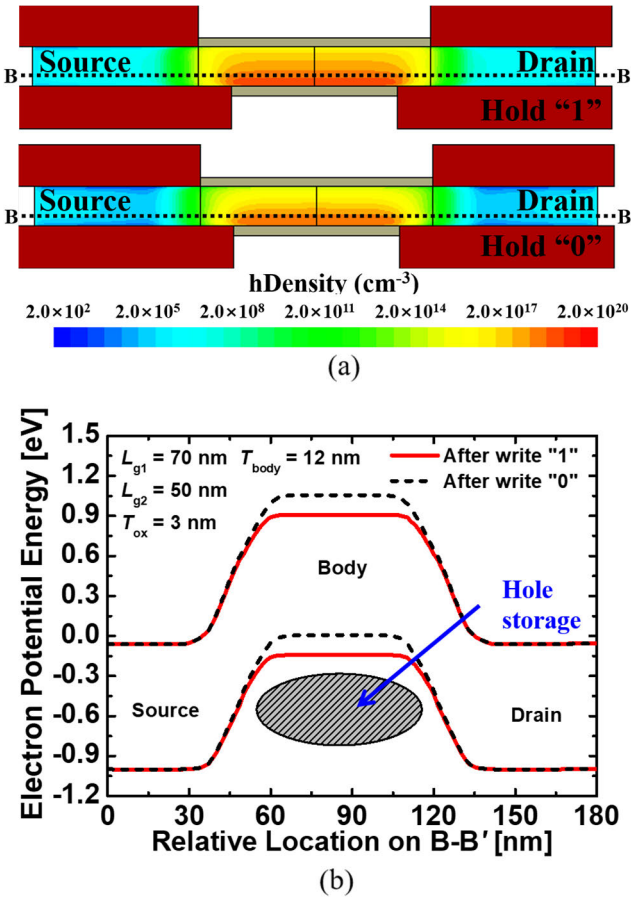

FIGURE 5. (a) Contour map of the BTBT rate and (b) energy band diagram of the proposed poly-Si MOSFET-based 1T-DRAM cell in the program operation. The energy band is extracted at the 3 nm above the control gate oxide.

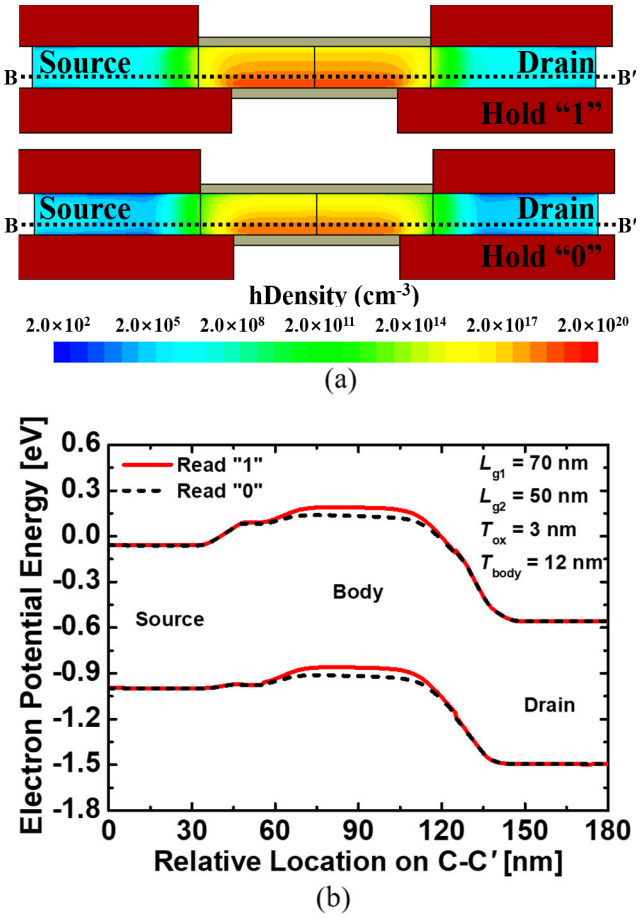

FIGURE 6. (a) Contour map of the BTBT rate and (b) energy band diagram of the proposed poly-Si MOSFET-based 1T-DRAM cell in the program operation. The energy band is extracted at a distance of 3 nm below the gate oxide.

BTBT tunneling occurs in the body region, a large number of excess holes gather in the body region. When excess holes exist in the body region, the 1T-DRAM is in the "1" state. During the erase operation, the stored holes are removed by the negative bias on the drain region. The state of the 1T-DRAM cell without excess holes is defined as the "0" state. As shown in Fig. 5(a), there is a significant difference in hole density between states "1" and "0", particularly in the area close to the control gate. As shown in Fig. 5(b), this difference entails a different energy band diagram for states "1" and "0" during the hold operation; a larger hole density can be seen in state "1". It also seems that positive voltage is applied by the excess holes in the body region and this has the same effect as energy barrier lowering.

Fig. 6(a) shows the contour maps of the electron current density in the proposed 1T-DRAM cell during the read "1" and read "0" operations, respectively. Fig. 6(a) shows that the current density of read "1" is larger than that of read "0". The read operations are conducted via conventional MOSFET operation by setting V_{GS1} to 1.0 V and V_{DS} to 0.5 V. As shown in Fig. 6(b), the existence of excess holes in the storage region affects the electric potential of the body region. Excess holes appear as if positive voltage is applied by the holes in the body region during the read "1" operation, and this has the same effect as lowering V_{th}, resulting in a higher read current. This difference in hole density corresponds to the difference between the read "1" current and the read "0" current, and is the value of the sensing margin of the 1T-DRAM

A. EFFECT OF $L_{underlap}$ VARIATIONS

The 1T-DRAM attempts to return to an equilibrium state during the hold time after program or erase operations. It is very important to analyze the time required for the device to return to the steady state because this is closely related to the retention time which is an indicator of memory performance. In order to accurately analyze the factors affecting retention time, it is important to know which factors have a significant impact on recombination/generation rates in the hold "1" and hold "0" states. Looking first at the hold "1" state which occurs after the program operation, the excess holes are gradually released through the body-to-source and body-to-drain junctions during the hold time. The rate of evacuation holes from the body is represented by the SRH recombination rate

of the proposed poly-Si MOSFET-based 1T-DRAM cell with different L_{underlap} during the hold "1" operation. In Fig. 7(a), the recombination rate reduces as the L_{underlap} increases. The recombination rate is related to the electric field. Fig. 7(b) shows the electric field of the proposed device with different L_{underlap} along the lateral direction. As shown in the figure, the electric field at the depletion region decreases as L_{underlap} increases because of the wider depletion region under the underlap structure. Therefore, the weakening of the electric field surrounding the storage region leads to a decrease in hole recombination [19]. When the cell is in the hold "0" state, its return to equilibrium depends on hole charging mainly via BTBT generation. In this state, the most critical factor for generation is BTBT tunneling. BTBT tunneling affects the return of the device to equilibrium because it generates excess carriers in the body region during the hold "0" state. As shown in Fig. 7(c), the BTBT generation rate decreases with increasing L_{underlap} because of the widening depletion region under the underlap structure as shown in Fig. 7(c). Consequently, the increase of L_{underlap} plays a role in reducing both SRH recombination in the hold "1" state and BTBT generation in the hold "0" state, which help to improve the retention time of the proposed 1T-DRAM.

Fig. 8 shows the sensing margin and retention time of the proposed device as a function of L_{underlap}. As L_{underlap} increases, the influence of the control gate with high work-function decreases. This causes the depletion area of the channel to be reduced, and this results in an improvement in the transfer characteristics related to the sensing margin. Consequently, the sensing margin is enhanced by increasing L_{underlap}. However, the retention time increases up to L_{underlap} of 10 nm but then subsequently decreases. Retention time is affected not only by the generation/recombination rate but also by the number of holes. As L_{underlap} increases, the physical size of the quantum well that can store holes in the body region decreases. Additionally, the generation/recombination rate decreases as L_{underlap} increases. Below an L_{underlap} of 10 nm, the generation/recombination rate decreases and hole density decreases, but retention time increases because the number of holes is sufficient. When L_{underlap} is more than 10 nm, the generation/recombination rate also decreases, however, hole density in the body region is not sufficient to cope with the decreasing number of holes by generation/recombination. As a result, when L_{underlap} is greater than 10 nm, the retention time decreases. As shown in the figure, the proposed 1T-DRAM cell had the highest performance when $L_{\text{underlap}} = 10$ nm, with a high retention time of 424 ms.

B. EFFECT OF T_{body} VARIATIONS

Fig. 9(a) shows a contour map of the recombination rate of the proposed 1T-DRAM cell with varying T_{body}. As indicated in the figure, the recombination rate decreases when T_{body} increases. As shown in Fig. 9(b), a body thickness of 10 nm has a sufficiently high sensing margin, but its retention time

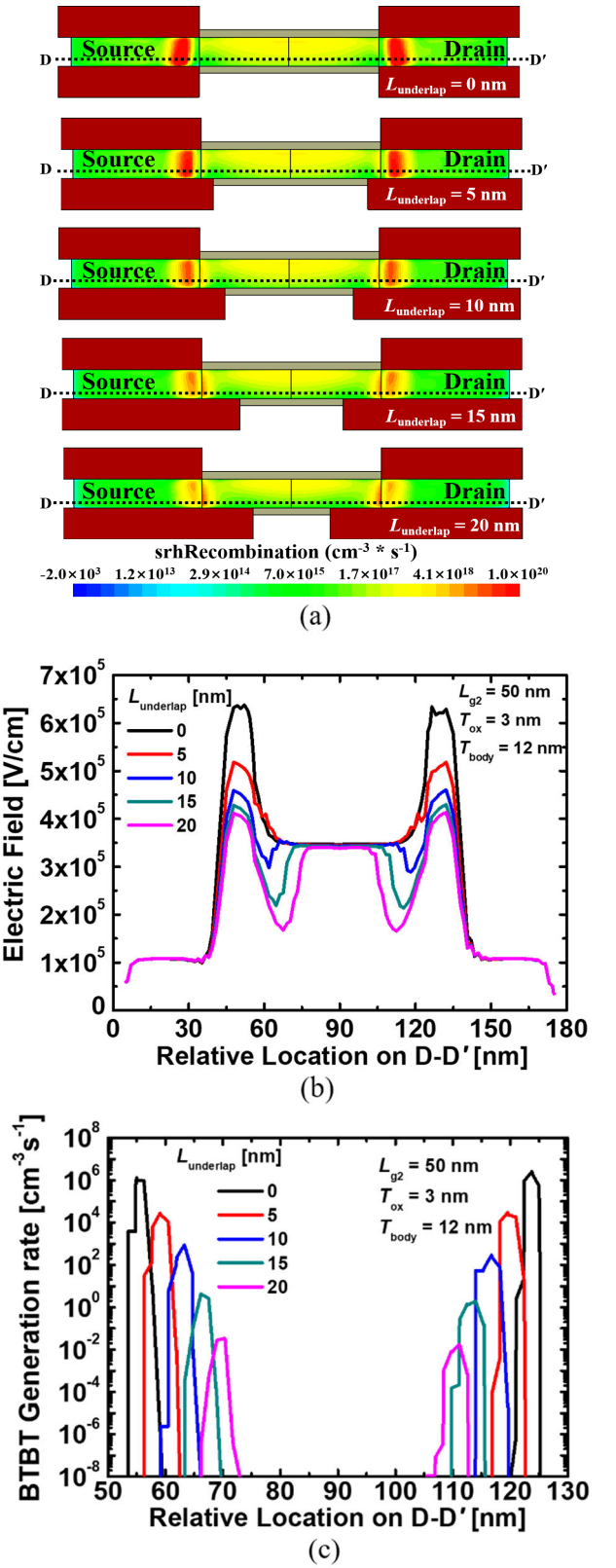

FIGURE 7. (a) Contour map of the SRH recombination rate and (b) electric field of the proposed poly-Si MOSFET-based 1T-DRAM cell with different L_{underlap} under hold "1" operation. (c) Band-to-band tunneling generation rate of the proposed poly-Si MOSFET-based 1T-DRAM cell under hold "0" operation with different L_{underlap}. The electric field and BTBT generation rate are extracted at a distance of 3 nm above the control gate oxide.

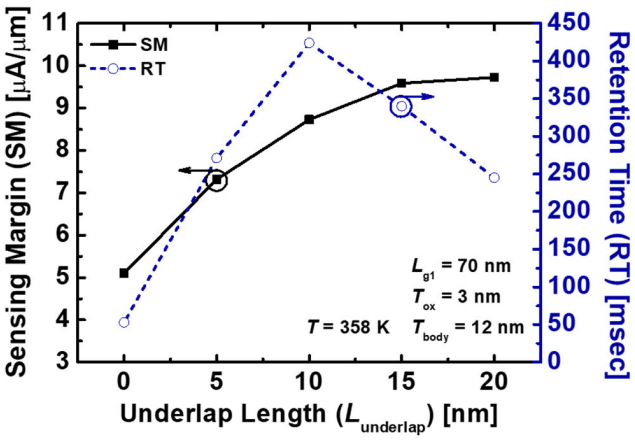

FIGURE 8. Sensing margin and retention time of the proposed 1T-DRAM cell as a function of $L_{underlap}$.

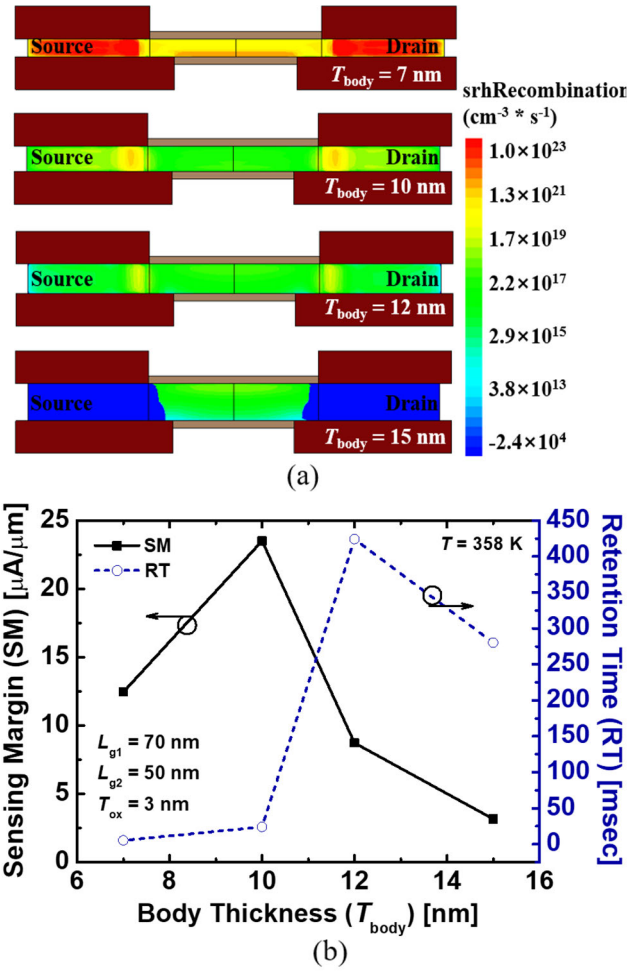

FIGURE 9. (a) Contour of the SRH recombination rate of the proposed poly-Si-MOSFET-based 1T-DRAM cell during hold operation with varying T_{body}. (b) Sensing margin and retention time of the proposed 1T-DRAM cell as a function of T_{body}.

is not sufficient to satisfy the International Roadmap for Devices and Systems (IRDS) (<64ms) [20]. The retention time degrades because of the decrease in the number of excess

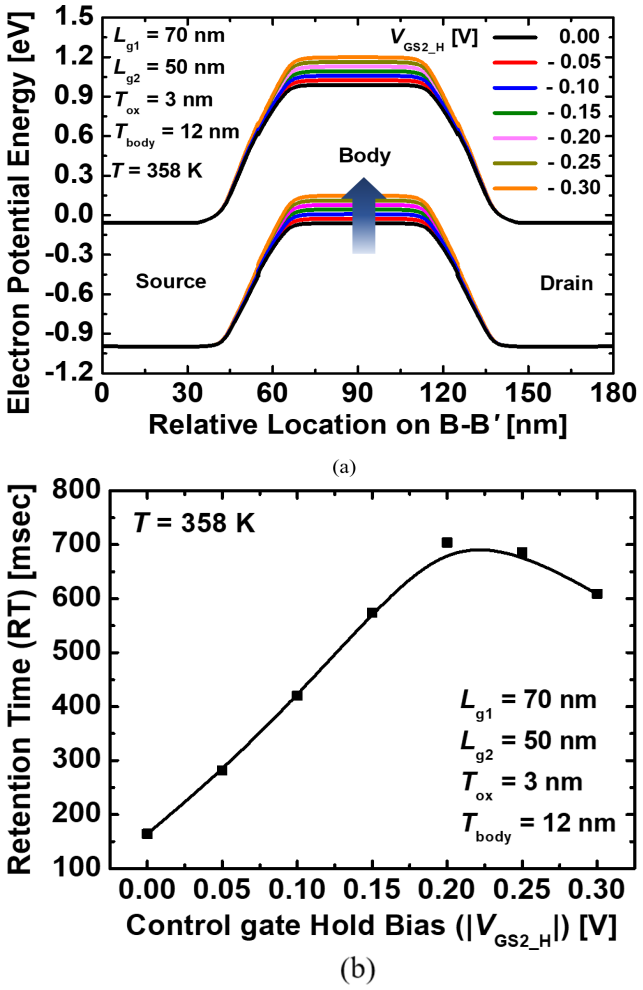

FIGURE 10. (a) Energy band diagram of the proposed poly-Si MOSFET-based 1T-DRAM cell under hold operation with different V_{GS2_H}. (b) Retention time of the proposed 1T-DRAM cell as a function of V_{GS2_H}. The energy band is extracted at a distance of 3 nm above the control gate oxide.

holes in the storage region. The BTBT rates during program operation are also reduced because of the decrease in the vertical electric field. In addition, it has a high retention time at a body thickness of 15 nm, but a poor sensing margin that is less than 3 μA/um [21]. Consequently, the proposed 1T-DRAM cell has the highest retention time of 424 ms when $T_{body} = 12$ nm.

C. EFFECT OF V_{GS2_H} VARIATIONS

Fig. 10(a) shows the variation in the energy band diagram of the proposed 1T-DRAM cell with different V_{GS2_H}. When a bias is applied at the control gate, the potential energy of the body region increases, forming a larger storage region. Fig. 10(b) shows the retention time of the proposed device with different V_{GS2_H} as a function of hold time. The retention time is enhanced because of the larger storage layer with lower V_{GS2_H}. However, when V_{GS2_H} is less than -0.2 V, the retention time decreases because of the hole

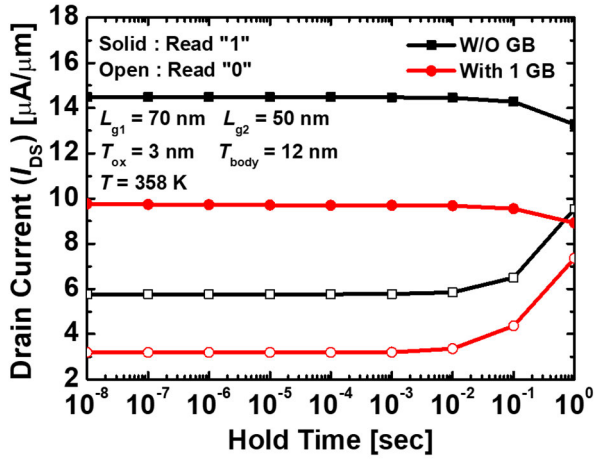

FIGURE 11. Read currents of the proposed 1T-DRAM cells with and without GB as a function of a hold time.

TABLE 3. Memory performance of various 1t-dram related papers.

No	Structure	Sensing margin [μA/um]	Retention time [ms]
1	Junctionless FinFET (w/o GB) [26]	11.2	196
2	Junctionless FinFET (Horizontal GB) [26]	11.3	148
3	Junctionless FinFET (Vertical GB) [26]	11.7	64.2
4	Double-gate [27]	6.16	131
5	Si/SiGe junctionless [28]	0.39	10
6	Shell-doped junctionless [29]	4.5~6	~11
7	Junctionless FET [30]	1.59	~0.01
8	Electron-bridge channel [31]	3.65	68
9	This work (w/o GB)	8.73	704.4
10	This work (w/ GB, GB #1)	6.58	340.1
11	This work (w/ GB, GB #4)	3.38	82.45

generation caused by tunneling through the thin barriers at the source/drain junctions. Therefore, it can be concluded that the proposed 1T-DRAM cell has superior performance with a high sensing margin of 8.73 μA/μm and a high retention time of 704.4 ms when $V_{GS2\_H} = -0.2$ V. It obtains a long retention time of 704.4 ms at 358 K, and this is almost 11 times longer than that required of DRAM cells by the IRDS [20].

D. EFFECT OF GBs IN 1T-DRAM

In poly-Si thin-film-based devices, randomly generated grain boundaries (GBs) exist in the poly-Si region [22]–[24]. Considering that traps in the GBs adversely affect device performance, the effect of GBs on the proposed device should be

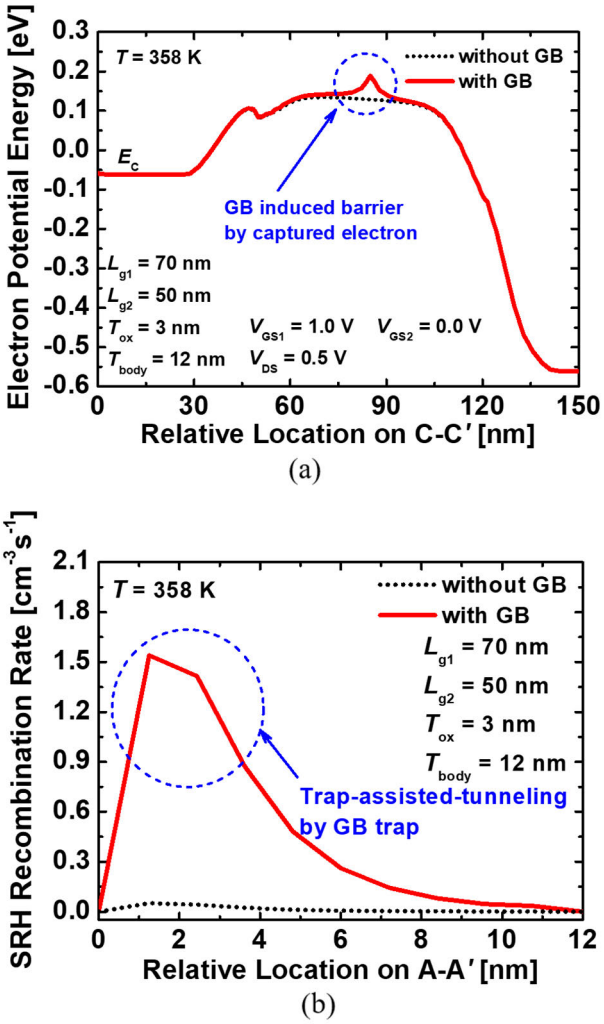

FIGURE 12. (a) E_C of the proposed devices with and without a GB under read operation. (b) Recombination rate of the proposed 1T-DRAM cells with and without a GB under hold operation. The energy band is extracted at the center of the body region and at a distance of 3 nm below the main gate oxide, respectively.

analyzed to ensure its reliability. To definitively determine the effects of the GBs, the proposed 1T-DRAM cell was simulated including a single GB. In the simulation, L_{g1} was set to 70 nm. Therefore, a single GB was assumed to be located at the center of the body region, given that the grain size of poly-Si is several hundred nanometers [22]–[24]. The trap distribution of the GB, which was applied within the simulation, was calibrated using experimental data [13] as shown in Fig. 2(b).

Fig. 11 illustrates the read currents of the proposed 1T-DRAM cells as a function of a hold time both with and without the GB. As indicated, the read "1" and read "0" currents are degraded with the GB present. The sensing margin decreased accordingly from 8.73 to 6.58 μA/μm.

As shown in Fig. 12(a), the energy barrier formed by electrons that are captured in the GB trap prevents current flow from the source to the drain. In addition, the hole

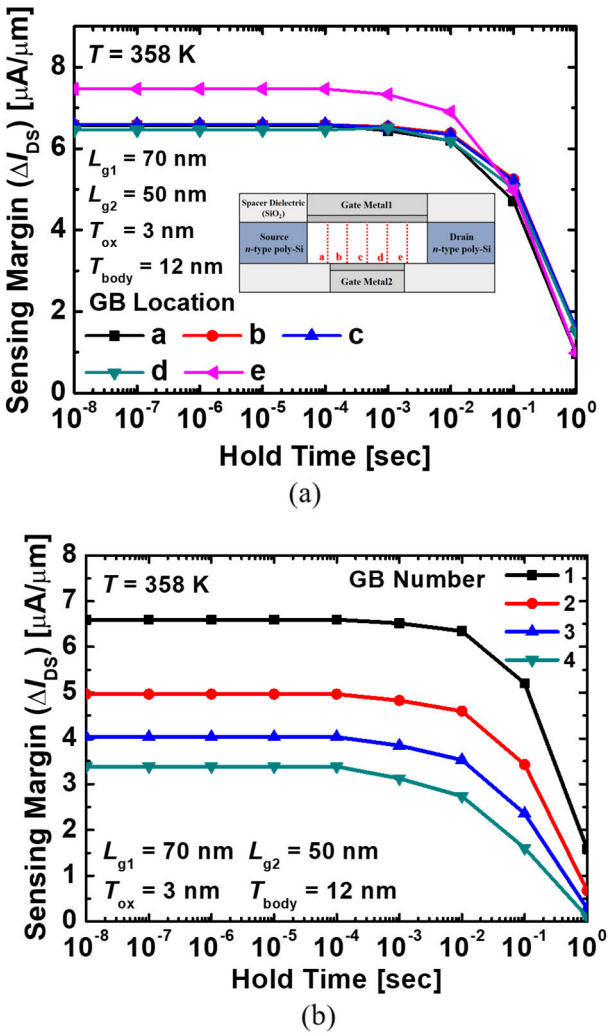

FIGURE 13. Sensing margin of the proposed poly-Si MOSFET-based 1T-DRAM cells with (a) different GB locations and (b) different GB number as a function of hold time.

recombination and generation rates increase as a result of the TAT mechanism through the GB traps, as shown in Fig. 12(b). However, the proposed device still exhibited a high retention time of 340.1 ms at $T = 358$ K even with the GB, proving its high reliability.

When GBs exist in the poly-Si body region, the location and the number of GBs is uncertain because of the random generation of grains. Therefore, the effect of the GB location on the proposed 1T-DRAM cells was determined as a function of hold time. When the GB is located at positions *b*, *c*, and *d* (Fig. 13(a), inset), there is little effect on the memory performance. However, when the GB is located at positions *a* or *e*, the read "1" and read "0" currents are increased. Since the GB-induced energy barrier is located in the depletion region, the effect on the electron flow decreases. In particular, when the GB is located at *e*, the read currents become larger because the energy barrier decreases due to drain bias, similar to the drain induced barrier lowering phenomenon [25]. Therefore, the sensing margin has the highest value of 7.46 μA/μm when the GB is at *e*. However, the retention time such a device is at the lowest value of 207.94 ms, although this is still demonstration of excellent retention characteristics (>64 ms when $T = 358$ K). Fig. 13(b) shows the sensing margin of the proposed 1T-DRAM cells with different GB number as a function of hold time. The GB number is limited to 4 because the body region is not large enough to have accommodate a larger number of GBs. The sensing margin decreased from 6.58 to 3.38 μA/μm when the number of GBs increased from 1 to 4. This is because the increasing GB-induced energy barrier disturbs the current flow and thus decreases the read currents and the sensing margin. The retention time also decreases when the number of GBs in the proposed 1T-DRAM cell increases. This increases because of the enlarged region in which TAT occurs. However, in cases like that, the number of GBs is 4, which means that the grain size is approximately 14 nm, and the high retention time of 82.45 ms is obtained when $T = 358$ K, indicating high retention performance (>64 ms when $T = 358$ K). Moreover, considering grain size, the proposed 1T-DRAM cell exhibits superior reliability in terms of memory characteristics even at a high temperature. Additionally, as can be clearly seen in Table 3, the 1T-DRAM proposed in this study exhibits excellent memory performance when compared to other devices reported previously.

IV. CONCLUSION

In this work, a novel 1T-DRAM based on a poly-Si MOSFET with an asymmetric dual-gate structure was designed and investigated with TCAD simulations. Various geometric and electrical parameters were varied to optimize the memory performance. The simulated 1T-DRAM cell achieved a high sensing margin of 8.73 μA/μm and a high retention time of 704.4 ms with the optimized parameters of $L_{\text{underlap}} = 10$ nm, $L_{g1} = 70$ nm, $L_{g2} = 50$ nm, $T_{\text{body}} = 12$ nm, $T_{ox} = 3$ nm, and $V_{GS2\_H} = -0.2$ V. Furthermore, the proposed 1T-DRAM cell demonstrated excellent reliability in terms of its retention characteristics (>64 ms when $T = 358$ K) with various GB locations and numbers. Therefore, our proposed 1T-DRAM has significant potential to replace the conventional 1T-1C DRAM via implementation of a high-density 3D memory array.

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SANG HO LEE received the B.Sc. degree in electronics engineering from the School of Electronics Engineering (SEE), Kyungpook National University (KNU), Daegu, South Korea, in 2019, where he is currently pursuing the M.Sc. degree in electrical engineering. His research interests include the design, fabrication, and characterization of gate-all-around logic devices and capacitorless 1T-DRAM transistors.

WON DOUK JANG (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, South Korea, in 2018 and 2020, respectively. He is currently working as a Flash Memory Process Architecture Engineer with Samsung Electronics Company Ltd.

YOUNG JUN YOON received the B.S. and Ph.D. degrees in electronic engineering from Kyungpook National University, Daegu, South Korea, in 2013 and 2019, respectively. He is currently a Postdoctoral Researcher with the Korea Multipurpose Accelerator Complex, Korea Atomic Energy Research Institute (KAERI). His research interests include design, fabrication, and characterization of logic transistor and memory.

JAE HWA SEO received the B.S. and Ph.D. degrees in electronic engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, South Korea, in 2012 and 2018, respectively. He held a postdoctoral position in electrical engineering with the School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU), Seoul, South Korea, in 2018 to 2019. He is currently working as a Staff Engineer with the Flash TD Team, Semiconductor Research and Development Center, Samsung Electronics Company. His research interests include the design, fabrication and characterization of V-NAND/1T-DRAM devices, nanoscale CMOS, tunneling FETs, and compound/silicon-based transistors.

HYE JIN MUN received the B.Sc. degree in computer engineering and the B.Sc. degree in electrical engineering from Yeungnam Unversity (YU), Gyeongsan, South Korea, in 2013. She is currently pursuing the M.Sc. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). Her research interests include the design and characterization of nano-scaled CMOS-based on poly silicon.

MIN SU CHO received the B.Sc. degree in computer engineering from the College of Electrical and Computer Engineering, Chungbuk National University (CBNU), Cheongju, South Korea, in 2015, and the M.Sc. degree from the School of Electronics Engineering (SEE), Kyungpook National University (KNU), where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include the design, fabrication, and characterization of compound CMOS, tunneling FETs, and III-V compound transistors.

JAEWON JANG (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2006 and 2008, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 2013. From 2013 to 2014, he was a Postdoctoral Researcher and was working for developing high performance metal oxide transistors by printing technology. From 2015 to 2016, he was a Researcher and was working for developing high performance organic thin film transistor with the Samsung Advanced Institute and Technology, Suwon, South Korea. Since 2016, he has been with Kyungpook National University, Daegu, South Korea, where he is currently an Assistant Professor with the School of Electronics Engineering.

JIN-HYUK BAE received the B.S. degree in electronics and electrical engineering from Kyungpook National University, Daegu, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2006 and 2010, respectively. From 2010 to 2012, he worked as a Postdoctoral Research Fellow with the Ecole Nationale Superiere des Mines de Saint-Etienne, Gardanne, France. He joined the Faculty of the School of Electronics Engineering, Kyungpook National University, in 2012, where he is currently an Associate Professor. His research interests include interfacial engineering and physics of organic based and metal-oxide-based electronic devices and their sensor applications.

IN MAN KANG (Member, IEEE) received the B.S. degree in electronic and electrical engineering from the School of Electronics and Electrical Engineering, Kyungpook National University (KNU), Daegu, South Korea, in 2001, and the Ph.D. degree in electrical engineering from the School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU), Seoul, South Korea, in 2007. From 2001 to 2006, he worked as a Teaching Assistant for semiconductor process education with the Inter-university Semiconductor Research Center (ISRC), SNU. From 2007 to 2010, he worked as a Senior Engineer with the Design Technology Team, Samsung Electronics Company. He joined the School of Electronics Engineering (SEE), KNU, as a full-time Lecturer, in 2010. He is currently working as an Associate Professor. His current research interests include CMOS RF modeling, silicon nanowire devices, tunneling transistor, low-power nano CMOS, and III-V compound semiconductors. He is a member of the IEEE EDS.