IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 26, 2021, accepted March 15, 2021, date of publication March 24, 2021, date of current version April 2, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3068482

An 0.4–2.8 GHz CMOS Power Amplifier With On-Chip Broadband-Pre-Distorter (BPD) Achieving 36.1–38.6% PAE and 21 dBm Maximum Linear Output Power

SELVAKUMAR MARIAPPAN[1], (Student Member, IEEE), JAGADHESWARAN RAJENDRAN[1,2], (Senior Member, IEEE), YUSMAN M. YUSOF[2], NORLAILI M. NOH[3], (Senior Member, IEEE), AND BINBOGA SIDDIK YARMAN[4], (Life Fellow, IEEE)

[1]Collaborative Microelectronics Design Excellence Center (CEDEC), Universiti Sains Malaysia, Penang 11900, Malaysia
[2]SilTerra Malaysia Sdn. Bhd., Kulim 09090, Malaysia
[3]School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Penang 11900, Malaysia
[4]Department of Electrical and Electronics Engineering, Istanbul University, 34320 Istanbul, Turkey

Corresponding author: Jagadheswaran Rajendran (jaga.rajendran@usm.my)

This work was supported in part by the Collaborative Research in Engineering Science and Technology (CREST) under Grant 304/PELECT/6050378/C121, in part by the Universiti Sains Malaysia Research University Grant (USM RUI) under Grant 1001/PCEDEC/8014079, in part by the Fundamental Research Grant Scheme (FRGS) under Grant 1001/PCEDEC/6071449, and in part by the QED Venture.

ABSTRACT A broadband 180 nm CMOS power amplifier (PA) operating from a frequency bandwidth of 400 MHz to 2.8 GHz is presented in this paper. The PA is integrated with an inductor-less Broadband-Pre-Distorter (BPD) to enhance its linearity for wide bandwidth. The BPD consists only of MOS transistors, resistors, and capacitors which contribute to the wideband operation thus independent of the Q factor of passive inductors which contributes to the effectiveness of many other APDs available. The integrated BPD improves the Amplitude Modulation-to-Amplitude Modulation (AM-AM) and Amplitude Modulation-to-Phase Modulation (AM-PM) deviation of the PA across maximum linear output power of 21 dBm. Utilizing a silicon area of 1.69 mm^2, mounted on Roger's RO4000/FR4 PCB, the BPD-PA produces a maximum output power of more than 22 dBm for 2.4 GHz bandwidth with a minimum power gain of 15 dB. The corresponding peak power added efficiency (PAE) of more than 35% is achieved across the operating bandwidth. The fabricated BPD-PA meets the Adjacent Channel Leakage Ratio (ACLR) specification of −30 dBc at a maximum linear output power of 21 dBm (3 dB back-off from maximum output power) when tested with 20 MHz LTE signal at 1.7 GHz.

INDEX TERMS Complementary metal oxide semiconductor (CMOS), power amplifier (PA), broadband, pre-distorter, power added efficiency (PAE), transceiver, adjacent channel leakage ratio (ACLR), amplitude modulation-amplitude modulation (AM-AM), amplitude modulation-phase modulation (AM-PM).

I. INTRODUCTION

Modern communication systems are concentrating on achieving higher data rates transmission at flexible frequencies while achieving high efficiency without trading off stringent linearity requirement of the communication protocols; i.e; LTE, NB-IoT. As such, power amplifiers (PAs) have been extensively focusing on bandwidth enhancement along with efficiency, linearity, and output power performances. The PAs have been extensively explored due to their cost-effectiveness and System-on-Chip (SoC) integration for transceivers [1]–[3]. However, CMOS PAs have various drawbacks which make it arduous to achieve the goal of SoC. CMOS PAs are required to outdo the limitations such as low trans-conductance, low breakdown voltage, high parasitic capacitances, and high loss silicon substrate in CMOS technology [4], [5]. Due to the aforementioned limitations of the CMOS process, designing a broadband and highly efficient as well as highly linear CMOS PA is strenuous than conventional narrowband CMOS PAs.

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

The significant contributors to the non-linearity effect in CMOS PAs are the intrinsic non-linear trans-conductance and the non-linear gate-source capacitance, C_{gs}. Various linearity and efficiency enhancement techniques have been extensively proposed to overcome the aforementioned drawbacks in CMOS PAs. In [6], an adaptively controlled biasing technique is utilized in a common-source PA to reduce its gain and phase distortion by controlling its gate bias voltage when the RF signal is more than a certain threshold. A hybrid class-G Doherty is proposed in [7] where it uses a mixed-signal linearization technique to optimize its amplitude and phase modulation through digital PA operation and analog phase compensation. In [8], it is proposed that the phase modulation distortion of a 2-stage PA operating in millimeter-wave (mmW) has been optimized by utilizing a compensation transformer integrated at its input. An external harmonic injection technique is also proposed as a technique to enhance linearity and efficiency as in [9]. A second-harmonic injection at the PA's output enables the voltage and current wave-shaping that optimizes the overall performance of the PA.

Besides that, linearization techniques such as Analogue Pre-Distortion (APD) and Digital Pre-Distortion (DPD) techniques are also customarily utilized [10]. Pre-distortion is an execution of cancelling out the non-linearity of PA by generating a distorted characteristic that is opposite in terms of amplitude and phase profiles as compared to that of PA. If the pre-distorter generates an intermodulation product that is equal in magnitude and out-of-phase to that of the PA, then an ideal cancellation of IMD products is achieved. These opposite characteristics between the stages cancel out the 3^{rd}-order intermodulation (IMD3) product produced [11]. Yet, the DPDs are highly complex in its integration [12] and consumes large chip area while APDs use variable phase and gain shifters which only works for narrowband [13], [14].

Multitudinous efforts have been put into achieving broadband operation with CMOS PA previously. In [15], a 130 nm CMOS common drain PA with an integrated transformer produces a broad bandwidth operation by cascading two amplifier stages. An interstage broadband matching network is constructed to compensate for the first and second stage's frequency response to achieve a flat in-band gain. Moreover, a 180 nm stacked Class-J PA has been proposed in [16], where an optimum 2^{nd}-order harmonic load impedance is matched at different frequencies to obtain high efficiency in broadband. Unlike [12] which emphasizes the 2nd-order harmonic termination only, [17] presents a 180 nm SOI CMOS wideband PA with adjacent channel leakage ratio (ACLR) improvement through the utilization of 2^{nd} and 3^{rd}-order harmonic traps. The harmonic traps act as a short circuit at 2^{nd}-harmonic and an open circuit at 3^{rd}-harmonic.

Furthermore, [18] demonstrates a 45 nm CMOS PA with the combination of voltage-mode Doherty and Class-G switched capacitor technique. The switched capacitor PA is based on the fragmentation of a voltage mode Class-D PA in which the capacitor and a totem-pole driver are divided into small unit cells. When a segment of unit cells is turned on, the output voltage is controlled proportionally to the number of active unit cells which improves the efficiency for wide bandwidth. Besides, [19] also presents a switched capacitor technique that has been utilized to tune the frequency of the PA. Fabricated in 65 nm CMOS, the switched capacitor PA is constructed in series with a fixed inductor and a digitally programmable capacitor that enables frequency tuning.

Also, a dual-mode CMOS 180 nm PA with dynamic load modulation is presented in [20] to reduce the effect of the peak-to-average power ratio (PAPR) on the PA's load impedance. The dynamic load modulation is realized with a π-type matching network to optimize the PA's efficiency for wide bandwidth. Besides this, a power-control loop is utilized to reconfigure the PA's operation mode by sensing the input signal PAPR in real-time. This is followed, in [21], a transformer-based two stages dual-radial power splitting/combining technique is proposed which is equipped with an in-phase RF power splitting/combining competency. Instead of the conventional current combining method, [22] uses a series combining transformer (SCT) to combine the output power and achieve the load modulation in a voltage combining Doherty PA. The challenge lies in preserving the linearity and efficiency of the PA across a broad bandwidth. In some literature, even though the frequency response is providing broad bandwidth, the linearity and efficiency performances are only reported for single frequency such as in [16], [20], and [21]. The linearity and efficiency performances of the PA degrade drastically when the operating frequency is shifted from the center frequency.

This paper proposes a Broadband-Pre-Distorter (BPD) linearization mechanism that extends the linear operating bandwidth of a CMOS PA with a minimum trade-off with its Power-Added-Efficiency (PAE). Unlike APD which utilizes inductors (thus narrowband), the proposed BPD technique comprises MOS transistors, resistors, and capacitors to be area-efficient while reducing the IMD3 distortion generated by the main PA. This paper is organized as follows. Section II describes the principle of operation of the BPD-PA. Section III discusses the measurement performance of the PA and finally, Section IV concludes.

II. BROADBAND-PRE-DISTORTER-POWER AMPLIFIER (BPD-PA)

A. CIRCUIT DESIGN

The schematic of the proposed broadband CMOS BPD-PA is depicted in Fig. 1. The operating bandwidth of the BPD-PA ranges from 400 MHz to 2.8 GHz while providing the desired gain and output power. The designed BPD-PA consists of an input matching network (IMN), BPD, main PA, output matching network (OMN), and biasing circuits integrated on-chip. The main PA is operated in class AB mode and the gate voltage is supplied by utilizing a current source configured biasing circuit comprised of R_6, M_5, and R_7. On the other hand, the biasing circuit for BPD consists of R_2, M_1, and R_3. M_1 and M_5 are diode-connected transistors that minimize

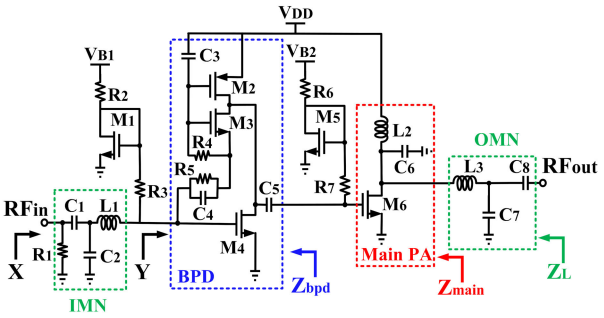

FIGURE 1. Schematic of the broadband CMOS BPD-PA.

the effect of C_{gd} thus greatly reduces the impact of bias modulation on the PA. The simplicity of the biasing circuits also saves the chip area.

The IMN is configured with R_1 (100 Ω), L_1 (4.83 nH), C_1 (1 pF), and C_2 (0.3 pF). C_1 also serves as a DC block capacitor. Referring to Fig. 1, Y represents the impedance before IMN whereas X is the impedance once IMN is added. With the aid of R_1, a wideband S_{11} is achieved as illustrated in Fig. 2. Other than that, the OMN consists of L_3 (1.98 nH), C_7 (1.5 pF), and C_8 (10 pF), where C_8 is the DC block capacitor to prevent DC current flow from supply V_{DD}. L_2 (11.64 nH) is the RF choke for the main PA and capacitor C_6 (0.5 pF) is used to reduce the harmonic frequency. As a result, the PAE increases by 6%. Also, C_5 (20 pF) serves as the capacitive coupling between the BPD and main PA.

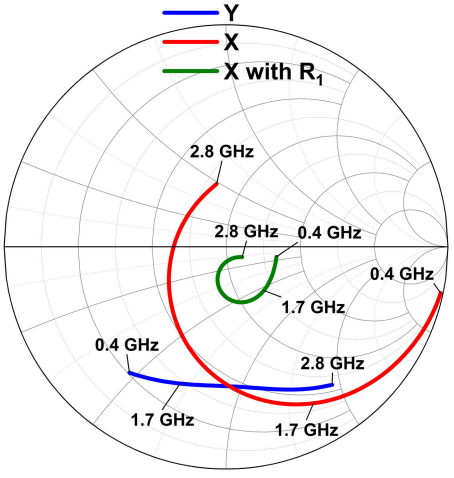

FIGURE 2. Location of input impedance points across frequency prior and after IMN integration.

The drain supply, V_{DD} for the BPD and main PA are 3.3 V. The drain supply of the biasing circuits is given as $V_{B1} = 1.2$ V and $V_{B2} = 1.5$ V respectively. The BPD is built upon M_2 (280 μm/0.3 μm), M_3 (10 μm/0.34 μm), M_4 (750 μm/0.18 μm), C_3 (55 fF), R_4 (15 Ω), and a parallel RC feedback R_5 (15 Ω) and C_4 (55 fF). M_2 is a thick oxide PMOS transistor, while M_3 is a thick oxide NMOS transistor. M_2 and M_3 act as a capacitive load, thus producing a capacitive impedance at the output of the BPD. Thick oxide transistors have higher breakdown voltage levels, thus utilized to sustain the drain voltage supply of 3.3 V to achieve higher linear output power. The capacitive output impedance produces an opposite phase response to the inductive output impedance of the main PA which is dominated by L_2. Parallel RC feedback (R_5 and C_4) extends the capacitive response over a large bandwidth, thus producing a broadband phase cancellation, resulting in broadband linearity and flat gain responses.

B. PRINCIPLE OF OPERATION

Since the 3rd-order intermodulation product (IMD3) is the main contributor for side lobe spectral regrowth in a PA, pre-distortion is one of the techniques customarily utilized to minimize it. Commonly, this is realized through the instigation of a distortion characteristic that is opposite to the PA's distortion. If the pre-distorter generates an IMD3 that is equal in magnitude but out-of-phase to that of the main PA, then an ideal IMD3 cancellation is achieved. Fig. 3 depicts the concept of pre-distortion in a block diagram [23].

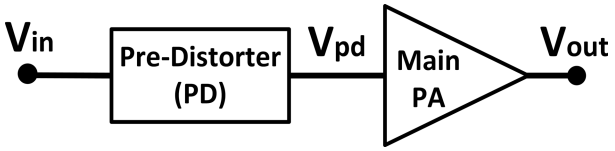

FIGURE 3. Concept of pre-distortion.

Referring to Fig. 3, the following power series expression delineates the operation of the pre-distortion when integrated with the PA:

$$f(x) = \sum_{n=0}^{\infty} a_n xn \tag{1}$$

$$V_{\text{out}} = a_0 + a_1 V_{\text{pd}} + a_2 V_{\text{pd}}^2 + a_3 V_{\text{pd}}^3 \tag{2}$$

$$V_{\text{pd}} = b_0 + b_1 V_{\text{in}} + b_2 V_{\text{in}}^2 + b_3 V_{\text{in}}^3 \tag{3}$$

where V_{out} is the output voltage of the main PA, V_{pd} is the output voltage of the pre-distorter, V_{in} is the input voltage of the RF signal, and a_{n} and b_{n} are the gain terms of the pre-distorter and main PA respectively.

By exploiting this concept, the proposed BPD is capable of achieving the IMD3 cancellation across a wide frequency range. Inherently, the BPD generates a 3rd-order component which is equal in magnitude but 180° out-of-phase in contrast to the main PA's 3rd-order component. Referring to Fig. 1 and substituting a_{n} and b_{n} from (2) and (3) with parameters from the circuit, the following power series expansion elucidates the interrelation of the BPD's and main PA's IMD3 products:

$$V_{\text{main}} = -g_{\text{m6,1}} Z_{\text{main,1}} V_{\text{bpd}} - g_{\text{m6,2}} Z_{\text{main,2}} V_{\text{bpd}}^2 - g_{\text{m6,3}} Z_{\text{main,3}} V_{\text{bpd}}^3 \tag{4}$$

$$V_{\text{bpd}} = -g_{\text{m4,1}} Z_{\text{bpd,1}} V_{\text{in}} - g_{\text{m4,2}} Z_{\text{bpd,2}} V_{\text{in}}^2 - g_{\text{m4,3}} Z_{\text{bpd,3}} V_{\text{in}}^3 \tag{5}$$

where V_{main} is the output voltage of the main PA, V_{bpd} is the output voltage of the BPD, V_{in} is the input voltage, $Z_{main,n}$ is the n[th]-order output impedance of the main PA, $Z_{bpd,n}$ is the n[th]-order output impedance of the BPD, $g_{m4,n}$ is the n[th]-order transconductance of M_4 and $g_{m6,n}$ is the n[th]-order transconductance of M_6.

Considering only the fundamental and 3[rd]-order components, and substituting (5) into (4), we'll obtain:

$$V_{main} = [-(g_{m6,1}Z_{main,1})(-g_{m4,1}Z_{bpd,1}V_{in} - g_{m4,3}Z_{bpd,3}V_{in}^3)] - [(g_{m6,3}Z_{main,3})(-g_{m4,1}Z_{bpd,1}V_{in} - g_{m4,3}Z_{bpd,3}V_{in}^3)]^3 \quad (6)$$

Solving (6) and nullifying the 3[rd]-order interaction components:

$$(g_{m6,1}Z_{main,1})(g_{m4,3}Z_{bpd,3}) + (g_{m6,3}Z_{main,3})(g_{m4,1}Z_{bpd,1})^3 = 0 \quad (7)$$

$$g_{m4,3}Z_{bpd,3} = \frac{-(g_{m6,3}Z_{main,3})(g_{m4,1}Z_{bpd,1})^3}{g_{m6,1}Z_{main,1}} \quad (8)$$

normalizing (8) in the subject of the linear fundamental gain, $g_{m6,1}Z_{main,1}/(g_{m4,1}Z_{bpd,1})^3$, yields:

$$g_{m4,3}Z_{bpd,3} = -g_{m6,3}Z_{main,3} \quad (9)$$

which is equivalent to:

$$A_{v,bpd,3} = -A_{v,main,3} \quad (10)$$

From (10), it can be concluded that to achieve IMD3 cancellation, the 3[rd]-order component of the BPD needs to achieve an opposite response in contrast to the 3[rd]-order component of the main PA. This can be viewed in terms of opposite amplitude-modulation to amplitude-modulation (AM-AM) and amplitude-modulation to phase-modulation (AM-PM) responses referring to the fundamental component [24]. Therefore, the fundamental gain component for the BPD and main PA required to be 180° out-of-phase response too, as given in (11):

$$A_{v,bpd} = -A_{v,main} \quad (11)$$

Both $Z_{bpd,3}$ and $Z_{main,3}$ in (9) are in the form of complex numbers, in where the real part of $Z_{bpd,3}$ is acquired through the resistances from the feedback (R_4 and R_{o3}) while, the imaginary part is contributed by C_3, C_4, and C_5. On the other hand, the real part for $Z_{main,3}$ is determined by M_6's output resistance (R_{o6}), and the imaginary part is contributed by L_2. Fig. 4(a) and Fig. 4(b) depict the small signal equivalent circuits of the BPD and the main PA, respectively. The gate-source capacitance of M_6, (C_{gs6}) is evaluated as a load of BPD. Based on the small-signal equivalent circuits, the BPD's and main PA's gain are derived. From the

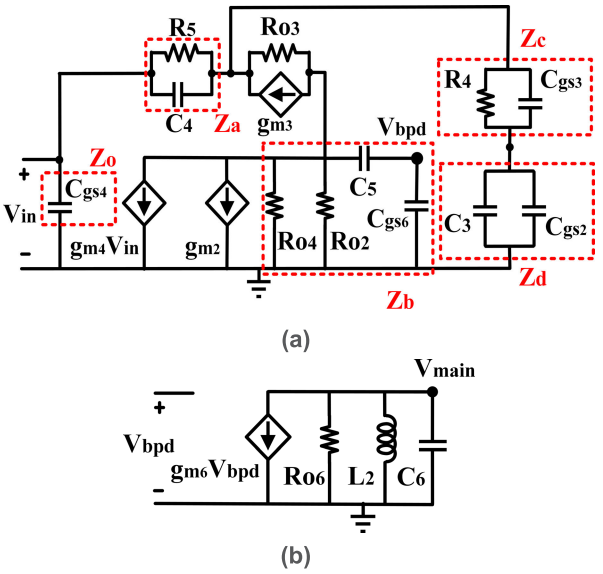

FIGURE 4. Small signal equivalent circuits. (a) BPD. (b) Main PA.

derivation, it is descried that the BPD's voltage gain, Av_{bpd} expresses a capacitive response as in (12) as shown at the bottom of this page, while the main PA's voltage gain, Av_{main} expresses an inductive response as in (18). A positive phase response is observed in (12) due to the dominance of g_{m4} and at the same time, a negative phase response is observed in (18) due to dominance of the g_{m6}. Av_{bpd} is expressed as in (12), where;

$$Z_o = \frac{1}{j\omega C_{gs4}} \quad (13)$$

$$Z_a = \frac{R_5}{1 + j\omega R_5 C_4} \quad (14)$$

$$Z_b = \frac{R_{o2}R_{o4}(C_{gs6} + C_5)}{(R_{o2} + R_{o4} + j\omega C_5 R_{o2}R_{o4})C_{gs6} + C_5(R_{o2} + R_{o4})} \quad (15)$$

$$Z_c = \frac{R_4}{1 + j\omega C_{gs3}R_4} \quad (16)$$

$$Z_d = \frac{1}{j\omega(C_{gs2} + C_3)} \quad (17)$$

The g_{m2}, g_{m3}, and g_{m4} are the transconductance, R_{o2}, R_{o3}, and R_{o4} are the output resistance, and C_{gs2}, C_{gs3}, and C_{gs4} are the gate-source capacitance of transistors M_2, M_3, and M_4 respectively. C_{gs6} is the gate-source capacitance of transistor M_6. Meanwhile Av_{main} is:

$$A_{v,main} = \frac{-g_{m6}(j\omega L_2 R_{o6})}{R_{o6} + j\omega L_2 - (\omega^2 L_2 C_6 R_{o6})} \quad (18)$$

where g_{m6} is the transconductance and R_{o6} is the output resistance of transistor M_6.

$$A_{v,bpd} = \frac{g_{m4}\left[(g_{m3}Z_bZ_oR_{o3}(Z_c + Z_d)) + ((g_{m2} + g_{m3})(Z_a + Z_c + Z_d + Z_o)R_{o3} + g_{m2}Z_b(Z_c + Z_d)(Z_o + Z_a))\right]}{[Z_o(Z_c + Z_d)(g_{m3}R_{o3} - g_{m2}Z_b)]} \quad (12)$$

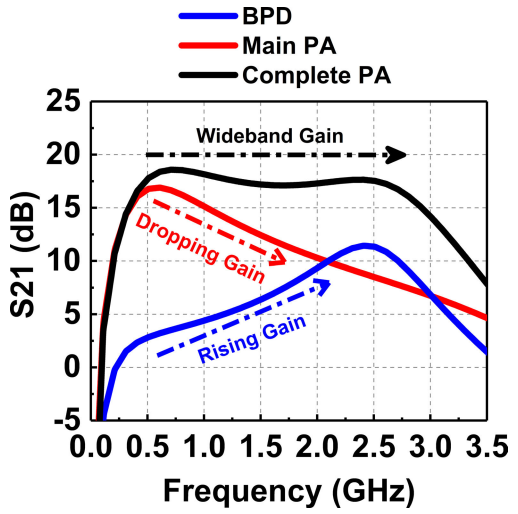

FIGURE 5. The gain response of the BPD-PA across frequency.

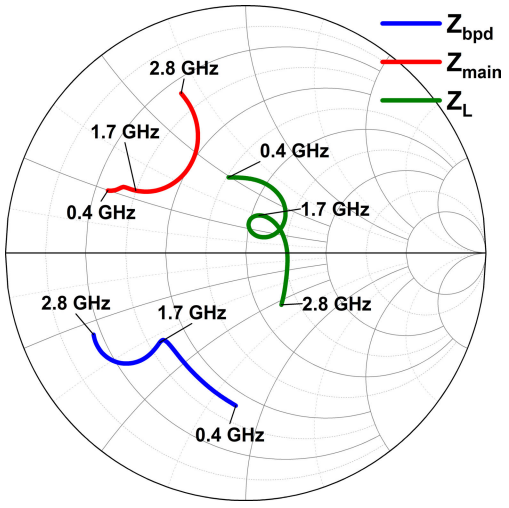

FIGURE 6. Location of impedance points of all stages across frequency.

The relationship between Av and S21 is given as follows:

$$S_{21} = A_v \frac{2Z_{in}}{Z_{in} + Z_o} \tag{19}$$

where Z_o is 50 Ω in our work, Z_{in} is the input impedance of the each stages. Utilizing (19), the frequency response in terms of S_{21} is given in Fig. 5 for the BPD, main and the complete wideband linearized PA.

The wideband operation of the BPD-PA is established by utilizing the gain compensation technique between the BPD and main PA stages. As shown in Fig. 5, the BPD produces a rising gain across frequency, while the main PA produces a descending gain across frequency. The capacitive response of the BPD generates high gain at a higher frequency band. In contrast, the inductive response of the main PA generates high gain at a lower frequency band. The gain compensation of both stages generates a wide frequency bandwidth from 0.4 to 2.8 GHz.

The main PA's gain magnitude and phase are dominated by L_2 thus, exhibiting an inductive response as expressed in (18). On the other hand, the BPD is constructed to be capacitive, which is dominated by C_3, C_4, and C_5 as expressed from (12) to (17). Therefore, the countervailing of the main PA's inductive effect by the BPD's capacitive output leads to a wideband distortion cancellation from 0.4 GHz to 2.8 GHz. The simulated locations of Z_{bpd}, Z_{main}, and Z_L are delineated in Fig. 6. As aforementioned, it can be observed that the main PA's impedance is inductive, while the BPD's impedance is capacitive. The load impedance after integration of the BPD-PA and matching networks is shifted closer to 50 Ω in where it provides an optimum flat broadband gain (S_{21}) across the operating frequency. The OMN is also designed

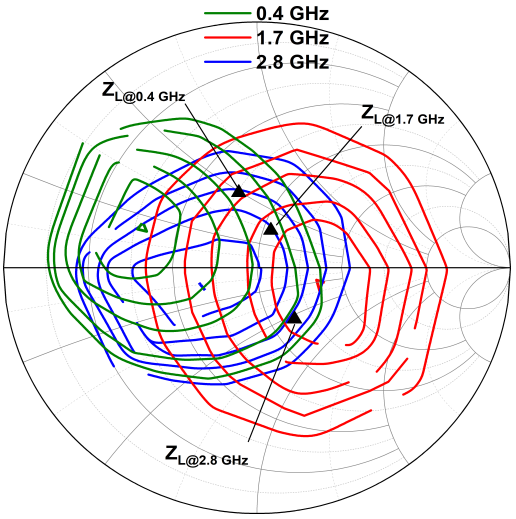

FIGURE 7. Load-pull simulation result of the BPD-PA at output power of 28 dBm across the frequency. The output power contour is plotted in 1 dB step.

to achieve an optimum output power across frequency points and thus, a load-pull simulation has been performed as shown in Fig. 7. The contour is plotted with a 1 dB step up to maximum output power of 28 dBm. Here, it can be observed that Z_L of Fig. 6 is located at the range of 24 to 27 dBm.

Furthermore, referring to (20) as shown at the bottom of this page, the cancellation after linearization observed that the C_{gs4} from M_4 (referring to Z_o) is the only capacitance effect that still exists. This shows that the source of the non-linearity has been reduced to C_{gs4} which is less significant as compared to the parasitic elements inherited within the main PA. This mitigates the amplitude and phase deviation that ensued

$$A_{v,\,after} = \frac{-g_{m4}g_{m6}R_{o6}\left[g_{m3}\left(R_{24}R_{o3}R_4Z_o\right) + \left[\left(g_{m2}+g_{m3}\right)\left(R_4+R_5+Z_o\right)R_{o3}\right] + g_{m2}\left(R_{24}\right)\left(R_5+Z_o\right)\right]}{Z_oR_4 + \left(g_{m3}R_{o3} - g_{m2}\left(R_{24}\right)\right)} \tag{20}$$

where $R_{24} = R_{02} \| R_{o4}$

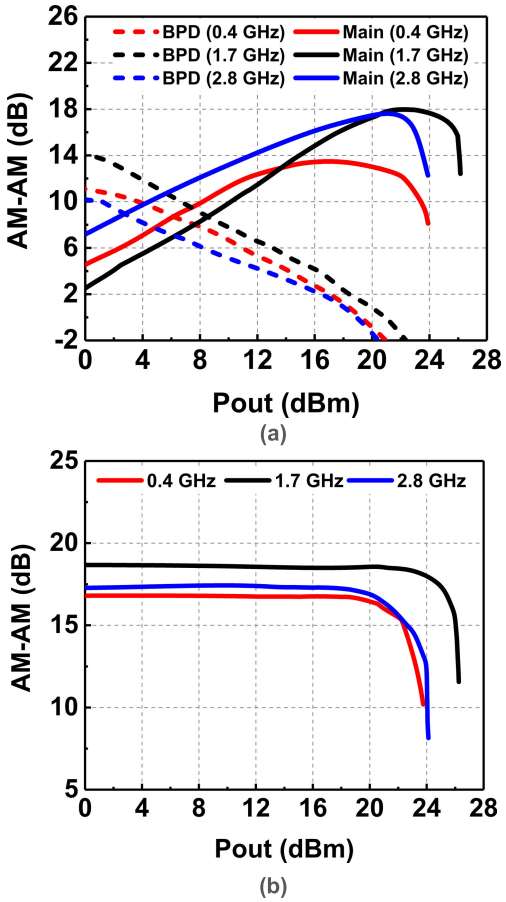

FIGURE 8. Simulated AM-AM responses. (a) Opposite AM-AM response of the BPD and main PA. (b) AM-AM response after integrating the BPD and main PA.

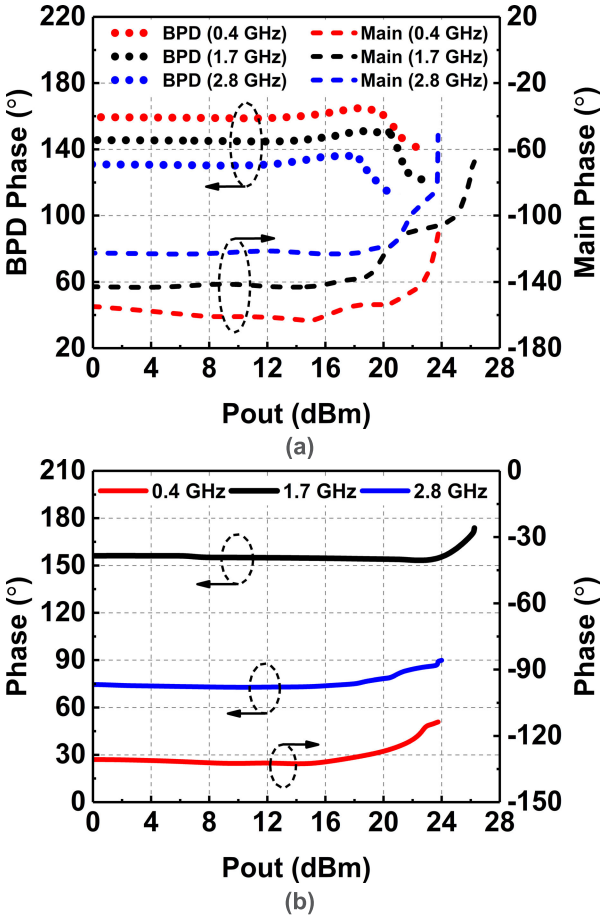

FIGURE 9. Simulated AM-PM responses. (a) Opposite AM-PM response of the BPD and main PA. (b) AM-PM response after integrating the BPD and main PA.

the flat AM-AM and AM-PM responses across the output power, thus conforming broad bandwidth and linearity across frequency.

Fig. 8(a) illustrates the simulated opposite AM-AM response produced by the BPD and main PA. The BPD produces a compressing AM-AM response which is opposite to the expanding AM-AM response of the main PA across output power. A flat AM-AM response and increased gain have been achieved up to near compression point across the output power after the two stages have been combined as shown in Fig. 8(b). By considering a deviation of ±0.5 dB, a flat gain is achieved across output power of 18.8 dBm at 0.4 GHz, 23 dBm at 1.7 GHz, and 20.1 dBm at 2.8 GHz, ahead of non-linear compression.

Also, Fig. 9(a) illustrates the simulated opposite AM-PM response of the BPD-PA, where substantial phase deviation across output power is observed in the main PA before the implementation of the BPD. As depicted in Fig. 9(b), the BPD integration abates the phase deviation, resulting in a phase deviation of ±4° up to output power of 23 dBm at 1.7 GHz (±3° for 19.8 dBm at 0.4 GHz, ±4° for 20.1 dBm at 2.8 GHz) conforming that the PA has been linearized. An AM-PM distortion of more than 5° is equivalent to gain compression of more than 1 dB [25].

The BPD's effectiveness is further validated through the IMD3 and power spectral density (PSD) simulations. The IMD3 simulation has been conducted across the frequency and its result is presented before and after the BPD integration in Fig. 10. By adopting the IMD3 specification of −30 dBc, it can be observed that before the BPD's integration the PA fulfills the specification up to 20 dBm output power at 1.7 GHz (16.5 dBm at 0.4 GHz, 18 dBm at 2.8 GHz). After employing the BPD, it can be perceived that the IMD3 has been enhanced in where the linear output power which fulfills the specification is extended up to 24 dBm at 1.7 GHz (22.3 dBm at 0.4 GHz, 21.7 dBm at 2.8 GHz). The enhanced linear output power validates that the cancellation of the IMD3 product does occur after the BPD's integration with the main PA.

Moreover, the PSD simulation was carried out at 1.7 GHz before and after the BPD integration. It can be observed in Fig. 11 that the spectral regrowth at the sideband frequency is −25 dBc at 24 dBm output power before the implementation of the BPD. After the implementation of the BPD, the spectral regrowth is significantly mitigated to −38 dBc at the same output power condition of 24 dBm in where it satisfies the 20 MHz LTE modulation signal requirement.

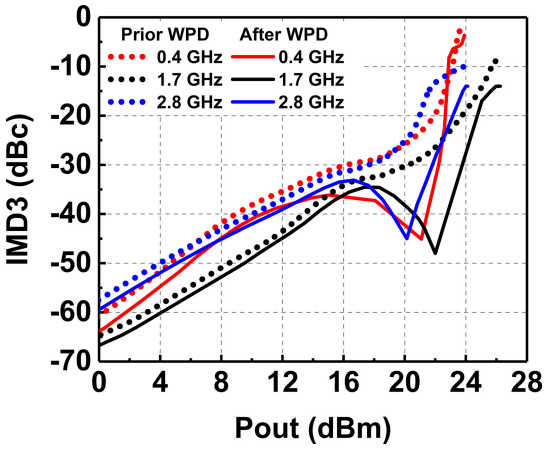

FIGURE 10. Simulated IM3D performance before and after BPD integration.

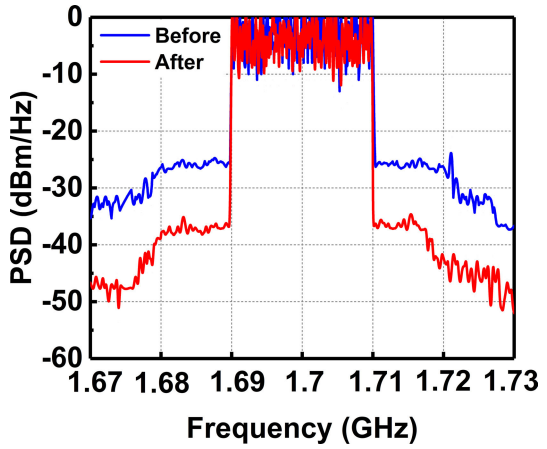

FIGURE 11. Simulated PSD of the PA before and after BPD integration.

The PSD simulation also validates the BPD's capability in reducing the spectral regrowth when tested with modulated signals.

III. MEASUREMENT RESULTS

The proposed BPD-PA is fabricated in a 180 nm CMOS process and integrated on Roger's RO4000 dielectric materials with FR4 cores, two-layer circuit board. The photomicrograph of the BPD-PA which consumes an area of 1.69 mm2 was captured using the eVue digital imaging system. The BPD-PA together with the PCB implementation is illustrated in Fig. 12.

Fig. 13 depicts the simulated and measured S-parameters and stability factor of the designed BPD-PA. In measurement, the maximum small signal gain, S_{21} achieved is 16.5 dB. The BPD-PA has an operating bandwidth of 2.4 GHz, from 0.4 to 2.8 GHz. The input return loss, S_{11} and output return loss, S_{22} are less than −10 dB across the aforementioned frequency bandwidth. The BPD-PA also exhibits unconditionally stable characteristics across the operating bandwidth as depicted in Fig. 13. The continuous wave (CW) measured performance at different frequencies for the designed BPD-PA is illustrated in Fig. 14. When measured at 1.7 GHz, it achieves a saturated

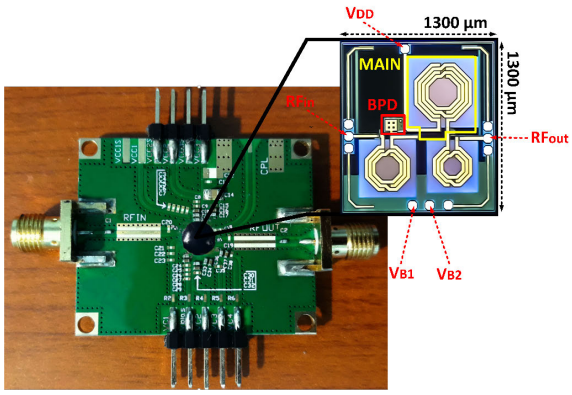

FIGURE 12. CMOS BPD-PA mounted on Roger's RO4000/FR4 PCB.

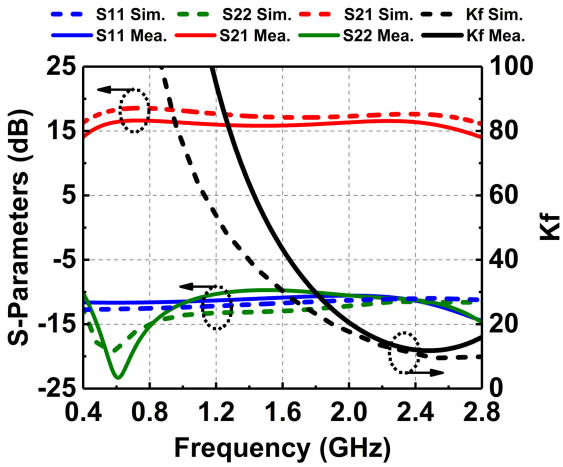

FIGURE 13. S-parameters and stability performance of the BPD-PA.

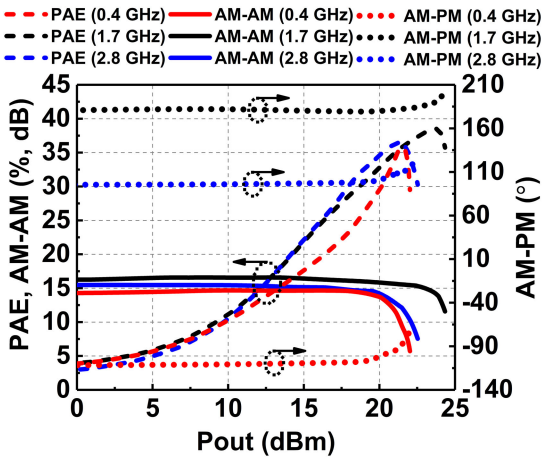

FIGURE 14. The BPD-PA's CW measured performance at 0.4 GHz, 1.7 GHz and 2.8 GHz.

output power of 24.3 dBm with a corresponding power gain of 16.5 dB. The peak PAE achieved is 38.7% at 23.7 dBm output power. At 0.4 and 2.8 GHz, the BPD-PA can deliver a saturated output power of 22 and 22.5 dBm with corresponding peak PAE of 36 and 37% respectively.

Also, the AM-AM and AM-PM performances are measured across the frequency as depicted in Fig. 14. It can be

TABLE 1. Proposed CMOS BPD-PA'S summary and work comparison.

Tech. (nm)	VDD (V)	Freq. (GHz)	Bandwidth (GHz)	Max Pout (dBm)	Linear Pout (dBm)	Peak PAE (%)	Linear PAE	Channel Bandwidth	Ref.
130 CMOS	1.2	2.8 - 6	3.2	11-14	7.5-11.5	25-36	15-25	-	[15]
180 CMOS	3.3	2.1 – 4.5	2.4	19-22	16.5	31-43.7	35	5 MHz WCDMA	[16]
180 SOI CMOS	2.5	1.9-2.7	0.8	27.5-28.5	21.5-22.4	36-46.8	18.5-21.7	20 MHz LTE	[17]
45 SOI CMOS	2.4	2.9-4.3	1.4	24.6-25.3	18.6-19.3	24-30	20-25.3	10 MHz OFDM	[18]
65 CMOS	2.4	1.4-2.5	0.9	20-21.7	14.1-15.1	25-38.1	15.7-23.7	20 MHz OFDM	[19]
180 CMOS	2	0.7-1.0	0.3	13.6*	6.7	25.5	15.4	5 MHz LTE	[20]
180 CMOS	5	4.9-5.8	0.9	29-31	19.8	15-25	5	802.11ac WLAN OFDM	[21]
180 CMOS	3.4	1.6-1.9	0.3	26-27.6	25.2	28-35	32	10 MHz WCDMA	[22]
65 CMOS	2.5	1.95/2.4	Dual-Band	31.8/32.0	28.0/23.7	29/32	18/10	WCDMA/WLAN	[26]
180 CMOS	**3.3**	**0.4 – 2.8**	**2.4**	**22.1-24.3**	**19.4-21.0**	**36.1-38.6**	**27.0-34.6**	**20 MHz LTE**	**This Work**

P1dB

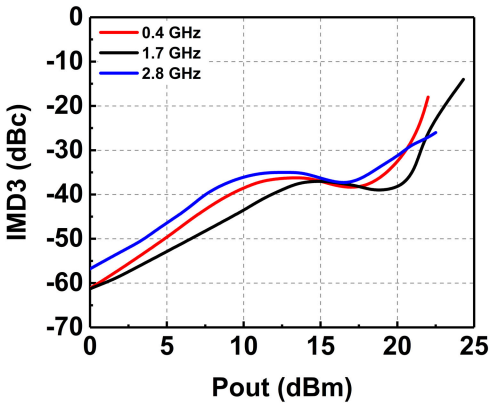

FIGURE 15. The BPD-PA's measured IMD3 performance at 0.4 GHz, 1.7 GHz and 2.8 GHz.

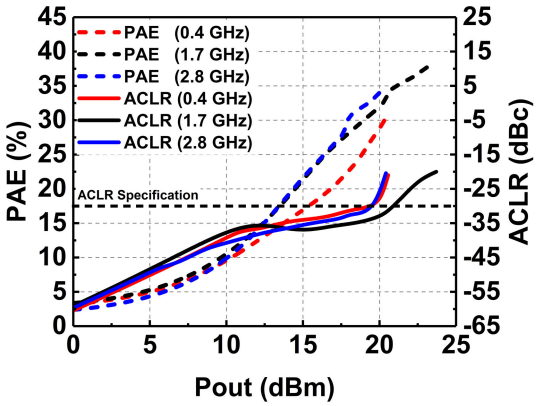

FIGURE 16. The BPD-PA's 20 MHz LTE signal measured performance at 0.4 GHz, 1.7 GHz and 2.8 GHz.

observed that the AM-AM deviation varies by ±0.5 dB up to 21 dBm of output power at 1.7 GHz. For both 0.4 and 2.8 GHz, the AM-AM deviation of ±0.5 dB is achieved up to output power of 19 dBm. An AM-PM deviation of ±4° is achieved up to output power of 22.4 dBm at 1.7 GHz, 19.4 dBm at 0.4 GHz, and 19.6 dBm at 2.8 GHz. Meanwhile, Fig. 15 depicts the measured IMD3 in where it is observed that IMD3 is below −30 dBc up to 21.6 dBm at 1.7 GHz. At both 0.8 and 2.8 GHz, the IMD3 is below −30 dBc up to 20.5 dBm. Further, the BPD-PA has been tested with 20 MHz LTE modulation signal with 7.88 dB PAPR at different frequencies where an ACLR specification value of less than −30 dBc is desired for maximum linear output power. Referring to Fig. 16, the ACLR of the BPD-PA meets the specification up to 21 dBm output power at 1.7 GHz (19.4 dBm at 0.4 GHz, 19 dBm at 2.8 GHz). It can be observed that the ACLR is extended across output power of more than 14 dBm.

This is the region where the effect of the BPD on distortion cancellation is occurring. The BPD extends the linear output power by fulfilling the ACLR specification at high output power levels. Fig. 17 illustrates the current consumption of the BPD-PA with respect to the output power and ACLR at 1.7 GHz. It can be observed that the current consumed by

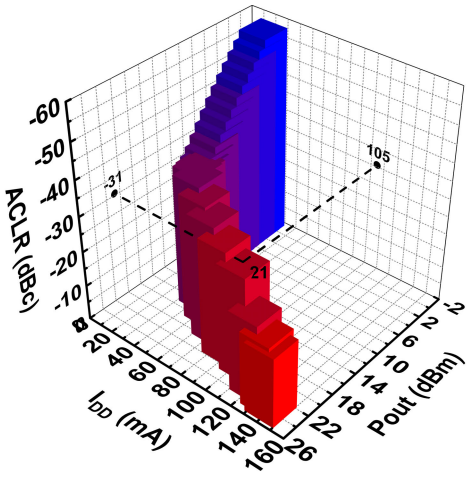

FIGURE 17. Current consumption of the BPD-PA with respect to output power and ACLR (105 mA at linear P_{out} of 21 dBm).

the BPD-PA is 105 mA at maximum linear output power of 21 dBm where the ACLR specification is met. The resulting power consumption is 347 mW at the maximum linear output power. Since the PCB has a good grounding structure, it allows the current to quickly flow to ground without heating the chip which further increases the efficiency.

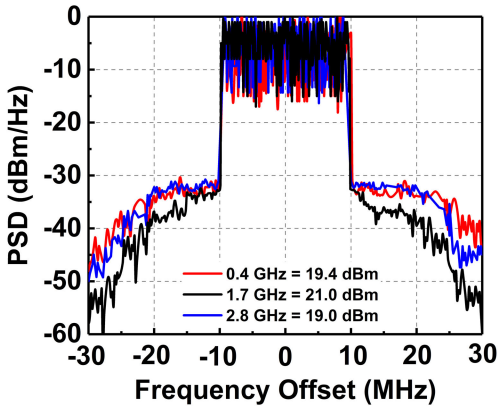

FIGURE 18. Measured power spectral density of the BPD-PA across the operating frequency.

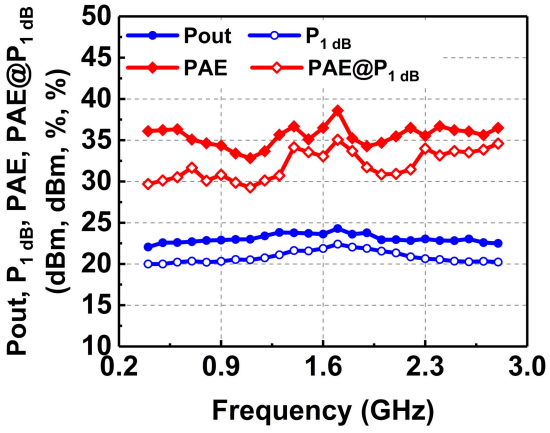

FIGURE 19. Measured performance of the CMOS BPD-PA across bandwidth.

Besides that, Fig. 18 shows the normalized PSD of the BPD-PA across the frequency under 20 MHz LTE signal. It can be seen that the sidebands of the PSD are kept below −30 dBm/Hz which indicate the fulfillment of the spectral specification. Fig. 19 depicts the performance of the BPD-PA across the aforementioned frequency bandwidth. Across the frequency bandwidth, the maximum output power varies from 22 dBm to 24 dBm while the peak PAE varies from 33% to 38.6%. The output power at 1 dB compression point ($P_{1\ dB}$) and its corresponding PAE are also plotted in Fig. 19. As can be seen, the $P_{1\ dB}$ achieved a minimum and maximum values of 20 dBm and 22.4 dBm respectively, followed by PAE@$P_{1\ dB}$ values of 29.7% and 35.1% respectively. Table 1 summarizes the performance of the proposed BPD-PA in comparison with recent published works.

IV. CONCLUSION

A broadband BPD-PA operating from 400 MHz to 2.8 GHz has been proposed. The integrated BPD resolves the AM-AM and AM-PM deviation faced by the main PA thus contributes to the linearity enhancement. Compared to APDs which utilize inductors that result in narrowband due to dependency on the Q factor, our BPD consists of only MOS transistors, resistors, and capacitors which contribute to the wideband operation. It is also area-efficient since the use of inductors is eradicated albeit a little more power consumed as compared to passive loads. A flat AM-AM response and a less than 4° AM-PM deviation have been achieved across output power for a wide frequency range. With CW signal, the BPD-PA achieved a maximum output power of 24.3 dBm with a corresponding power gain of 16.5 dB as well as a peak PAE of 38.6% at 1.7 GHz. The BPD-PA also fulfills the 20 MHz LTE signal's ACLR requirement of −30 dBc for output power up to 21 dBm. The designed BPD-PA serves to be a good solution to be implemented in broadband transmitters, with a reduced trade-off in PAE.

REFERENCES

[1] A. Vasjanov and V. Barzdenas, "A review of advanced CMOS RF power amplifier architecture trends for low power 5G wireless networks," *Electronics*, vol. 7, no. 271, pp. 1–17, Oct. 2018.

[2] A. Hajimiri, "Next-generation CMOS RF power amplifiers," *IEEE Microw. Mag.*, vol. 12, no. 1, pp. 38–45, Feb. 2011.

[3] A. M. Niknejad, D. Chowdhury, and J. Chen, "Design of CMOS power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1784–1796, Jun. 2012.

[4] T. Johansson and J. Fritzin, "A review of watt-level CMOS RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 1, pp. 111–124, Jan. 2014.

[5] A. H. Issa, S. M. Ghayyib, and A. S. Ezzulddin, "Toward a fully integrated 2.4GHz differential pair class-E power amplifier using on-chip RF power transformers for Bluetooth systems," *AEU Int. J. Electron. Commun.*, vol. 69, no. 1, pp. 182–187, Jan. 2015.

[6] G. Jeong, B. Koo, T. Joo, and S. Hong, "Linearization of RF CMOS power amplifiers," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Aug. 2015, pp. 154–156.

[7] S. Hu, S. Kousai, and H. Wang, "A broadband mixed-signal CMOS power amplifier with a hybrid Class-G Doherty efficiency enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

[8] S. N. Ali, P. Agarwal, J. Baylon, S. Gopal, L. Renaud, and D. Heo, "A 28GHz 41%-PAE linear CMOS power amplifier using a transformer-based AM-PM distortion-correction technique for 5G phased arrays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 406–408.

[9] A. Dani, M. Roberg, and Z. Popovic, "PA efficiency and linearity enhancement using external harmonic injection," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4097–4106, Dec. 2012.

[10] A. Katz, J. Wood, and D. Chokola, "The evolution of PA linearization: From classic feedforward and feedback through analog and digital predistortion," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 32–40, Feb. 2016.

[11] U. R. Jagadheswaran, H. Ramiah, P.-I. Mak, and R. P. Martins, "A 2-μm InGaP/GaAs class-J power amplifier for multi-band LTE achieving 35.8-dB gain, 40.5% to 55.8% PAE and 28-dBm linear output power," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 200–209, Jan. 2016.

[12] M. Vigilante and P. Reynaert, "A wideband class-AB power amplifier with 29–57-GHz AM–PM compensation in 0.9-V 28-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1288–1301, May 2018.

[13] Y.-Y. Huang, H. Jeon, Y. Yoon, W. Woo, C.-H. Lee, and J. S. Kenney, "An ultra-compact, linearly-controlled variable phase shifter designed with a novel RC poly-phase filter," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 2, pp. 301–310, Feb. 2012.

[14] Y.-Y. Huang, W. Woo, H. Jeon, C.-H. Lee, and J. S. Kenney, "Compact wideband linear CMOS variable gain amplifier for analog-predistortion power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 68–76, Jan. 2012.

[15] A. Basaligheh, P. Saffari, M. Taherzadeh-Sani, and F. Nabki, "A highly efficient and linear broadband common-drain CMOS power amplifier with transformer-based input-matching network," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 12, pp. 814–816, Dec. 2015.

[16] Y. Dong, L. Mao, and S. Xie, "Fully integrated class-J power amplifier in standard CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 1, pp. 64–66, Jan. 2017.
[17] B. Francois and P. Reynaert, "Highly linear fully integrated wideband RF PA for LTE-advanced in 180-nm SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 649–658, Feb. 2015.
[18] V. Vorapipat, C. Levy, and P. Asbeck, "2.8 a class-G voltage-mode Doherty power amplifier," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 46–47.
[19] Z. Bai, A. Azam, and J. S. Walling, "A frequency tuneable switched-capacitor PA in 65nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 295–298.
[20] X. Yu, M. Wei, Y. Song, Z. Wang, and B. Chi, "A PAPR-aware dual-mode subgigahertz CMOS power amplifier for short-range wireless communication," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, pp. 44–48, Jan. 2016.
[21] J.-H. Tsai, "Design of a 5.2-GHz CMOS power amplifier using TF-based 2-Stage dual-radial power splitting/combining architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3690–3699, Oct. 2019.
[22] C. Zhao, H. Liu, Y. Wu, and K. Kang, "Analysis and design of CMOS Doherty power amplifier based on voltage combining method," *IEEE Access*, vol. 5, pp. 5001–5012, 2017.
[23] E. Uthirajoo, H. Ramiah, J. Kanesan, and A. W. Reza, "Wideband LTE power amplifier with integrated novel analog pre-distorter linearizer for mobile wireless communications," *PLoS ONE*, vol. 9, no. 7, pp. 1–16, Jul. 2014.
[24] A. Katz, R. Gray, and R. Dorval, "Truly wideband linearization," *IEEE Microw. Mag.*, vol. 10, no. 7, pp. 20–27, Dec. 2009.
[25] R. S. Nitesh, J. Rajendran, H. Ramiah, and A. A. Manaf, "A 700MHz to 2.5GHz cascode GaAs power amplifier for multi-band pico-cell achieving 20dB gain, 40dBm to 45dBm OIP3 and 66% peak PAE," *IEEE Access*, vol. 6, pp. 818–829, 2018.
[26] K. Onizuka, H. Ishihara, M. Hosoya, S. Saigusa, O. Watanabe, and S. Otaka, "A 1.9 GHz CMOS power amplifier with embedded linearizer to compensate AM-PM distortion," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1820–1827, Aug. 2012.

SELVAKUMAR MARIAPPAN (Student Member, IEEE) is currently pursuing the Ph.D. degree in microelectronics with Universiti Sains Malaysia (USM), Pinang. He is also a Postgraduate Intern with Silterra Malaysia Sdn. Bhd. His current research interest includes CMOS RF power amplifier design.

JAGADHESWARAN RAJENDRAN (Senior Member, IEEE) received the B.Eng. (Hons.) degree from Universiti Sains Malaysia, the M.Eng. degree (telecommunications) from Malaysia Multimedia University, and the Ph.D. degree in RFIC design from the University of Malaya. He is currently serving as a Senior Lecturer with the Collaborative Microelectronic Design Excellence Centre (CEDEC) and the School of Electrical and Electronic Engineering, Universiti Sains Malaysia, working on CMOS analog IC design, CMOS radio frequency (RF), IC design, and monolithic microwave integrated circuit (MMIC) design. He was with Laird Technologies as an Antenna Designer followed by serving Motorola Technology, from 2005 to 2007, as a Research and Development Engineer, working on mobile phone receiver system. In 2008, he joined Broadcom as a MMIC Designer, working mainly on GaAs based power amplifier, LNA, and gain blocks, where he was elevated to the rank of Principal Engineer later. In 2015, he joined Silterra Malaysia, working on CMOS RFIC design and device modelling. Till date, he has published more than 30 research articles, mainly journals and holds one US patent. He was a recipient of the IEEE Circuit and System Outstanding Doctoral Dissertation Award, in 2015. He served as the Chairman for IEEE ED/MTT/SSC Penang Chapter, in 2011 and 2018, respectively.

YUSMAN M. YUSOF received the B.Eng. degree in electronic and computer engineering from Universiti Putra Malaysia (UPM), in 1999. He is currently working at Silterra Malaysia Sdn. Bhd. focusing on devices characterization and device models development for radio frequency (RF) and electrostatic discharge (ESD).

NORLAILI M. NOH (Senior Member, IEEE) received the B.Eng. degree (Hons.) electrical engineering from Universiti Teknologi Malaysia, the M.Sc. degree in electrical and electronic engineering, and the Ph.D. degree in integrated circuit design from Universiti Sains Malaysia. She is currently an Associate Professor with the School of Electrical and Electronic Engineering, Universiti Sains Malaysia. Her specialization is in analog RFIC design. She is also a Professional Engineer registered with the Board of Engineers Malaysia and a Chartered Engineer registered with the UK Engineering Council.

BINBOGA SIDDIK YARMAN (Life Fellow, IEEE) received the B.Sc. degree from the Technical University of Istanbul, in 1974, the M.Sc. degree from the Stevens Institute of Technology, Hoboken, NJ, USA, in 1977, and the Ph.D. degree from Cornell University, Ithaca, NY, USA, in 1982. He was a member of Technical Staff with the General David Sarnoff Microwave Technology and Research Center (previously RCA Sarnoff Research Center), Princeton, NJ. He served as a Professor and an Administrator for various Universities, including Anadolu University, Middle East Technical University, Istanbul University, Isik University of Turkey, Ruhr University of Germany, Tokyo Institute of Technology of Japan, and Wuhan Technology University of China. He was the Founding President of Isik University, from 1996 to 2004, and served as the Chairman for the Board of Trustees, until 2017. He is currently with Istanbul University and the University of Lincoln, U.K. He is one of the founders of Savronik Group of Companies and serves as the Chairman for the Board of Directors. He has published seven books, such as *Design of Ultra-Wideband Antenna Matching Networks* (Springer, 2008), *Design of Ultra-Wideband Power Transfer Networks* (Wiley, 2010), *Intelligence Based Decision Making* by Nobel Press of Turkey (2014), *Broadband RF and Microwave Amplifiers* (CRC, 2016; this book is translated to Chinese), *Broadband RF and Microwave Amplifiers* (IET, 2019), and *Design of Digital Phase Shifters for Multipurpose Communication Systems* (River Publisher, 2019). He holds four US and nine Turkish Patents. He published numerous articles in the field of microwave engineering, circuit and systems, signal processing, mathematical modeling, and decision making. He was a member of The New York Academy of Sciences, in 1994. He is also an Alexander Von Humboldt Fellow and Salzburg Fellow of USIS. He was selected as the Man of the Year in Science and Technology of Cambridge Biography, U.K., in 1999. He was a recipient of the Young Turkish Scientist Award, in 1986, and the Technology Award of the Scientific and Research Council of Turkey, in 1987.