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# Design and Analysis of Simultaneous Wideband Input/Output Matching Technique for Ultra-Wideband Amplifier

**TO-PO WANG, (Senior Member, IEEE)**
Department of Electronic Engineering, National Taipei University of Technology, Taipei 10608, Taiwan
e-mail: tpwang@ntut.edu.tw

**ABSTRACT** A simultaneous wideband input/output matching technique for ultra-wideband (UWB) low-noise amplifier (LNA) is proposed in this paper. Feedback resistors leading the gate inductors combined with inductive dividers at output ports achieve an extended bandwidth and good input/output return loss. Moreover, *Q*-factor improved vertical solenoid inductors are used in the matching networks for high gain and low noise figure (NF). The proposed matching technique, not only enhances the bandwidth, but also achieves a high gain and a low NF for the fabricated 3.1-10.6-GHz monolithic 180-nm CMOS UWB amplifier. Operating at low supply voltage, the measured power consumption is 18.9 mW, the measured gain of the UWB LNA is 15.02 dB, and the NF is 3.1 dB. Moreover, the measured input/output reflection coefficients $S_{11}$ and $S_{22}$ are lower than −9.4 dB and -15.8 dB, respectively, covering the full-band UWB frequencies. Compared to previously published full-band 3.1-10.6-GHz 180-nm CMOS UWB LNAs, the proposed LNA measurements demonstrate high gain, low NF, low supply voltage, low power dissipation, and good input/output reflection coefficients.

**INDEX TERMS** Low-noise amplifier (LNA), noise figure (NF), ultra-wideband (UWB).

## I. INTRODUCTION

The demand for radio frequency (RF) and high data rate communication systems has led to the use of higher frequencies and larger bandwidths [1]–[11].

While the size of transistors continues to shrink, the supply voltage must be scaled down proportionally, due to the reliability of the gate oxide [5]. However, the low transconductance of the MOSFET at high frequencies affects significantly the design of low voltage and low power RF front-ends. To improve circuit performance, a network for simultaneous wideband input and output matching is proposed in this work. Wideband input matching is achieved by a feedback resistor at the input inductor of the cascode input stage. Moreover, an inductive divider is used at the output of the LNA for a better reflection coefficient $S_{22}$. Using these approaches, the small signal gain and the NF of the UWB LNA covering all UWB frequencies, are improved.

This paper is organized as follows. In Section II, the proposed UWB LNA with wideband input and output matching networks is introduced and design considerations of the bandwidth enhancement technique are presented. Section III provides experimental results and the characterization of the LNA. Finally, conclusions are provided in Section IV.

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## II. PROPOSED MATCHING TECHNIQUE FOR UWB LNA

The operating principles and the performance limitations of several circuit topologies for wideband LNAs are presented. The first topology, shown in Fig. 1(a), uses a resistive termination of the input port to provide an input impedance of 50 Ω. Although this topology attains a good reflection coefficient ($S_{11}$) over the band of interest, the noise performance that is achieved is low.

Fig. 1(b) illustrates the second architecture using a self-biased inverter amplifier with resistive feedback as the first stage of the UWB LNA design [7]. With dual feedback and *LC*-ladder matching network, the architecture provides broadband matching for a common-source amplifier. However, the noise performance is limited because of the input matching network where resistive losses increase the minimum possible noise figure ($NF_{min}$) of the circuit.

The third circuit topology employing a common-gate MOSFET device is shown in Fig. 1(c). The advantage of


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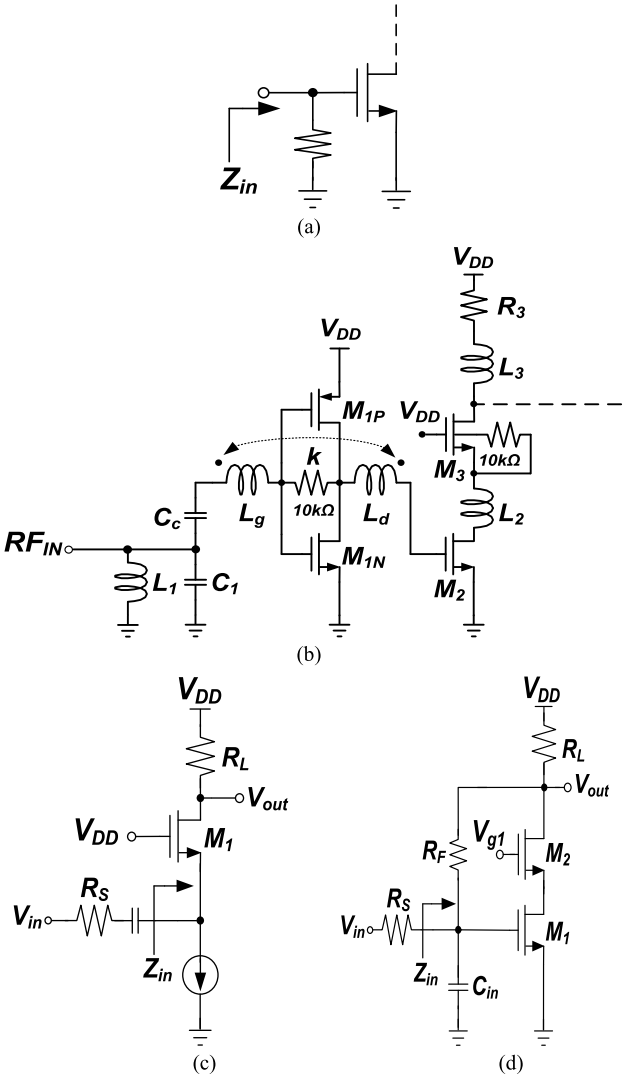


**FIGURE 1.** Circuits with widely used wideband input matching topologies: (a) resistive termination, (b)self-biased inverter amplifier with a feedback resistor, (c)common-gate MOSFET device, (d)resistive shunt-shunt feedback.

common-gate (CG) LNA is its low input impedance, which can easily be adjusted and matched to 50 Ω. Note that the dominant noise source in CMOS devices is channel thermal noise [6], [10]. This source of noise is typically modeled as a shunt current source at the output circuit of the MOSFET. Fig. 1(d) depicts the widely used architecture for UWB LNAs. Based on the cascode configuration and on a resistive shunt-shunt feedback, the architecture allows extending the bandwidth of the LNA [10] and improving the gain, the stability and the isolation between the output and the input.

To enhance the circuit performance of an UWB amplifier in terms of bandwidth, gain, NF, supply voltage, and DC power dissipation, a novel bandwidth enhancement technique (feedback resistors $R_{F1}$, $R_{F2}$, leading gate inductors $L_{g2}$, $L_{g3}$ and inductive dividers $L_{D3}$ and $L_{D4}$ combined with $C_{F2}$ and $R_{F2}$ at output ports) is proposed in this work, as shown in Fig. 2. The

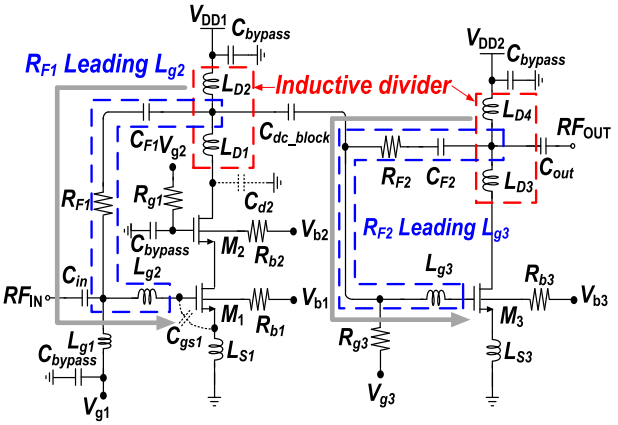


**FIGURE 2.** Circuit topology of the proposed wideband LNA employing the simultaneous wideband input/output matching technique (feedback resistors $R_{F1}$, $R_{F2}$ leading gate inductors $L_{g2}$, $L_{g3}$ and combining with inductive dividers at output ports).

design considerations of the proposed matching technique and application for an UWB amplifier are presented in details as follows.

### A. SIMULTANEOUS WIDEBAND INPUT/OUTPUT MATCHING CONSIDERATIONS

To achieve a high gain, the matching circuit at the input of the LNA is essential. Fig. 3(a) shows a widely used narrowband input matching technique; the input impedance of the circuit can be derived as [12, p. 173]

$$Z_g = s(L_{g1} + L_{S1}) + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_{S1}}{C_{gs1}} \tag{1}$$

where $g_{m1}$ is the device transconductance and $C_{gs1}$ is the parasitic capacitance between the gate and the source terminals of the active device $M_1$. Moreover, the inductors $L_{S1}$ and $L_{g1}$ are selected to resonate with $C_{gs1}$ and to cancel the imaginary part of the input impedance. The value of the $C_{gs1}$ is 150 fF. The values of the $L_{S1}$ and $L_{g1}$ are 0.16 nH and 1.4 nH, respectively. Setting the imaginary part of (1) to zero, the resonance frequency can be expressed as

$$f_{o1} = \frac{1}{2\pi\sqrt{C_{gs1}\left(L_{g1} + L_{S1}\right)}} \tag{2}$$

At matching, the input impedance of the LNA is equal to $Z_o$, the resistance of the signal source. Given that the real part of (1) is equal $Z_o$, it follows that

$$L_{S1} = \frac{Z_o C_{gs1}}{g_{m1}} \tag{3}$$

Therefore, the inductance of $L_{S1}$ can be determined by the parameters $Z_o$, $C_{gs1}$, and $g_{m1}$. Although the input matching network consisting of $L_{S1}$, $L_{g1}$, and $C_{gs1}$ shown in Fig. 3 (a) can be perfectly achieved, the matching is suitable only for a narrowband LNA design. For wideband input matching, resistive shunt-shunt feedback is adopted in regular LNAs, as shown in Fig. 3(b). However, the noise performance and

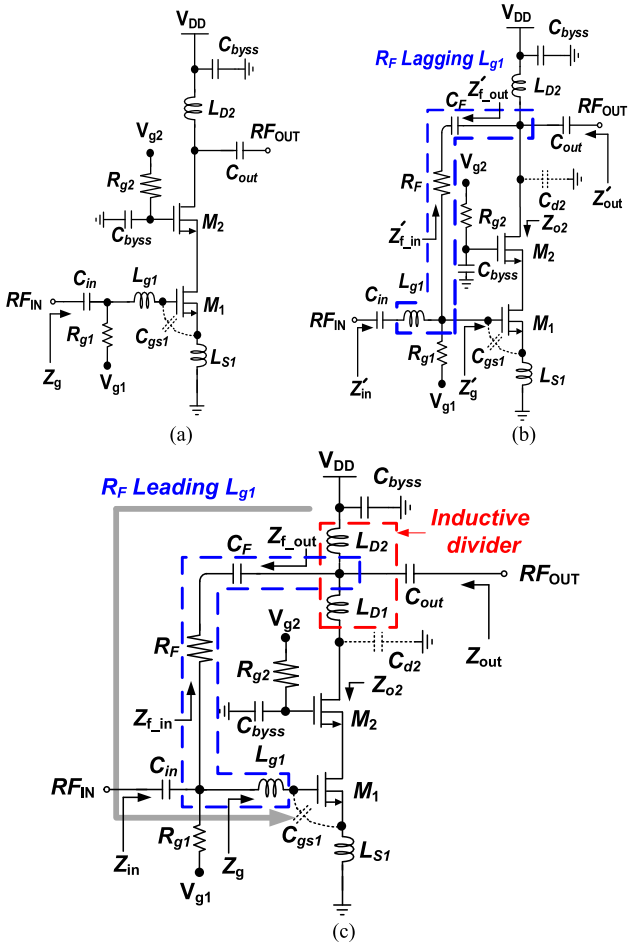


**FIGURE 3.** Circuit topology with (a) narrowband matching, (b) regular matching with $R_F$ lagging $L_{g1}$, without inductive divider at output, and (c) proposed simultaneous wideband input/output matching technique (feedback resistor $R_F$ leading gate inductor $L_{g1}$ and combining with inductive divider at output port).

the gain of the circuit in Fig. 3(b) are still limited, compared to Fig. 3(a).

To further improve the input/output reflection coefficients and small-signal gain, a cascode resistive shunt-shunt feedback with a bandwidth enhancement technique (feedback resistors $R_F$ leading gate inductor $L_{g1}$ and combining with inductive dividers at output port) is proposed in this work, as shown in Fig. 3(c). The input impedance of the proposed circuit can be written as $Z_{in} = Z_g//Z_{f\_in}$, where $Z_g$ is the input impedance of the amplifier stage without the feedback circuit, and $Z_{f\_in}$ is the impedance looking into the feedback resistor $R_F$. The impedance $Z_g$ can be written as (1), and the passives $L_{g1}$, $L_{S1}$, $C_{gs1}$ are determined by (2)-(3).

The impedance $Z_{f\_in}$ can be formulated as

$$Z_{f\_in} = \frac{R_F + \left[sL_{D2}||\left(sL_{D1} + \frac{1}{sC_{d2}}\right)\right]}{1 + \frac{g_{m1}\left[sL_{D2}||\left(sL_{D1}+\frac{1}{sC_{d2}}\right)\right]}{[s^2C_{gs1}(L_{g1}+L_{S1})+sg_{m1}L_{S1}+1][s^2C_{d2}(L_{D1}+L_{D2})+1]}} \quad (4)$$

where $C_{gs1}$ and $C_{d2}$ are the parasitic capacitors. In a typical design, $s^2C_{gs1}\left(L_{g1}+L_{S1}\right) + sg_{m1}L_{S1} \ll 1$, $s^2C_{d2}(L_{D1} + L_{D2}) \ll 1$, and $g_{m1}\left[sL_{D2}||\left(sL_{D1}+\frac{1}{sC_{d2}}\right)\right] \gg 1$ are satisfied. Consequently, the expression of $Z_{f\_in}$ in (4) can be approximated by (5)

$$Z_{f\_in} = \frac{R_F}{g_{m1}\left[sL_{D2}||\left(sL_{D1}+\frac{1}{sC_{d2}}\right)\right]} + \frac{1}{g_{m1}} \quad (5)$$

Setting the imaginary part of (5) to nil allows determining the resonance frequency $f_{o2}$ of the circuit in Fig. 3(c)

$$f_{o2} = \frac{1}{2\pi\sqrt{C_{d2}\,(L_{D1}+L_{D2})}} \quad (6)$$

where $C_{d2}$ is the parasitic capacitance between the drain of $M_2$ and the inductor $L_{D1}$. The value of the $C_{d2}$ is 250 fF. Moreover, the inductors $L_{D1}$ and $L_{D2}$ are selected to provide the required output impedance. The values of the $L_{D1}$ and $L_{D2}$ in this work are 0.4 nH and 8.9 nH, respectively. Considering (1) and (5), the overall input impedance ($Z_{in}$) of the proposed circuit shown in Fig. 3(c) can be written as (7), as indicated earlier.

$$Z_{in} = Z_g||Z_{f\_in} \quad (7)$$

In this UWB LNA, the circuit parameters are $C_{gs1}$ =150 fF, $C_{d2}$ =250 fF, $L_{D1}$ =0.4 nH, $L_{D2}$ =8.9 nH, $L_{S1}$ =0.16 nH, $L_{g1}$ =1.4 nH, $g_{m1}$ =27 mS, and $R_F$ =190 Ω. Fig. 4 plots the calculated input return loss $S_{11}$ with respect to frequency for $Z_g$, $Z_{f\_in}$, and $Z_{in}$ (= $Z_g//Z_{f\_in}$) of the proposed matching circuit in Fig. 3(c). As seen in Fig. 4, the wideband input matching can be effectively achieved by introducing a pole of frequency $f_{o2}$.

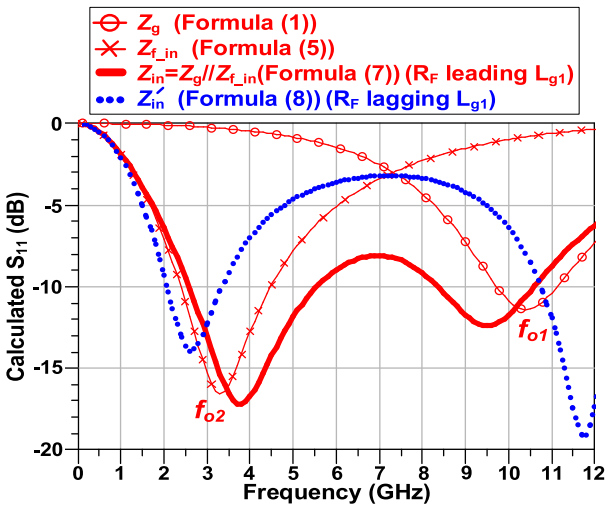


**FIGURE 4.** Calculated input return loss $S_{11}$ with respect to the frequency for $Z_g$, $Z_{f\_in}$, $Z_{in}$ (= $Z_g//Z_{f\_in}$; $R_F$ leading $L_{g1}$) of the proposed topology in Fig. 3(c) and $Z'_{in}$ ($R_F$ lagging $L_{g1}$) of the conventional topology in Fig. 3(b).

Consider the circuit topology in Fig. 3(b) of regular matching with feedback resistor $R_F$ lagging gate inductor $L_{g1}$,

the overall input impedance of the circuit can be written as

$$Z'_{in} = sL_{g1} + \left[ Z'_{f\_in} || \left( sL_{S1} + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_{S1}}{C_{gs1}} \right) \right]. \quad (8)$$

$Z'_{in}$ is plotted in Fig. 4 and it is found that the proposed input matching circuitry (feedback resistor $R_F$ leading gate inductor $L_{g1}$ and combining with inductive divider at output) achieves a better input return loss from 3.1 to 10.6 GHz than the regular circuit in Fig. 3 (b) (feedback resistor $R_F$ lagging gate inductor $L_{g1}$).

For UWB amplifiers, the design of output impedance matching is also critical. However, it is seldom considered for UWB LNAs in the literature. Considering the proposed circuit topology in Fig. 3(c), the output impedance $Z_{out}$ without feedback resistor $R_F$ can be expressed as

$$\begin{aligned} Z_{out\_wo\_fb} &= sL_{D2} || \left[ \left( Z_{o2} || \frac{1}{sC_{d2}} \right) + sL_{D1} \right] \\ &= \frac{sL_{D2}\left( s^2 C_{d2} L_{D1} Z_{o2} + sL_{D1} + Z_{o2} \right)}{s^2 C_{d2} Z_{o2} \left( L_{D1} + L_{D2} \right) + s\left( L_{D1} + L_{D2} \right) + Z_{o2}} \end{aligned} \quad (9)$$

where $Z_{o2}$ is the output impedance of the cascode stage. The output impedance $Z_{f\_out}$ looking into the feedback resistor $R_F$ can be written as

$$Z_{f\_out} = R_F + \frac{1}{sC_{in}} || Z_g \quad (10)$$

where $C_{in}$ is a DC block, and its value is 4.11 pF. The combination of an inductor $L_{D2}$ and a capacitor $C_{byss}$ is the RF choke. Considering (9) and (10), the overall output impedance of the proposed circuit in Fig. 3(c) is

$$Z_{out} = Z_{out\_wo\_fb} || Z_{f\_out} \quad (11)$$

Fig. 5 shows the calculated output return loss $S_{22}$ with respect to the frequency for $Z_{out\_wo\_fb}$ and $Z_{out}$ of the proposed LNA. It is indicated that not only the output reflection coefficient $S_{22}$ is significantly improved, but also the bandwidth ($S_{22}$ <−10 dB) is effectively extended.

Consider the regular output matching circuit topology shown in Fig. 3(b), the overall output impedance can be driven as

$$Z'_{out} = Z'_{f\_out} || \left[ sL_{D2} || \left( Z_{o2} || \frac{1}{sC_{d2}} \right) \right] \quad (12)$$

which is also plotted in Fig. 5. Compared to the conventional design, the presented inductive divider circuitry at output not only achieves much better output return loss ($S_{22}$), but also extends the bandwidth.

### B. SMALL-SIGNAL GAIN AND NOISE FIGURE CONSIDERATIONS

Fig. 6 shows the small-signal equivalent circuit of the proposed UWB LNA plotted in Fig. 2, where $C_{gs1}$, $C_{gd1}$, $C_{gs3}$, and $C_{gd3}$ are the parasitic capacitances, and $R_{Lg2}$, $R_{Ld1}$, $R_{Ld2}$, and $R_{Ld4}$ are losses from the on-chip inductors $L_{g2}$, $L_{d1}$,

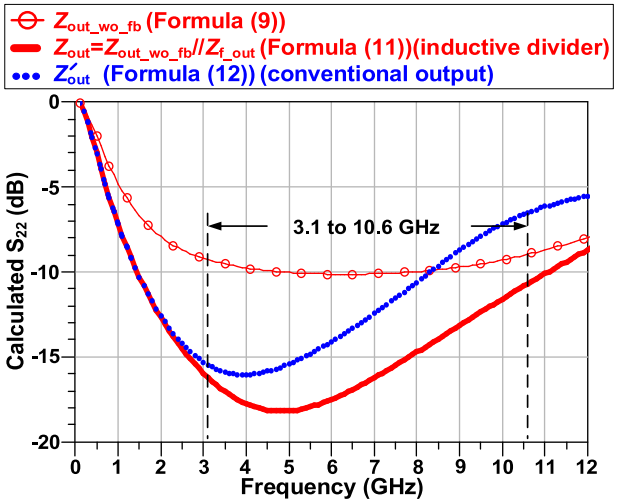


**FIGURE 5.** Calculated output return loss $S_{22}$ with respect to the frequency for $Z_{out\_wo\_fb}$, $Z_{out}$ of the proposed topology in Fig. 3(c) and $Z'_{out}$ ($R_F$ lagging $L_{g1}$) of the conventional topology in Fig. 3(b).

$L_{d2}$, and $L_{d4}$, respectively. For simplification of the analysis procedure, the parasitic capacitance $C_{gd1}$ and $C_{gd3}$ are neglected. Moreover, it is assumed that the currents flowing through the intrinsic resistors ($r_{o1}$, $r_{o3}$) and the forward-body biased currents ($g_{mb1}v_{bs1}$, $g_{mb3}v_{bs3}$) are much smaller than the current sources ($g_{m1}v_{gs1}$ and $g_{m3}v_{gs3}$). Therefore, the small-signal gain of the proposed UWB LNA can be expressed as

$$\begin{aligned} \frac{v_{o2}}{v_{in1}} &= \frac{v_{o1}}{v_{in1}} \cdot \frac{v_{o2}}{v_{in2}} \\ &= \frac{-g_{m1}\frac{sL_{d2}R_{F1}^2}{C_{gs1}(L_{g2}+L_{S1})(R_{F1}+sL_{d2})}}{s^2 + s\left(\frac{\omega_{o,in1}}{Q_{in1}}\right) + \omega_{o,in1}^2} \\ &\quad \times \frac{-g_{m3}\frac{sL_{d4}R_{F2}^2}{C_{gs3}(L_{g3}+L_{S3})(R_{F2}+sL_{d4})}}{s^2 + s\left(\frac{\omega_{o,in2}}{Q_{in2}}\right) + \omega_{o,in2}^2} \end{aligned} \quad (13)$$

where

$$\omega_{o,in1} = \frac{1}{\sqrt{C_{gs1}\left(L_{g2}+L_{S1}\right)}} \quad (14)$$

$$Q_{in1} = \frac{(R_{F1}+sL_{d2})\sqrt{C_{gs1}\left(L_{g2}+L_{S1}\right)}}{(R_{F1}+sL_{d2})\left(g_{m1}L_{S1}+C_{gs1}\left(\frac{sL_{g2}}{Q_{Lg2}}+R_{F1}\right)\right)+g_{m1}R_{F1}L_{d2}} \quad (15)$$

$$\omega_{o,in2} = \frac{1}{\sqrt{C_{gs3}\left(L_{g3}+L_{S3}\right)}} \quad (16)$$

$$Q_{in2} = \frac{(R_{F2}+sL_{d4})\sqrt{C_{gs3}\left(L_{g3}+L_{S3}\right)}}{(R_{F2}+sL_{d4})\left(g_{m3}L_{S3}+R_{F2}C_{gs3}\right)+g_{m3}R_{F2}L_{d4}} \quad (17)$$

The $\omega_{o,in1}$ and $\omega_{o,in2}$ are the series resonance frequencies, and $Q_{in1}$ and $Q_{in2}$ represent the $Q$-factors of input networks at the frequencies ($\omega_{o,in1}$ and $\omega_{o,in2}$) for LNA's first

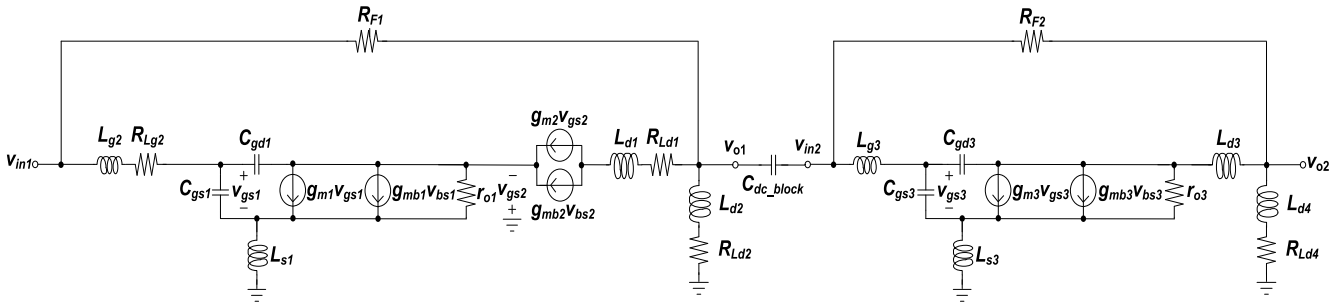


**FIGURE 6.** Small-signal equivalent circuit for the proposed full-band 3.1- to 10.6-GHz UWB LNA employing the simultaneous wideband input/output matching technique (feedback resistors $R_{F1}$, $R_{F2}$ leading gate inductors $L_{g2}$, $L_{g3}$ and combining with inductive dividers at output ports).

and second stages, respectively. According to Section II(A) and Fig. 4, it is known that the created series resonance frequencies ($\omega_{o,in1}$ and $\omega_{o,in2}$) indeed improves the input reflection coefficient ($S_{11}$) and effectively extended the bandwidth. Moreover, the $Q$-factor of the input matching network ($Q_{in1}$) can be improved by using fully-integrated on-chip vertical solenoid inductors due to improved $Q$-factor ($Q_{Lg2}$) than that of conventional planar inductors, leading to high gain.

The noise factor of the proposed circuit topology with simultaneous wideband input/output matching technique (feedback resistor $R_F$ leading gate inductor $L_{g1}$ and combining with inductive divider at output port) shown in Fig. 3(c), is expressed in (34). It is known that the coefficients ($\kappa$ and $\xi$) in (31) and (33) have influences on overall NF in (35). It is also observed that the coefficients ($\kappa$ and $\xi$) are function of $\omega_{o,in1}$. By utilizing the proposed matching technique, the bandwidth is extended due to the series resonance frequency ($\omega_{o,in1}$). Moreover, it minimizes the coefficients ($\kappa$ and $\xi$) in (31) and (33), leading to a reduced noise factor $F$ and noise figure NF. From (34) and (35), it is found that using $Q$-factor improved vertical solenoid inductors in this work can lead to reduced NF.

Moreover, to minimize the body leakage current, the 5-kΩ resistors are inserted between the bodies and supply voltages ($V_{b1}$, $V_{b2}$, and $V_{b3}$), as shown in Fig. 2. This can lead to the minimized body leakage currents of 59.7 pA, 35.8 pA, and 2.05 pA, respectively.

## III. EXPERIMENTAL RESULTS

The LNA was fabricated in a 180-nm CMOS process and the size of the fabricated chip is 0.945 × 0.82 mm$^2$, excluding the testing pads. The microphotograph of the chip is represented in Fig. 7. On-wafer probing was used to characterize the UWB LNA. The losses of the measurement setups were de-embedded and calibrated in the experimental results. In this work, the MOSFETs ($M_1$-$M_3$) operate in saturation region with supply voltages of $V_{DD1}$ =1.5 V and $V_{DD2}$ =0.75 V, leading to the measured overall DC power dissipation of 18.9 mW. In [13]–[15], the adopted 1.5-V supply voltage is also widely used for low-voltage low-power 180-nm CMOS circuits. For applications, the used

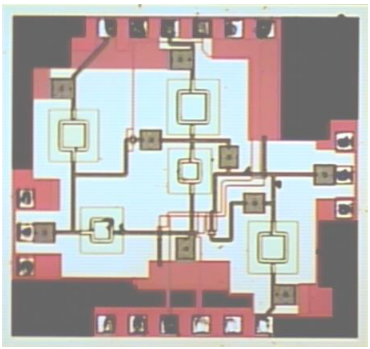

**FIGURE 7.** Microphotograph of the fabricated 3.1-10.6-GHz monolithic UWB amplifier.

0.75-V supply voltage can be generated from a bandgap circuit [16].

Fig. 8(a) shows the measured and simulated S-parameters of the UWB LNA with simultaneous wideband input/output matching technique (feedback resistors $R_{F1}$, $R_{F2}$ leading gate inductors $L_{g2}$, $L_{g3}$ and combining with inductive dividers at output ports). It is observed that the measured maximum gain ($S_{21}$) of the UWB LNA is 15.02 dB. In addition, the measured 3-dB bandwidth of the UWB LNA is 2.4 GHz to 13 GHz, while the gain ($S_{21}$) varies from 12.02 dB to 15.02 dB. This results in 138% fractional bandwidth. Fig. 8(b) illustrates the measured, simulated, and calculated input return loss ($S_{11}$) of the LNA. As shown from this figure, the measured input return loss ($S_{11}$) of the UWB LNA is below −9.4 dB. Fig. 8(c) illustrates the measured, simulated, and calculated output return loss ($S_{22}$) of the UWB LNA. It shows that from 3.1 to 10.6 GHz, the measured $S_{22}$ of the LNA is below −15.8 dB. According to Fig. 8(b) and Fig. 8(c), the derived formulas (7) and (11) in Section II can be used to evaluate the input and output impedances.

The measured and simulated NF of the proposed UWB LNA is depicted in Fig. 9. It is observed that the measured minimum NF of the LNA is 3.1 dB. Moreover, the measured NF of the LNA covering the full-band UWB frequency (3.1-10.6-GHz) varies between 3.1 dB to 4.4 dB. Furthermore, the differences between the calculated noise figure (35) and the measured result are within 1 dB in entire UWB.

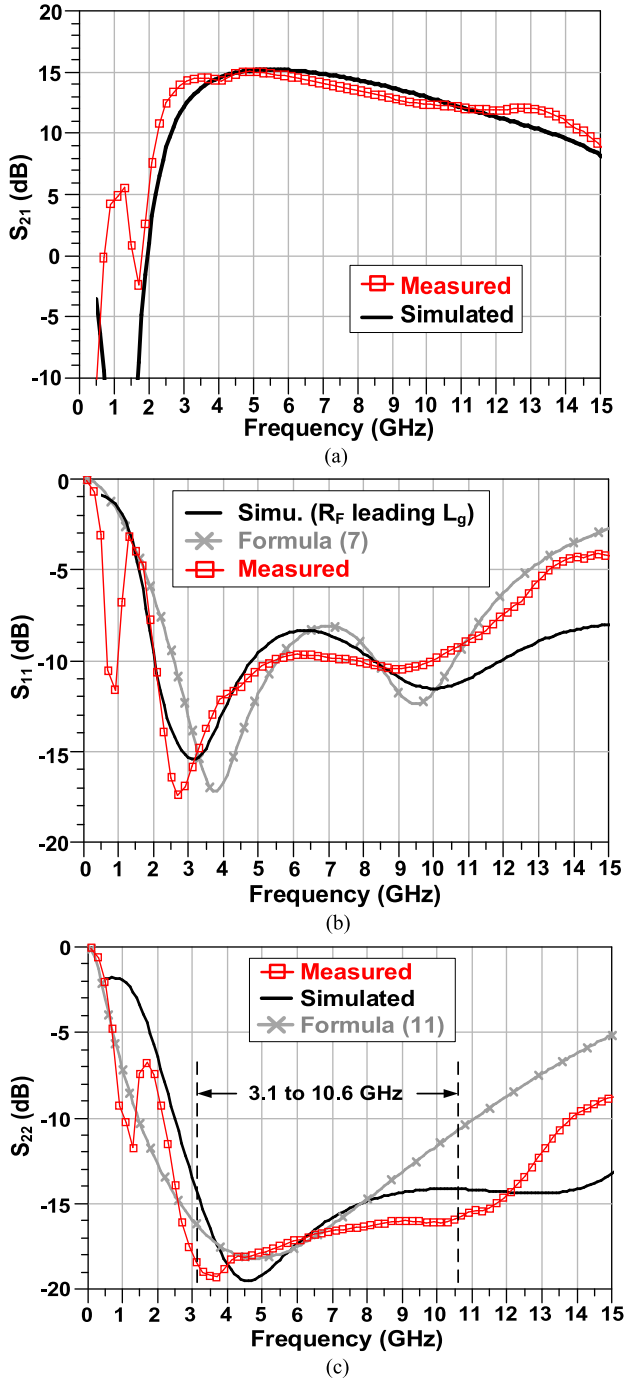


**FIGURE 8.** Measured and simulated (a) $S_{21}$, (b) $S_{11}$, and (c) $S_{22}$ of the fabricated 3.1-10.6-GHz UWB LNA employing the proposed simultaneous wideband input/output matching technique (feedback resistors $R_{F1}$, $R_{F2}$ leading gate inductors $L_{g2}$, $L_{g3}$ and combining with inductive dividers at output ports).

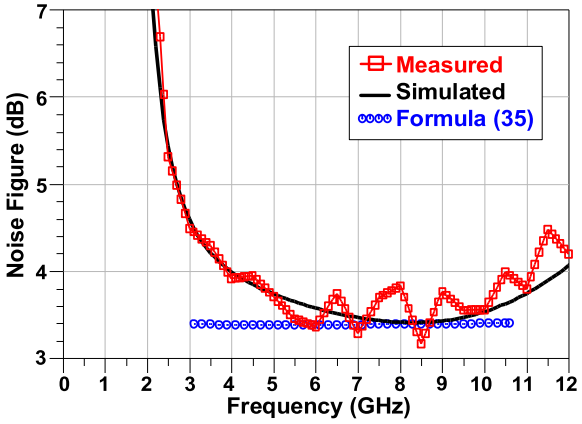


**FIGURE 9.** Measured and simulated noise figure of the fabricated 3.1-10.6-GHz UWB LNA.

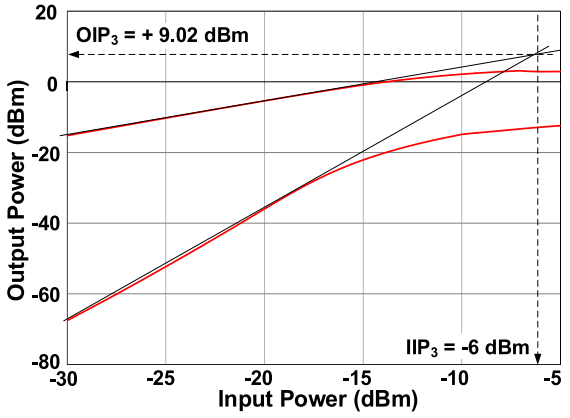


**FIGURE 10.** Measured input-referred third-order intercept point ($IIP_3$) of the fabricated 3.1-10.6-GHz UWB LNA.

This justifies the transistor noise model used in this work for predicting NF.

Fig. 10 represents the measured input-referred third-order intercept point ($IIP_3$) of the UWB LNA. The characterization is carried out by using two-tone tests, and the frequencies of these two-tones for the UWB LNA are at the maximum gain frequency of 4.9 GHz with 1-MHz spacing. By inspecting Fig. 10, the value of $IIP_3$ for the UWB LNA is $-6$ dBm. Fig. 11 shows the simulated $IIP_3$ of the fabricated 3.1-10.6-GHz wideband LNA, and the average $IIP_3$ over the entire frequency band is $-6.1$ dBm. It is known that the linearity ($IIP_3$) of a receiver is typically dominated by the following stages (e.g., mixer or IF amplifier) [22]. Moreover, the $IIP_3$ greater than $-18.1$ dBm is acceptable for a UWB system [23]. Fig. 12 depicts the measured and simulated group delay of the fabricated UWB LNA. It observed that a minimum group delay of 71.3 ps is achieved. The measured and simulated stability factor (K-factor) is shown in Fig. 13, indicating that the UWB LNA is stable ($K > 1$) in the entire frequency band.

Table 1 summarizes the measured performance of the proposed UWB LNA shown in Fig. 2, and compares them to the performances of previously published full-band 3.1-10.6-GHz 180-nm CMOS UWB LNAs. It is confirmed from table 1 that the proposed UWB LNA achieves low supply voltage with low DC power dissipation of 18.9 mW, high gain of 15.02 dB, low NF of 3.1 dB, and good input/output return loss $-9.4$ dB/$-15.8$ dB. It is observed that the output return loss ($S_{22}$) is significantly improved by using the proposed technique. In addition, figures of merit (FOM) for LNA

**TABLE 1.** Performance summarized and compared with previously published full-band 3.1-10.6-GHz 180-nm CMOS UWB LNAs.

| Process | Max Gain (dB) | S11 (dB) | S22 (dB) | Min. NF (dB) | NF (dB) | IIP3 (dBm) | Supply Voltage (V) | DC Power (mW) | Chip Size ($mm^2$) | FOM1 | FOM2 | FOM3 | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 180-nm CMOS | 9.7 | < -11 | < -10 | 4.5 | 4.5–5.1 | -6.2 | 1.8 | 20 | 0.59 | 1.07 | 0.57 | -11.83 | [10], JSSC |
| 180-nm CMOS | 14 | < -11 | n.a. | 4.5 | ~4.5 | -12 | 1.8 | 21 | 0.46 (Active Area) | 2.14 | 6.61 | -17.39 | [7], TMTT |
| 180-nm CMOS | 15 | < -7 | < -8 | 4.0 | 4.0–4.4 | 2.5 | 1.8 | 21.5 | 0.66 | 1.97 | 5.87 | 10.87 | [11], SiRF |
| 180-nm CMOS | 13.2 | < -10 | n.a. | 4.5 | 4.5–6.2 | -1.4 | 1.8 | 23 | 1.41 | 0.58 | -4.71 | -7.51 | [17], MWCL |
| 180-nm CMOS | 11.9 | < -10 | < -13 | 2.9 | 2.9–3.8 | 4 | 1.8 | 29.16 | 0.71 | 1.50 | 3.53 | 11.53 | [18], IET |
| 180-nm CMOS | 14.5 (2-5 GHz) | < -10 | n.a. | 8.6 | 8.6–10 | n.a. | 1.8 | 3.8 | 1.44 | 1.17 | 1.33 | n.a | [2], TVLSI |
| 180-nm CMOS | 14.8 | < -12 | < -12 | 3.9 | 3.8–4.5 | -11.5 | 1.5 | 3.4 (wo buffer) | 1.12 | n.a | n.a | n.a | [13], IET |
| **180-nm CMOS** | **15.02** | **< -9.4** | **< -15.8** | **3.1** | **3.1–4.4** | **-6** | **1.5** | **18.9** | **1.02** | **2.15** | **6.65** | **-5.35** | **This Work** |

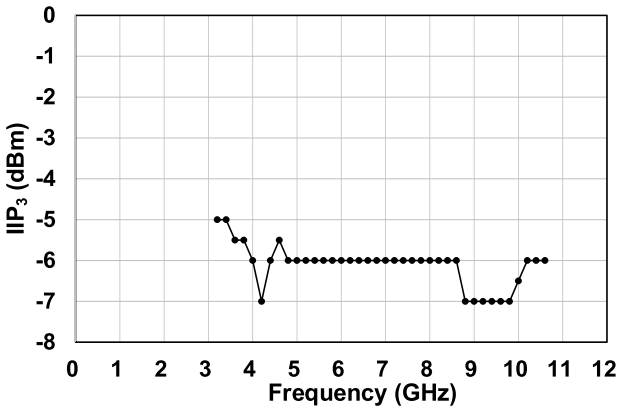


**FIGURE 11.** Simulated $IIP_3$ of the fabricated 3.1-10.6-GHz UWB LNA.

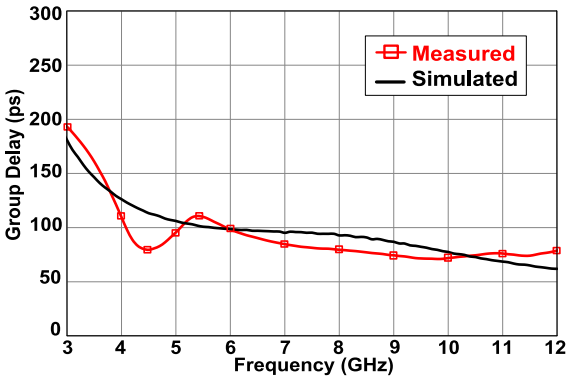


**FIGURE 12.** Measured and simulated group delay of the fabricated 3.1-10.6-GHz UWB LNA.

presented in [19] can be written as

$$\text{FOM1}\left(\frac{\text{GHz}}{\text{mW}}\right) = \frac{\text{Gain}_{[\text{lin}]} \times \text{BW}_{[\text{GHz}]}}{(\text{NF}_{[\text{lin}]} - 1) \times \text{P}_{\text{DC}[\text{mW}]} \times A_{[\text{mm}^2]}}. \quad (18)$$

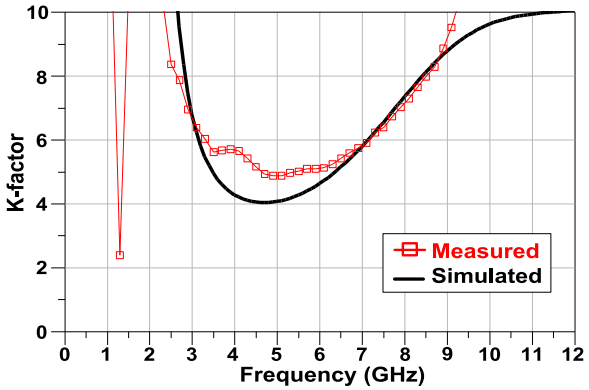


**FIGURE 13.** Measured and simulated stability factor (K-factor) of the fabricated 3.1-10.6-GHz UWB LNA.

$$\text{FOM2} = 20 \cdot \log_{10}\left(\frac{\text{Gain}_{[\text{lin}]} \times \text{BW}_{[\text{GHz}]}}{(\text{NF}_{[\text{lin}]} - 1) \times \text{P}_{\text{DC}[\text{mW}]} \times A_{[\text{mm}^2]}}\right). \quad (19)$$

$$\text{FOM3} = 20 \cdot \log_{10}\left(\frac{\text{Gain}_{[\text{lin}]} \times \text{BW}_{[\text{GHz}]} \times \text{IIP3}_{[\text{mW}]}}{(\text{NF}_{[\text{lin}]} - 1) \times \text{P}_{\text{DC}[\text{mW}]} \times A_{[\text{mm}^2]}}\right). \quad (20)$$

Table 1 shows that the proposed LNA achieves superiors FOM1 and FOM2 of 2.15 and 6.65, respectively, and a comparable FOM3 of −5.35.

## IV. CONCLUSION

This work has proposed an UWB LNA using a simultaneous wideband input/output matching technique (feedback resistors $R_{F1}$, $R_{F2}$ leading gate inductors $L_{g2}$, $L_{g3}$ and combined with inductive dividers at output ports). Wideband input matching is achieved by the addition of a pole resulting from an inductive divider at the output port and whose frequency $f_{o2}$ is given by (6). Moreover, the wideband

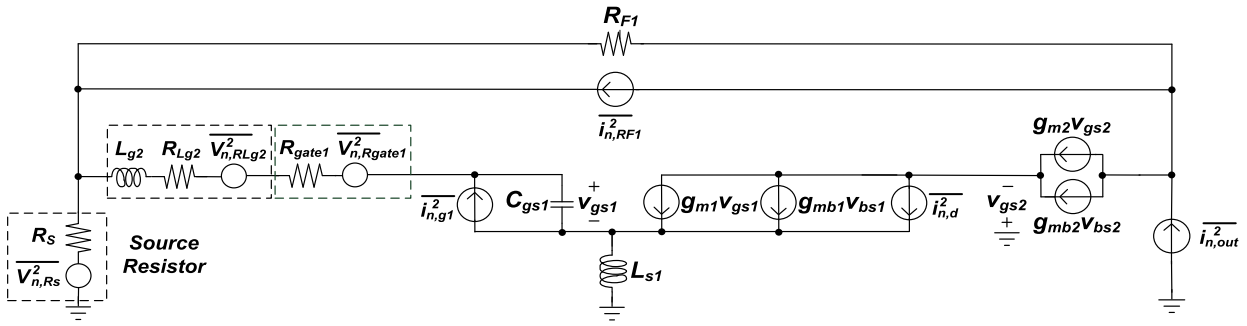


**FIGURE 14.** Equivalent circuit of the proposed circuit in Fig. 3(c) including the noise sources.

output matching is significantly improved owing to the $R_F$ leading $L_g$ at the input port and the inductive divider at the output port, as illustrated in Fig. 5. Furthermore, the NF of the LNA is improved owing to the series resonance frequency ($\omega_{o,in1}$) in the wideband input matching network, leading to a low noise figure covering the full UWB. Measurement results show that the fabricated UWB LNA, using simultaneous wideband input/output matching technique, compares favorably with similar designs.

## APPENDIX
## NOISE FIGURE FORMULATION

In this appendix, the NF of the proposed circuit shown in Fig. 3(c) is analyzed. It noted that the dominant noise source for MOSFET devices is the channel thermal noise [6], [10]. Moreover, this type of noise source is typically modeled as a shunt current source at the output circuit of a MOSFET, and its value can be formulated as

$$\overline{i^2_{n,d}} = 4kT\gamma g_{d0}\cdot\Delta f \tag{21}$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $\gamma$ is a bias-dependent factor, $g_{d0}$ is the zero-bias drain conductance of the device, and $f$ is the frequency. Operating in saturation, the value of $\gamma$ is 2/3 for long-channel devices. As for a deep-submicron MOSFET, (21) has to be modified as

$$\overline{i^2_{n,d}} = 4kT\gamma g_{\rm m}\Delta f/\alpha \tag{22}$$

where $g_{\rm m}$ is the transconductance of MOSFET, and $\alpha$ is the ratio of $g_{\rm m}$ to the zero-bias drain conductance $g_{d0}$. The values of $\alpha$ and $\gamma$ of deep-submicron MOSFETs are typically less than 1 and greater than 1, respectively [20]. Thus, this will result in a raised channel thermal noise $\overline{i^2_{n,d}}$ for the deep-submicron MOSFET.

From Fig. 14, the output noise power density due to the source resistance $R_{\rm S}$ at the frequency of interest $\omega_{o,in1}$ can be formulated as

$$S_{a,source}\left(\omega_{0,in1}\right) = \frac{4kTR_S g_{m1}^2}{\omega_{0,in1}^2 R_S^2\left\{\frac{g_{m1}L_{S1}}{R_S}+C_{gs1}\left(1+\frac{R_{gate1}}{R_S}+\frac{R_{F1}}{R_S}+\frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \tag{23}$$

Moreover, the output noise power density due to the series resistors $R_{Lg2}$ and $R_{gate1}$ can be written as

$$S_{a,R_{Lg2},R_{gate1}}\left(\omega_{0,in1}\right) = \frac{4kT\left(R_{Lg2}+R_{gate1}\right)g_{m1}^2}{\omega_{0,in1}^2 R_S^2\left\{\frac{g_{m1}L_{S1}}{R_S}+C_{gs1}\left(1+\frac{R_{gate1}}{R_S}+\frac{R_{F1}}{R_S}+\frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \tag{24}$$

Furthermore, the dominant noise contributor internal to a UWB LNA is the channel current of MOSFET for the amplifier's first stage. Its output noise power density arising from this channel thermal source around the frequency $\omega_{o,in1}$ is

$$S_{a,i_{n,d}}\left(\omega_{0,in1}\right) = \frac{\frac{\overline{i^2_{n,d}}}{\Delta f}}{\omega_{0,in1}^2 R_S^2\left\{\frac{g_{m1}L_{S1}}{R_S}+C_{gs1}\left(1+\frac{R_{gate1}}{R_S}+\frac{R_{F1}}{R_S}+\frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \tag{25}$$

Substituting (21) into (25), the formula (25) can then be rewritten as

$$S_{a,i_{n,d}}\left(\omega_{0,in1}\right) = \frac{4kT\gamma g_{d0}}{\omega_{0,in1}^2 R_S^2\left\{\frac{g_{m1}L_{S1}}{R_S}+C_{gs1}\left(1+\frac{R_{gate1}}{R_S}+\frac{R_{F1}}{R_S}+\frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \tag{26}$$

In addition, a gate noise current $\overline{i^2_{n,g}}$ will be induced due to the capacitive coupling from a channel noise current $\overline{i^2_{n,d}}$. From [21], the induced noise current at gate terminal is presented by

$$\overline{i^2_{n,g}} = 4kT\delta g_g\cdot\Delta f \tag{27}$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}. \tag{28}$$

The $\delta$ is the coefficient with a value of 4/3 for long-channel devices. The channel noise current $\overline{i^2_{n,d}}$ and the induced gate noise current $\overline{i^2_{n,g}}$ are closely related with a coefficient $c$,

which is defined as [20], [21]

$$c \equiv \frac{\overline{i_{n,g} i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2}\,\overline{i_{n,d}^2}}} \tag{29}$$

For this work, the values of $\delta$ and $c$ are 3.4 and $1.0j$ for the 180-nm MOS, respectively [24].

As a result, the output noise power density from the internal noise current at the frequency of interest $\omega_{o,in1}$ can be divided into two categories. The first term represents the combined effect of the drain noise current and the correlated portion of the gate noise current, and it is given by

$$\begin{aligned} &S_{a,i_{n,d},i_{n,g},c}\left(\omega_{0,in1}\right) \\ &= \kappa \cdot S_{a,i_{n,d}}\left(\omega_{0,in1}\right) \\ &= \frac{4kT\gamma\kappa g_{d0}}{\omega_{0,in1}^2 R_S^2 \left\{\frac{g_{m1}L_{S1}}{R_S} + C_{gs1}\left(1 + \frac{R_{gate1}}{R_S} + \frac{R_{F1}}{R_S} + \frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \end{aligned} \tag{30}$$

where

$$\kappa\left(\omega_{0,in}\right) = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + \frac{|c|}{\omega_{0,in}R_S C_{gs1}}\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{31}$$

The second term is with the uncorrelated gate current noise, which can be written as

$$\begin{aligned} &S_{a,i_{n,g},u}\left(\omega_{0,in1}\right) \\ &= \xi \cdot S_{a,i_{n,d}}\left(\omega_{0,in1}\right) \\ &= \frac{4kT\gamma\xi g_{d0}}{\omega_{0,in1}^2 R_S^2 \left\{\frac{g_{m1}L_{S1}}{R_S} + C_{gs1}\left(1 + \frac{R_{gate1}}{R_S} + \frac{R_{F1}}{R_S} + \frac{sL_{g2}}{R_S Q_{Lg2}}\right)\right\}^2} \end{aligned} \tag{32}$$

where

$$\xi\left(\omega_{0,in}\right) = \frac{\delta\alpha^2}{5\gamma}\left(1 - |c|^2\right)\left(1 + \frac{1}{\omega_{0,in}^2 R_S^2 C_{gs1}^2}\right) \tag{33}$$

To evaluate the NF reduction of the UWB amplifier, the calculated total output noise including (23), (24), (30), and (32) is divided by the total output noise due to the source resistance (23). Assuming the bandwidth is 1 Hz, it yields the noise factor $F$, which can be derived as

$$F = 1 + \frac{sL_{g2}}{R_s Q_{Lg2}} + \frac{R_{gate1}}{R_s} + \frac{\gamma(\kappa + \xi)g_{d0}}{R_S g_{m1}^2} \tag{34}$$

Consequently, the noise figure can be given as

$$\mathrm{NF} = 10\log_{10} F \tag{35}$$

For this work, the values of $\alpha$, $\gamma$, and $g_{d0}$ for the 180-nm MOSFETs are 0.6, 1.8, and 2.5 mS respectively [24], [25]. Moreover, the value of $R_{gate1}$ for the $W/L$ =152$\mu$m/180nm NMOS in this work is 42 Ω.

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**TO-PO WANG** (Senior Member, IEEE) received the Ph.D. degree from National Taiwan University, Taipei, Taiwan.

In 2009, he joined the Faculty of the Department of Electronic Engineering, National Taipei University of Technology, Taipei, where he is currently a Professor.

Dr. Wang was a recipient of the Best Paper Award of the Symposium on Nano Device Technology (SNDT), in 2012, and the IEEE Service Award, in 2017. He was the General Secretary of the 2017 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-Taiwan), the Session Chair of the 2017 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-Taiwan), the 2012 IEEE Topic Meeting on Silicon Monolithic Integrated Circuits in RF System (2012 SiRF), the 2012 IEEE International Conference on Wireless Information Technology and Systems (ICWITS), and the 2012 IEEE International Conference on Electron Devices and Solid-State Circuits (IEEE EDSSC). He also serves as an Associate Editor for IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS (MWCL).