IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 20, 2021, accepted March 9, 2021, date of publication March 22, 2021, date of current version March 31, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3067930

Charge Loss Induced by Defects of Transition Layer in Charge-Trap 3D NAND Flash Memory

FEI WANG, (Member, IEEE), YUAN LI, (Member, IEEE), XIAOLEI MA, AND JIEZHI CHEN, (Senior Member, IEEE)

School of Information Science and Engineering (ISE), Shandong University, Qingdao 266237, China

Corresponding authors: Yuan Li (yuan.li@sdu.edu.cn) and Jiezhi Chen (chen.jiezhi@sdu.edu.cn)

This work was supported in part by the China Key Research and Development Program under Grant 2016YFA0201802; in part by the National Natural Science Foundation of China under Grant 62034006, Grant 61874068, and Grant 91964105; and in part by the Fundamental Research Funds of Shandong University under Grant 2018TB013.

ABSTRACT In charge-trap (CT) three-dimensional (3D) NAND flash memory, the transition layer between Si_3N_4 CT layer and SiO_2 tunneling layer is inevitable, and the defects in the transition layer are expected to cause both lateral and vertical charge loss. Here, by first-principles calculations, we present a detailed study on the defects in the transition layer Si_2N_2O to comprehend their impacts on charge loss in CT 3D NAND flash memory. It is shown that shallow-trap centers, such as intrinsic nitrogen vacancy (V_N) and interstitial Ti (Ti_i), can couple with the conduction band of Si_2N_2O to lead to lateral charge loss. On the other hand, the N substituting Si atom (N_{Si}) and Ti substituting Si atom (Ti_{Si}) defects in the transition layer can couple through resonance with the trap centers in Si_3N_4, leading to vertical charge loss from the CT layer to the transition layer. Our results strongly suggest that appropriate treatment of the transition layer and hydrogen passivation are both important for avoiding charge loss in CT 3D NAND flash memory.

INDEX TERMS Silicon oxynitride (Si_2N_2O), Ti doping, charge loss, 3D NAND.

I. INTRODUCTION

Ultra-high density storages are urgently needed for data storage and management at the age of big data. Three-dimensional (3D) NAND flash memory represents a mainstream non-volatile memory aiming to break the inherent restrictions of 2D planar NAND in terms of storage density [1], [2]. While the transition from 2D to 3D structures has achieved a huge reduction in device size and bit cost, size scaling is still highly required for further development of 3D NAND flash memory. For instance, 3D charge-trap (CT) NAND flash memory, which usually adopts a macaroni-like vertical channel structure, has been rapidly developed because of its ultra-high storage density, low cost, well reliability, and diversity in novel applications [3]–[8]. The cylindrical shape of 3D CT NAND with ONO stack ($SiO_2/Si_3N_4/SiO_2$) from inside out is beneficial to the field distribution in the CT layer (Si_3N_4), which allows thicker tunneling oxide (SiO_2) to enlarge the memory window [9]. However, this well-established structure also brings issues that have yet to be solved. A typical example is the reliability issue generated as a result of the common CT layer in the same NAND string. In particular, lateral charge migration between adjacent cells can lead to read disturb (RD) and data retention (DR), [10], [11] which issues could be much more serious with size scaling. As such, several approaches, such as metallic doping [12] and process optimization [13], were proposed to suppress charge migration in 3D CT NAND flash memory. As one of the most frequently used methods, process optimization could greatly improve device reliability by reducing defects at the interface to guarantee the purity of Si_3N_4. However, previous experimental studies revealed that, at the interface between SiO_2 and Si_3N_4, it is very likely to form silicon oxynitride of which the impact is poorly understood [14], [15].

It is found that silicon oxynitride represents a functional material with good mechanical stability, tunable refractive index, and cracking dielectric properties [16], [17], which are promising for applications in microelectronic devices [18]–[21]. As an essential procedure for the fabrication of 3D NAND, N_2-annealing is expected to introduce a thin layer of Si_2N_2O on the surface of Si_3N_4 [22], [23]. This issue is also expected to be more serious with size scaling. As a unique compound in the SiO_2-Si_3N_4

The associate editor coordinating the review of this manuscript and approving it for publication was Nagarajan Raghavan.

quasi-binary system, the intrinsic Si_2N_2O has long been studied intensively. However, little attention was paid to the impacts of Si_2N_2O on the charge loss in 3D NAND, which essentially depends on the ability of trapping charges rather than the thickness of the CT layer itself. Therefore, it is important to reveal how Si_2N_2O as a transition layer impacts the reliability of a CT 3D NAND flash memory, which is instructive for size scaling of the devices.

In this work, by first-principles calculations, we present a detailed study on various defects in Si_2N_2O to comprehend their impacts on charge loss in CT 3D NAND flash memory, which is critical to the reliability and size scaling of the devices. As will be shown, our results reveal that appropriate treatment of the transition layer (Si_2N_2O) and hydrogen passivation are both important for improving the reliability in 3D NAND flash memory.

II. METHODOLOGY

We employ crystalline structures of Si_2N_2O to reveal the internal mechanisms of charge loss by introducing different defects. As shown in Fig. 1(a), a supercell of Si_2N_2O crystal (with side lengths of 17.7384 Å, 16.4793 Å, and 14.5473 Å; crystal system: Base-Centered Orthorhombic; H-M symbol: Cmc21) [24] containing 360 atoms was employed for calculating accurate trap energy levels. Due to the high symmetry of Si_2N_2O crystal, all the defect sites can be identified exclusively. Even though in the case of interstitial doping, the big ring of Si_2N_2O with the lowest energy configurations could be located easily.

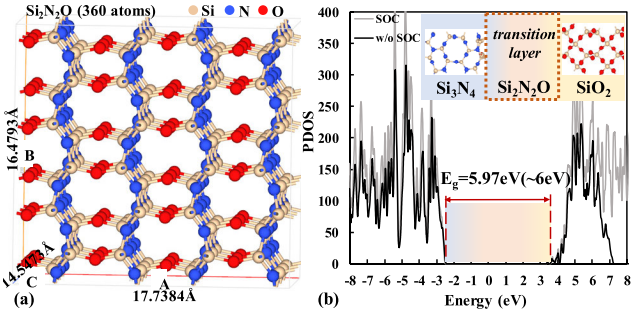

FIGURE 1. (a) Geometric structure and (b) projected density of states (PDOS) of a Si_2N_2O supercell (side lengths of 17.7384 Å, 16.4793 Å, and 14.5473 Å) with and without spin-orbit coupling, respectively. The inset in (b) displays schematically the location of the transition layer (Si_2N_2O).

The geometric optimization of the supercell was calculated at the level of density functional theory (DFT) by using the generalized gradient approximation Perdew-Burke-Ernzerhof (GGA-PBE) exchange-correlation functional. A k-points grid of $1 \times 1 \times 1$ was adopted in the calculations. In order to obtain the correct value of 5.97 eV for the band gap of Si_2N_2O [25], the electronic properties were calculated by using the screened hybrid functional of Heyd, Scuseria, and Ernzerhof (HSE) with Hartree-Fock mixing constant of $a = 0.14$ and screen parameter of $\omega = 0.2$. The spin-orbital coupling (SOC) was omitted in our calculations because it has little impact on the electronic properties of Si_2N_2O, in particular the band gap (see Fig. 1(b)). Similar calculations were performed for both β-SiO_2 and β-Si_3N_4. All the calculations were performed by using the GPU accelerated PWmat package based on the plane wave and the pseudopotential method [26]. In practice, total energy convergence of less than 10^{-4} eV, energy cut-off of 50 Ry, and residual force of 0.01 eV/Å on each atom were employed in the calculations.

To study the defect properties, we calculated the formation energy of various defects. The formation energy for a defect α in the charged state q is defined by following formula [27]:

$$\Delta H(\alpha, q) = E(\alpha, q) - E(\text{host}) + \Sigma n_i(E_i + u_i) + q[E_{\text{VBM}}(\text{host}) + E_{\text{F}} + \Delta V]$$

Here, α denotes the defect type; q, the number of electrons transferred from the supercell to the reservoirs forming the defect cell; $E(\alpha, q)$, the energy of the supercell with the defect; E(host), the energy of a perfect supercell without defect; E_i, the atomic energy of element i; E_{F}, the Fermi level of the host relative to the valence band maximum E_{VBM}; n_i, the number of atoms for element i; and μ_i, the chemical potential of element i added to ($\mu_i < 0$) or removed ($\mu_i > 0$) from the defect-free supercell, which depends on the experimental conditions. It is noted that, different from previous work [28], μ_i is considered in our calculations such that more accurate formation energy can be obtained. The electrostatic potential correction term ΔV was used to align the reference potential of the supercell with or without defects ($\Delta V = V(\alpha, q, R) - V(\text{host}, R)$), and R denotes a place far away from the defect. To correct for the spurious interaction of the charge with the neutralizing background charge as well as with its mirror images in periodic boundary condition, a charge-correction term was calculated by the equation $(2/3)(e^2/4\pi\varepsilon_0)(q^2\alpha_{\text{M}}/2\varepsilon_{\text{r}}L)$ [29], where e denotes the elementary charge; ε_0, the vacuum permittivity; α_M, the Madelung constant (with value of 1.64) [30]; ε_r, the relative dielectric constant; and $L = V_{supercell}^{1/3}$ [31]–[33]. Given the values of the parameters used in our calculations, a charge correction of only 76 meV is obtained. The impact of such small amount of charge correction, as will be shown, is negligible and will not be considered in our study here.

Charge loss affecting the performance of 3D CT memory mainly takes place by means of electron emission and drift-diffusion. Here, we focus on the emission rate from the trap to the conduction band. The Poole-Frenkel (PF) model was used to obtain the electron emission rate R_{E} (ΔE_t) at temperature T by the following equation:

$$R_E(\Delta E_t) = \nu_{PF} \cdot \exp\left(\frac{\beta\sqrt{F} - E_t}{k_B T}\right), \quad \beta = \sqrt{\frac{e^3}{\pi\varepsilon_0\varepsilon_r}}$$

where ν_{PF} denotes the attempt-to-escape frequency for the emission [34]; F, the strength of electric field at the transition layer; E_t, the trap energy with respect to the nitride

conduction band; and ε_r, the relative dielectric constant of silicon oxynitride tuned by chemical composition. In practice, $T = 85$ °C, $\nu_{PF} = 5 \times 10^7$, and $\varepsilon_r = 6.2$ [35], [36] were utilized in the calculations.

The SiO_2, Si_2N_2O, and Si_3N_4 were combined to construct the interface layers of SiO_2/Si_3N_4 or $SiO_2/Si_2N_2O/Si_3N_4$ without interface defects. The dangling bonds at the sideward of interface were saturated by hydrogen to eliminate the gap defect states. The electrostatic interaction between the interface and its mirror was eliminated in the calculations by employing a vacuum space of 2 nm. The total density of states (DOS) was calculated based on the constructed interface layers. The band alignment was obtained from the partial density of states (PDOS) by projecting the DOS onto the atoms at the interface. Similar methods were employed for estimating interfacial band alignment in previous studies [37], [38]. However, diifferent from other method [39] in which the interfacial materials were calculated separately, our calculations were performed by treating the interface as a whole such that the quantum confinement effect is also included.

III. RESULTS AND DISCUSSION

We first consider the geometric and band structures of Si_2N_2O. The DFT-calculated results have been shown in Fig. 1. The band gap of Si_2N_2O obtained in our calculation is about 5.97 eV both with and without spin-orbit coupling. This result agrees with the value range of 5.2 ∼ 5.97 eV reported previously for the band gap of silicon oxynitrides [25].

A. DEFECTS-INDUCED LATERAL CHARGE LOSS

Due to the N_2-annealing processes in 3D NAND flash memory, Si_2N_2O could be formed at the Si_3N_4/SiO_2 interface, whose defects could also trap charges and thereby cause reliability issues similar to that in the CT layer. Therefore, based on the intrinsic Si_2N_2O supercell, we consider the formation energy of different types of defects, such as vacancy, substitution, and interstice. A schematic diagram of the formation energy has been shown in Fig. 2(a), in which the electron trap level (E_t, marked by filled circle) of a defect is defined as the energy difference between the conduction band minimum (CBM) and that of the transition level. The geometric structures of some typical defects in Si_2N_2O have been illustrated in Fig. 2(b). These defects include intrinsic nitrogen vacancy (V_N), interstitial Si (Si_i), Si substituting N atom (Si_N), and O substituting N atom (O_N). The calculated formation energy of these defects has been displayed in Figs. 2(c), 2(d), and 2(e), respectively. In 3D NAND flash memory, the electron trap level was reported as about 1.4 eV [40]. As such, a region of $E_t < 1.4$ eV is labelled in Figs. 2(c), 2(d), and 2(e) to highlight the energy levels close to or shallower than the electron trap level, where the shallow-trap levels could be identified easily.

It is found that the defects V_N, interstitial O (O_i), and O_N have lower formation energy in the cases of vacancy, interstice, and substitution, labelled by filled dashed ellipses.

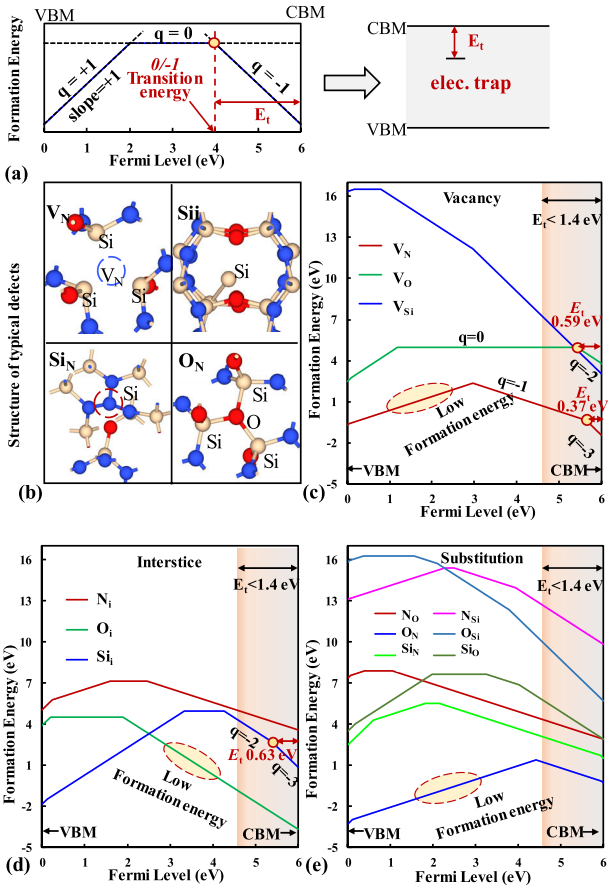

FIGURE 2. (a) Schematic diagram of transition level (vertical dashed line) and electron trap level (solid lines). (b) Geometric structures of typical defects of intrinsic nitrogen vacancy (V_N), interstitial Si (Si_i), Si substituting N atom (Si_N), and O substituting N atom (O_N). (c)-(e) Calculated formation energy of the defects of vacancy, interstice, and substitution, respectively. In (c)-(e), the electron trap levels are marked by filled circles and a region of $E_t < 1.4$ eV is labelled to highlight the energy levels close to or shallower than electron trap level.

It suggests that they could be formed easily during fabrication processes. The shallow-trap defects in Si_2N_2O, i.e., V_N ($E_t \sim 0.37$ eV), oxygen vacancy (V_O, $E_t \sim 0.59$ eV), and Si_i ($E_t \sim 0.63$ eV), have been highlighted in yellow by filled circles in Figs. 2(c) and 2(d). There are no shallow-trap defects of substitution in Fig. 2(e). Given the magnitude of the trap levels, the nature of the shallow-trap centers would not be affected even if the charge correction of 76 meV is taken into account. On the other hand, it is known that Si_3N_4 with shallow-trap centers could lead to reliability issues such as charge loss. Electrons trapped in the shallow-trap centers will detrap within a few milliseconds after program, leading to fast charge loss. Moreover, charges could be re-trapped by these released trap levels rather than by other traps that are energetically deeper and more stable. Thus, it is vital to reducing these shallow-trap centers in Si_2N_2O.

To compare different trap centers, the trap energy of the defects has been summarized in Fig. 3(a). There is usually more than one trap energy for each type of defect. For

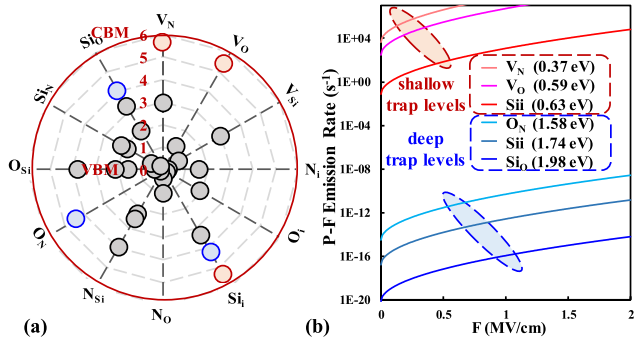

FIGURE 3. (a) Calculated trap energy of defects in Si_2N_2O. (b) Calculated emission rates of various trap energy (E_t) by using the Poole-Frenkel equation at temperature of 85 °. The large red circle in (a) denotes the conduction band minimum (CBM ~ 3.5 eV) of Si_2N_2O.

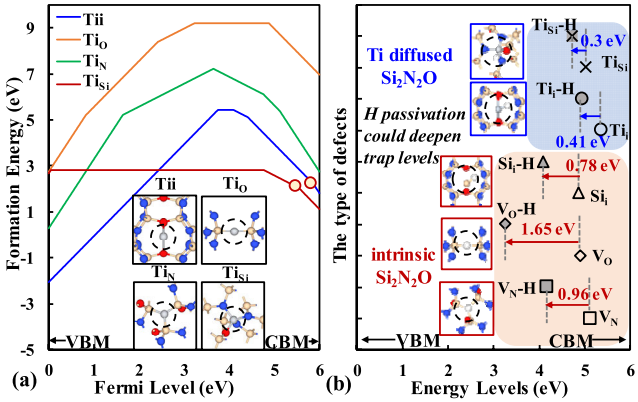

FIGURE 4. (a) Formation energy of the defects in Si_2N_2O with Ti doping; the inset shows the geometric structures of the Ti-related defects. (b) Schematic diagram of H-incorporated defects with or w/o Ti doped; the inset shows the geometric structures of the defects with H-passivation.

instance, three E_t (0.63 eV, 1.98 eV, and 2.67 eV) of Si_i defect could be observed. It is noted that emission from traps can take place in terms of two different mechanisms, i.e., quantum tunneling and thermionic emission. The quantum tunneling can occur at any temperature between all allowed states, such as from trap states to band states or from one trap to another. The thermionic emission causes the release of carriers from traps to band at finite temperature, which can be described by the Poole-Frenkel model. By focusing on the thermionic emission from the traps to the conduction band of Si_2N_2O, both shallow and deep trap centers (labelled in red and blue, respectively) in Fig. 3(a) were selected to calculate the emission rate by using the Poole-Frenkel equation. The results have been shown in Fig. 3(b), in which the emission rates are distinct for different types of defects. Large emission rates are obtained in the case of shallow-trap centers, such as V_N, V_O, and Si_i. In this situation, charge loss occurs during the early stage of data retention. Meanwhile, low emission rates are obtained in the case of deep-trap centers, such as the defects of O_N (E_t ~ 1.58 eV), Si_i (E_t ~ 1.74 eV), and Si_O (E_t ~ 1.98 eV), which hardly contribute to fast electron diffusion. Thus, according to the emission rates, the shallow- and deep-trap centers could be distinguished in intrinsic Si_2N_2O.

We turn to consider the impact of metallic doping, such as Ti doping, which was proved to be efficient in Si_3N_4 for suppressing the shallow-trap centers in 3D NAND [12]. During this process, Ti-doping could easily take place in Si_2N_2O. The calculated formation energy of defects in Ti-doped Si_2N_2O has been shown in Fig. 4(a). The inset displays the geometric structures of the Ti defects. The defect Ti substituting Si atom (Ti_{Si}) has the lowest formation energy and a shallow-trap energy (E_t ~ 0.46 eV). Because the Si_2N_2O is Si-rich, there are fewer Si atomic defects such that Ti substituting N atom (Ti_N) could represent the dominant defect. Importantly, since Ti_N has deep trap energy larger than 0.88 eV, it will not contribute to shallow traps. In terms of defect interstitial Ti (Ti_i), ultra-shallow trap energy (E_t ~ 0.14 eV) is obtained, which can be reduced by doping optimization. As a result, Ti-doping in Si_2N_2O will result in additional shallow-trap centers. These results suggest that, to achieve robust reliability of 3D NAND flash memory, it is necessary to propose an effective method for deepening the trap energy in both intrinsic and Ti-doped Si_2N_2O.

We also consider H passivation because it represents an alternative effective measure to eliminate shallow-trap centers [41]. Previous experimental evidence demonstrated that hydrogen annealing could be an effective approach for introducing H-passivation in the devices [42]. The properties of shallow-trap centers, such as V_N, V_O, Si_i, Ti_i, and Ti_{Si}, with H passivation were calculated, and the results have been shown in Fig. 4(b). The inset displays the geometric structures of these defects with H passivation. It is noted that the trap energy can be obviously deepened by H passivation. For instance, in the case of V_N defect, the H atom will fill the N vacancy, forming V_N-H defect, in which the H-passivation can change the defect type by passivating one Si dangling-bond, forming Si-H bond. As a result, intrinsic trap energy of V_N defect is deepened from 0.37 eV to 1.33 eV, which is deep enough to trap electrons. Similarly, by H passivation, the shallow-trap V_O and Si_i defects turn to be V_O-H (2.24 eV) and Si_i-H (1.41 eV) in intrinsic Si_2N_2O, which both become deep-trap centers. In the case of defects in Ti-doped Si_2N_2O, H passivation can deepen the shallow-trap energy by 0.3 eV from Ti_{Si} to Ti_{Si}-H and 0.41 eV from Ti_i to Ti_i-H defect, respectively. Indeed, these results demonstrate that hydrogen passivation represents an effective method to deepen trap energy for suppressing lateral charge loss in both intrinsic and Ti-doped Si_2N_2O. Our results also reveal that it is important to optimize the transition layer by hydrogen passivation, which is efficient to avoid the generation of shallow traps for suppressing lateral charge loss.

B. DEFECTS-INDUCED VERTICAL CHARGE LOSS

In addition to lateral charge loss, vertical charge loss, which takes place between different layers, also represents an

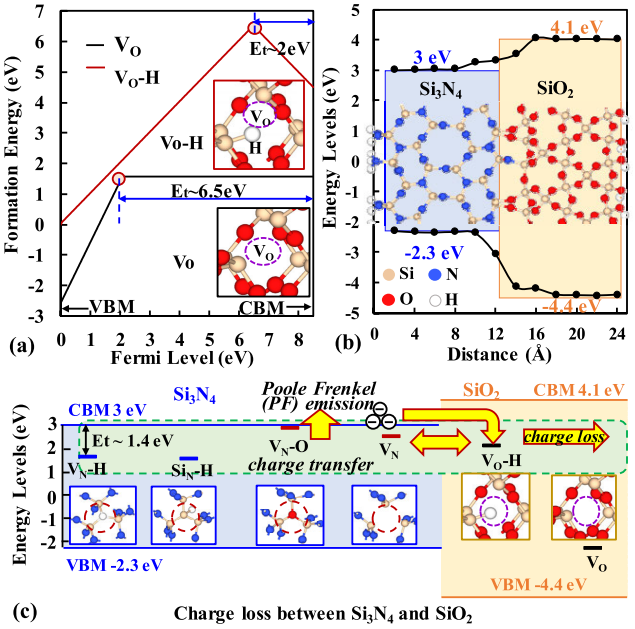

FIGURE 5. (a) Calculated formation energy of oxygen vacancy (V_O) and H-passivated oxygen vacancy (V_O-H) in SiO_2. The inset displays the geometric structures of the defects. (b) Schematic diagram of band alignment for Si_3N_4 and SiO_2. The inset displays the geometry of the Si_3N_4/SiO_2 interface; (c) Schematic diagram of charge migration between Si_3N_4 and SiO_2.

important factor responsible for the reliability of CT NAND flash memory [43]. The defects in the transition layer Si_2N_2O are expected to serve as links connecting different layers of the device, leading to vertical charge loss. However, the current understanding of such effects still remains very limited. We now turn to consider the vertical charge loss induced by defects in Si_2N_2O, which can occur theoretically between all allowed resonant states in different layers. Due to the stacked structure of $SiO_2/Si_3N_4/SiO_2$, the vertical charge loss could take place between layers. The formation energy of V_O and V_O-H, which are typical defects in the tunneling layer (SiO_2), were calculated and the results have been shown in Fig. 5(a). It is noted that defect V_O in SiO_2 serves as a hole trap instead of an electron trap and an extremely deep trap energy level ($E_t \sim 6.5$ eV) is obtained. Moreover, single V_O defect in bulk system could be formed more easily than V_O-H because of its low formation energy. In previous work [44], [45], the virtual interactions between vacancy clusters and their images result in higher V_O defect formation energy, which error is eliminated in our calculations here for single V_O defect. In contrast, as compared with V_O, defect V_O-H has shallower trap energy ($E_t \sim 2$ eV), which is expected to be a key defect for vertical charge loss from Si_3N_4 to SiO_2.

The calculated bandgap of the separate SiO_2 and Si_3N_4 is consistent with that of previous work [46], which is labelled as color filled rectangles in Figs. 5(b). The band alignment extracted by PDOS at the Si_3N_4/SiO_2 interface shows that band bending effect and quantum confinement take place, which impact, however, is ignorable and does not affect the rationality of our results. Because of the consistency between the band diagrams of isolated bulks and those of SiO_2/Si_3N_4 and $SiO_2/Si_2N_2O/Si_3N_4$ heterojunctions, the defect levels computed in isolated bulk systems also make much sense to the heterojunctions.

Based on the band alignment, the trap energy levels were extracted and the results have been displayed in Fig. 5(c). Here, Si_3N_4 serves as a CT layer in 3D NAND flash memory, in which the electron trap centers are V_N-H and Si_N-H defects [40]. While electrons could be trapped in the shallow-trap centers (V_N and V_N-O) of Si_3N_4, these trapped electrons are able to escape from the CT layer due to the PF emission. The escaped electrons could be trapped again by V_O-H in SiO_2, leading to vertical charge loss. Meanwhile, charge-transfer from electron trap centers (V_N-H and Si_N-H) in Si_3N_4 to V_O-H in SiO_2 could also take place directly because of resonance. Our results indicate that the V_O-H defects in SiO_2 are responsible for charge loss, which is consistent with previous work [47]. From our results, it is very important to minimize the V_O-H defects in SiO_2 in order to suppress the vertical charge loss. However, while the transition layer may affect the vertical charge loss, the impacts of Si_2N_2O defects on the tunneling from Si_3N_4 to SiO_2 still remains open for further study in CT 3D NAND flash memory.

Due to the stacked structure of $SiO_2/Si_3N_4/SiO_2$ and N_2-annealing processes, Si_2N_2O can be easily formed at the interface between the stacked layers. In this context, a schematic diagram including Si_2N_2O of the vertical charge loss has been shown in Fig. 6(a). The calculated results of band alignment at the $Si_3N_4/Si_2N_2O/SiO_2$ interfaces have been shown in Fig. 6(b). While similar band bending effects are observed, our results still make difference. To understand how the defects impact vertical charge loss, we have summarized the results of trap energy levels of the defects based on the band alignment, as shown in Figs. 6(c) and 6(d) in the cases of intrinsic and Ti-doped Si_2N_2O, respectively. As discussed above, the defects with shallow-trap energy in Si_2N_2O is critical for lateral charge loss. However, the coupling between the defects in Si_3N_4, Si_2N_2O, and SiO_2 plays a more important role in causing vertical charge loss. Thus, we focus on the defects in Si_2N_2O that can easily couple with their counterparts in Si_3N_4 and SiO_2.

In the case of intrinsic systems, as shown in Fig. 6(c), there exist multiple electron trap centers for data storage in Si_3N_4, such as V_N-H and Si_N-H, for which the electron trap level is around 1.4 eV. Other typical defects with similar magnitude of trap energy in SiO_2, such as V_O and V_O-H, and in Si_2N_2O, such as O substituting Si atom (O_{Si}), N substituting Si atom (N_{Si}), Si_i, and Si substituting O atom (Si_O), are also summarized for comparison, as shown in Fig. 6(c). Because these intrinsic defects have energy levels close to each other and part of them has shallow-trap levels, they could induce not only lateral charge loss in Si_2N_2O but also vertical charge loss between layers. As an effective measure restraining lateral charge loss, H-passivation could also deepen these

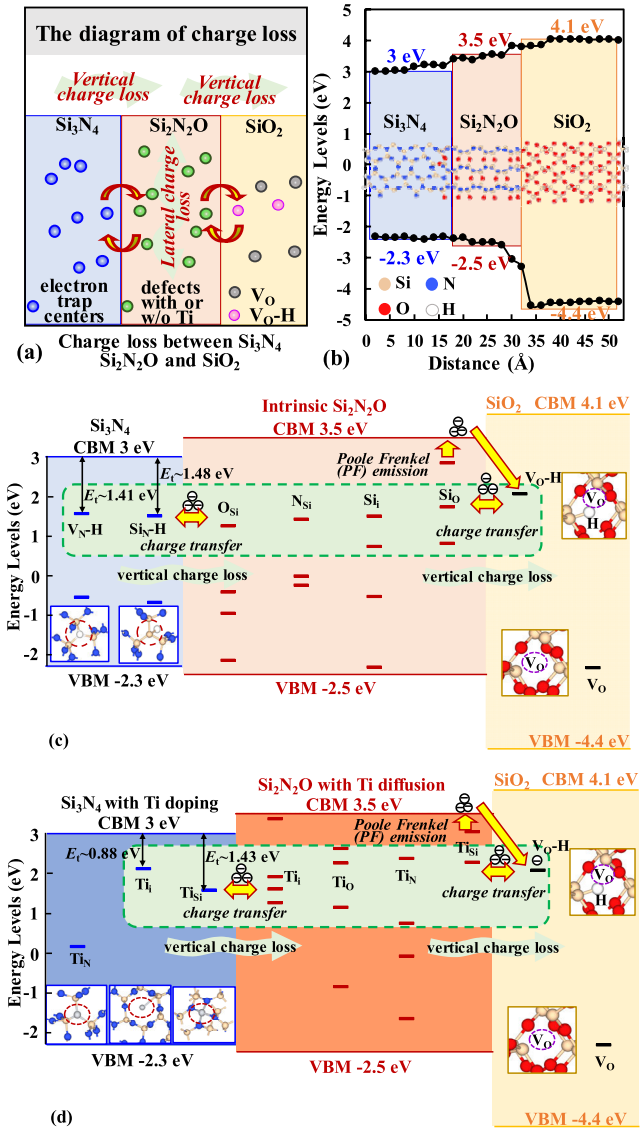

FIGURE 6. (a) Schematic diagram of charge migration between Si_3N_4, Si_2N_2O, and SiO_2; (b) schematic diagram of band alignment for Si_3N_4 and SiO_2. The inset displays the geometry of the $Si_3N_4/Si_2N_2O/SiO_2$ interface; (c) trap energy alignment of defects in intrinsic Si_3N_4, Si_2N_2O, and SiO_2; (d) trap energy alignment of defects in Si_3N_4 with Ti doping, Si_2N_2O with Ti-doping, and intrinsic SiO_2.

trap energy levels to break resonance. As a result, reduced vertical charge loss could be achieved. Thus, it is important to reduce defects in intrinsic Si_2N_2O by H-passivation, which is expected to improve the reliability in 3D NAND flash memory.

In the case of Ti-doped systems, as shown in Fig. 6(d), the intrinsic trap centers in Si_3N_4 are replaced by defects with Ti doping, such as the 2.12 eV Ti_i ($E_t \sim 0.88$ eV) and 1.57 eV Ti_{Si} ($E_t \sim 1.43$ eV) defects serving as electron trap centers [12]. As discussed above, the electrons stored in the Ti_i and Ti_{Si} defects in Si_3N_4 could tunnel to the Ti-related defects in Si_2N_2O because of the resonance of the trap energy. Obviously, there also exist multiple Ti-related defects in Si_2N_2O for vertical charge loss, such as Ti_i (1.6 eV) and Ti_N (1.14 eV). Importantly, these defects are close in trap energy to the V_O-H defects in SiO_2. As a result, vertical charge loss can take place from Si_3N_4 to Si_2N_2O and then to SiO_2. Thus, when Ti doping strategy in Si_3N_4 is adopted, it is necessary to appropriately treat the interface to suppress the transition layer. In particular, the Ti defects in Si_2N_2O could promote vertical charge loss because all Ti-related defects have trap energy levels close to that in both Si_3N_4 and SiO_2. Similar impacts of H-passivation in Ti-doped Si_2N_2O on vertical charge loss could be obtained. With Ti-doping in Si_3N_4, it is particularly important to reduce the transition layer Si_2N_2O to improve the reliability of 3D NAND flash memory.

It should be noted that the stack layers in 3D NAND flash memory are usually amorphous materials, for which the morphology is too diverse and complicated to model accurately. As such, our modeling here was carried out based on crystalline materials instead of amorphous structures to avoid the morphology issue. While there are differences in the V_O and V_O-H defects between our results with that of the studies in literature because of the materials diversity and methodology difference, the major findings of our study here are adequate and reasonable for the crystalline materials of Si_3N_4, Si_2N_2O, and SiO_2. It can be expected that, in an amorphous Si_2N_2O, more localized states near the band edges would be generated, bringing huge difficulties for identifying the defect states of interest. Although the approximation made in our modeling fails to account for the diversity of the amorphous structures, the use of crystalline Si_2N_2O could reveal the internal mechanism without loss of generality. Moreover, as compared with its 2D counterpart, 3D NAND flash memory has the same ONO stacking such that the interfacial geometry at the atomic scale is expected to be very similar. As such, we believe that the major findings obtained in our study here are also applicable to CT type 2D flash memory.

IV. CONCLUSION

In summary, by first-principles calculations, we have systematically studied the properties of defects in Si_2N_2O, which serves as a transition layer between Si_3N_4 and SiO_2 in charge-trap 3D NAND flash memory. It is found that V_N, V_O, and Si_i defects in intrinsic Si_2N_2O and Ti_{Si} and Ti_i defects in Ti-doped Si_2N_2O are shallow-trap centers, which could result in lateral charge loss in the device. On the other hand, because the O_{Si}, N_{Si}, Si_i, Si_O, and all Ti-related defects in Si_2N_2O are close in trap energy, they can couple with the defects with electron traps in Si_3N_4 and significant defects (V_O-H) in SiO_2, leading to vertical charge loss from Si_3N_4 to SiO_2. Hydrogen passivation is found to be an effective way in deepening shallow-trap centers and reducing resonant trap levels for charge loss. It suggests that the transition layer should be appropriately treated to suppress charge loss, especially with Ti doping. These findings are instructive for improving the reliability and performance of 3D NAND flash memory from a perspective at the atomic scale.

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FEI WANG (Member, IEEE) received the bachelor's degree in physics from Shandong Normal University, in 2016. She is currently pursuing the Ph.D. degree with the School of Physics and the School of Information Science and Engineering, Shandong University. Her research interests include the reliability of 3D NAND flash memory and nano-device fabricating.

YUAN LI (Member, IEEE) received the Ph.D. degree in condensed matter physics from Shandong University, in 2009. From 2010 to 2016, he was a Postdoctoral Fellow and a Research Scientist with the Georgia Institute of Technology and the King Abdullah University of Science and Technology (KAUST). In 2017, he joined the Faculty of Shandong University, as an Associate Professor with the School of Information Science and Engineering. He has coauthored more than 60 peer-reviewed articles published in international journals, including one invited review paper and one book chapter. His research interests include the computational design and characterization of advanced materials for information applications, in particular the flexible electronic materials, such as organic semiconductors and conjugated polymers. He also serves as an independent Reviewer for the National Natural Science Foundation of China and several international journals.

XIAOLEI MA received the bachelor's degree in physics from Qilu Normal University, in 2015, and the Ph.D. degree from the School of Information Science and Engineering, Shandong University, in 2020. He currently holds a postdoctoral position with Peking University.

JIEZHI CHEN (Senior Member, IEEE) received the Ph.D. degree from the Department of Informatics and Electronics, The University of Tokyo, in 2009. In 2010, he joined the Research and Development Center, Toshiba Corporation. He is currently a Professor with the School of Information Science and Engineering, Shandong University, China. He has published many articles in journals and conference proceedings. His research interests include the characterization and process engineering of nano-scale transistors and non-volatile memories, with main focus on reliability physics. He acted as a reviewer of several international journals. Since 2008, he has been the leading author or the corresponding author, working on nanoscale devices and device reliabilities, for more than ten times in the VLSI Symposium and the IEEE International Electron Device Meeting (IEEE IEDM). He also served as a Technical Program Committee (TPC) Member for IEDM, in 2016 and 2017. He has been serving as a TPC Member for the Silicon Nanoelectronics Workshop since 2018, the IEEE International Reliability Physics Symposium since 2019, and the IEEE International Memory Workshop since 2020.